“Test vehicle” in 130nm TSMC for CMS HGCAL

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Organization for Micro-Electronics desiGn and Applications

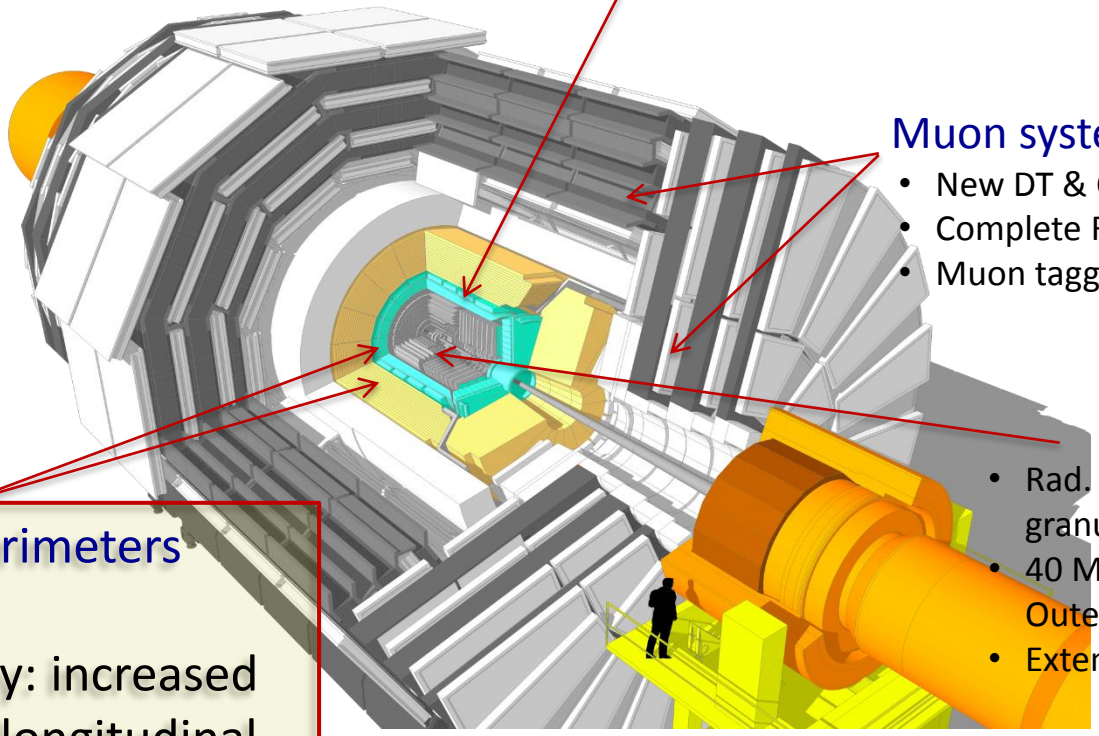
CMS Phase-II upgrades

Trigger/HLT/DAQ

- Track information in Trigger (hardware)
- Trigger latency 12.5 μs - output rate 750 kHz
- HLT output 7.5 kHz

Barrel EM calorimeter

- New FE/BE electronics with improved time resolution
- Lower operating temperature (8∘)



Muon systems

- New DT & CSC FE/BE electronics
- Complete RPC coverage $1.6 < \eta < 2.4$
- Muon tagging $2.4 < \eta < 3$

New Tracker

- Rad. tolerant - increased granularity - lighter
- 40 MHz selective readout in Outer Tracker for Trigger
- Extended coverage to $\eta \simeq 3.8$

New Endcap Calorimeters

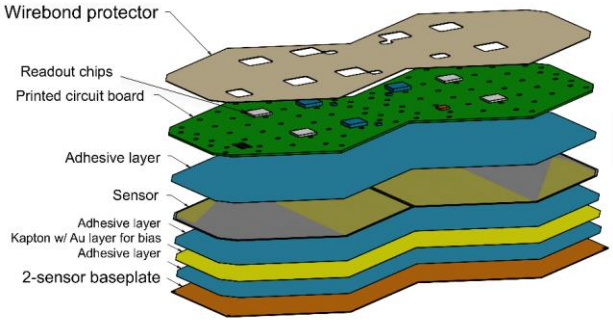
- Rad. tolerant
- High Granularity: increased transverse and longitudinal segmentation
- precise timing capability

Two major motivations for the upgrade

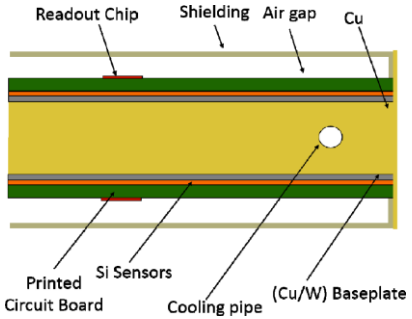
- **Unprecedented radiation dose** => replace End Cap Calorimeters
- **Much higher data flows** => replace most of the readout systems (5-10 Gb/s)

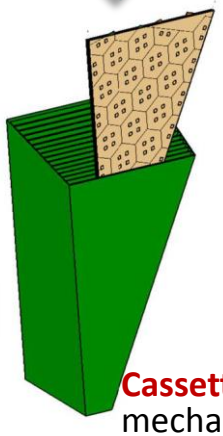
Modules, Cassettes and Mechanics (technical proposal)

Modules
With 2x 6 - 8" Hexagonal Si sensors, PCB, FE chip, on W/Cu baseplate

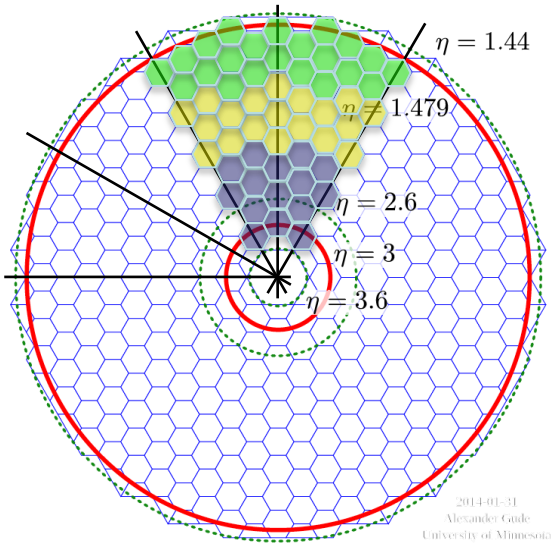


Modules mounted on Cu Cooling plate with embedded pipe
=> **Cassettes**

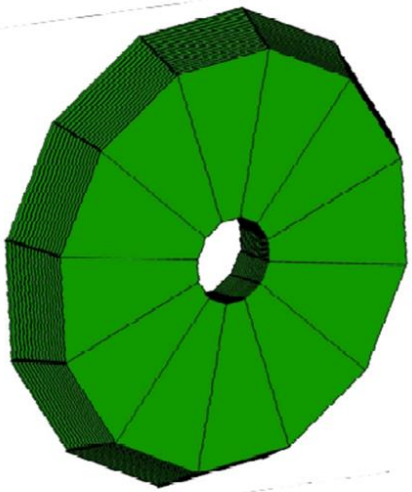




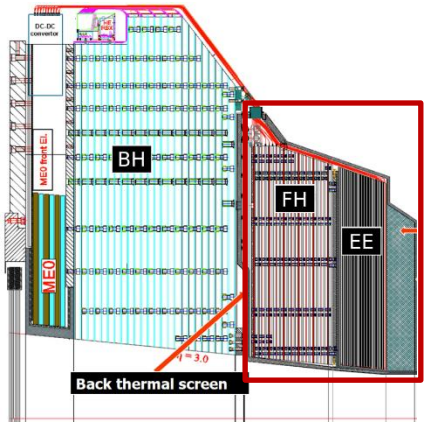
Cassette inserted in mechanical structure (containing absorber)



3 sensor active thicknesses 100-200-300 µm
0.5(1) cm^2 pads for 100(200/300) µm



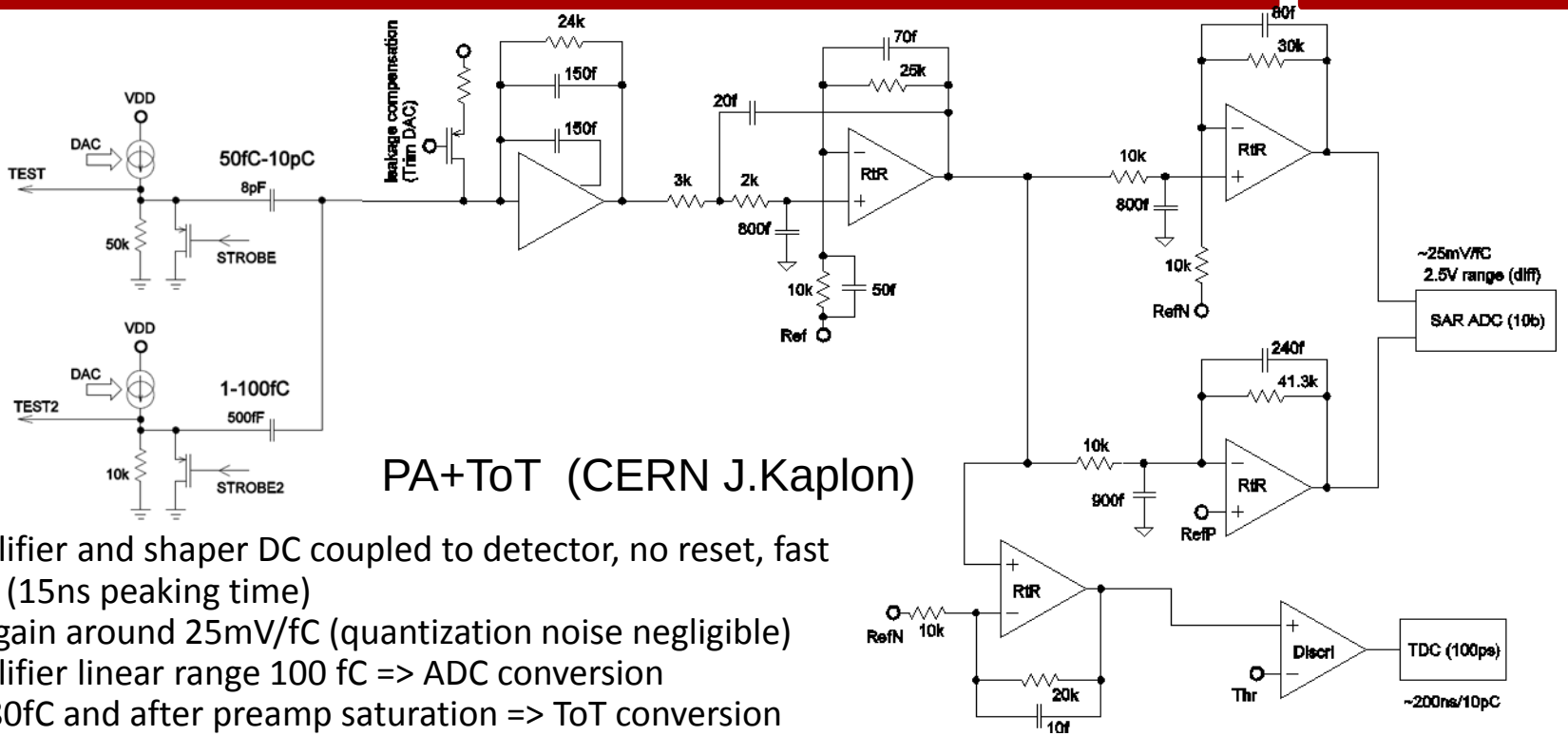
12 **Cassettes** mounted together to form the **ECAL (EE)** **and** **Front HCal (FH)**



Replaced EndCap (maintained at -30°C

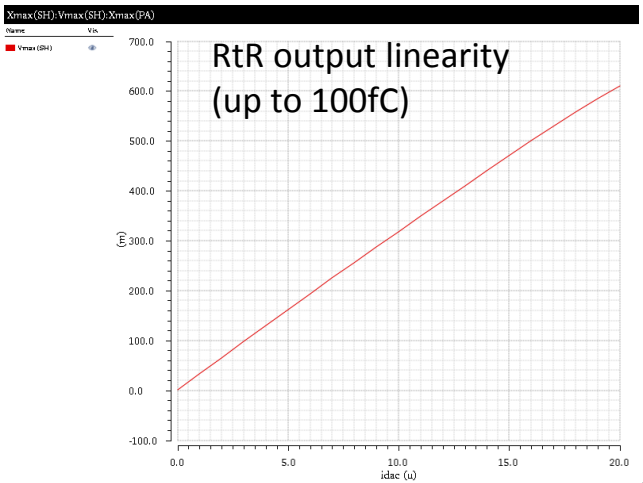
- Stringent requirements for Front-End Electronics
  - Low power (~5 mW for analogue channel)
  - Low noise: <2000 e- (0,32 fC)
  - MIP: 10k – 20k e- (1,5 – 3 fC)
  - Dynamic range up to 2000 MIP (10 pC), **17 bits** required with 0,1 fC resolution
  - High radiation (200 Mrad, 10^{16} N)
  - Detector capacitance 40-60pF
  - Detector leakage: up to 10 µA
  - System on chip (digitization, processing…)
  - High speed readout
  - ~ 92,000 FE chips (~6M channels)

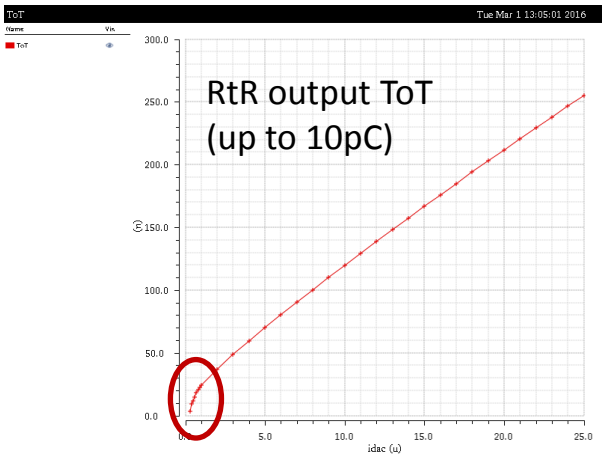
Baseline architecture (Technical Proposal)

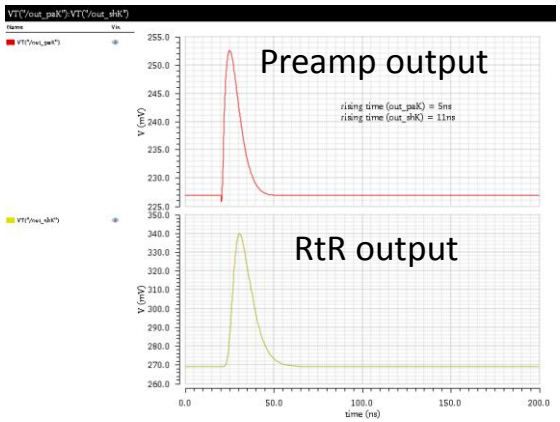


PA+ToT (CERN J.Kaplon)

- Preamplifier and shaper DC coupled to detector, no reset, fast shaping (15ns peaking time)
- Analog gain around 25mV/fC (quantization noise negligible)
- Preamplifier linear range 100 fC => ADC conversion
- Above 80fC and after preamp saturation => ToT conversion

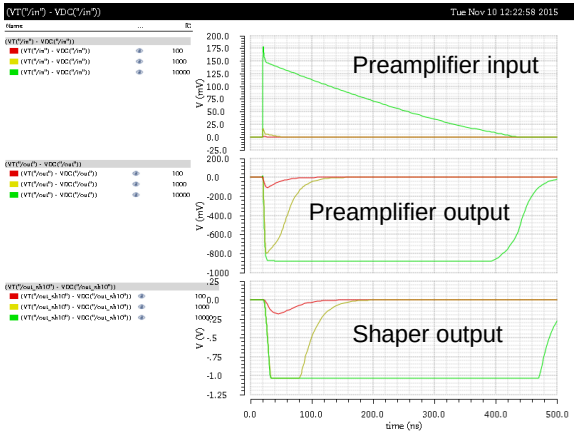




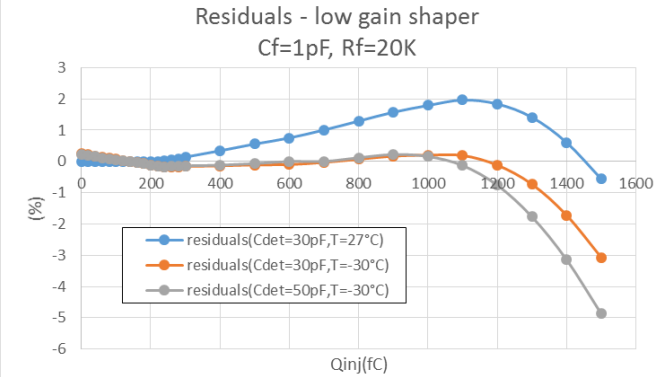


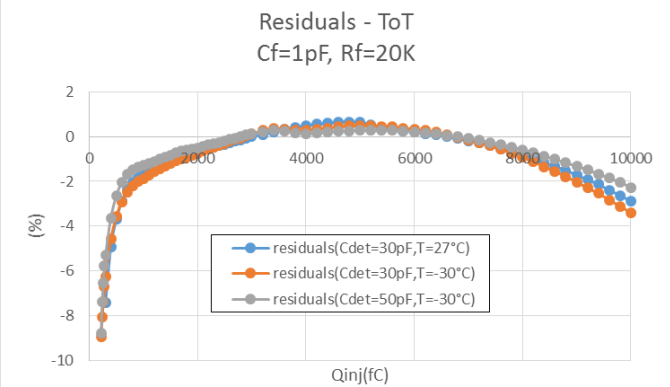
ToT problematic

- High crosstalk when preamplifier is saturating
- Long dead time due to ToT. It depends of preamplifier feedback resistance
- There is never a good overlap between low gain and ToT, precise characterization is needed. It is due to the non-linear behavior when preamplifier pass through from the non-saturation mode to the saturation mode
- The system has to manage with ADC data (mV) and ToT data (ns) and with a non-linear ToT behavior at the first. The ToT data have to be linearized.



Transient signals for 100, 1000 and 10000 fC injected charge





Milestones for electronics

15-Feb-16	**Submit v0 FE chip (SKIROC2-CMS) in 0,35 µm**
Mid-May-16	**Submit FE test vehicles in TSMC130 nm technology**
1-Jun-16	1st Comprehensive Review
30-Sep-16	**1st results from FE test vehicles and second test vehicle submission**
31-Oct-16	Confirm choice of front-end electronics (130 nm)
15-Dec-16	Define architecture & specs for LV/HV supply
15-Dec-16	Define location of DC-DC converters
15-Dec-16	Define location of electrical/optical links
31-Mar-17	**Submit V1 ASIC** ⇒ First 32/64 ch ASIC with full functionnality
31-Mar-17	Choice of Si sensors type: all n-on-p or mixed (i.e. n-on-p and p-on-n)
1-Jun-17	2nd Comprehensive Review
30-Sep-17	1st results from tests of V1 ASIC
1-Nov-17	Submit TDR
30-Jun-18	**Submit V2 ASIC**

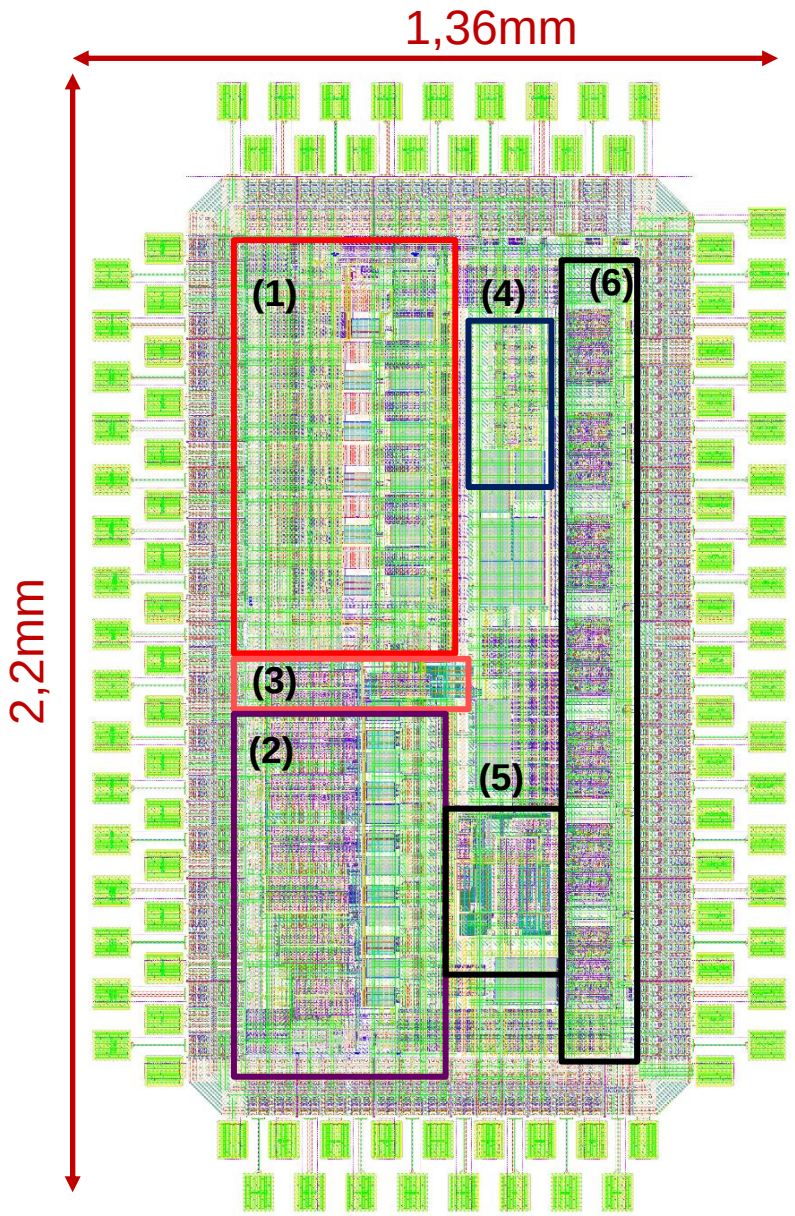
Test vehicle floorplan: 130nm TSMC

- Area: 2,2x1,36 mm²
- 101 PADs, 100µm pitch
- Power supply: 1,2 – 1,5 V
- Submission date: mid-may 2016

- Floorplan
  - (1) positive input preamps x6
  - (2) negative input preamps x6
  - (3) baseline channel (CERN) x1
  - (4) discriminators x4
  - (5) CRRC shapers: HG and LG
  - (6) digital part

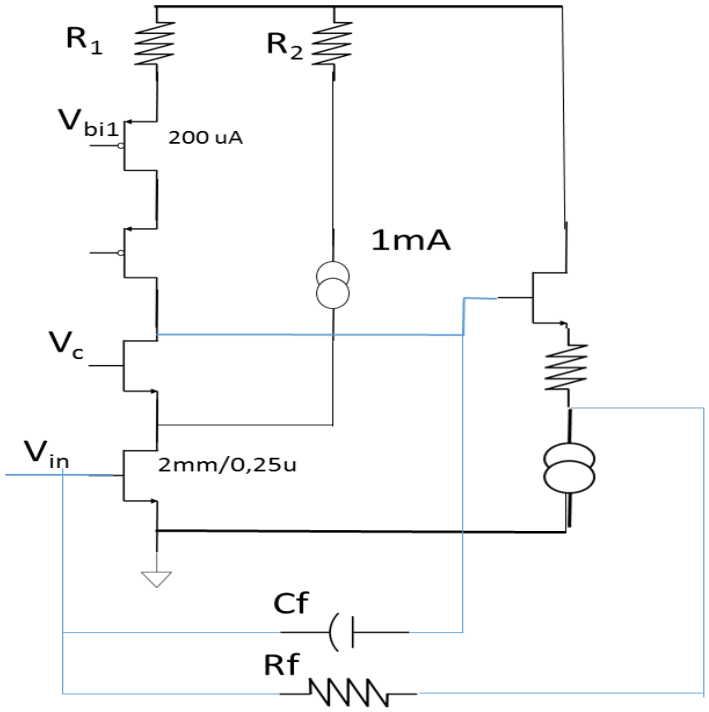
- Available outputs
  - Direct preamp output
  - Preamp after shaper
  - Preamp after discriminator

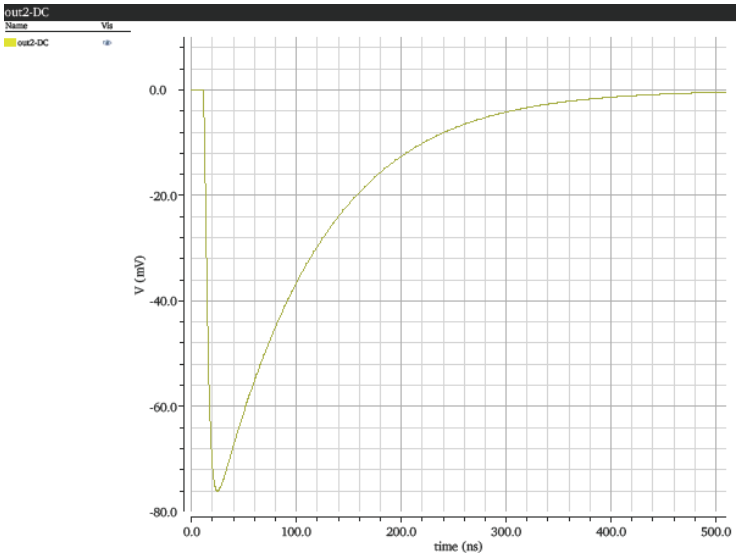
- Dedicated PAD available to characterize the shapers or the discriminators
- All bias can be externally tuned



(1) Input NMOS transistor preamplifier for positive signal

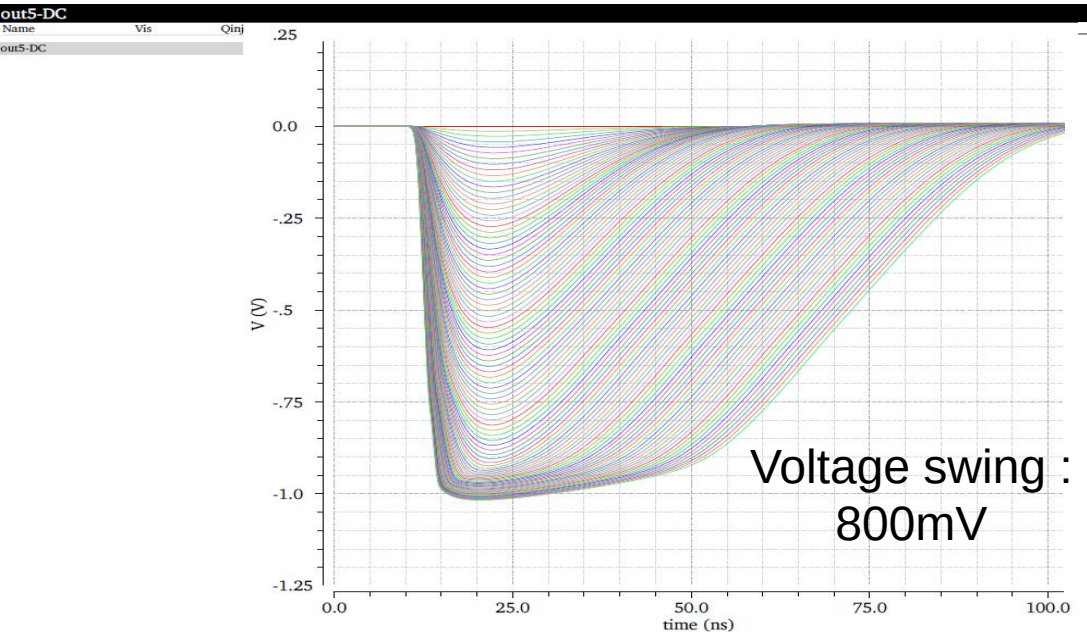
- 6 different preamps for positive signals
- Based on a cascode architecture with NMOS transistor
- Used different NMOS sizes (1200µ, 2400µ, 3600µ) and transistor flavors proposed by the technology (“normal”, “HiVt”, “LoVt”)
- Variable Cf from 100fF to 1,5pF step 100fF
- Variable Rf: 20k, 200k and 1MΩ
- Optimize to get open loop gain above 60dB and minimize noise
- Power consumption: ~2mW

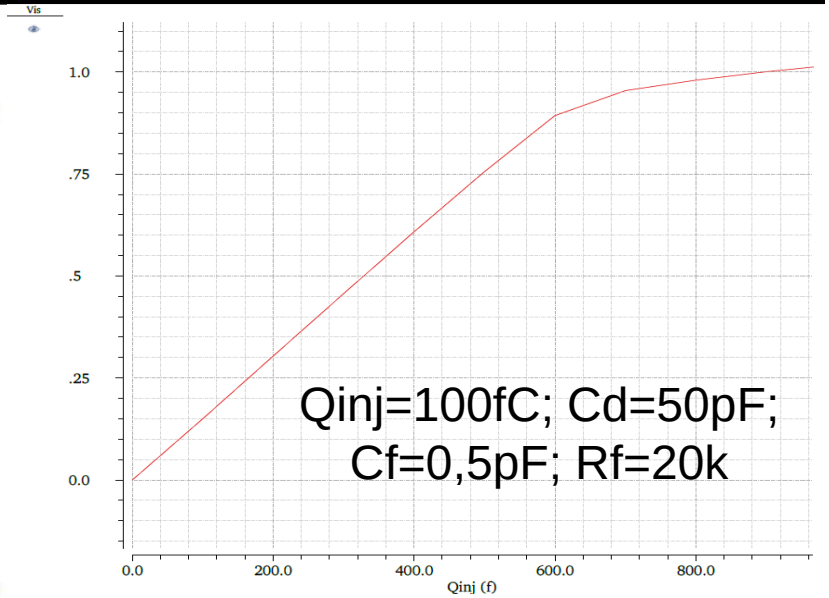


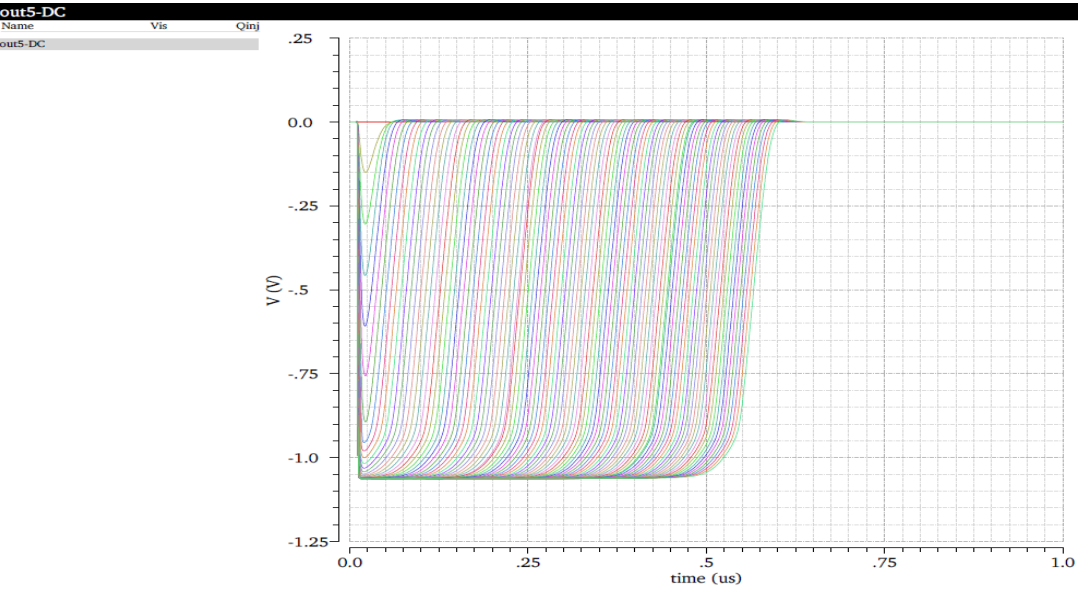


Qinj=100fC; Cd=50pF; Cf=1pF; Rf=20k

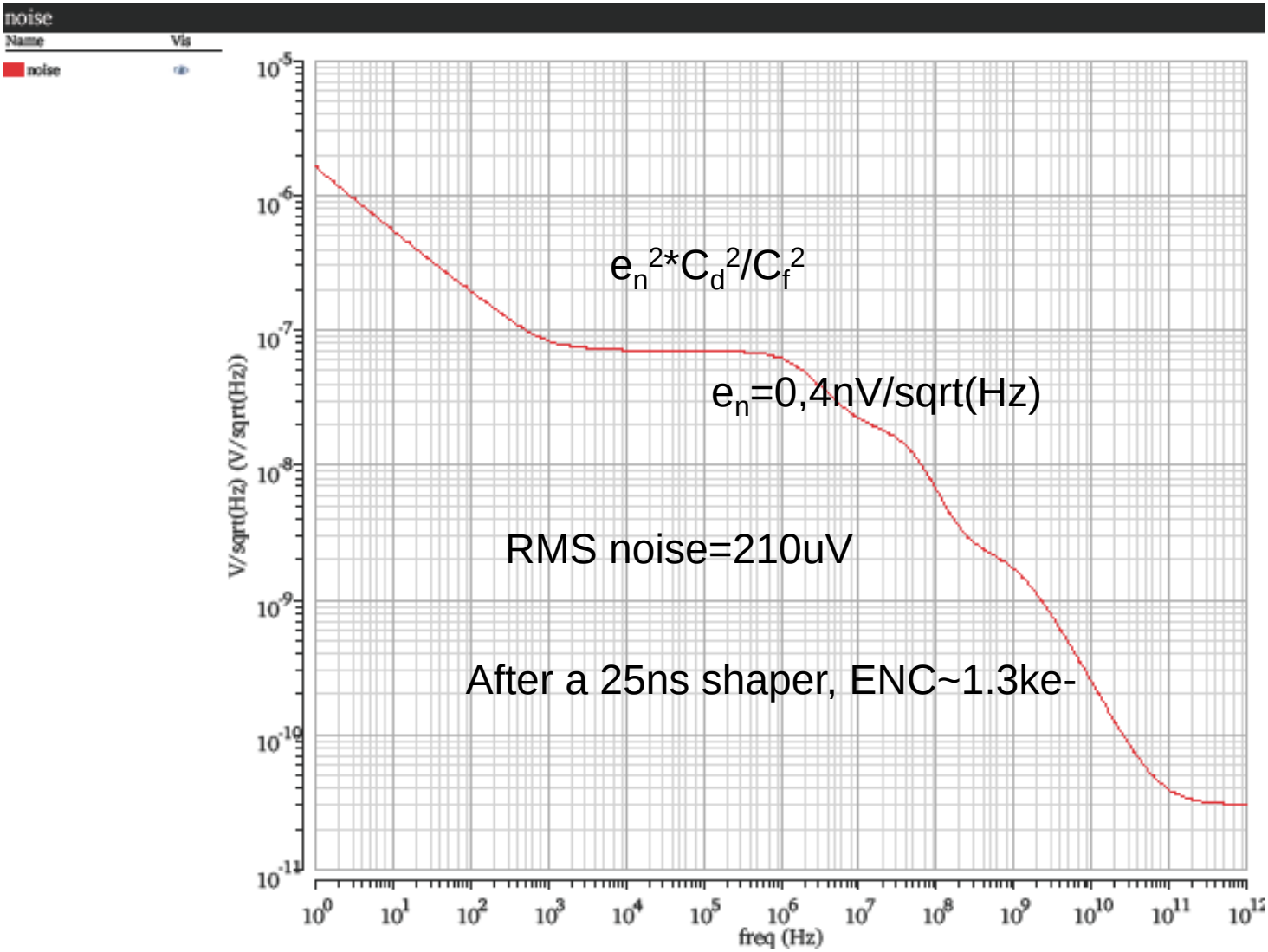
Input NMOS transistor preamplifier for positive signal





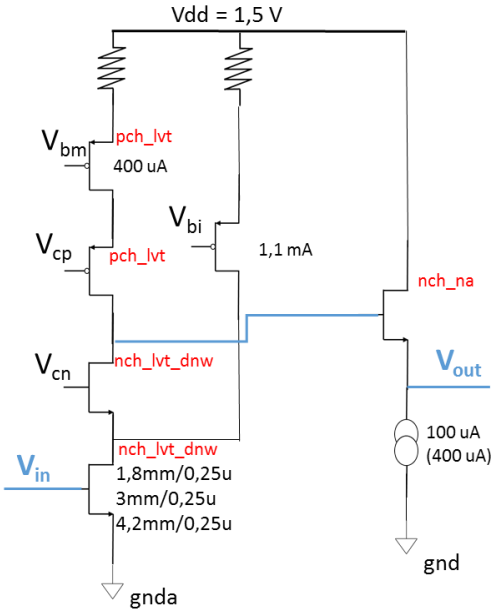


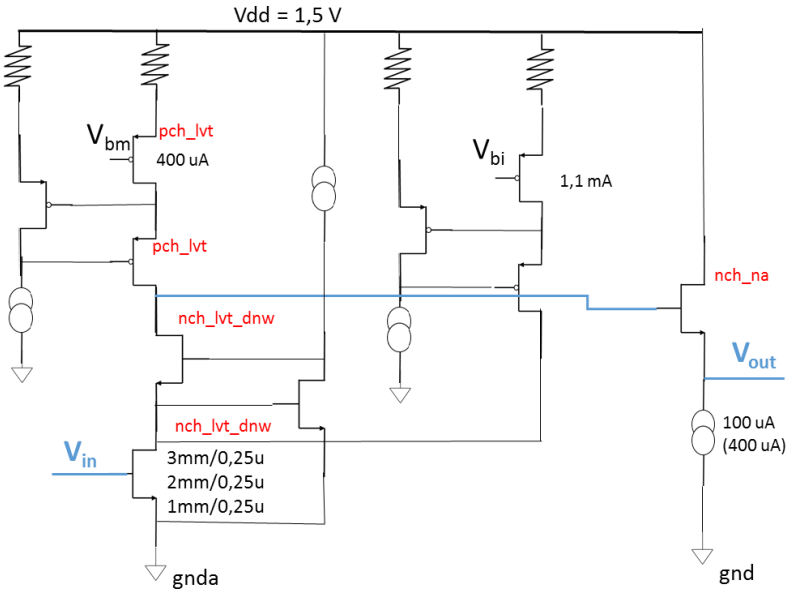
Input NMOS transistor preamplifier for positive signal



(2) Input NMOS transistor preamplifier for negative signal

- 6 different preamps for negative signals
- Used different NMOS sizes and architectures
- Variable Cf from 100fF to 1,5pF step 100fF
- Variable Rf: 20k, 200k and 1MΩ

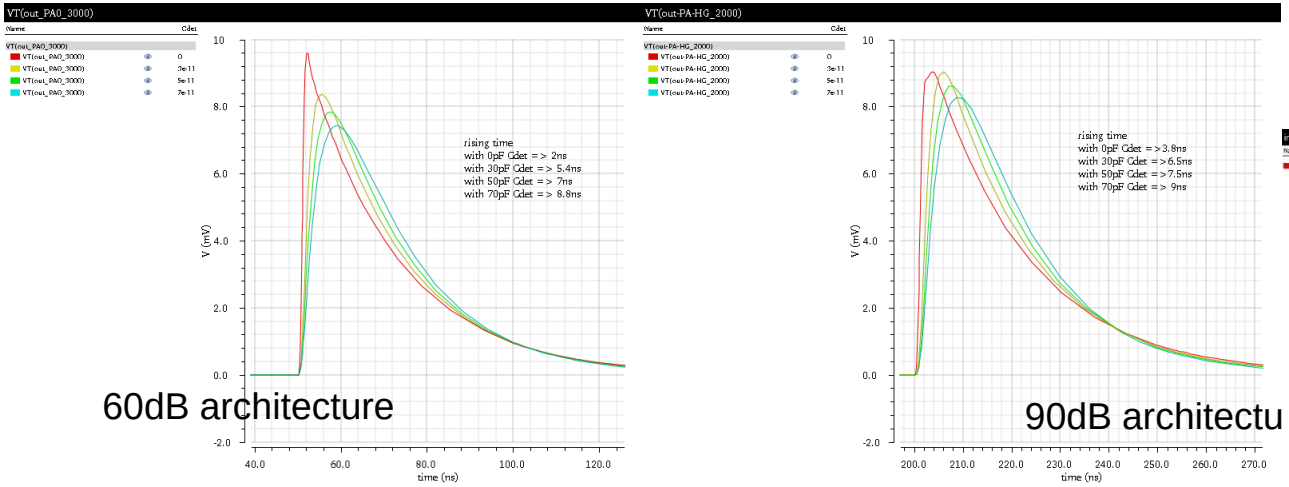


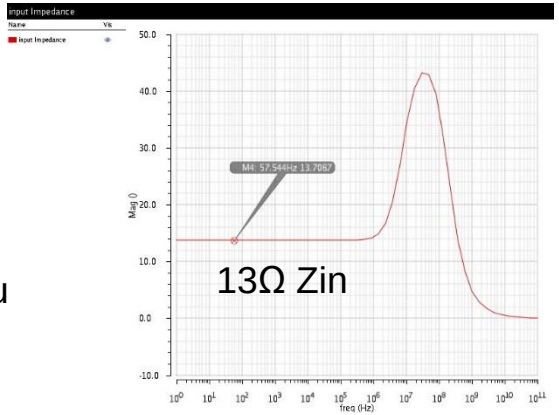


- Input stage: cascode with NMOS input transistor
- Output buffer: source follower with NMOS native transistor biased with 100µA
- 62 dB open loop gain; 2,4 GHz GBP; Input impedance: 16Ω (50Ω @ 50MHz)
- Power consumption: 2,4 mW (@ 1,5V)
- Three sizes of input NMOS transistors

- Input stage: regulated cascode with NMOS input transistor
- Output buffer: source follower with NMOS native transistor biased with 100µA
- 94 dB open loop gain; 3,5 GHz GBP; Input impedance: 0,5Ω (43Ω @ 50MHz)
- Power consumption: 2,85 mW (@ 1,5V)
- Well suited for high loop gain preamp (0,2pF Cf)
- Three sizes of input NMOS transistors

(2) signal shaper vs. Cdet



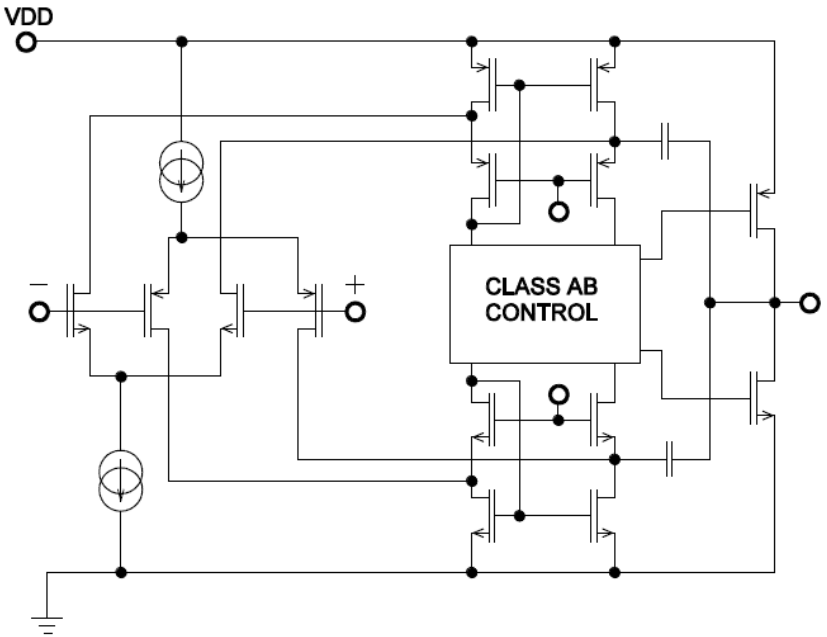


Input impedance, Rf=20k, Cf=0,5pF

ENC (electrons)	60dB negative preamp	90dB negative preamp
0pF Cdet, current sensitive	644	476
30pF Cdet, current sensitive	1058	910
60pF Cdet, current sensitive	1400	1320
0pF Cdet, charge sensitive	658	480
30pF Cdet, charge sensitive	959	844
60pF Cdet, charge sensitive	1200	1140

(5) CRRC shapers

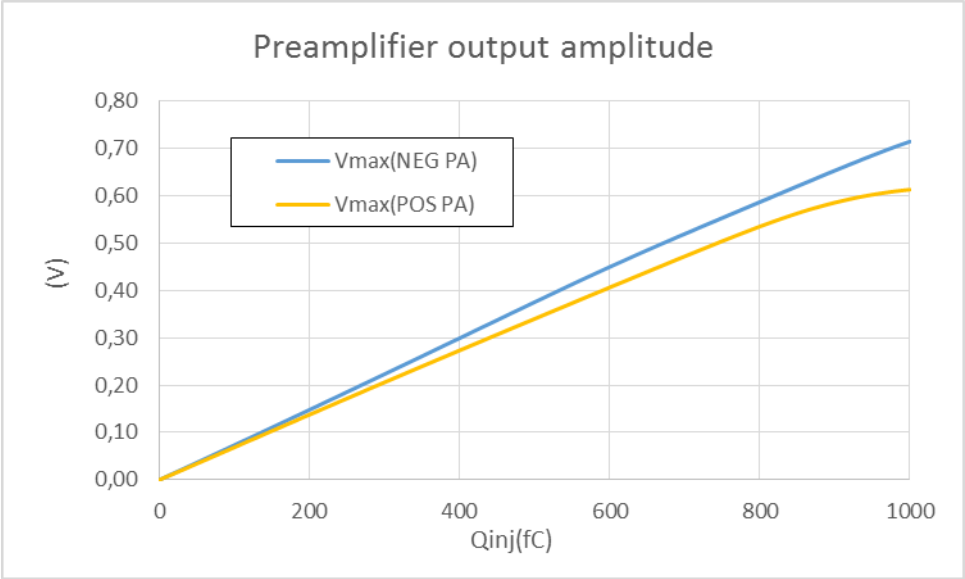
- Rail-to-Rail class AB operational amplifier
  - Cascode-miller compensation tunable on 5 bits
- 2 shapers
  - Gain 1 and gain 10
  - Variable shaping time: global 4 bits, from 5ns to 75ns
  - Based on Rail-to-Rail amplifier



(5) Preamplifier and shapers linearities

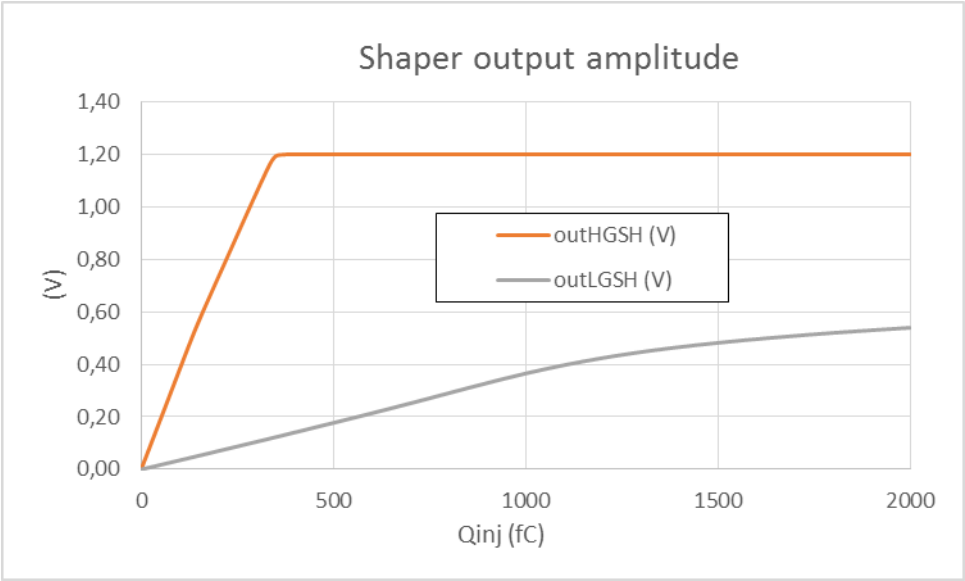
Preamplifier output

- Negative: +/- 0,5% linear up to 900fC
- Positive: +/-0,5% linear up to 800fC



Shaper output

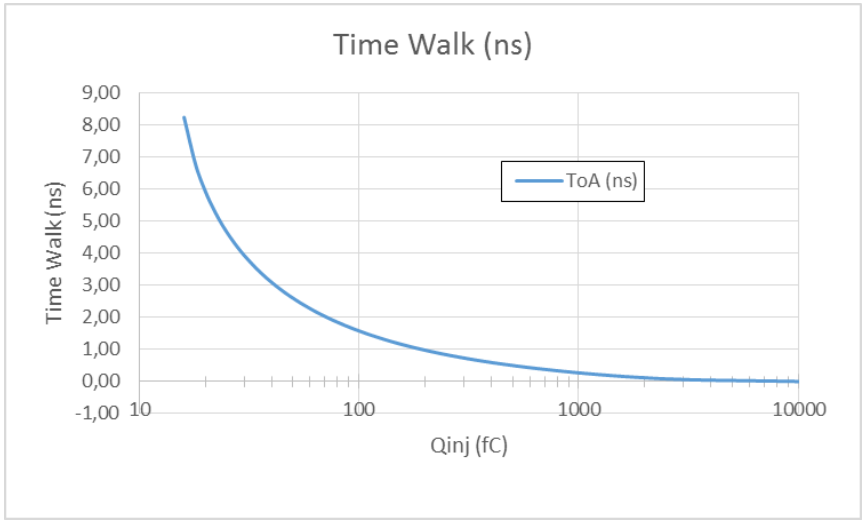
- High gain: +/- 1% linear from 0 to 400fC
- Low gain: +/-1% linear up to 900fC
- Lack of linearity for both low gain and ToT between 800fC to 1pC

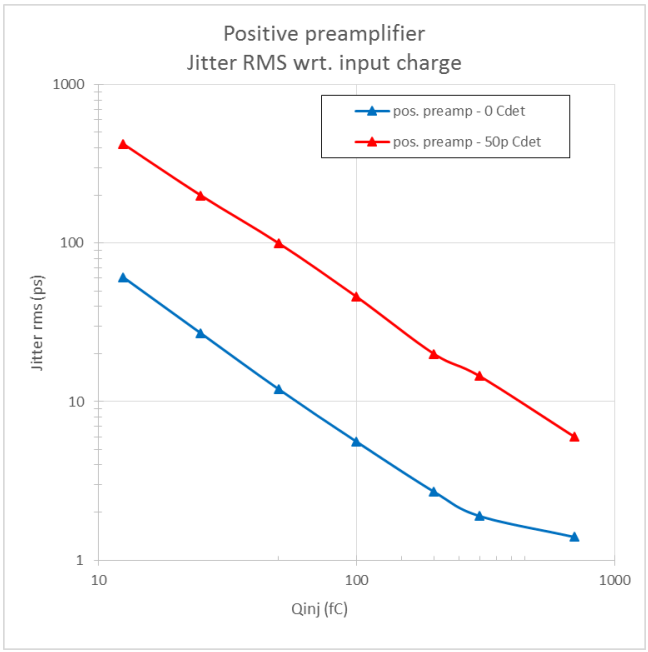


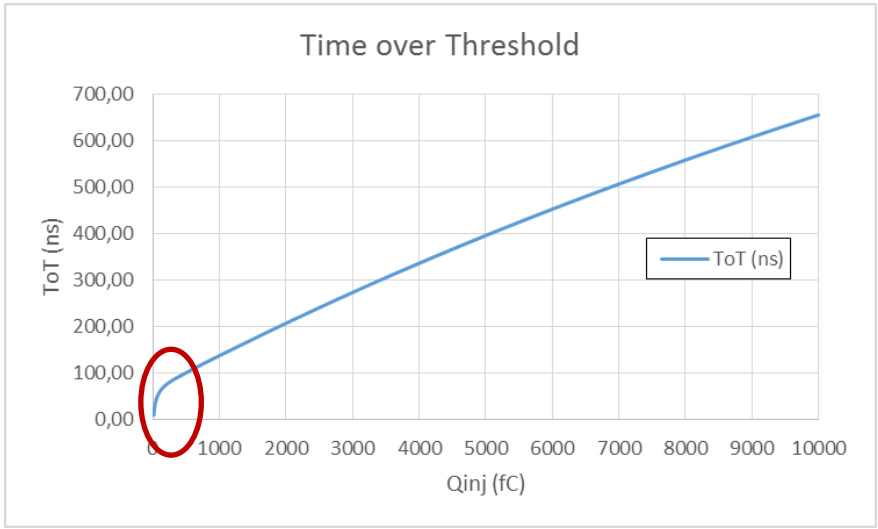
(4) Discriminators

- 4 fast discriminators designed (2 designs for each polarity) for ToA, ToT and ADC
- Power consumption: ~750uW
- Offset: 3,5mV rms

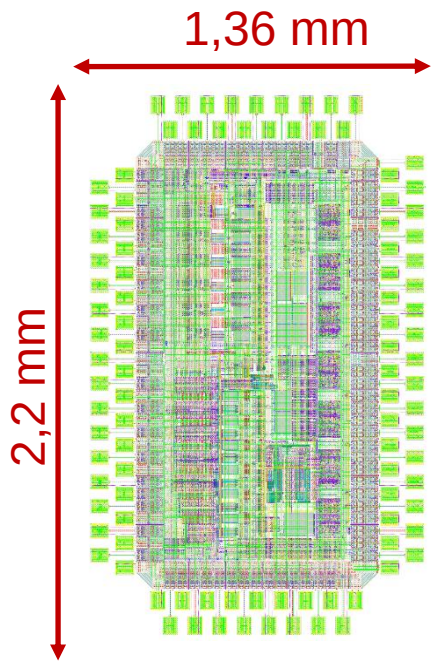
- Time Walk
  - 6ns @ 20fC (~7 – 14 MIP)
  - 1,5ns @ 100fC (~30 – 60 MIP)
- ToT
  - Linear from 1pC to 10pC
- Jitter
  - Without detector capacitance: 60ps rms @ 10fC (~3 - 6 MIP)
  - With 50pF detector capacitance: 400 ps rms @ 10fC (~3 - 6 MIP), 50 ps rms @ 100 fC (~30 - 60 MIP)
  - Jitter performances should be improved with a fast and high gain shaper after preamplifier

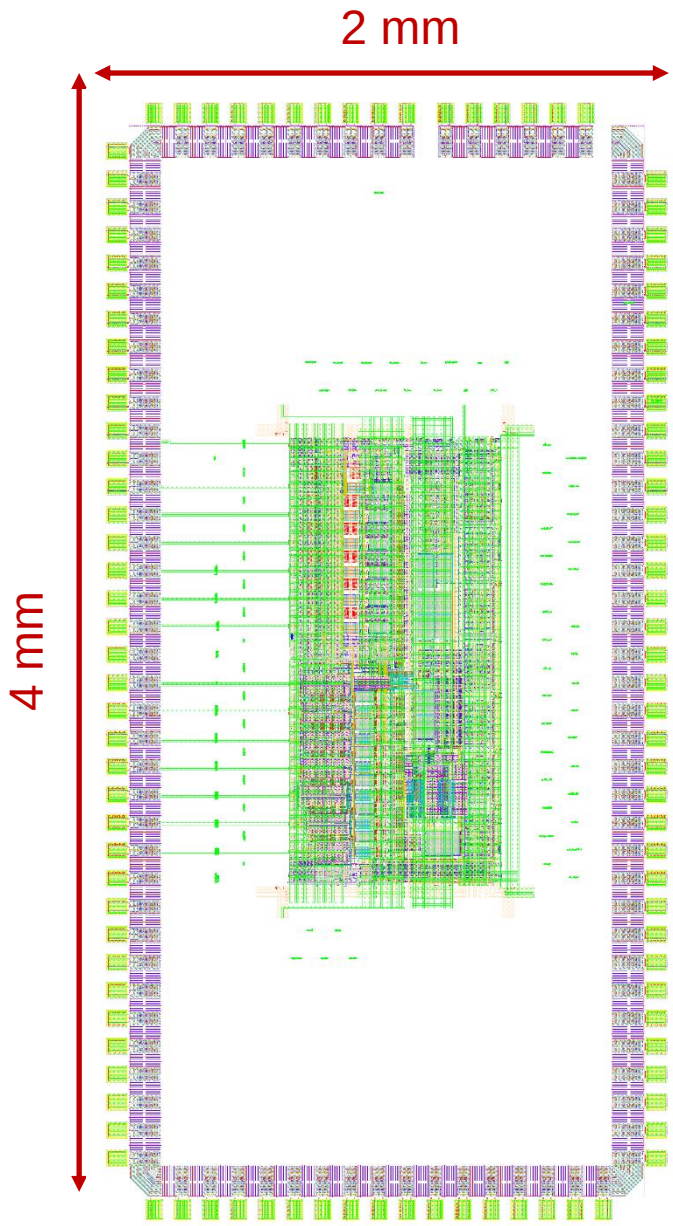






- Packaging issues
  - Wire bond angles between chip pads and package plots cannot be higher than 20°
  - Wire bond length issue
  - Finally enlarged pad ring => 2x4mm single in-line

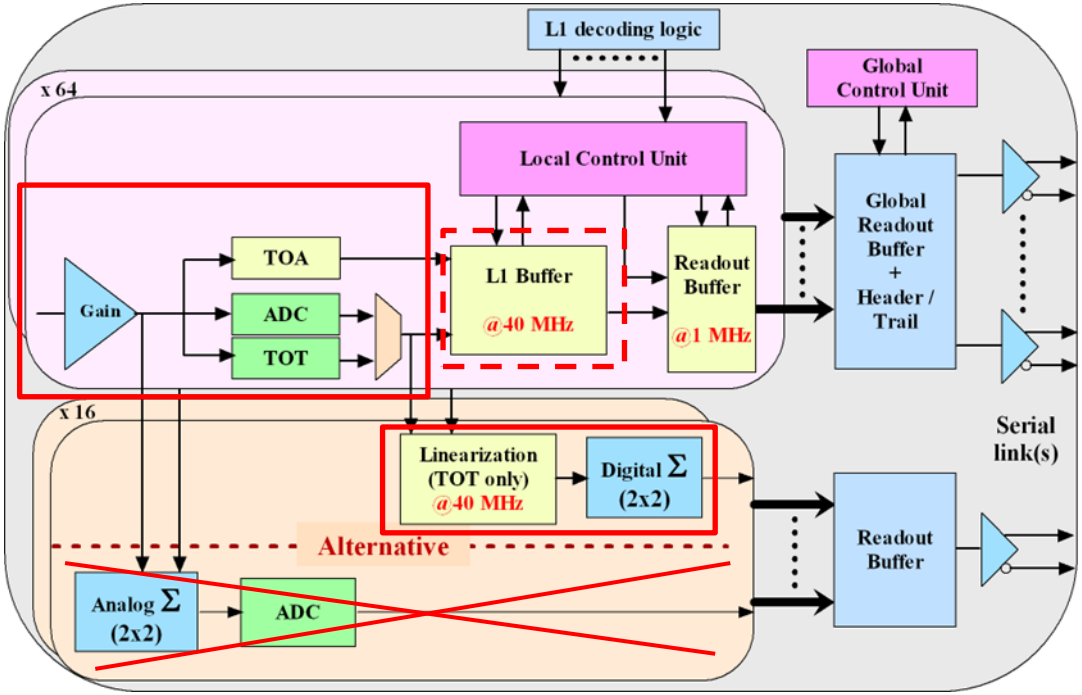




What do we plan to submit in TV2 ?

- Full analogue channel
  - Preamplifiers, shapers, comparators, input DAC (leakage compensation)
  - 10-bit ADC, 12-bit TDC
- Digital sum for trigger path
  - Linearization ToT @ 40 MHz
  - Digital sum: 2x2 cluster
  - L1 buffer for 1 MHz readout
- Common services
  - 10-bit DAC, bandgap, LVDS, PLL and DLL

September 2016



Conclusion

- “test vehicles” submitted in TSMC 130nm (May 2016)
  - Preamplifiers
    - Two polarities
    - 0.1, 0.5, 1, 3 pF Cf
    - 10k, 20k, 100k, 1M Rf
  - RtR Shapers
  - Fast discriminator for ToA

- Simulations are encouraging

Digital block: 1MHz readout architecture / trigger sums

- Study 2x2 linearization to be ready for 2nd TV:
  - ADC data
  - TOT without non-linear region
- Focusing on "method 3"
- Solution applicable for baseline or bi-gain PA

Paul slides @ TPG-BE electronics (26 April 2016)