Omega

New preamplifier in TSMC130nm for the ATLAS LArg Electromagnetic Calorimeter upgrade

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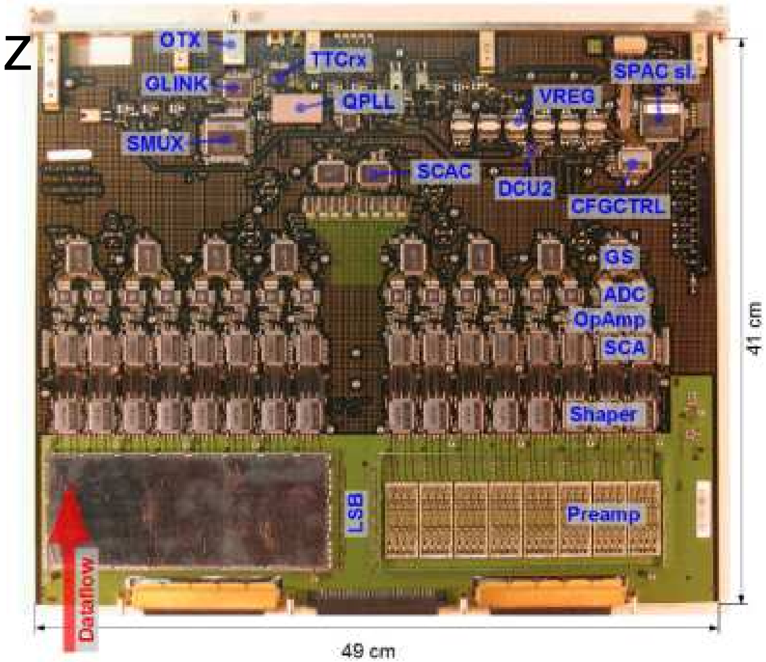
Organization for Micro-Electronics desiGn and Applications

Upgrade motivations for front-end readout

- Speed up the digitization up to 40MHz
- Decrease power dissipation by 10

  → Gather all blocks in an ASIC



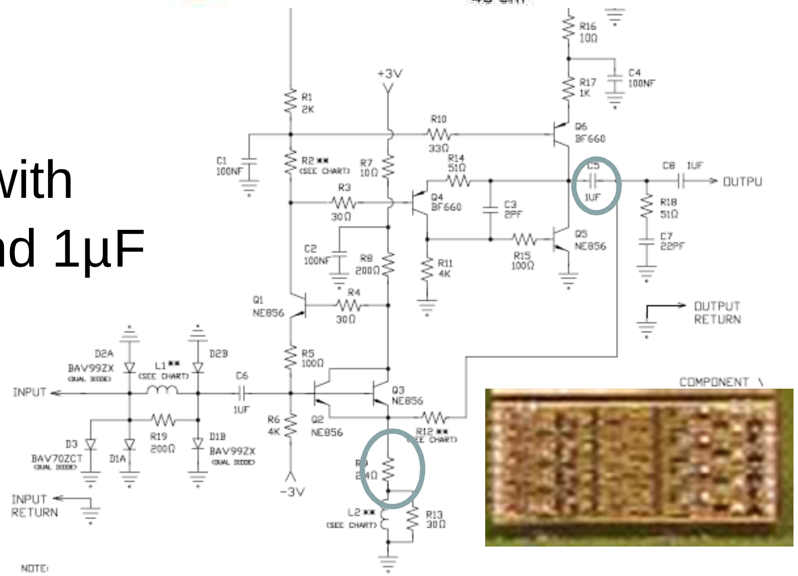
Cornerstone = Preamplifier :

"Universal" preamplifier with selectable dynamic range and input impedance (25/50 Ohm)

Preamp : 0T configuration with discrete components such as 2.4 Ω and 1µF

⇒ difficult to integrate in an ASIC

⇒ New design



PREAMP REQUIREMENTS

Ωmega

- Precise Input impedance Z_{in} 50 Ω (Front) or 25 Ω (Middle/Back) to terminate the cables from the detector
- Low noise < 10 Ω, with C_d 400 pF (Front) or 1 nF (Middle/Back) and tp=50 ns
- ENI as low as possible (large Cd, long duration signal) :

  0T50 400pF: ENI@50ns=55nA, 0T25 1.5nF: ENI@50ns=150 nA

- Dynamic range:
  - Input current 10 µA up to 2 mA (Front)
  - Input current 10 µA up to 10 mA (Middle/Back)
- Radiation resistance

New line-terminating preamp

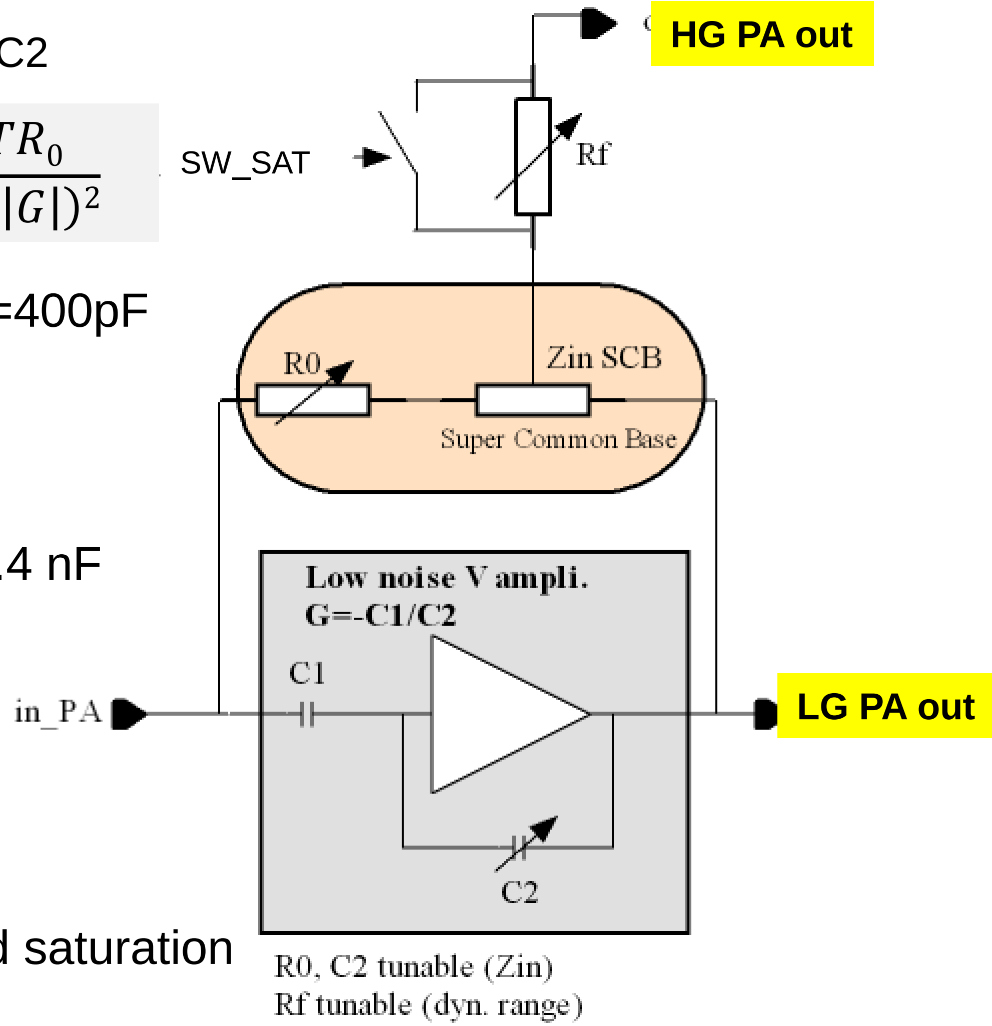
Ωmega

- New « negative noise figure preamp » (patent filed)
- Preamp Input impedance
  - Super Common Base: low input impedance
  - Amplifier = low noise voltage sensitive
  - Fine tuning of Zin (±5%) possible with C2

$$Z_{in}\,PA = \frac{R_0 + Zin(SCB)}{1 + |G|}$$

- Noise
  - Electronically cooled resistor $\dfrac{4kTR_0}{(1+|G|)^2}$

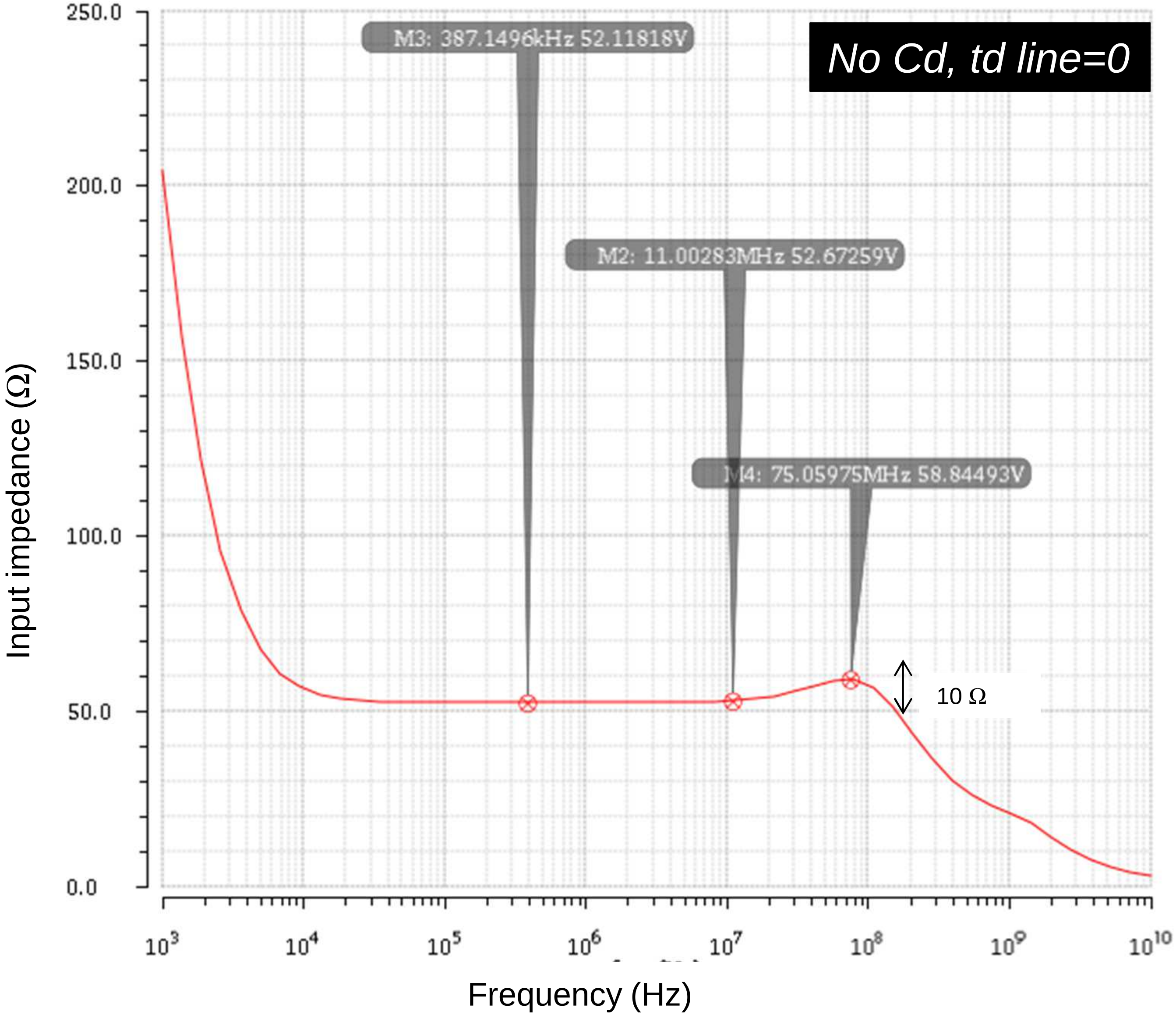
- Preamp 50 Ω, 10µA to 2 mA max, Cd=400pF
  - Z_{in} tuning: R_0= 500 Ω, G = -C_1/C_2=-9
  - Noise : 5 Ω
  - HG dynamic range: R_f =5K (or 10K)
- Preamp 25 Ω, up to10 mA max, Cd=1.4 nF
  - R_0= 100 Ω, G = - C_1/C_2 = -3
  - Noise : 6 Ω
  - HG dynamic range: R_f =1K (or 2K)



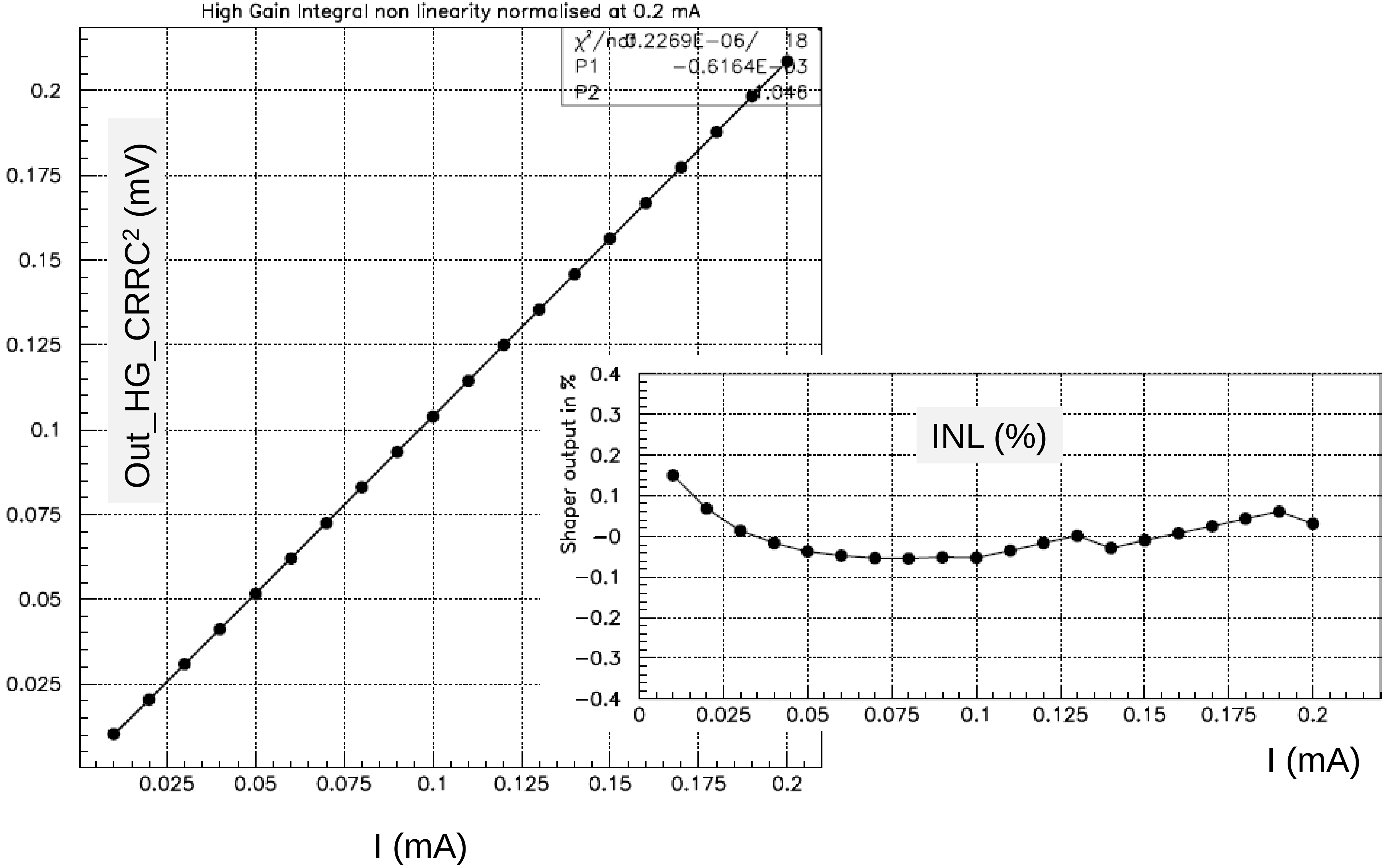
- HG and LG outputs available :

Switch (SW_SAT) to short Rf and to avoid saturation

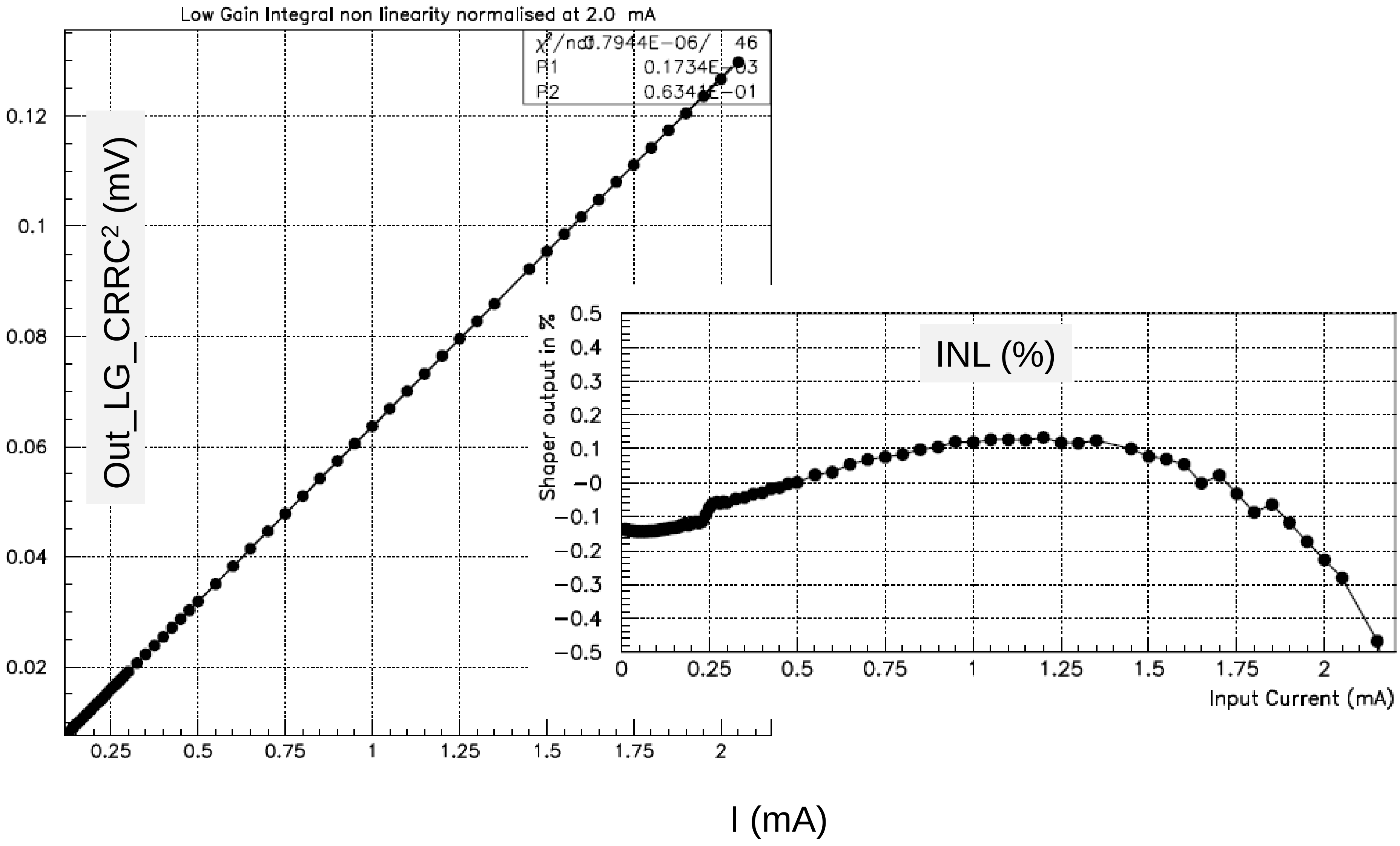
Simulation results: Zin (50 PA) vs frequency



Simulation results: 50 Ω HG CRRC² Linearity



Simulation results: 50 Ω LG CRRC² Linearity



Simulation results: Zin 50 Ω PA vs Input current

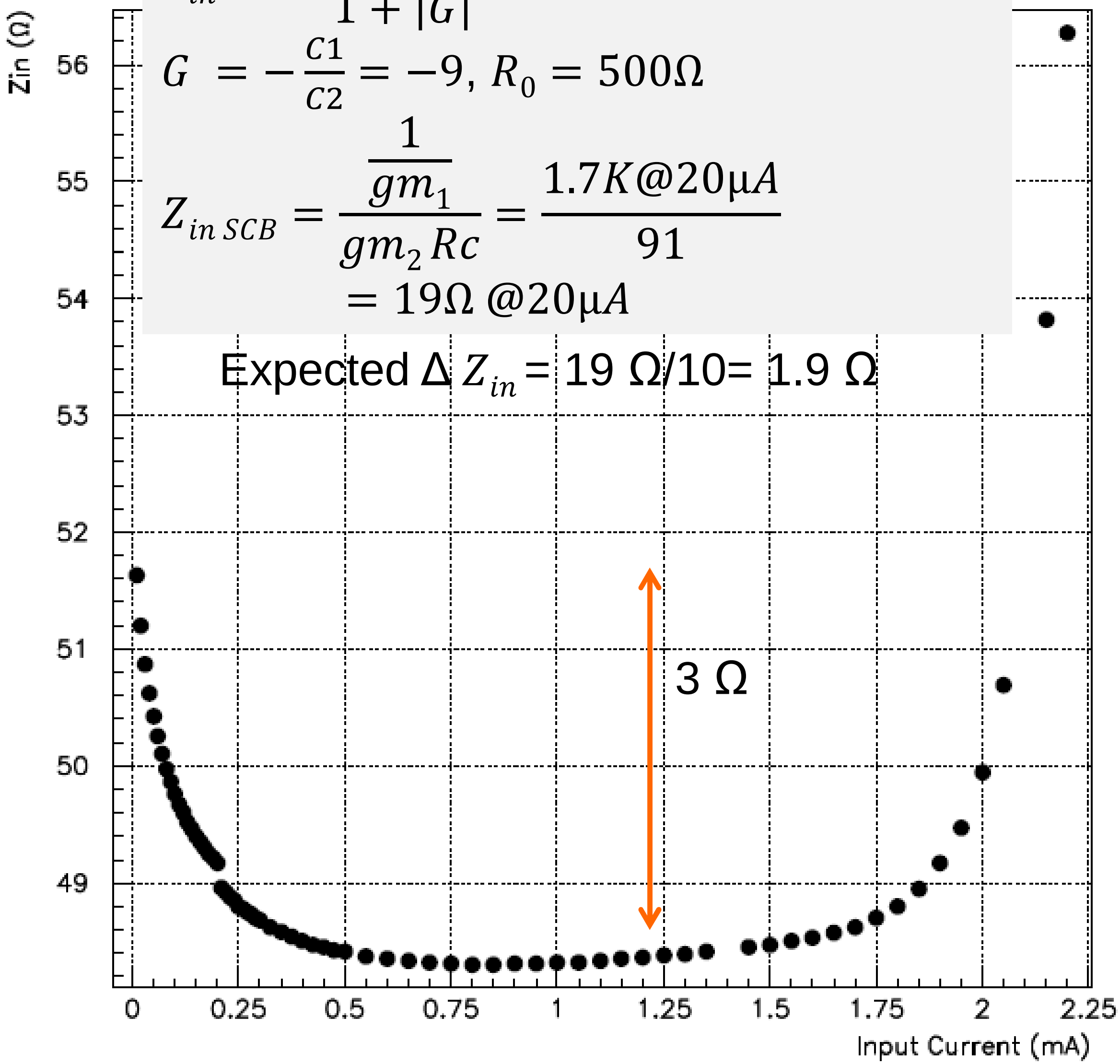
$$Z_{in} = \frac{R_0 + Zin_{SCB}}{1 + |G|}$$

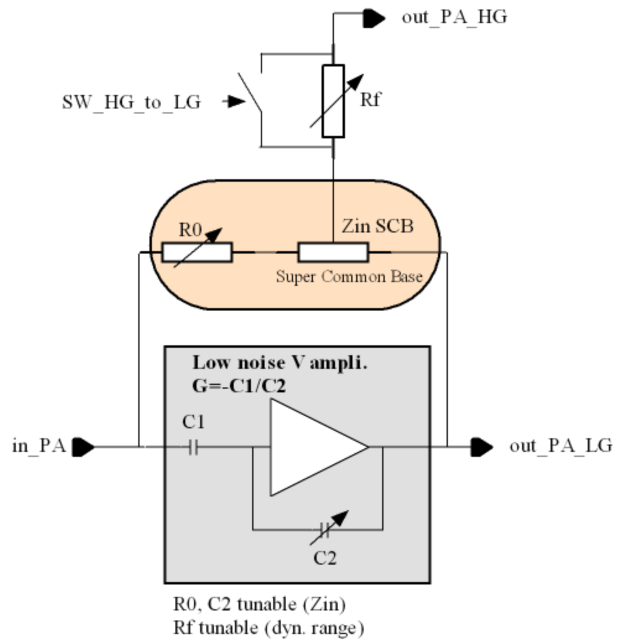
$$G = -\frac{C1}{C2} = -9,\ R_0 = 500\Omega$$

$$Z_{in\,SCB} = \frac{\frac{1}{gm_1}}{gm_2 Rc} = \frac{1.7K@20\mu A}{91}$$

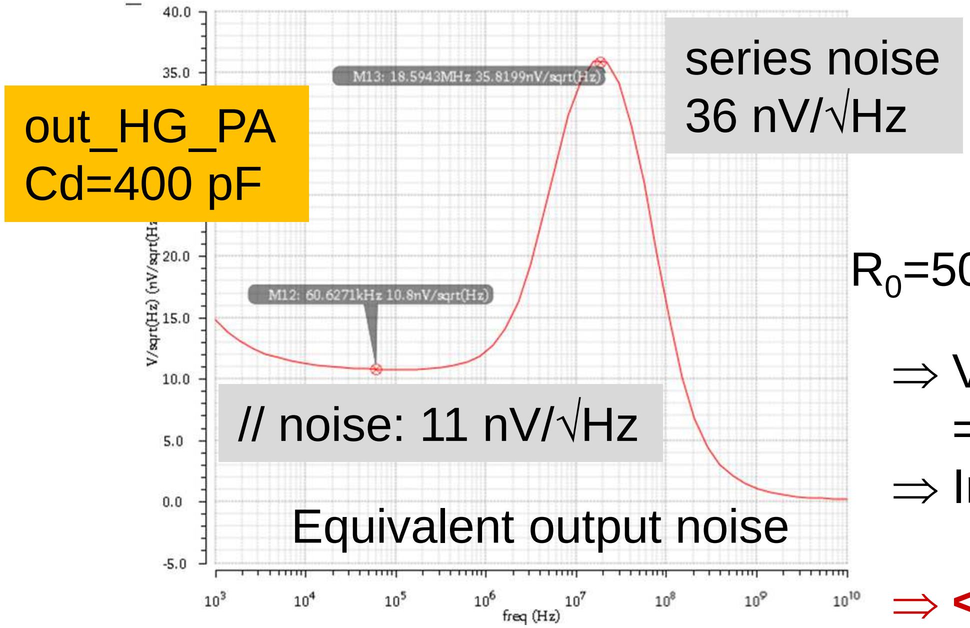
$$= 19\Omega\ @20\mu A$$

Expected ΔZ_{in} = 19 Ω/10= 1.9 Ω





Simulation results: HG 50Ω PA Noise



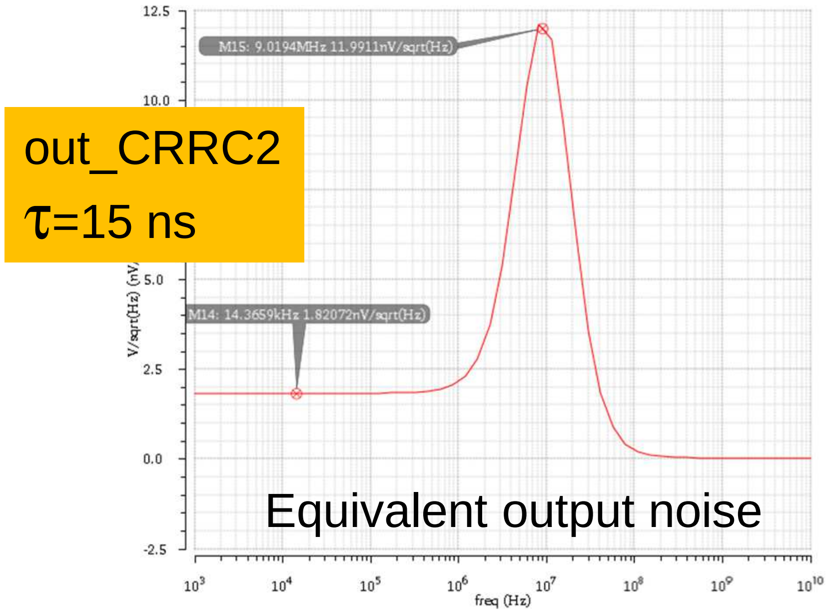
$$\frac{4kTR_0}{(1+|G|)^2}$$ with G=-9

R_0=500 Ω =>Equ. Noise: 0.28 nV/sqrt(Hz) or 5 Ω

⇒ Voltage gain @ output of the preamp R_f / Z_{in} =5K/50=100

⇒ Input Noise: 36 nV/100=0.36 nV/√Hz or 8 Ω

⇒ < 10 Ω requirement



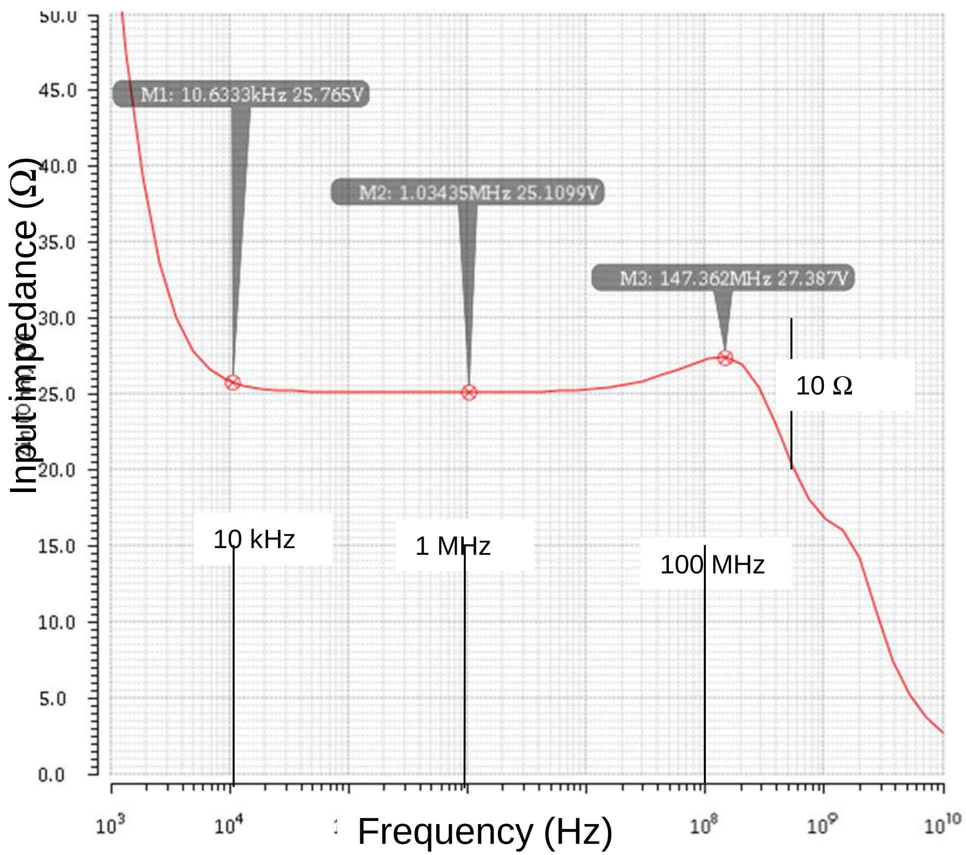
rms noise= 46 µV
I_{det} =100 µA gives 100 mV at the output of the HG $CRRC^2$

=> ENI=46 nA

ENI similar to the ENI measured with the current 0T

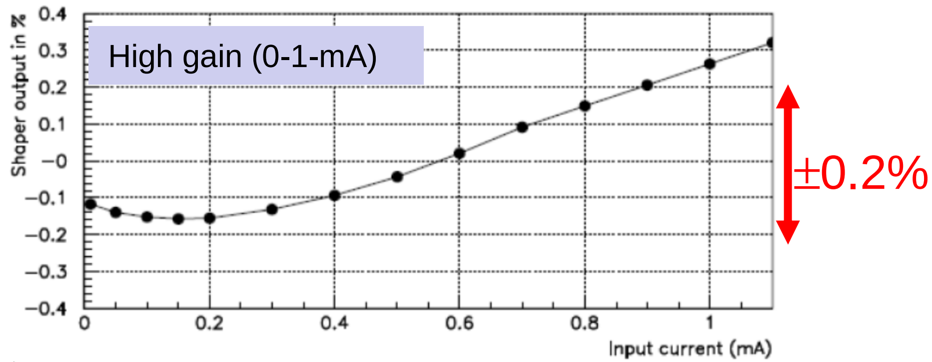
0T50 400pF: ENI@50ns=55nA,
0T25 1.5nF: ENI@50ns=150 nA

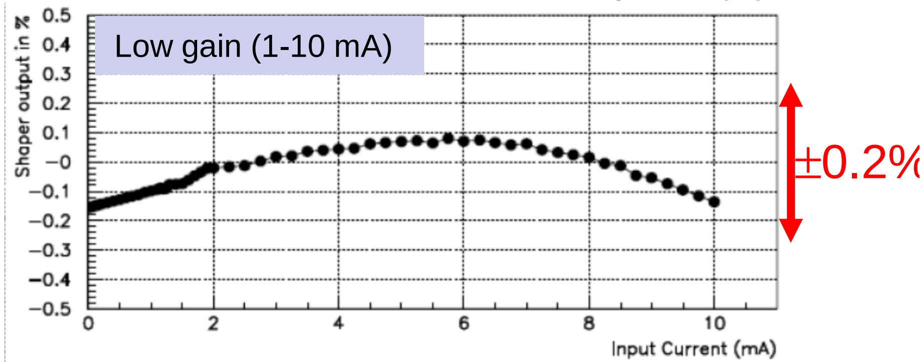
Simulation performance results (25 Ω /10 mA)



Impedance flat from 10 kHz to 100 MHz
< 1 Ω variation versus current due to
Super Common base Zin variation

Integral non linearity (/linear fit) with CR-RC2 (40 ns peaking time)



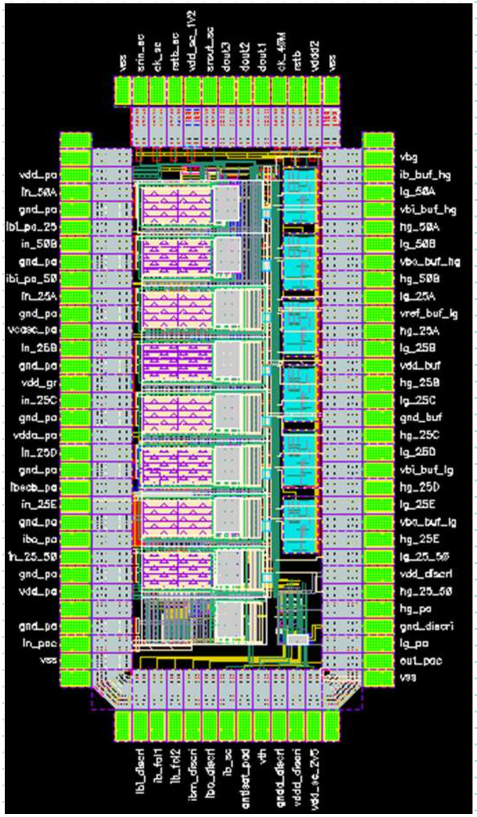


Noise dominated by R0 and NMOS ampli : 150 nA with 1.5 nF

Chip submitted

8 channels with various preamps :

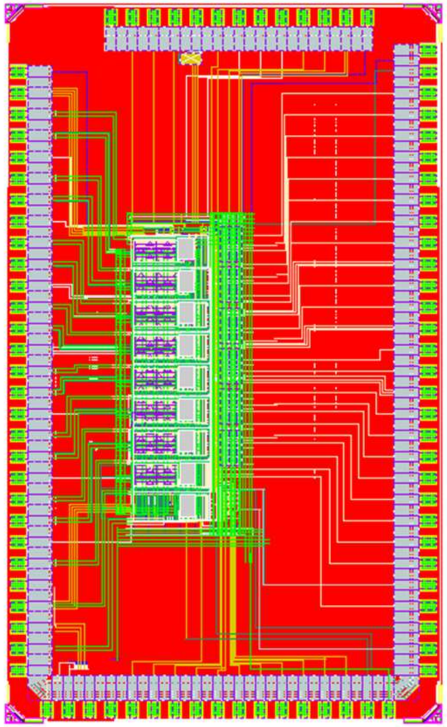
	Zin	Gain&Dyn range	Others
PA 50A	Fixed Zin (fixed R0 and C2)	Fixed Rf	
PA 50B	Adjustable Zin (with C2)	Adjustable Rf	
PA 25A	Adjustable Zin (with C2)	Adjustable Rf	Input trans area = Nominal size
PA 25B	Adjustable Zin (with C2)	Adjustable Rf	Input trans area = Nominal size/2
PA 25C	Adjustable Zin (with C2)	Adjustable Rf	Input trans area = 2xNominal size
PA 25D	Adjustable Zin (with C2)	Adjustable Rf	protection diodes
PA 25E	Fixed Zin (with C2)	Fixed Rf	
PA 25-50	Switches to choose 25 or 50 Ω Adjustable Zin (with C2 and R0)	Adjustable Rf	



Slow Control parameters and switches to change R_0 and C_2 (Zin) and R_f (dyn. Range)
Each PA can be switched OFF when not used. Outputs (HG and LG) go to pads thru buffer and LG go to discri
Discri provides antisat signal (1 architecture with 3 various grounding to characterize techno).
24-bit counter triple voting @ 100MHz to test the digital kit and to simulate digital activity in chip.

Conclusion

Use of 130 nm layout kit has shown to be a bit difficult but chip was submitted on May 15th through CERN/IMEC .



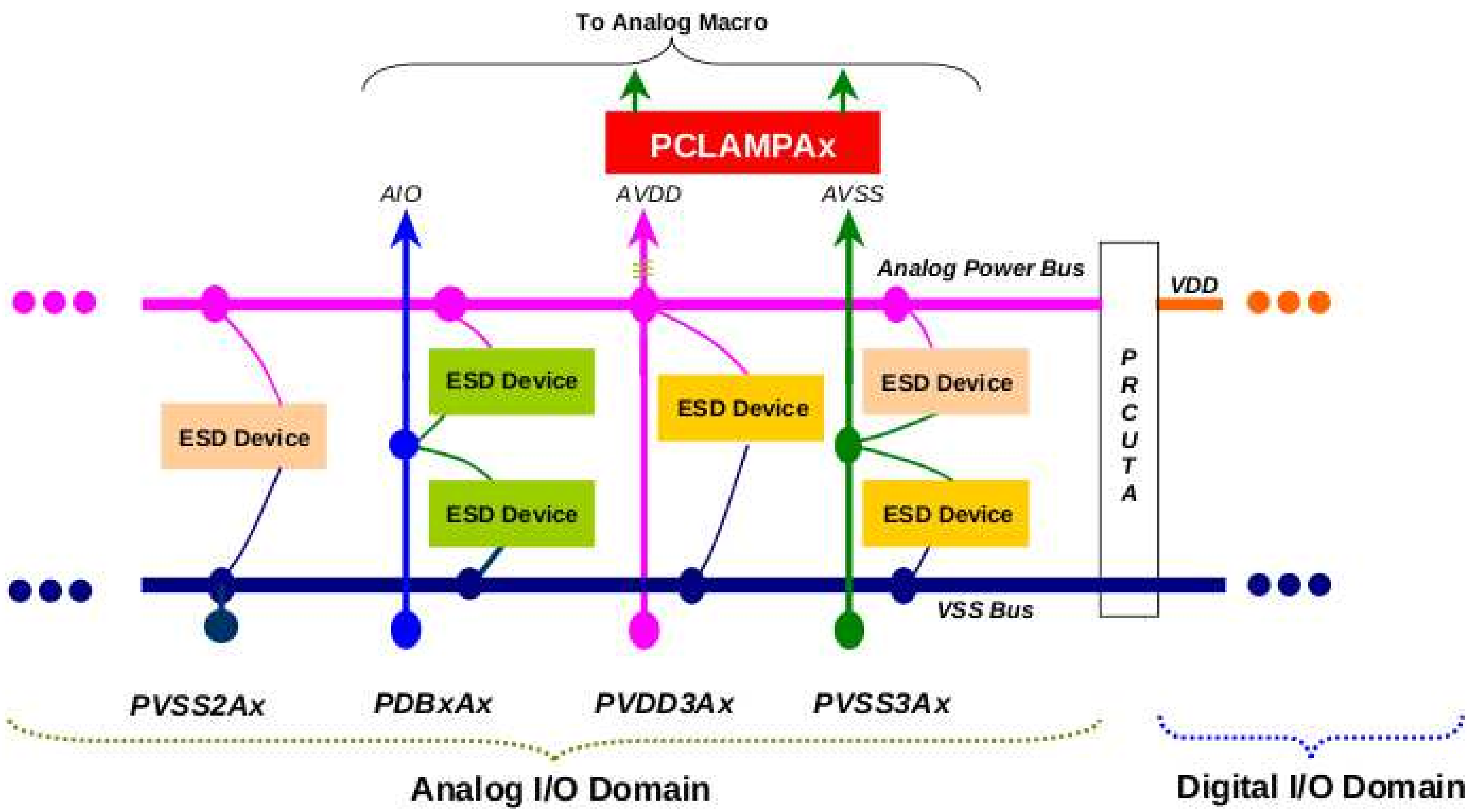
- Collaboration: LAL, OMEGA (+BNL)
  - LAL: N. Morange, L. Serin, S. Simion
  - OMEGA: P. Dinaucourt, C. de La Taille, G. Martin-Chassard, N. Seguin-Moreau
- Integrated preamp
  - 3 designs: OMEGA+LAL (130nm CMOS), BNL (65 nm CMOS) and Penn University (130nm SiGe)
  - Collaborative effort with BNL to converge toward common achitecture
- Testbench designed by LAL + BNL
  - Preamps characterization
  - Irradiation tests

mega

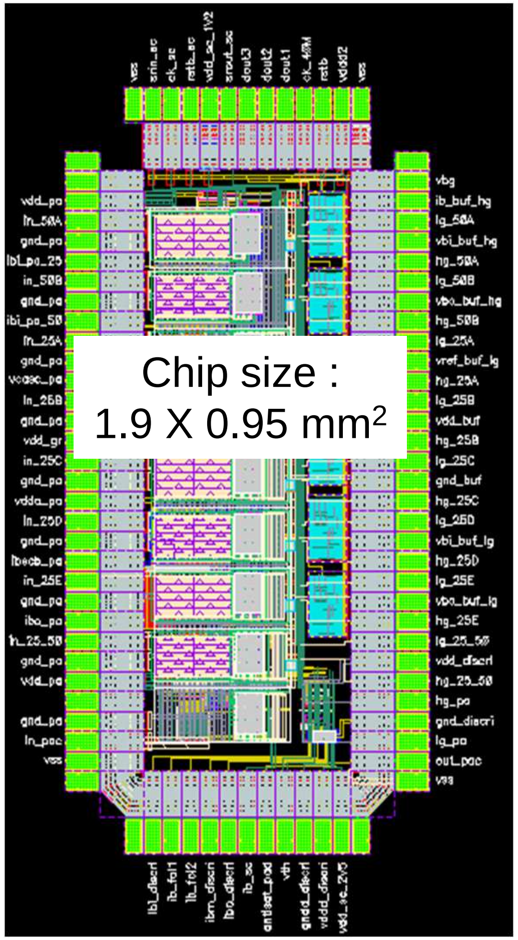
- Pour séparer les masses numeriques et analogiques :

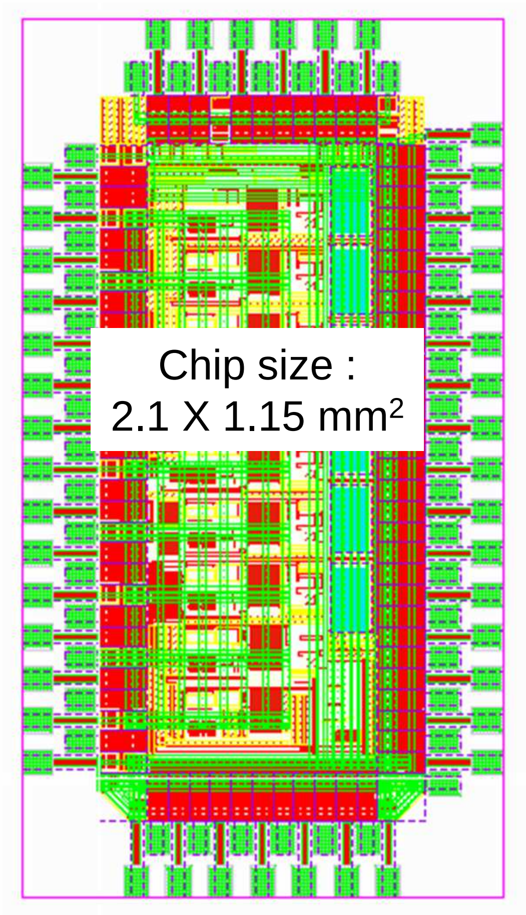
PVSS3A non relié au VSS mais necessite un PCLAMP

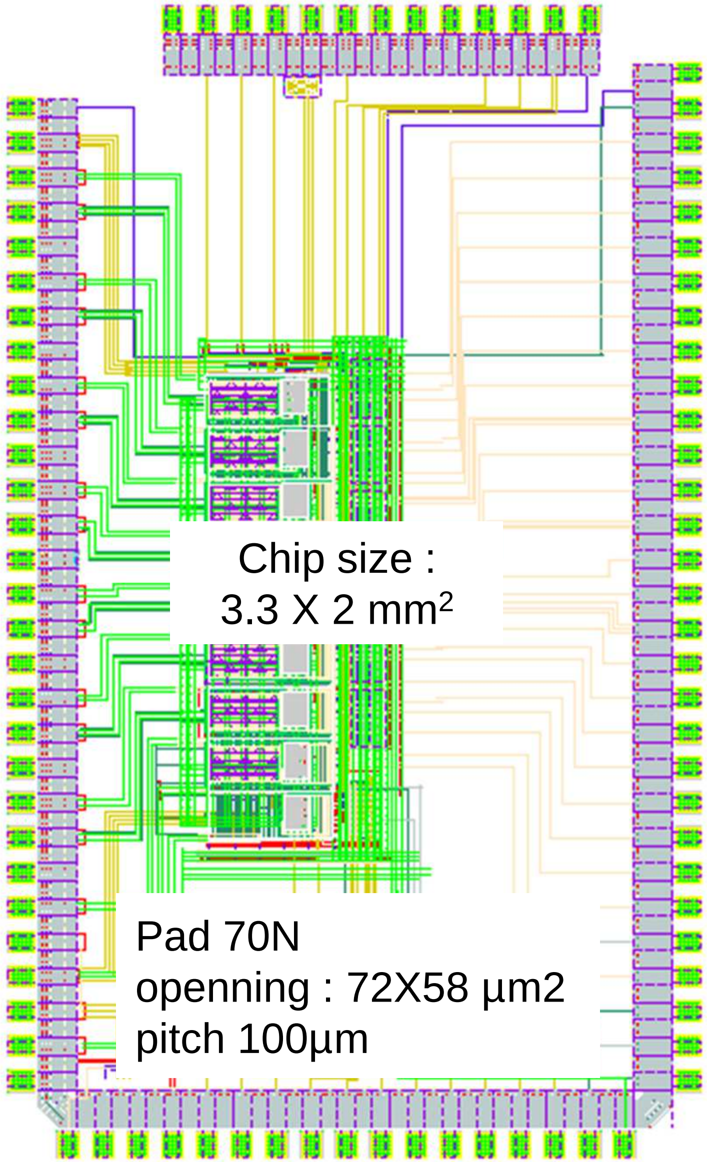
- Pour séparer les alim. PRCUTA



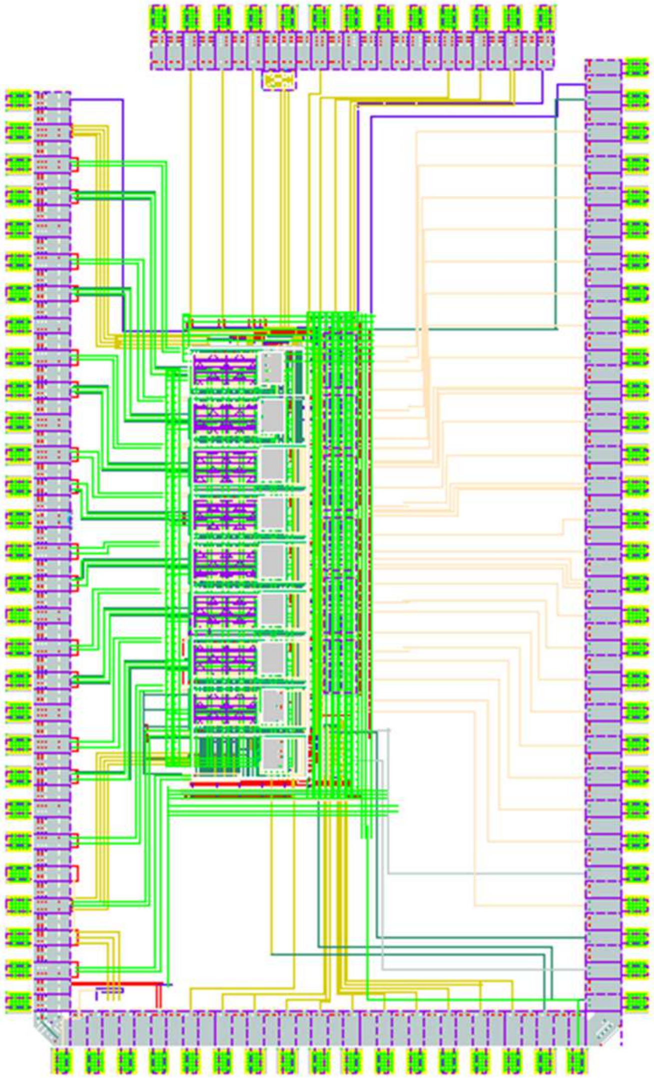
Packaging in PGA144 – cavity : 10X10 mm2







Pad 70N + 70G (en quinconces)
openning : 72X58 μm^2
pitch 50µm



Sealring :
- scribeline
- corners

Filling :
- diffusion
- metalx
- slots