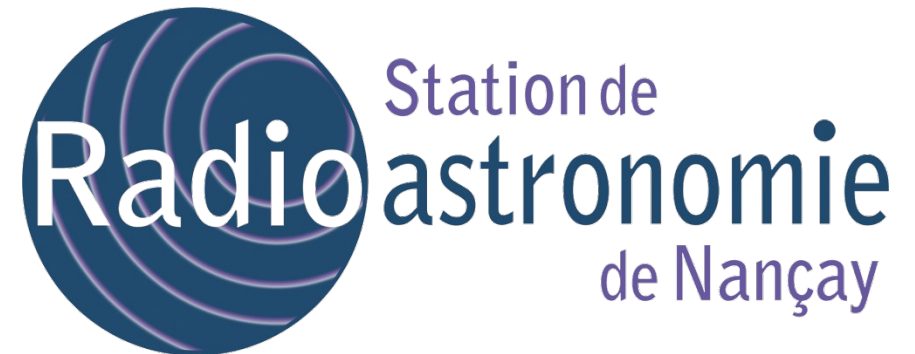


IN2P3 FPGA System Planner

Journées VLSI 2016

NEBULA DESIGN

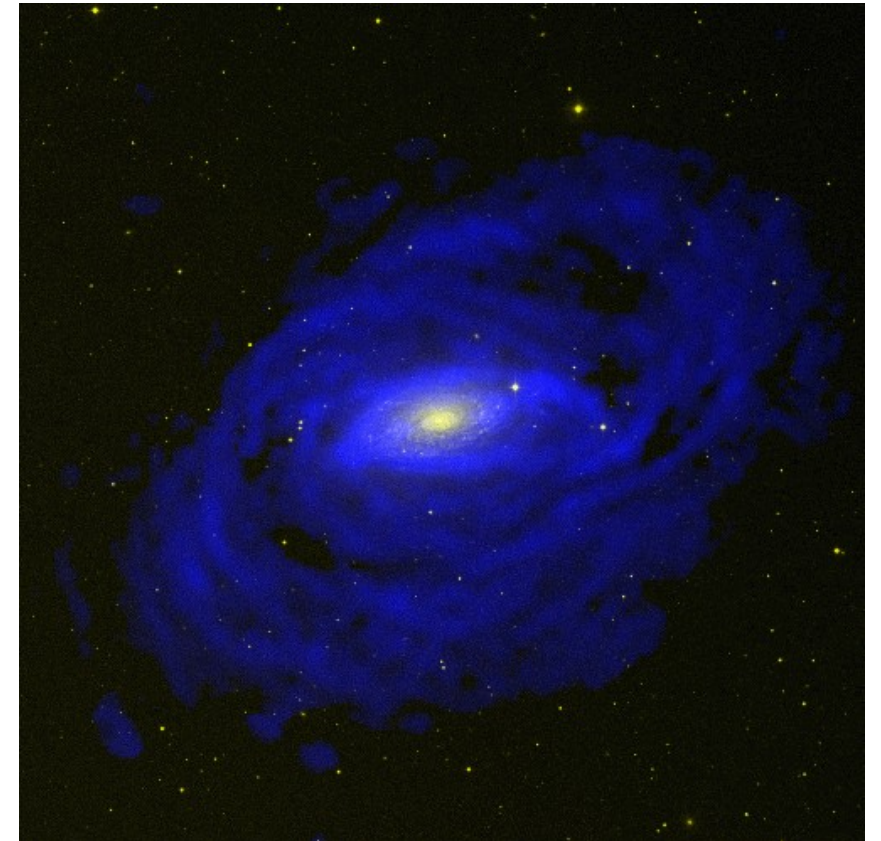


Agenda

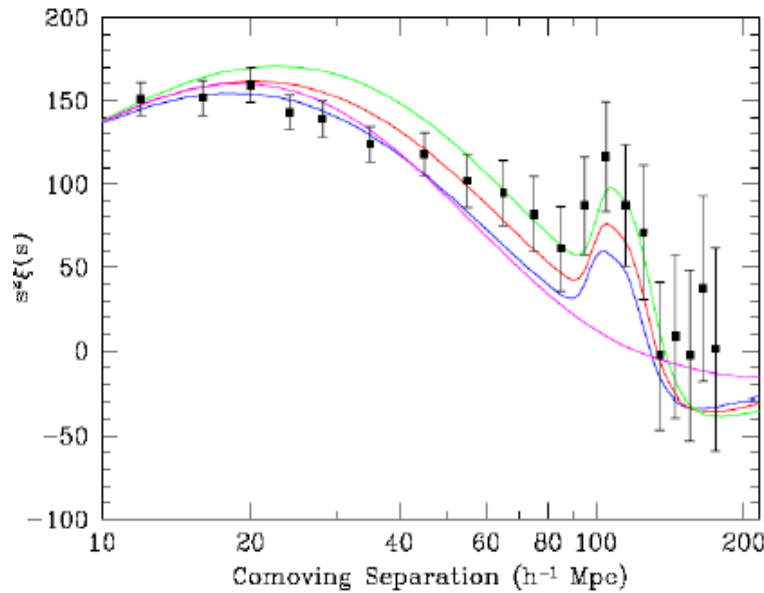
- PAON IV project
- NEBULA board
- IN2P3's old design methodology
- Overview of FSP
- IN2P3's methodology using FSP
- Improvements seen by using FSP

BAO project in radio

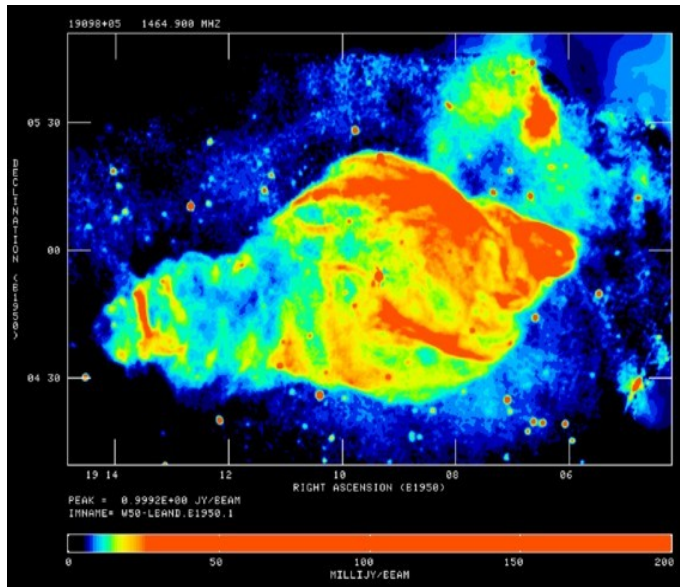
**Fast acquisition
system
for 3D mapping of
cosmological
matter
distribution in radio**



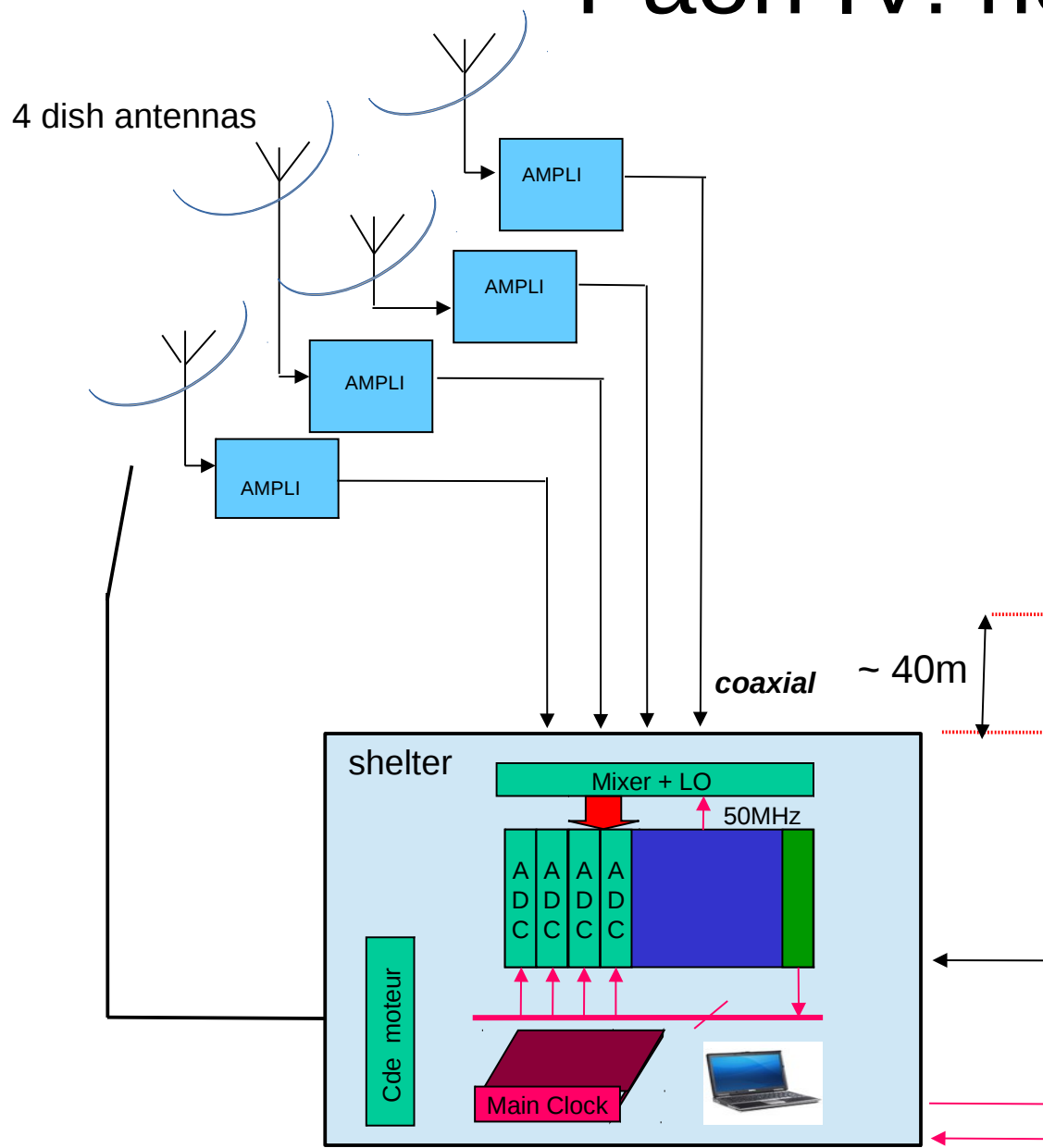
BAO : Baryonic Acoustic Oscillations



- Imprints left by the baryon-photon fluid (before recombination) in the distribution of ordinary (baryonic) matter
- Slight modulation of the distribution of matter, (and galaxies as tracers). Structure formation being mainly driven by CDM which dominates structure formation
- In Radio : Use 21 cm HI emission
- 3D HI mass distribution measurement through total 21 cm emission intensity mapping (No individual galaxy detection)
- Hyperfine transition (spin-orbit) of atomic hydrogen: $\nu \approx 1,420405$ GHz $\rightarrow \lambda \approx 21$ cm



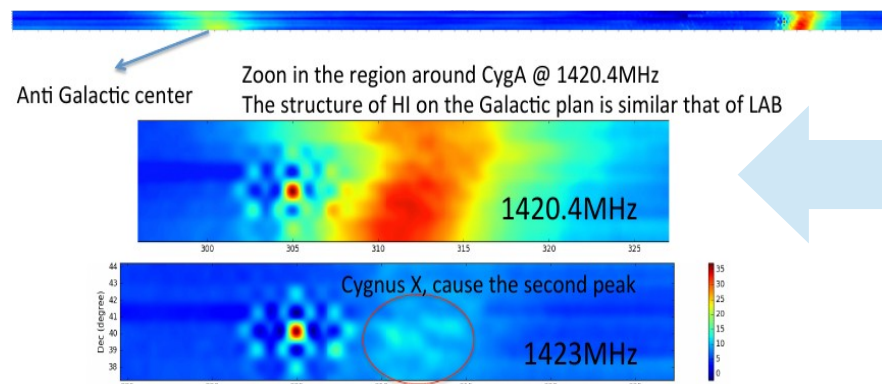
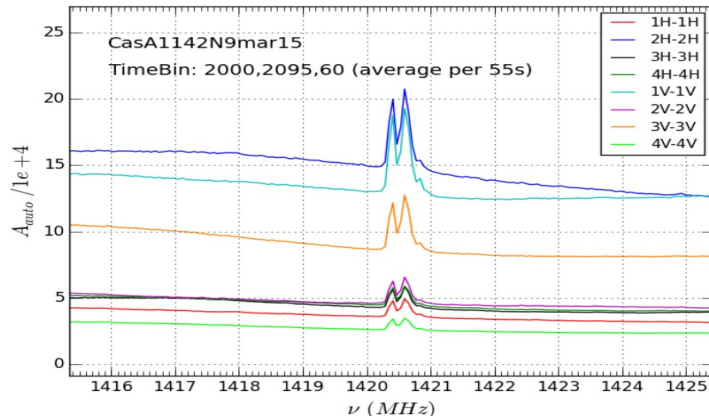
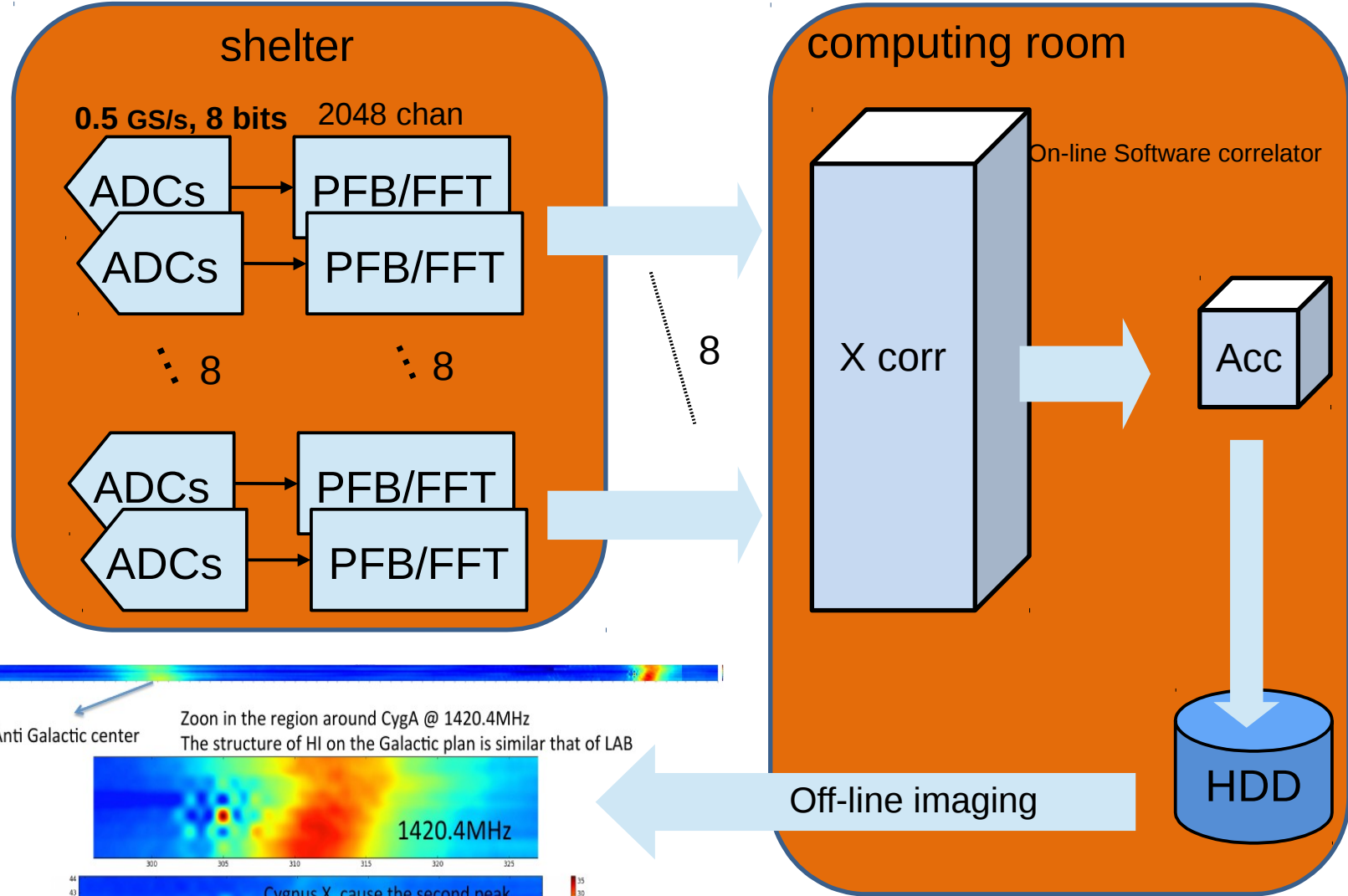
Paon IV: nowday Configuration.



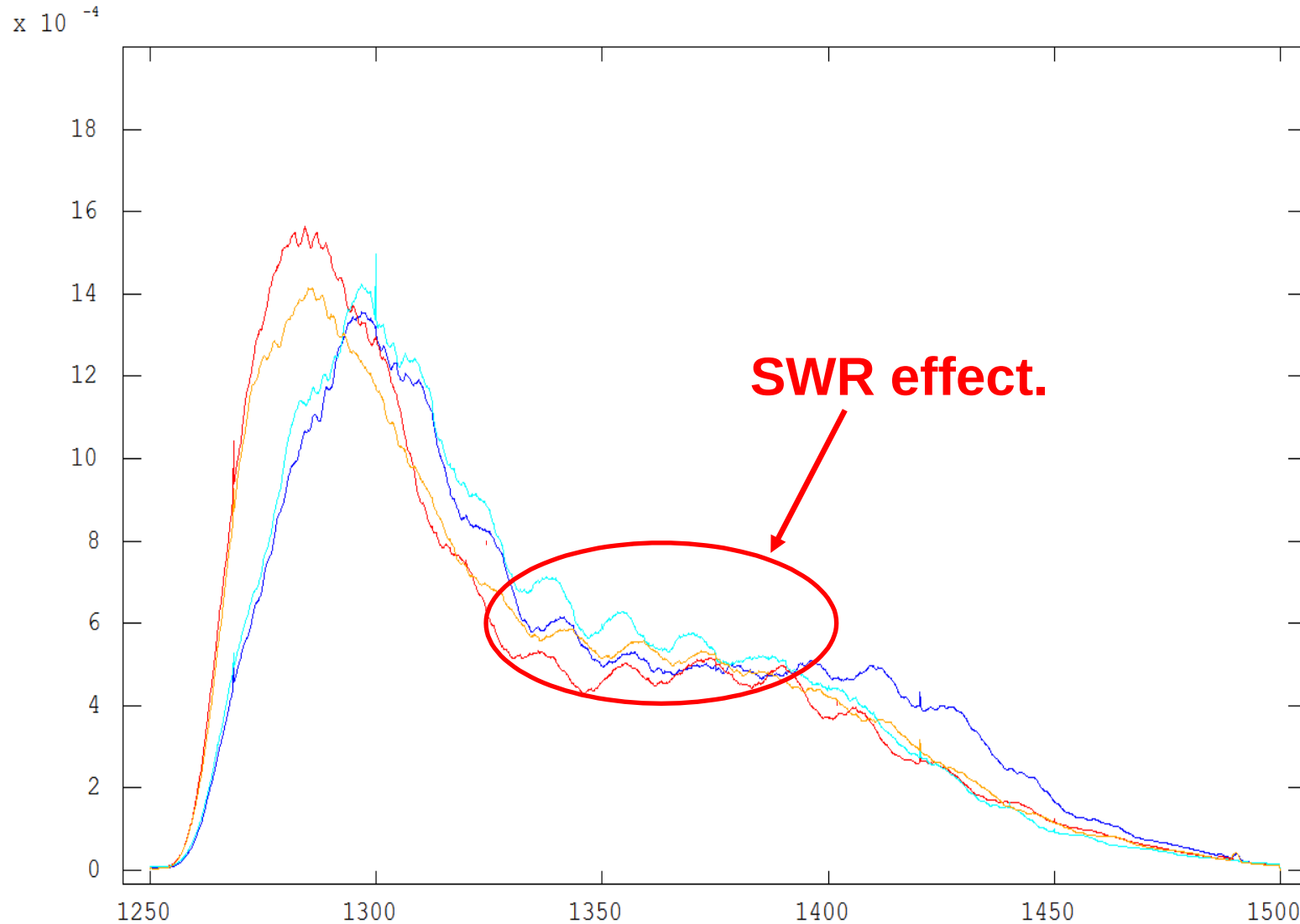
computing room



Data processing for off-line beam forming



Paon IV current analog limitation

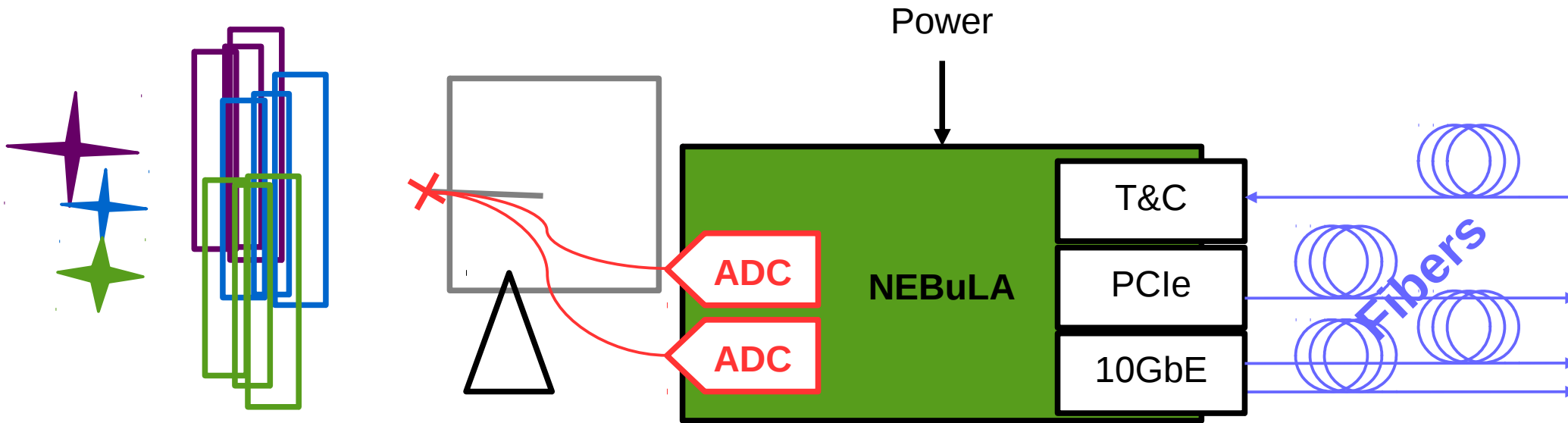


SWR depends of:

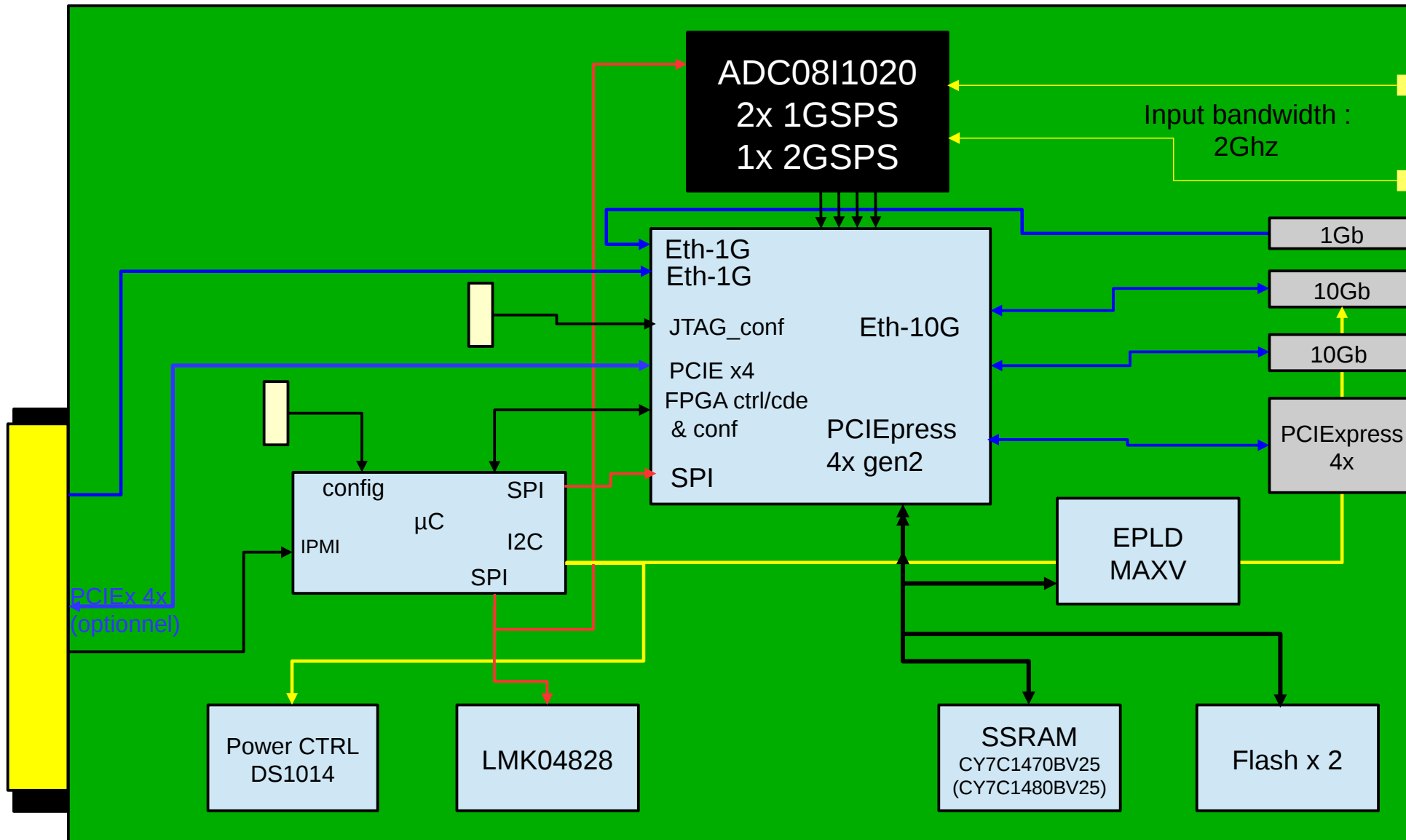
- long RF cables,
- adaptation mismatch,
- wide band acquisition.

NEBULA

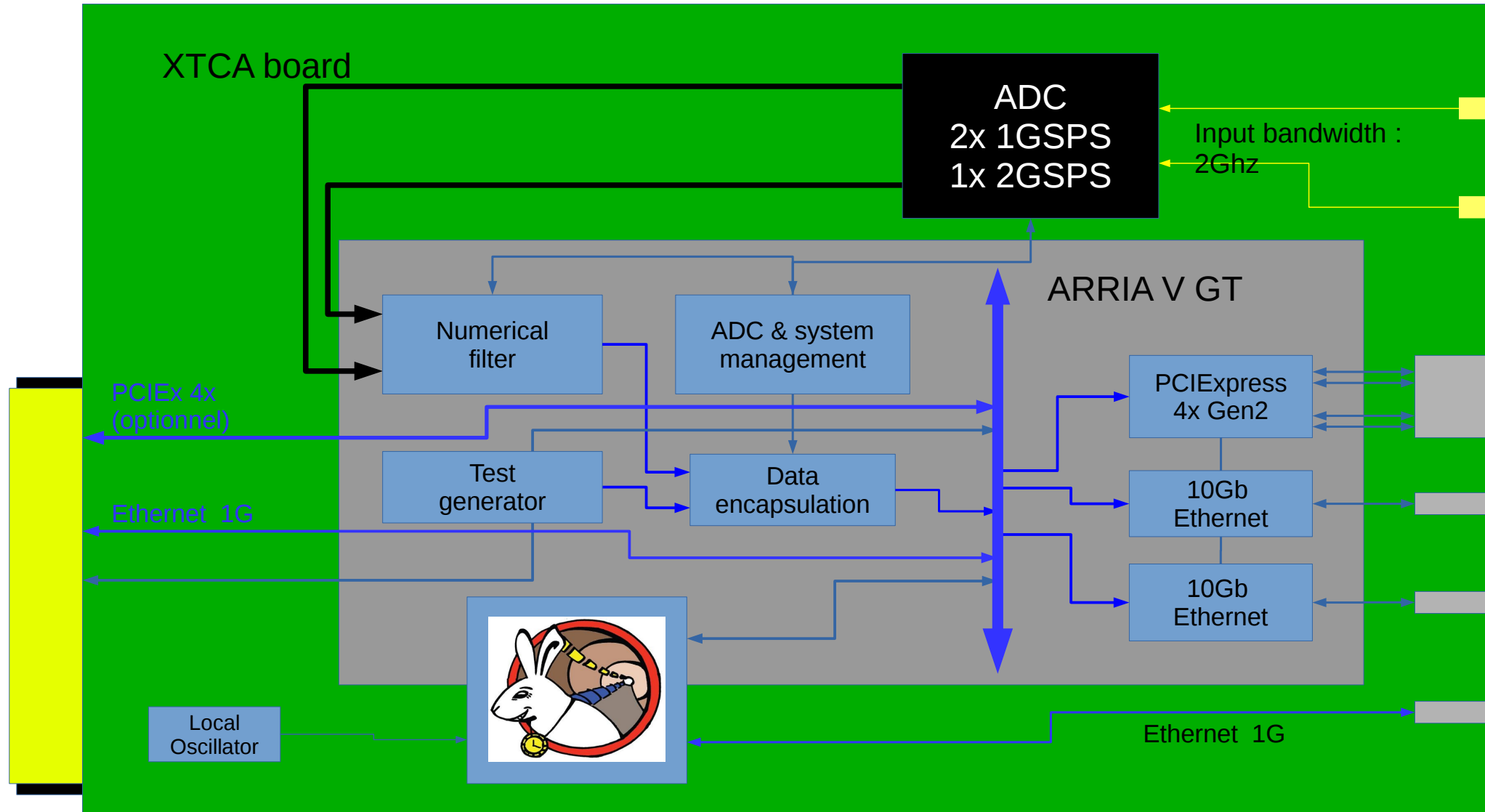
NumEriseur à Bande Large pour l'Astronomie



Nebula Design Architecture



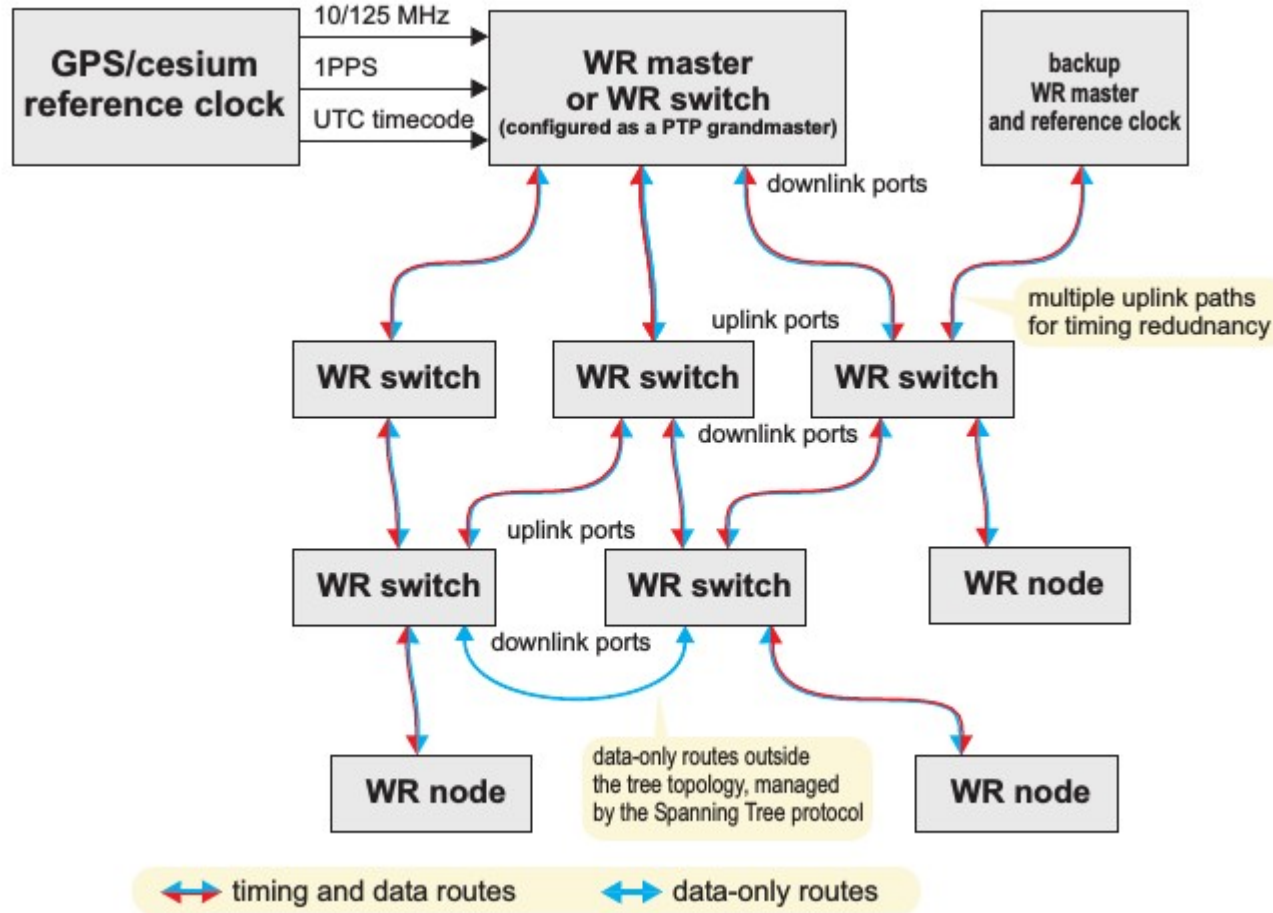
NEBULA FPGA content



White Rabbit



Network topology



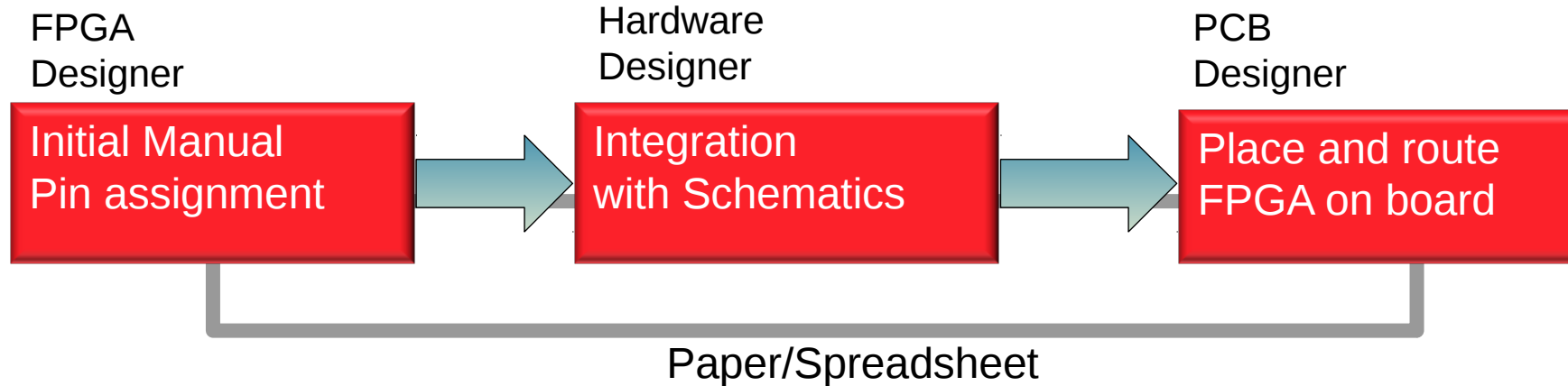
Extension of Ethernet

- Synchronous mode (Synch-E) – common clock for physical layer in entire network, allowing for precise time transfer.
- Deterministic routing latency

Technical concept

- Synchronous Ethernet
- Hardware -assisted PTP (IEEE1588) – Precision Time Protocol
- Packed preemption and deterministic protocol

IN2P3's old design methodology



TOOLS

- Build Quartus FPGA in order to export .pin file

- Part developer librarian
- Import .pin file
- Schematic design tools

- PCB design tools

PAIN

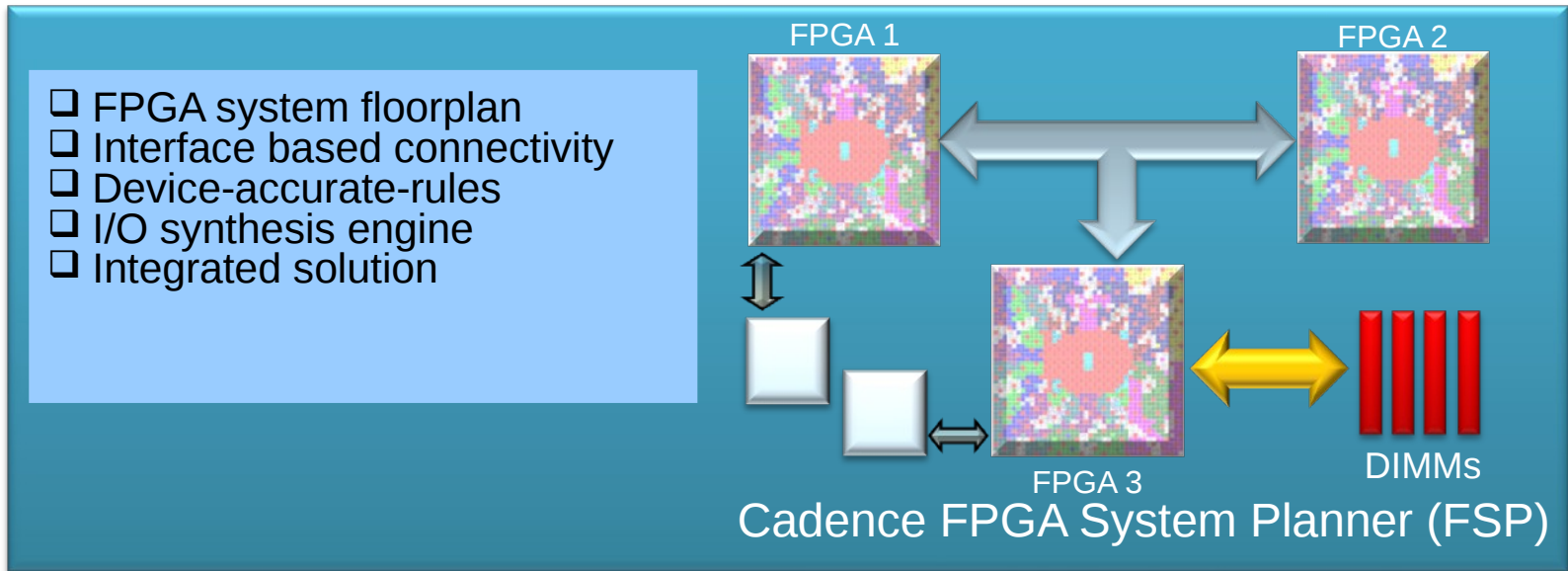
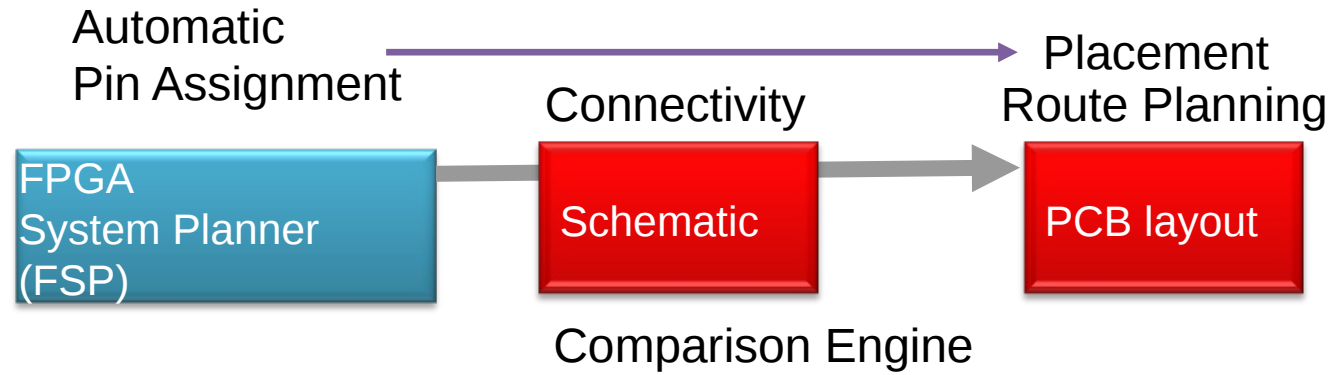
- Manual pin assignment
- one FPGA at a time
- Redo pin assignment with every ECO

- Place symbols and connect them
- Redo with each ECO

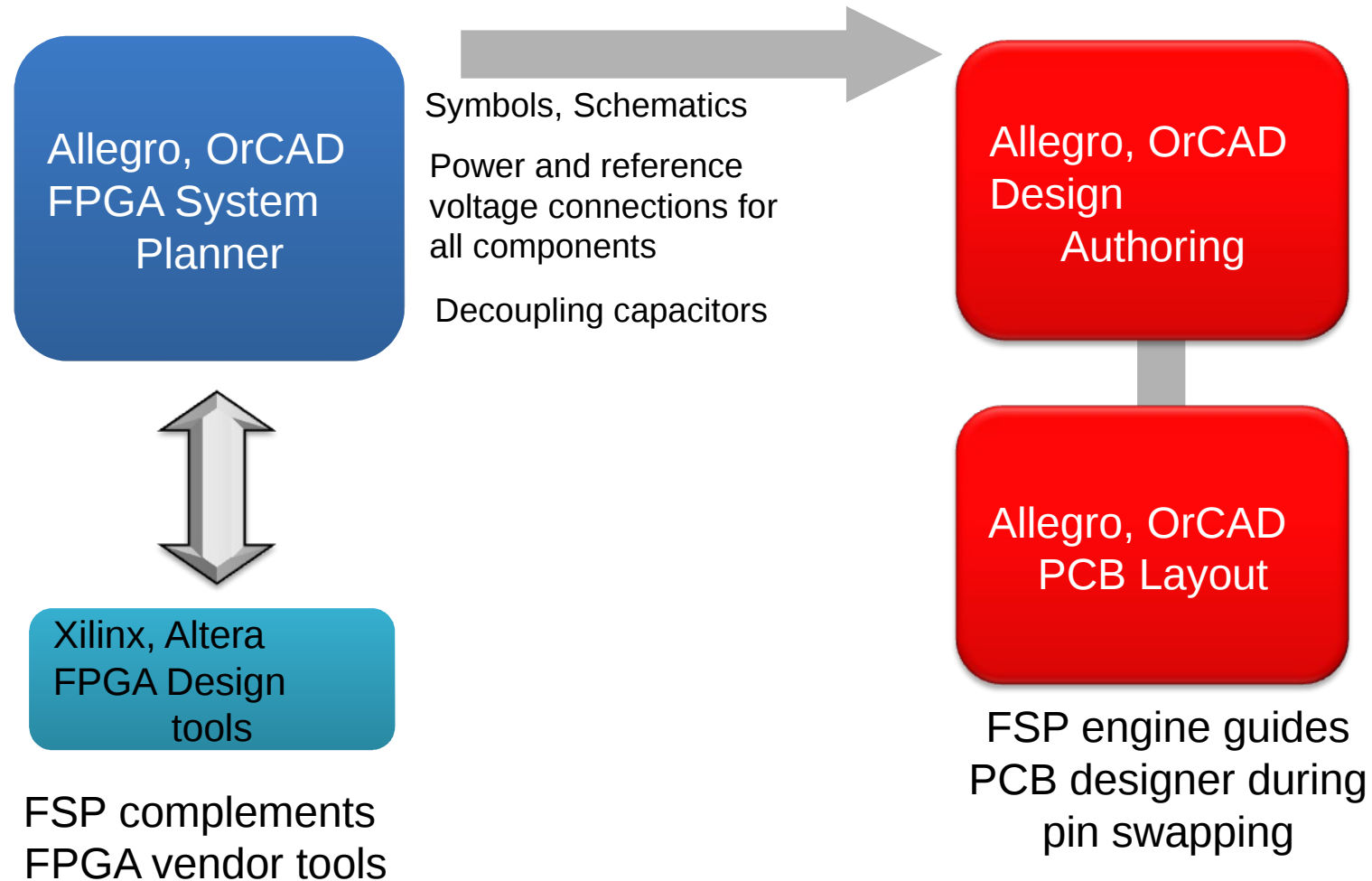
- No swapping possible

Overview of FSP :

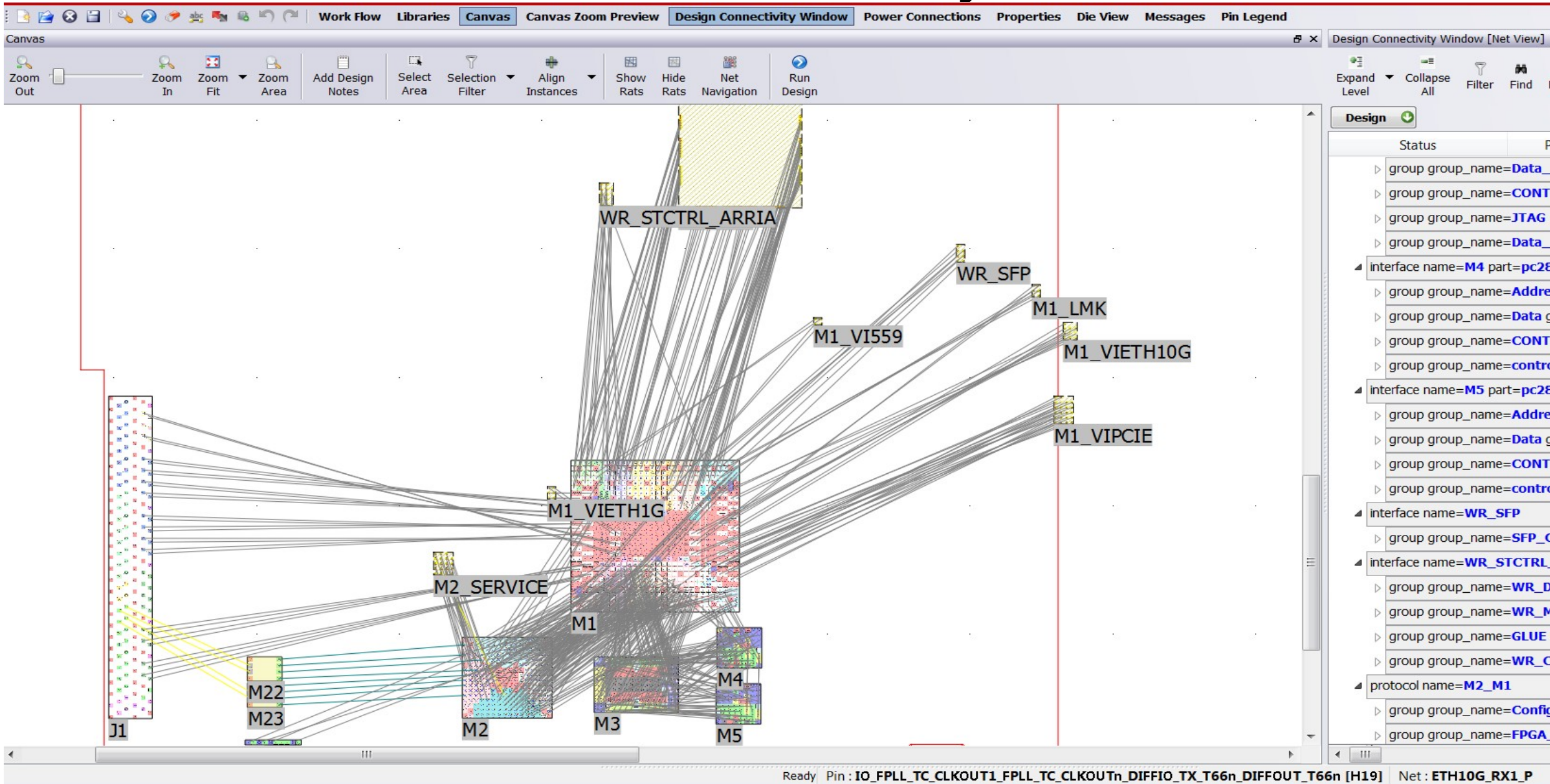
Three Main Components of FPGA System Planner



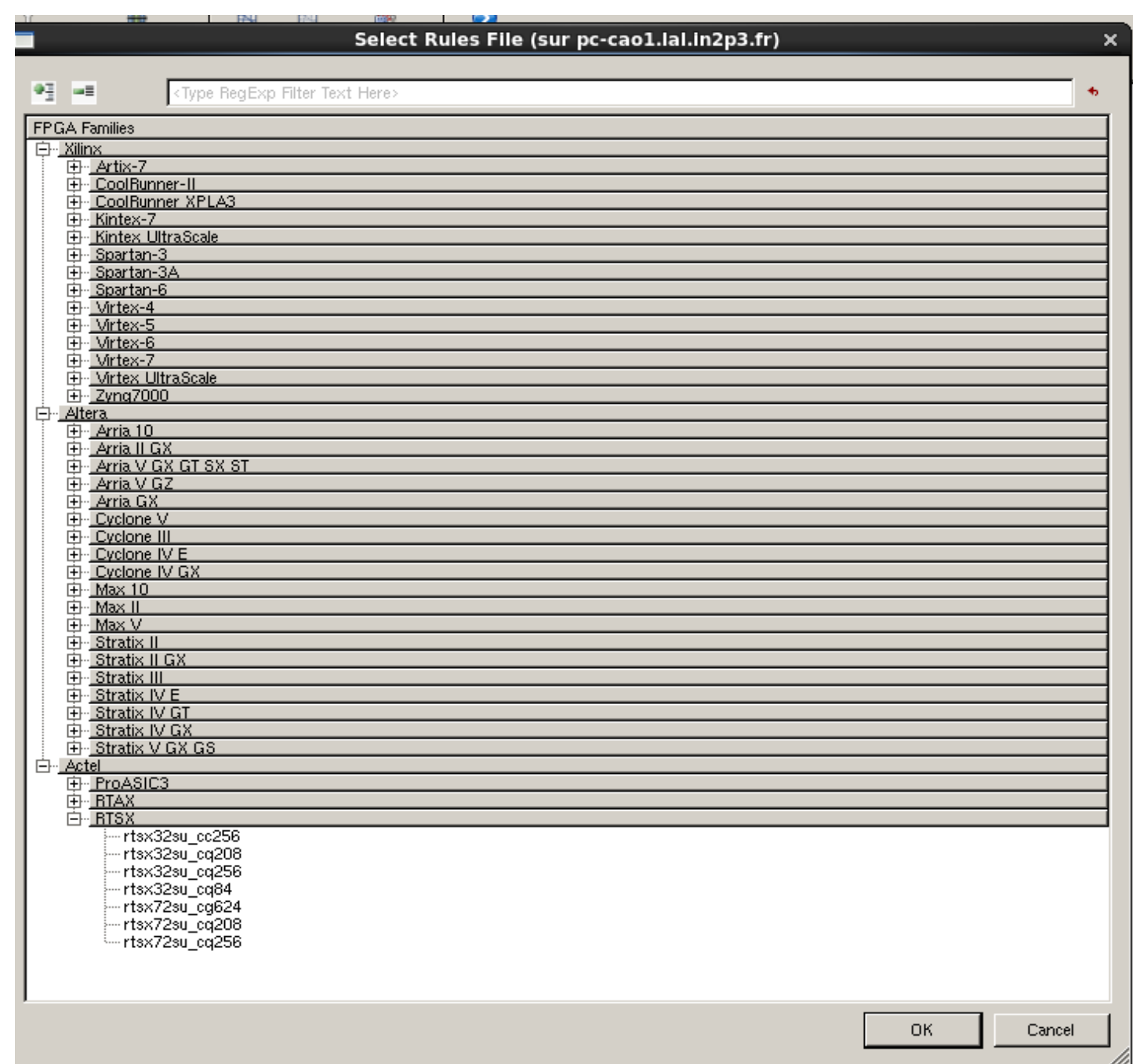
FSP Flow



Nebula FSP Project



FPGA selection FSP Project



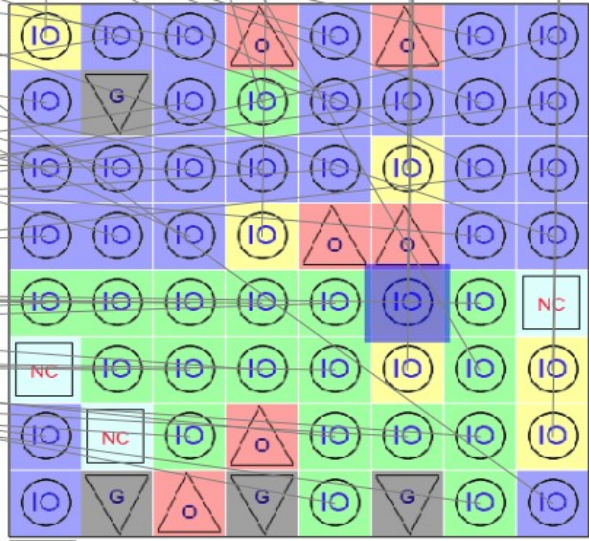
Component definition 1 FSP Project

Rules Viewer (pc28f00ap30bf) (sur laob.lal.in2p3.fr)

Expand All Collapse All Undo Redo Filter Find Replace Cut Copy Paste Show/Hide Columns Reset Width Clear Highlight Refresh Export CSV Import CSV

Pin Name	Pin Number	Pin Type	Symbol Pin Name	Voltage Level	IO Standard	Target Pin Function	Diff. Type	Diff. Pair Pin	Serial IO TX/RX Pin	Clock Group
lrf interface_type=NormalInterface target_family=ArriaVGX,MaxV unit=mm pin_size=1.00000 jedec_type=bga64h8_1000 instance_prefix=M pdescription=Parallel%20NOR%20flash%20memory part_height=7000000 part_width=7000000 x_offset=-0 y_offset=7										
+ group group_name=power group_number=4 group_color=#ff0000 gdescription=vccq%20vccp%20vcc										
+ group group_name=gnd group_number=5 group_color=#000000 gdescription=gnd%20vss										
+ group group_name=Address group_constraint=same_bank group_number=6 group_color=#0000ff gdescription=lvcmos2.5v%20to%203.3v										
+ group group_name=Data group_constraint=same_bank group_number=7 group_color=#00ff00 gdescription=lvcmos%202.5v%20to%203.3v										
- group group_name=CONTROL group_constraint=same_bank group_number=8 group_color=#ff0000 gdescription=lvcmos%202.5v%20to%203.3v										
..ADD<1>	A1	Input	ADD<1>		LVCMS25	GIO				
..ADVN	F6	Input	ADVN		LVCMS25	GIO				
..CLK	E6	Input	CLK		LVCMS25	GIO				
..OEN	F8	Input	OEN		LVCMS25	GIO				
..RESETN	D4	Input	RESETN		LVCMS25	GIO				
..WEN	G8	Input	WEN		LVCMS25	GIO				
..WPN	C6	Input	WPN		LVCMS25	GIO				
+ group group_name=NC group_number=9 group_color=#aaffff gdescription=NO%20CONNECT										
+ group group_name=control_2 group_number=10 group_color=#00ff00 gdescription=CONTROL_2										

Show Package View



Component definition 2 FSP Project

protocol interface_type=VirtualExtInterface

Port Name	Pin Type	Reserve Type	IO Standard	Target Pin Function	Diff. Type	Diff. Pair Signal	Serial IO TX/RX Signal	FPGA Ext. Termination	Net Nam
group group_name=WR_DAC_CTRL use_bank=7A group_number=2									
group group_name=WR_MEM_I2C group_number=3									
group group_name=GLUE group_number=4									
EXT_TRIG	Input		LVC MOS25	GIO					EXT_TRIG
GLB_RST	Input		LVC MOS25	CONFIG_D14					GLB_RST
IRQ_ARRIA	Output		LVC MOS25	CONFIG_D15			serie_24		IRQ_ARRIA
OVERTEMP	Output		LVC MOS25	CONF_DONE					OVERTEMP
SERIAL_NUM_TEMP	InOut		LVC MOS25	CRCERROR					SERIAL_NUM_TE
SYNCH_LMK	Output		LVC MOS25	CvP_CONFDONE					SYNCH_LMK
group group_name=WR_CK_20 use_bank=7A group_number=7									
group group_name=SPI group_number=8									
group group_name=LED_ARRIA group_number=9									

Name : WR_STCTRL_ARRIA

Create From Save As... Save Hide Log Validate OK Cancel

Component definition 3 FSP Project

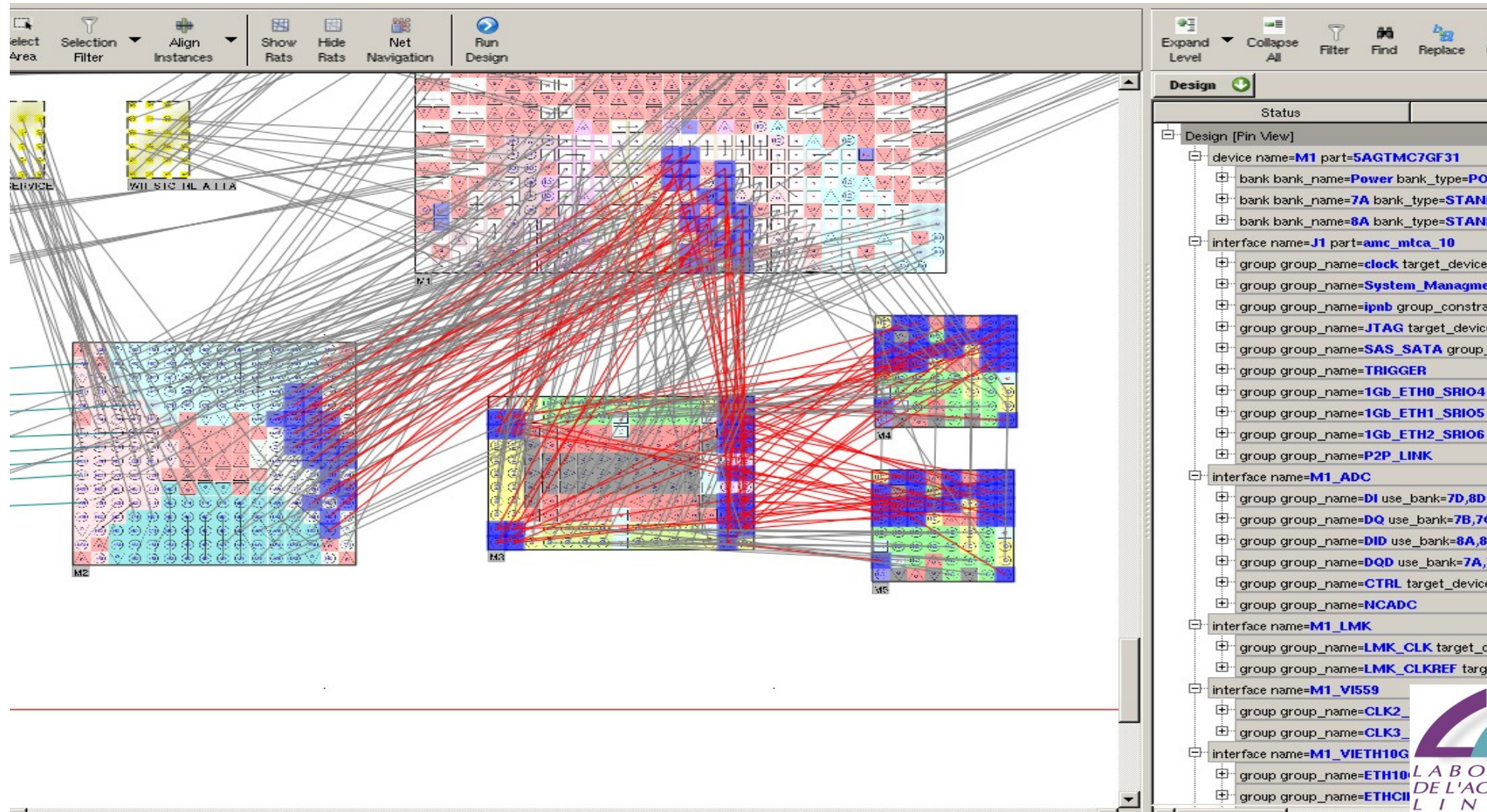
protocol interface_type=VirtualExtInterface

Port Name	Pin Type	Reserve Type	IO Standard	Target Pin Function	Diff. Type	Diff. Pair Signal	Serial IO TX/RX Signal	FPGA Ext. Termination	Net Nam
EXT_TRIG	Input		LVCMOS25	GIO					EXT_TRIG
GLB_RST	Input		LVCMOS25	GIO					GLB_RST
IRQ_ARRIA	Output		LVCMOS25	GIO			serie_24		IRQ_ARRIA
OVERTEMP	Output		DIFF_..._I_18	GIO					OVERTEMP
SERIAL_NUM_TEMP	InOut		DIFF_..._UL_12	GIO					SERIAL_NUM_TE
SYNCH_LMK	Output		DIFF_SSTL135	GIO					SYNCH_LMK
			DIFF_SSTL15	GIO					
			DIFF_...L18_I						
			DIFF_...18_II						
			DIFF_SSTL2_I						
			DIFF_SSTL2_II						
			DIFF_...L_125						
			DIFF_...II_15						
			DIFF_..._I_15						
			HCSL						
			HSTL_I						
			HSTL_II						
			HSTL_II_12						
			HSTL_II_18						
			HSTL_I_12						
			HSTL_I_18						
			HSUL_12						
			LVCMOS12						
			LVCMOS15						
			LVCMOS18						
			LVCMOS25						
			LVCMOS30						
			LVCMOS33						
			LVDS_25						
			LVDS_E_1R						
			LVDS_E_3R						
			LVPECL_25						
			LVTTL						

Name : WR_STCTRL_ARRIA

Create From Save As... Save Hide Log Validate OK Cancel

Address Bus Optimized and Assigned by FSP (In Red the Bus Data_Isb)



Decoupling assignment and associated to the chips

Define Decoupling Capacitors

Select decoupling capacitors for power regulators connected to the instances. Select the power regulator and click on "Add" button to start adding decoupling capacitors. Ensure that power regulators are defined and mapped in the design before defining decoupling capacitors.

+ Add X Delete Modify

Decap Symbol	Pin Count	Decap Value	Decap Count
passive_fsp:capa:sym_1		10u	8
passive_fsp:cpol:sym_1		100u	8
▲ J7	1	100uf	1
▲ P2V5	1	100uf	1
passive_fsp:capa:sym_1		100n	1
▲ M1	166	8211uf	216
▲ P2V5	62	1844uf	50
passive_fsp:capa:sym_1		10u	8
passive_fsp:capa:sym_1		1u	12
passive_fsp:capa:sym_1		100n	14
passive_fsp:capa:sym_1		22n	16
▲ P2V5_VCCA_GX	4	201uf	3
passive_fsp:capa:sym_1		1u	1
passive_fsp:capa:sym_1		100n	2
▲ P2V5_VCCA_FPLL	6	2162uf	17
passive_fsp:capa:sym_1		10u	2
passive_fsp:capa:sym_1		470n	3
passive_fsp:capa:sym_1		100n	6
passive_fsp:capa:sym_1		22n	6
▲ P1V5_VCCH_GX	4	408.8uf	8
passive_fsp:capa:sym_1		2.2u	4
passive_fsp:capa:sym_1		100n	4
▲ P1V5_VCCD_FPLL	7	192uf	8
passive_fsp:capa:sym_1		1u	4
passive_fsp:capa:sym_1		47n	4
▲ P1V2_VCCR_GX	10	800uf	20
passive_fsp:capa:sym_1		10u	2
passive_fsp:capa:sym_1		1u	4
passive_fsp:capa:sym_1		100n	6
passive_fsp:capa:sym_1		22n	8

OK Cancel

Power assignment

Allegro 4 FPGA System Planner Option - D:/In2P3_CDN_LIVE/nebula/Nebula/Nebula/Nebula_FSP_Cadence/nebula/nebula_1.fsp

File Library Component Design Tools Generate Custom Projects Window Help

Work Flow Libraries Canvas Canvas Zoom Preview Design Connectivity Window Power Connections Properties Die View Messages Pin Legend

Power Connections

Add Reg. Delete Reg. Auto Add Reg. Map Missing Reg. Reset and Map Reg. Reset To Default Voltages Check Power Connections

Regulator Name	Voltage	J1 [amc_mtca_10]	J7 [jtag_altera]	M1 [5AGTMC7GF31]
P2V5	2.5		VREF	VCCIO8D,VCCPD4A,VCCIO3D,VCCIO4A,VCCIO4B,VCCIO4C,VCCPD7BCD,VCCIO4D,VCCPD3,VCCPD4BCD,VCCPGM,VCCPD8,VCCPD7A,V...
GND	0	GND	GND	GND
PV12	12	12		
P1V8	1.8			VCCIO7B
P3V3	3.3			
P2V5_VCCA_GX	2.5			VCCA_GXBL1,VCCA_GXBL0,VCCA_GXBR1,VCCA_GXBR0
P2V5_VCCA_FPLL	2.5			VCCA_FPLL,VCC_AUX
P1V5_VCCH_GX	1.5			VCCH_GXBR1,VCCH_GXBR0,VCCH_GXBL1,VCCH_GXBL0
P1V5_VCCD_FPLL	1.5			VCCD_FPLL,VCCBAT
P1V2_VCCR_GX	1.2			VCCR_GXBL,VCCR_GXBR
P1V1	1.1			VCC
P1V1P	1.1			VCCP
P1V2_VCCT_GX	1.2			VCCT_GXBL0,VCCT_GXBL1,VCCT_GXBR0,VCCT_GXBR1
P2V5_VREFIO	2.5			
P1V2_VCCL_GX	1.2			VCCL_GXBR0,VCCL_GXBR1,VCCL_GXBL0,VCCL_GXBL1

Automatic Schematic Generation

Generate Allegro DE-HDL Schematics

Placement

- Skip Unused Symbol Splits**
Exclude symbol splits that have no net connections. By default, unconnected symbol splits are not placed in order to minimize the number of generated schematic sheets.
- Do Not Mix Symbols and Hierarchical Blocks**
Place only one FPGA or connector hierarchical block per page. This helps to avoid overlaps with other components if the number of connections to the block increases.
- Do Not Mix Symbols of Different Instances**
Use a unique schematic pages for each instance. Checking this option will prevent symbols of different instances from being intermixed within a single page.

General

- Preserve Schematics**
Generate schematics in preserve mode. Use this option to preserve any manual changes made to schematic placement or to preserve the placement of symbols on specific schematic pages.
- Display Net Name as Instance Pin Name**
Use the net name connected to the pin instead of the symbol pin name for FPGA components. Note that this is a purely textual overlay in the generated schematic and the symbols are not modified.
- Propagate FSP Net Groups**
Propagate FSP-defined net groups into Constraint Manager. These net groups are used to create default bundles in Allegro.

Hierarchy

- Use Actual Port Type For Hierarchical Ports**
Use the port's direction to determine which hierarchical port symbol to use. If this option is unchecked, FSP uses an 'inout' port symbol for all hierarchical ports.
- Flatten Hierarchical Termination Blocks**
For terminations defined using hierarchical blocks, remove the hierarchy and place the underlying discrete components directly into the schematic.
- Generate Hierarchical Blocks for FPGAs**

Hierarchical Block	Block Location	
M1(5AGTMC7GF...	nebula_lib:h1_5agtmc7gf31	...
M2(5m2210zf256)	nebula_lib:h141_5m2210zf256	...
M22(mlvds200_r...	nebula_lib:h298_mlvs200_rule	...
M23(mlvds200_r...	nebula_lib:h313_mlvs200_rule	...

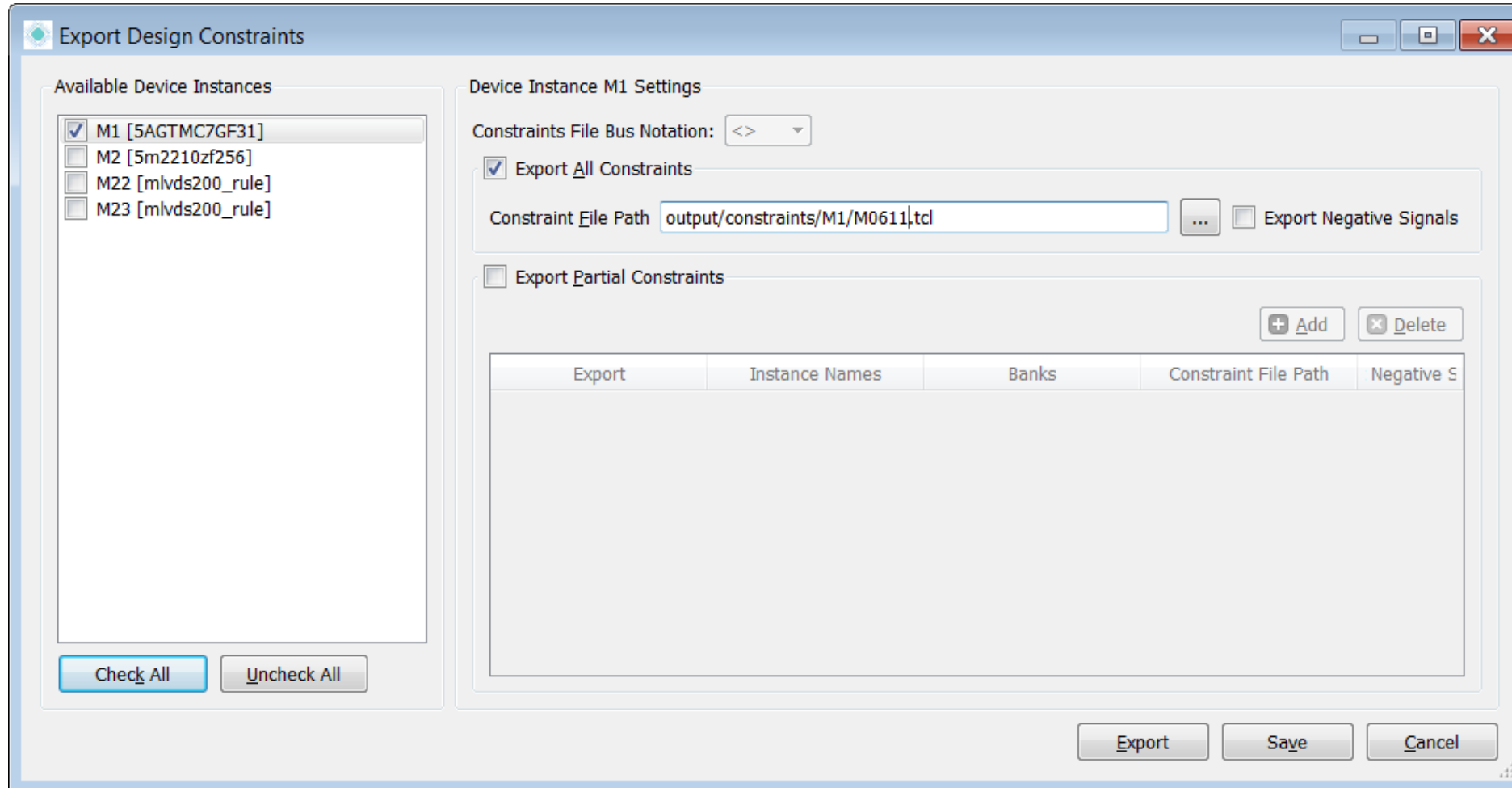
Advanced Settings ...

OK Cancel

Output result from Generate design

The image displays two screenshots of the Allegro Design Entry HDL XL software interface. The top screenshot shows the main workspace with a PCB layout. The layout features a central component with numerous pins, connected to a network of green traces. Labels such as 'GND', 'PWR', and 'IP' are visible. A Hierarchy Viewer on the left lists pages from page7 to page11. The bottom screenshot shows a signal timing diagram with two vertical axes. The left axis is green and the right axis is orange, both showing a series of pulses. The diagram is overlaid on a grid.

Automatic FPGA Pin Placement Constraint file for Quartus/Altera..

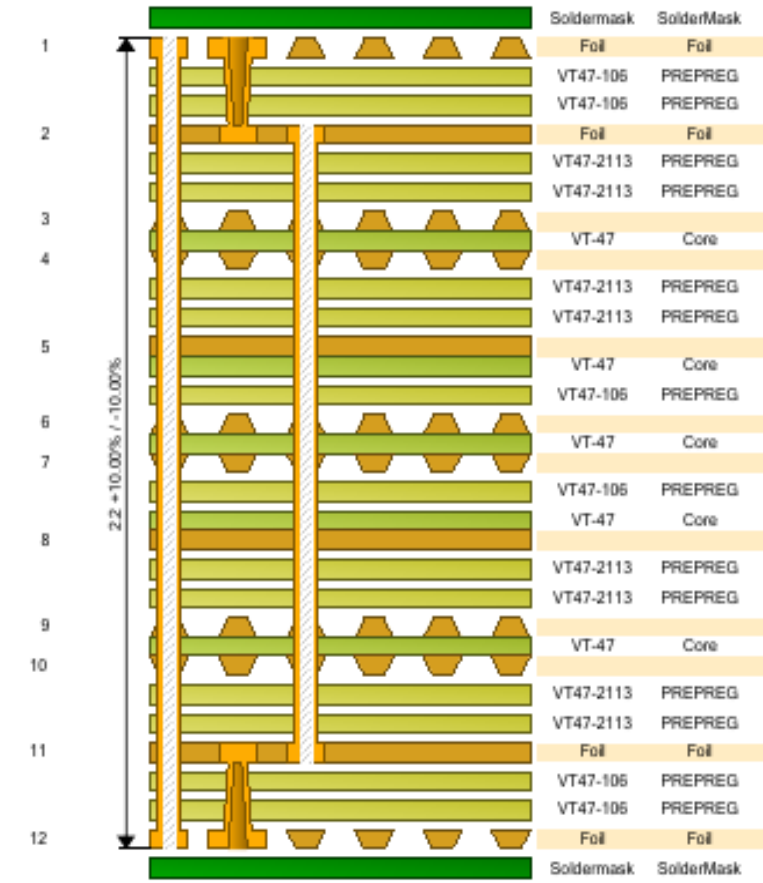
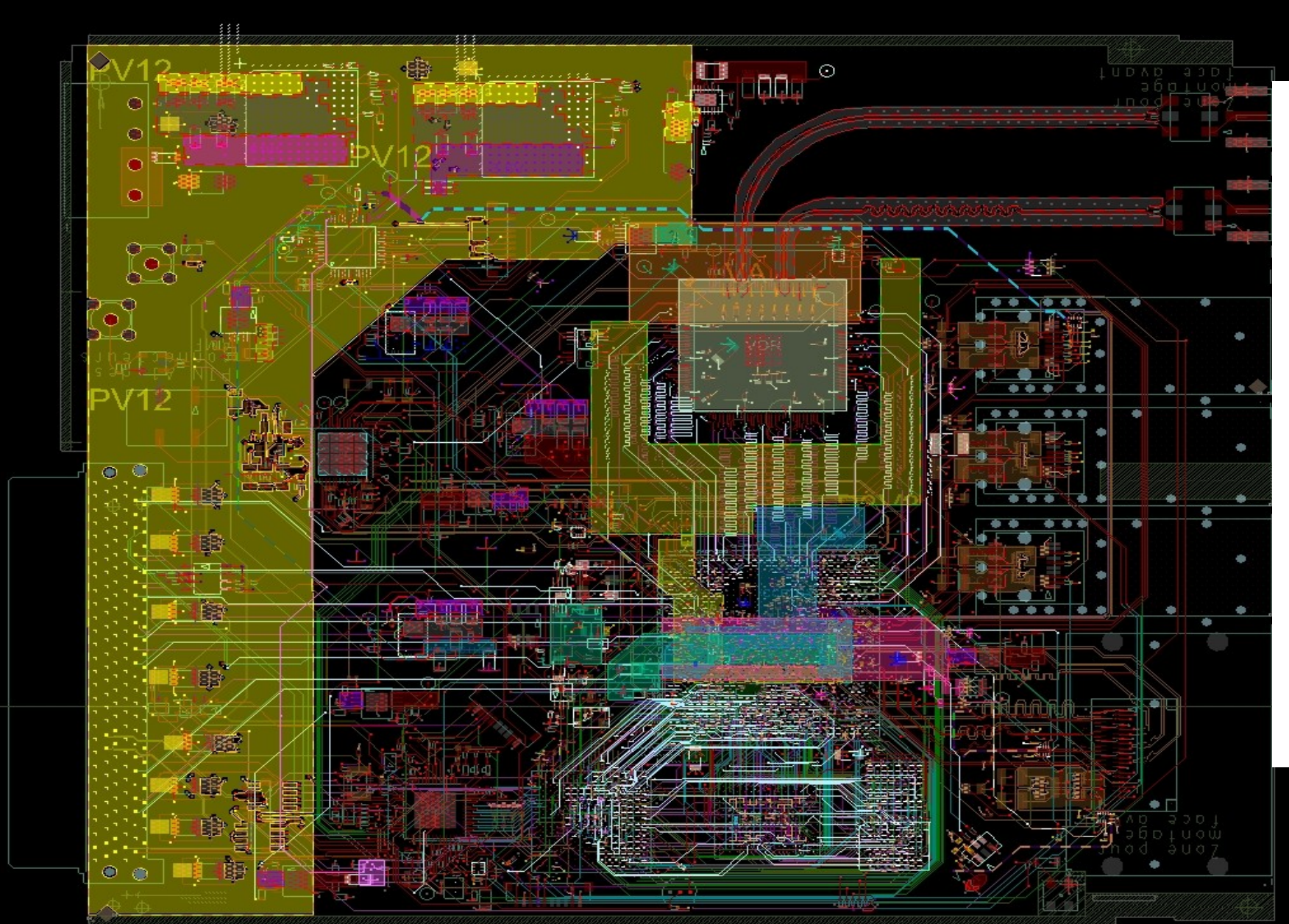


Automatic FPGA Pin Placement Constraint file for Quartus/Altera..

```
emacs@lao2.lal.in2p3.fr (sur lao2.lal.in2p3.fr)
File Edit Options Buffers Tools Tcl Help
set_instance_assignment -name IO_STANDARD "2.5 V" -to RATE_SELECT
set_instance_assignment -name IO_STANDARD "2.5 V" -to SB_RTN
set_instance_assignment -name IO_STANDARD "2.5 V" -to SYNCH_LMK
set_instance_assignment -name IO_STANDARD "2.5 V" -to TSD_SCL
set_instance_assignment -name IO_STANDARD "2.5 V" -to TSD_SDA
set_instance_assignment -name IO_STANDARD "2.5 V" -to TK_DISABLE
set_instance_assignment -name IO_STANDARD "2.5 V" -to TK_FAULT
set_instance_assignment -name IO_STANDARD "2.5 V" -to WR_RX
set_instance_assignment -name IO_STANDARD "2.5 V" -to WR_TX
set_instance_assignment -name IO_STANDARD "LVDS" -to XO_156M_P

##### LOCATION - NET #####
set_location_assignment PIN_AH23 -to ADD[0] -comment "Bank : 3D"
set_location_assignment PIN_R9 -to CLK1_P -comment "Bank : B1R"
set_location_assignment PIN_D1 -to CLK20_VCXO -comment "Bank : 7A"
set_location_assignment PIN_AB22 -to CPERSTn -comment "Bank : 3D"
set_location_assignment PIN_AA22 -to CPRSNTr -comment "Bank : 3D"
set_location_assignment PIN_AC25 -to CWAKEr -comment "Bank : 3A"
set_location_assignment PIN_A21 -to DCLK_P -comment "Bank : 8D"
set_location_assignment PIN_J22 -to DID_P[0] -comment "Bank : 8D"
set_location_assignment PIN_F19 -to DID_P[1] -comment "Bank : 8D"
set_location_assignment PIN_F23 -to DID_P[2] -comment "Bank : 8D"
set_location_assignment PIN_D24 -to DID_P[3] -comment "Bank : 8A"
set_location_assignment PIN_D26 -to DID_P[4] -comment "Bank : 8A"
set_location_assignment PIN_C27 -to DID_P[5] -comment "Bank : 8A"
set_location_assignment PIN_A23 -to DID_P[6] -comment "Bank : 8A"
set_location_assignment PIN_A26 -to DID_P[7] -comment "Bank : 8A"
set_location_assignment PIN_D18 -to DI_P[0] -comment "Bank : 7D"
set_location_assignment PIN_D22 -to DI_P[1] -comment "Bank : 8D"
set_location_assignment PIN_C20 -to DI_P[2] -comment "Bank : 8D"
set_location_assignment PIN_B16 -to DI_P[3] -comment "Bank : 7D"
set_location_assignment PIN_B22 -to DI_P[4] -comment "Bank : 8D"
set_location_assignment PIN_J20 -to DI_P[5] -comment "Bank : 8D"
set_location_assignment PIN_A19 -to DI_P[6] -comment "Bank : 7D"
set_location_assignment PIN_B18 -to DI_P[7] -comment "Bank : 7D"
set_location_assignment PIN_F8 -to DQD_P[0] -comment "Bank : 7B"
set_location_assignment PIN_E1 -to DQD_P[1] -comment "Bank : 7A"
set_location_assignment PIN_E7 -to DQD_P[2] -comment "Bank : 7B"
set_location_assignment PIN_D9 -to DQD_P[3] -comment "Bank : 7B"
set_location_assignment PIN_A2 -to DQD_P[4] -comment "Bank : 7A"
set_location_assignment PIN_A3 -to DQD_P[5] -comment "Bank : 7A"
set_location_assignment PIN_A6 -to DQD_P[6] -comment "Bank : 7A"
set_location_assignment PIN_A5 -to DQD_P[7] -comment "Bank : 7A"
set_location_assignment PIN_C11 -to DQ_P[0] -comment "Bank : 7B"
set_location_assignment PIN_C8 -to DQ_P[1] -comment "Bank : 7B"
set_location_assignment PIN_A7 -to DQ_P[2] -comment "Bank : 7B"
set_location_assignment PIN_C10 -to DQ_P[3] -comment "Bank : 7B"
set_location_assignment PIN_A11 -to DQ_P[4] -comment "Bank : 7B"
set_location_assignment PIN_B13 -to DQ_P[5] -comment "Bank : 7C"
set_location_assignment PIN_A14 -to DQ_P[6] -comment "Bank : 7C"
```

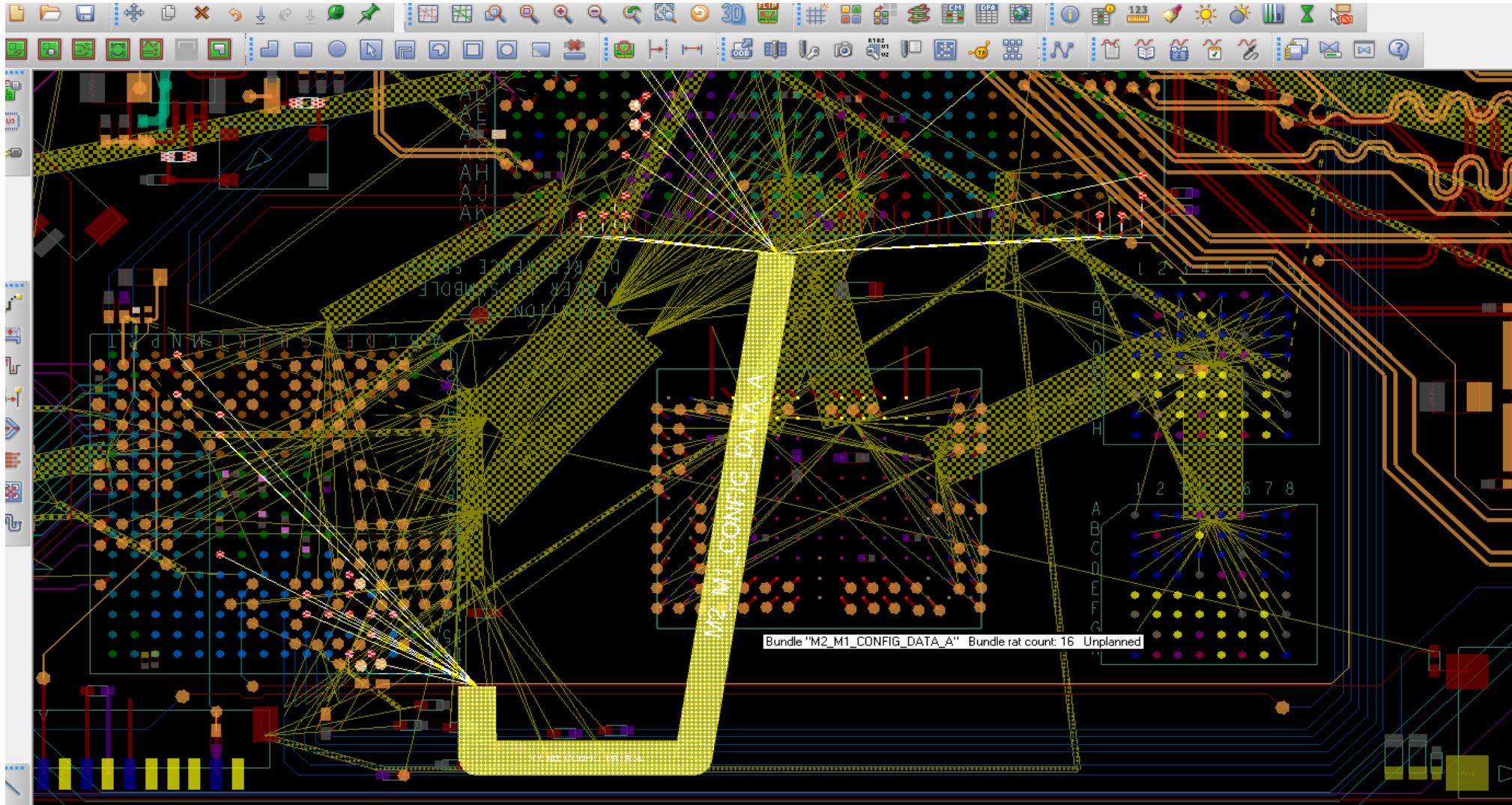
PCB design in development



Copper Thickness = 0.314 | D

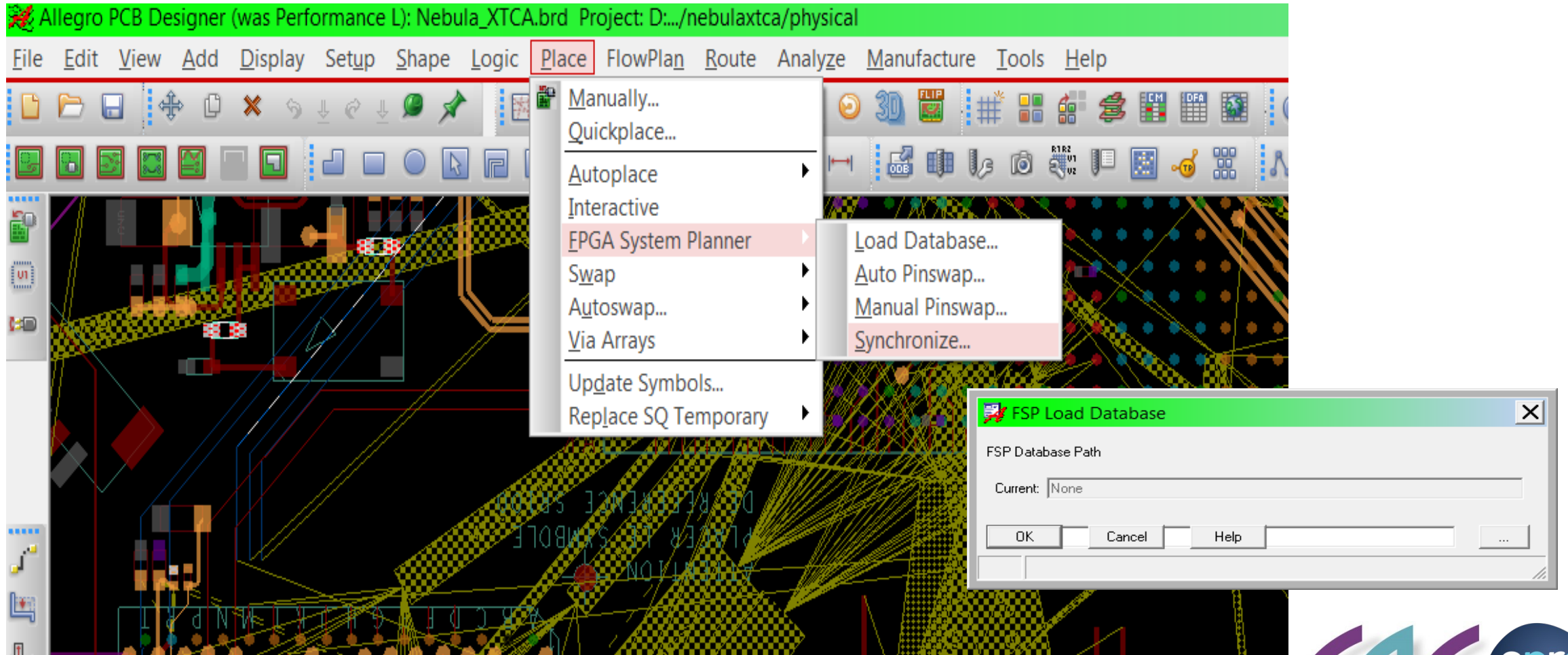
Bundle pin swap optimization

Scheduling and bus slide

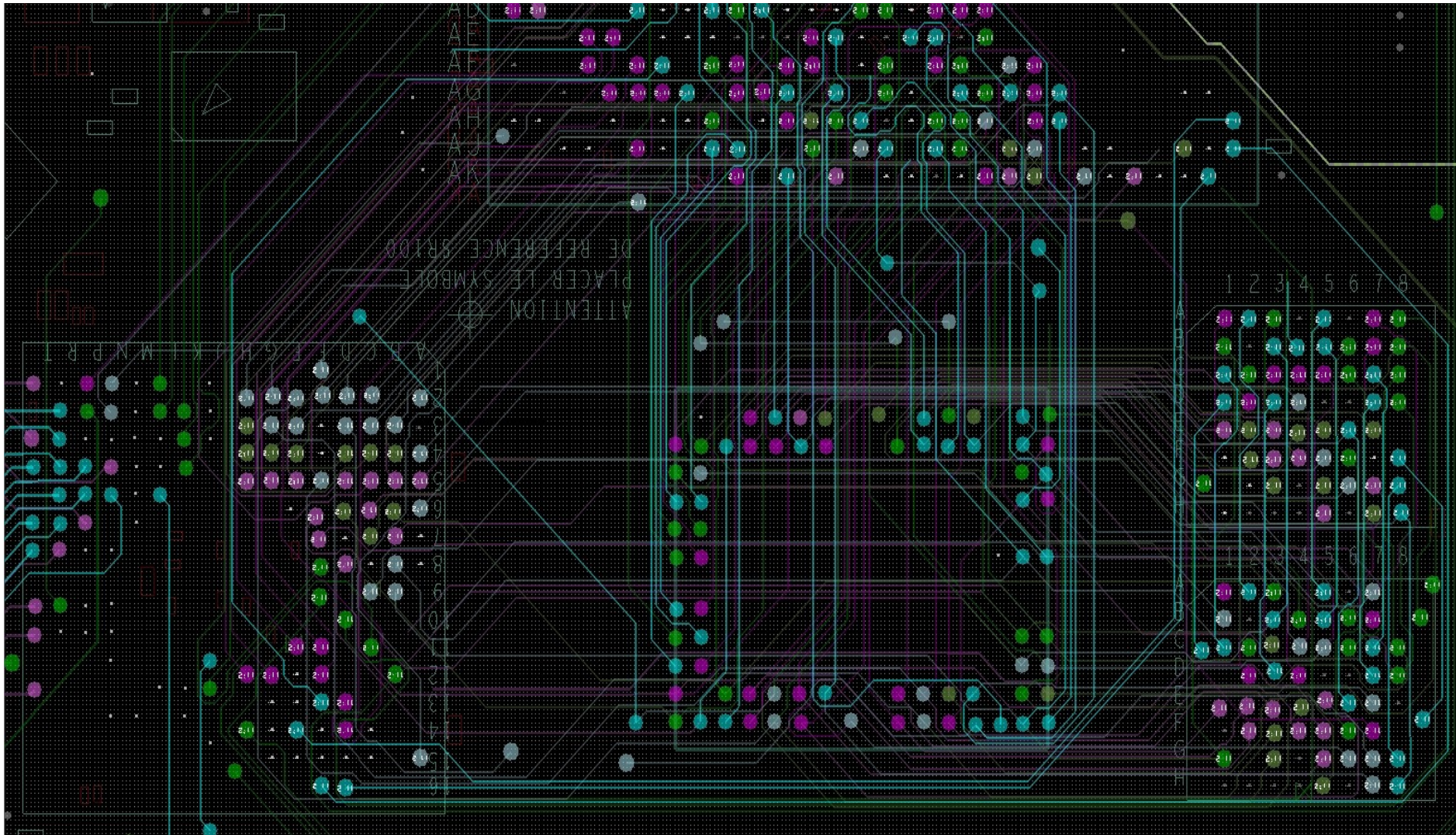


Allegro PCB Designer connected to FSP database

Automatic feedback when PCB is written



Allegro PCB connected to FSP database real time pin swapping.



PCB swapping back annotation Compare master FSP design to changes made in PCB

Allegro 4 FPGA System Planner Option - /exp/elec/charlet/LHCb/SpecsPCIEV2/sfp/specsv2a5/specsv2a5_copy.fsp (sur lao2.lal.in2p3.fr)

Design Comparison (sur lao2.lal.in2p3.fr)

Design 1 /exp/elec/charlet/LHCb/SpecsPCIEV2/sfp/specsv2a5/specsv2a5_ref.fsp Design 2 /exp/elec/charlet/LHCb/SpecsPCIEV2/sfp/specsv2a5/specsv2a5_copy.fsp Compare Connectivity

M6 (0) M1 (299) M9 (0) M8 (0) M11 (0) M10 (0) M5 (0) M7 (0) M4 (0) Merge All Instances To Left Merge All Instances To Right Net View Pin View

Expand Collapse Sort Ascen Sort Descen Copy Find Show/Hide Columns Refresh Move Right Move Left Show Next Diff Show Previous Diff Show Only Diff Undo Redo

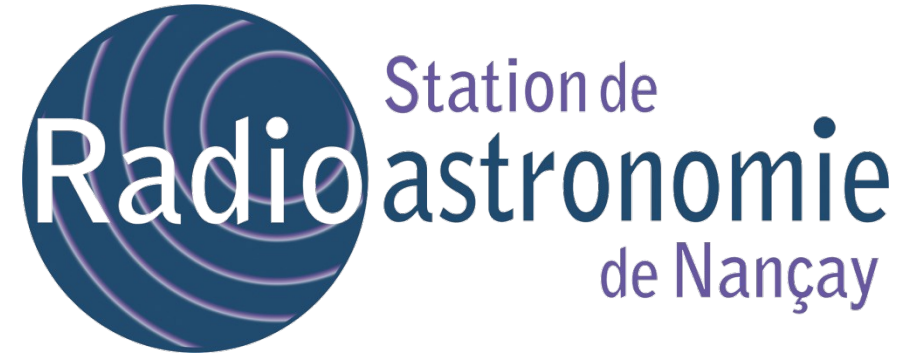
Difference Count 299

Pin Number	Pin/Port Name
AA25	nCS0_DATA4
AE23	IO_DIFFIO_TX_B14p_DIFFOUT_B14p
AE27	IO_DIFFIO_TX_B3n_DIFFOUT_B3n
AF24	IO_DIFFIO_RX_B13n_DIFFOUT_B13n
AF28	IO_RZQ_0_DIFFIO_TX_B1n_DIFFOUT_B1n
AF29	TDI
AF30	TDO
AG24	IO_DIFFIO_RX_B13p_DIFFOUT_B13p
AG28	IO_DIFFIO_TX_B1p_DIFFOUT_B1p
AG29	TCK
AG30	TMS
AH25	IO_DIFFIO_RX_B11n_DIFFOUT_B11n
AH30	AS_DATA3_DATA3
AJ24	IO_DIFFIO_RX_B15n_DIFFOUT_B15n
AJ25	IO_DIFFIO_RX_B11p_DIFFOUT_B11p
AJ29	DCLK
AJ30	AS_DATA2_DATA2
AK24	IO_DIFFIO_RX_B15p_DIFFOUT_B15p
AK25	IO_DIFFIO_TX_B6p_DIFFOUT_B6p
AK26	IO_DIFFIO_TX_B8n_DIFFOUT_B8n
AK28	AS_DATA0_ASDD_DATA0

```
Successfully checked all models for part .
Reading part flash_conf_con...
Successfully checked all models for part .
Missing attribute group_color for group group1. Setting it to default value #00ff00.
Reading part nlv290_rule...
Validating device model...
Validating pin locations of device...
Validating pin logical information for connectors...
Successfully checked device model.
Completed loading parts from cache.
Reading protocol between instances M4_Md...
Reading protocol between instances M6_Md...
Reading protocol between instances M7_Md...
Reading protocol between instances M9_Md...
Reading protocol between instances M5_Md...
Reading protocol between instances M8_Md...
Reading protocol between instances M10_Md...
Reading protocol between instances M11_Md...
```

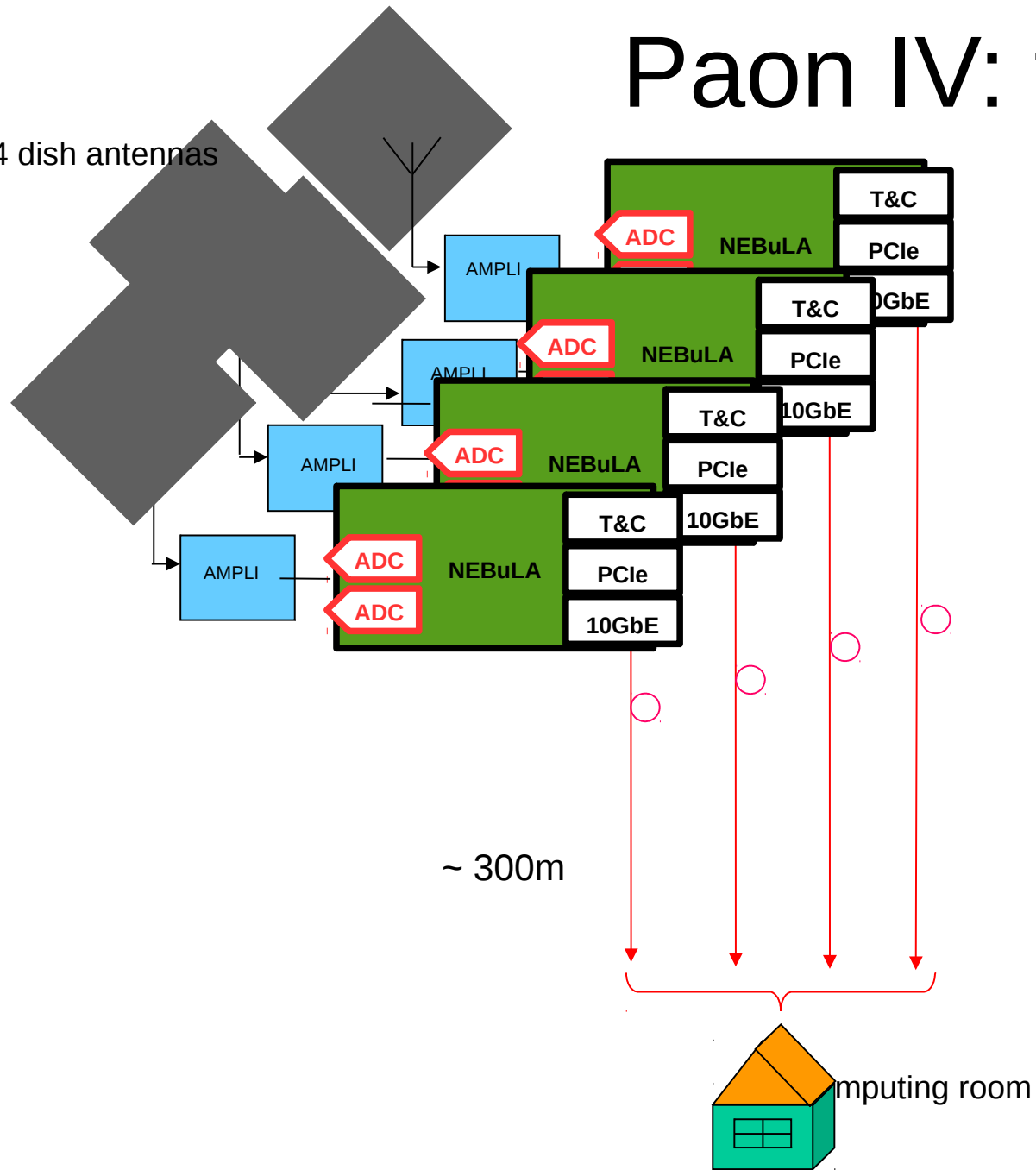
Improvements seen by using FSP

- ✓ Board development before FPGA firmware development
- ✓ Easy upgrade of FPGA during design
- ✓ Exchange physical/logical during development
- ✓ Easy swapping in place and route phase with back annotation
- ✓ Easy decoupling definition
- ✓ Easy power supply assignment
- ✓ Save 50% time of previous manual method
- ✓ Concurrent engineering between software architecture and PCB
- ✓ Automatic schematic generation
- ✓ Automatic FPGA pin placement constraint file for Quartus/Altera..



Paon IV: future Configuration.

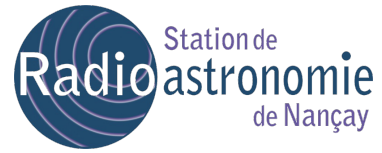
4 dish antennas



IN2P3 FPGA System Planner

Journées VLSI 2016

NEBULA DESIGN



1

Daniel Charlet – FSP -- VLSI 2016

This is the agenda of my presentation
First I will introduce the CNRS and IN2P3

Trouver la définition des BAO

Le lien avec les ondes gravitationnelles

Surtout lié a la recherche de matier/energie noire

L'ampleur de la collaboration

Le temps depuis

Trouver la définition des BAO

Le lien avec les ondes gravitationnelles

Surtout lié a la recherche de matier/energie noire

L'ampleur de la collaboration

Le temps depuis

The PAON IV demonstrator has a Classic structure for radio astronomy acquisition system

Dishes antenna equipped with low noise amplifier at the top and a long cable to the digitizer system

The Data transfer is performed by optical fiber to the computing room

PAON IV comprises 8 channels ,2 polarity by antenna

The bandwidth of the analog chain is 250MHz between 1.25Ghz and 1.5Ghz

The digitalization is performed at 500Mhz with 8bits of dynamics

The dish diameter is 5m with a beam antenna around 3°

After digitalization a fast Fourier transformation of 2048 point is made on-line by an FPGA. The FPGA format and send data to the computing room by optical fibers at 5Gb/s using home made protocol. In the computing room, by PC farm, computation of the cross correlation at each frequency
Data accumulated and disk storage

Off line processing data to clean data and to performed maps at different frequency .
A snapshot of the cyg A galaxy whit the arm of our own galaxy realize by the PAON IV detector

Due to bandwidth and also of the sensitivity of the system we encounter SWR problem . This has the effect of modification of signal.

The extend of the signal modification is proportional of the mismatch adaptation, the bandwidth , the cable length.

Classically on radio astronomy there is a narrow bandwidth and there are not affected by this issue.

SWR Standing wave ratio

I will present you the NEBULA project and how we have designed it using FSP

The NEBULA board is based on the xTCA for physics standard but

It can also work in stand alone mode, only 12v power supply and optical link are mandatory to the board.

The heart of the system is an FPGA ARRIA V GX

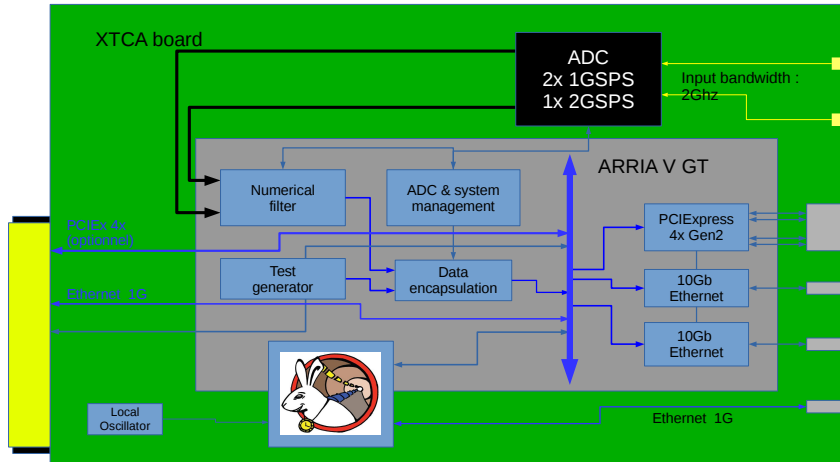
The board integrates one double channel ADC at 1G sample on 8bits with the possibility to configure in one channel at 2G samples

For configuration synchronization and time tagging we have implemented the white-rabbit protocol developed by the CERN

that permits to synchronize a distributed system with an accuracy under 20ps

The data rate transfer could reach 20Gb/s using 2 x 10Gb Ethernet link or one 4x Gen2 external PCIe Express link

NEBULA FPGA content



10

Daniel Charlet – FSP -- VLSI 2016

- Common clock for the entire network

All network nodes use the same physical layer clock,
generated by the System Timing Master

Clock is encoded in the Ethernet carrier and recovered by
the PLL in the PHY.

- PTP IEEE1588

- Synchronizes local clock with the master clock by measuring

- and compensating the delay introduced by the link.

For electronic development the institute use cadence product since 25 years.

I will described the classical methodology used for a board study incorporating FPGA

- First stage generation of FPGA pin assignment using EDA products in my case it's ALTERA and QUARTUS

- Generation of the component with part developer to integrate in the schematics entry

 - You do manually your design whit CONCEPT schematic

 - Finally Placing and Layout with ALLEGRO

This classic methodology are further inconvenient:

- Time consuming

- Numerous possible human error at different stage mainly due to the iterative process.

- At the first stage when we fix the FPGA pin assignment we have only a rough idea of the relative chips placement on the board, and no idea how the net will be routed.

 - To swap pin he is necessary to do an iterative process

The FSP Methodology

The main feature is it 's interface base connectivity
(you define bus function like address, data, ctrl...)

It's a system floor-plan, the inter-connexion are guided by the relative placement of the components, the designer can also early define placement

The system has a accuracy component pin rules like logic standard, functions

The resulting data base is linked to PCB designer tools (allegro, orcad)

FSP provide FPGA libraries and additional components like memories , connectors,

Designer can define it's own components

The design interconnection is under the control of the designer

The FSP flow

- Generation of interconnection between components according to the relative components placement and I/O rules
- Generation of powers and reference voltage for all components
- Decoupling capacitor definition
- Generation by FSP of a database compatible with ALLEGRO
- Generation by FSP PCB design placement and HDL schematics .
- Generation by FSP of FPGA pin file assignment
- Import of the FSP schematic in top design
- Import of the FSP allegro database In allegro
- Layout of the design with pin swap capability under control of FSP engine
- Export to FSP of the modify data-base for more accuracy check and validation by the designer
- Export to FPGA tools the new pin file assignment

During all different stage no manually enter potentially source of error

The numerical part of the board have been designed using FSP.

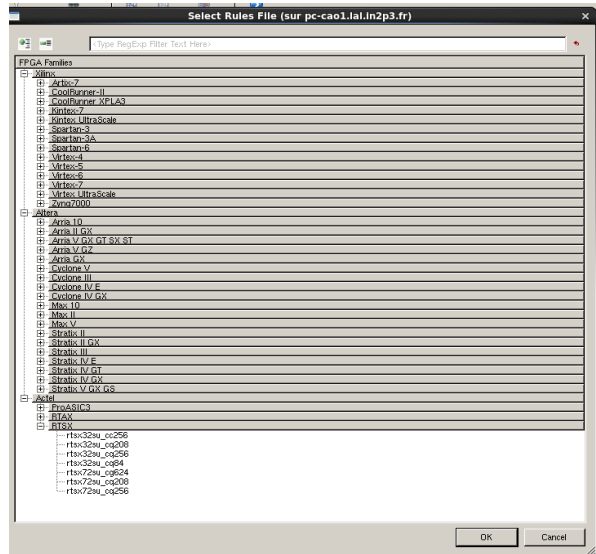
To achieve this FSP project I have use FPGA libraries delivered by Cadence, and also some others like connectors but we have to define nearly all the others

A snapshot of FSP board canvas with all the interconnection realize by FSP in dependence of the relative placement of the components and by taking into account of the pins rules.

To succeed to properly interconnect all the net it's necessary to schedule the interface routing and fix the routing of some nets

Canvas toile

FPGA selection FSP Project

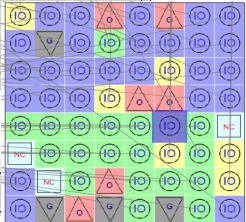


Component definition 1 FSP Project

Rules Viewer (pc28f00ap30bf) (sur laob.lal.in2p3.fr)

Expand All Collapse All Undo Redo Filter Find Replace Cut Copy Paste Show/Hide Columns Reset Width Clear Highlight Refresh Export CSV Import CSV

Pin Name	Pin Number	Pin Type	Symbol Pin Name	Voltage Level	ID Standard	Target Pin Function	Diff. Type	Diff. Par. Pin	Serial ID TRX Pin	Clock Grp.
<ul style="list-style-type: none"> Interface_Type=NormalInterface target_Family=Armv7VGA_MiscV unit=bus pin_size=100000 isde_type=pad-96_1000 instances_prefix=H gdescription=Paradelet20VOR120Vack120necessary par_L_height=700000 par_width=700000 x_offset=-8 y_offset=7 group.group_name=power group_number=1 group_color=#FF0000 gdescription=vcq120vcq120vc group.group_name=pad group_number=5 group_color=#000000 gdescription=pad120vss group.group_name=Address group_constraint=same_bank group_number=6 group_color=#0000FF gdescription=hwms25v120w12033v group.group_name=Data group_constraint=same_bank group_number=7 group_color=#00FF00 gdescription=hwms25v120w12033v group.group_name=CONTROL group_constraint=same_bank group_number=8 group_color=#FFFF00 gdescription=hwms25v120w12033v ADD11 A1 Input ADD11 LVCMOSS GIO ADVN P6 Input ADVN LVCMOSS GIO CLK E6 Input CLK LVCMOSS GIO DEN P8 Input DEN LVCMOSS GIO RESETN D4 Input RESETN LVCMOSS GIO WEN D8 Input WEN LVCMOSS GIO WPN C6 Input WPN LVCMOSS GIO group.group_name=HC group_number=9 group_color=#000000 gdescription=NO120CONNECT group.group_name=ctrl_2 group_number=10 group_color=#00FF00 gdescription=CONTROL_2 										



Show Package View

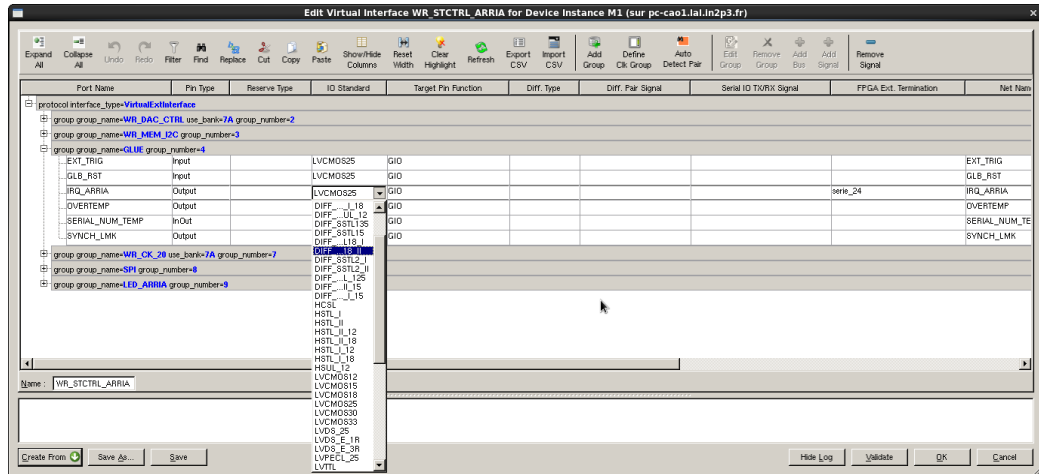
Component definition 2 FSP Project

protocol interface type=VirtualInterface

Port Name	Pin Type	Reserve Type	IO Standard	Target Pin Function	Diff. Type	Diff. Pair Signal	Serial IO TX/RX Signal	FPGA Ext. Termination	Net Name
group_name=WR_DAC_CTRL use_bank=TA group_number=2									
group_name=WR_MEM_DCC group_number=3									
group_name=GLIE group_number=4									
.EXT_TRIG	Input		LVMOS2S	GPIO					EXT_TRIG
.GLB_RST	Input		LVMOS2S	CONFIG_D14					GLB_RST
.IRQ_ARRIA	Output		LVMOS2S	CONFIG_D15					IRQ_ARRIA
.OVERTEMP	Output		LVMOS2S	CRCERROR			sern_24		OVERTEMP
.SERIAL_NUM_TEMP	InOut		LVMOS2S	CVP_CONFDONE					SERIAL_NUM_TE
.SVNCH_LMK	Output		LVMOS2S	DCLK					SVNCH_LMK
group_name=WR_CK_20 use_bank=TA group_number=7									
group_name=SPI group_number=8									
group_name=LED_ARRIA group_number=9									

Name: WR_STCTRL_ARRIA

Component definition 3 FSP Project



A zoom of the connectivity where we can see the capability of the system to manage a daisy interconnection between 4 components

On the left side the net view windows that allows to check the realize connectivity order by components

One of the very interesting feature is decoupling capacitor. You can define for each components and each power supply the decoupling capacitor .

Advantageously, In ALLEGRO when you place the capacitor there are grouped by component and by power supply .

In old development methodology you have to attach manually capacitor to component

Other functionality, the power assignment.
For each component yo can define power supply.

For big FPGA , up to 2 thousand pins, you have a huge numbers of powers pins (further hundred), as the system has the exact knowledge of all powers pins there is no risk to forgot any power pins.

The schematic generation.

Related to the design connectivity, FSP can generate HDL schematics. The main contribution of this state is the automatic generation of HDL component as well as the writing of net interconnect. As there is no human intervention no error possible at this stage. The HDL schematic is the exact replica of the interface interconnect define by the designer

Furthermore it automatically add the capacitor on the schematics

This schematics can be easily imported in the top design.

A view of the resulting schematic This one could be modified by users and be preserved at each new iteration.

The other main contribution is the generation of the pin constrain for the FPGA. It can be made for all the FPGA of the project and at any stage of design.

A view of the generated files with I/O standard definition and the pin assignment

An Allegro view of the current board

As FSP is base on interface base connectivity, this concept is passed to ALLEGRO by the ability to define and use bundle. Each interface define at FSP level became a bundle in ALLEGRO.

The bundle shape can be modifies to take into account the layout possibility

During iterative process you need to synchronize FSP to ALLEGRO, this can be done easily in allegro using a set of command.

During the routing with ALLEGRO the system highlight the authorize pins and assign color code for the different interfaces. This pin swap capability is under control of FSP data base.

During this stage it's not mandatory to refer to this pin planner of the EDA tools to check if is it possible to swap those pins

At the end of the swap modification it's mandatory that the designer validate the modification with a full synchronize ALLEGRO to FSP data-base. At this level the system perform an extensive verification.

A new schematics generation and import in the top design is necessary to keep the synchronism everywhere.

Last step a new FPGA pins constraints need to be generate.

My conclusion

Main feature of fsp

Improvement on somme points

My design save time

Changemnent

Easy design reuse



The future acquisition system

It's Distributed acquisition system where digitalization is performed the most closer as possible of the LNA to decrease the cable length to limits the SWR effect

The new issue of this architecture is the synchronization of a distributed system.

With this architecture there is no limitation of distance between antennas

This architecture has been made possible by using new FPGA family ARRIA V. there are fast and low cost and integrate further transceivers up to 10Gb/s