Développements en TSMC 65nm dans le cadre de la collaboration RD53

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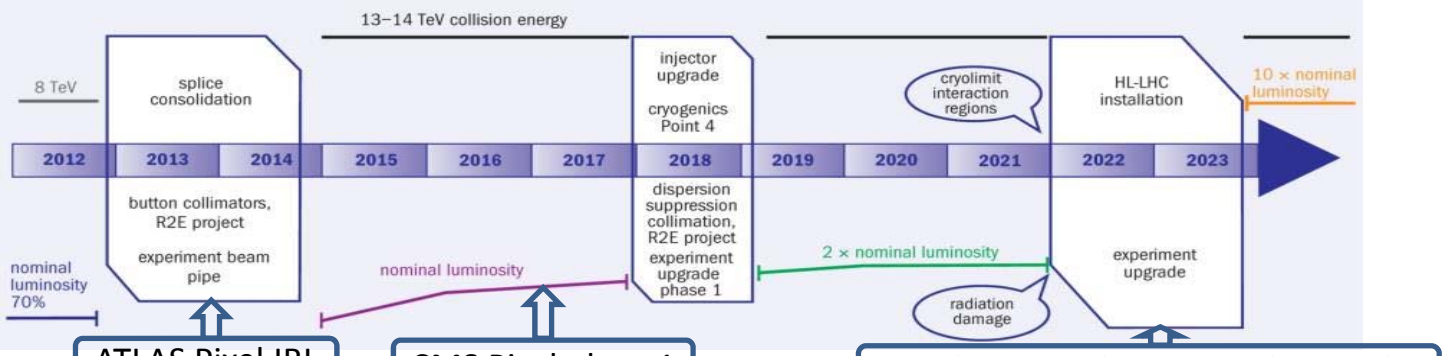
M. Menouni[1], A. Rozanov[1]

(1): CPPM
(2): LAPP

plan

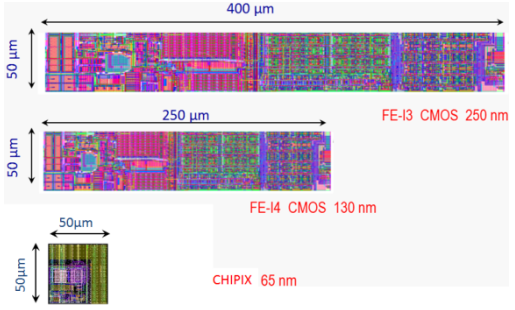
- Contexte
  - RD53
    - Objectif
    - Structure
- IP Block
  - Chip
    - PROTO65V1
    - PROTO65V2
  - Description Blocks
- Irradiation
  - Banc de test
  - Résultats
  - Model Irradiation
- Perspectives

RD53 objectif



Chip	FEI3	IBL-FEI4	Phase2-FEx5
Taille pixel	50x400um^2	50x250um^2	50x50um^2
Taille puce	7.5x10.5mm^2	20x20mm^2	> 20 x 20 mm^2
Transistors	3.5M	87M	~0.5G
Freq. évts	100MHz/cm^2	400MHz/cm^2	1-2 GHz/cm^2
BPW	40Mb/s	320Mb/s	2-4Gb/s
Radiation	100MRad	200MRad	1GRad ->0.5GRad
Technologie	250nm	130nm	65nm
Pixel density	4000 pix/cm^2	8000 pix/cm^2	40000 pix/cm^2
Pixel quantity	2880	27000	<160000
Conso.	~1/4 W/cm^2	~1/4 W/cm^2	~1/4 W/cm^2

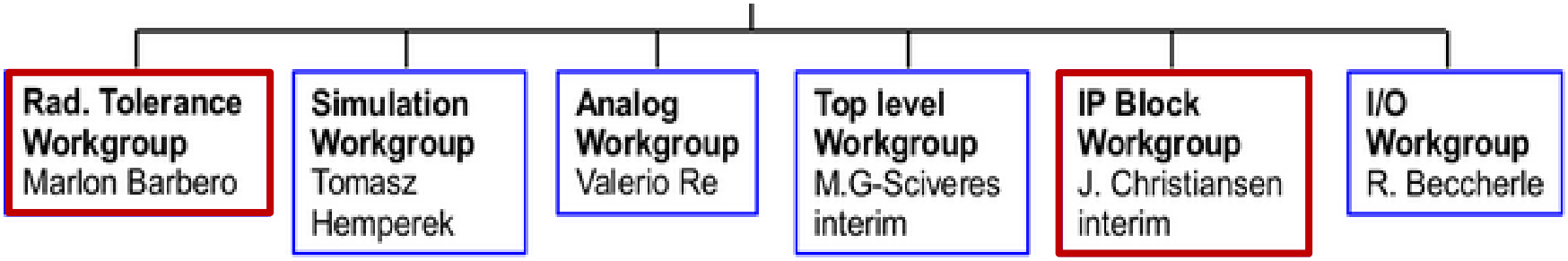
- Conception ASIC de lecture tech. 65nm
  - Détecteur pixel hybride - ATLAS – CMS Phase 2
- Points critiques:
  - Radiation élevée: 1 Grad (estimée sur 10 ans).
    - Possible avec des restrictions
  - Taille:
    - Chip: ~ 2×2 cm^2
    - Pixel: 50x50µm^2



  - Bande Passante: 2-4 Gbps / IC

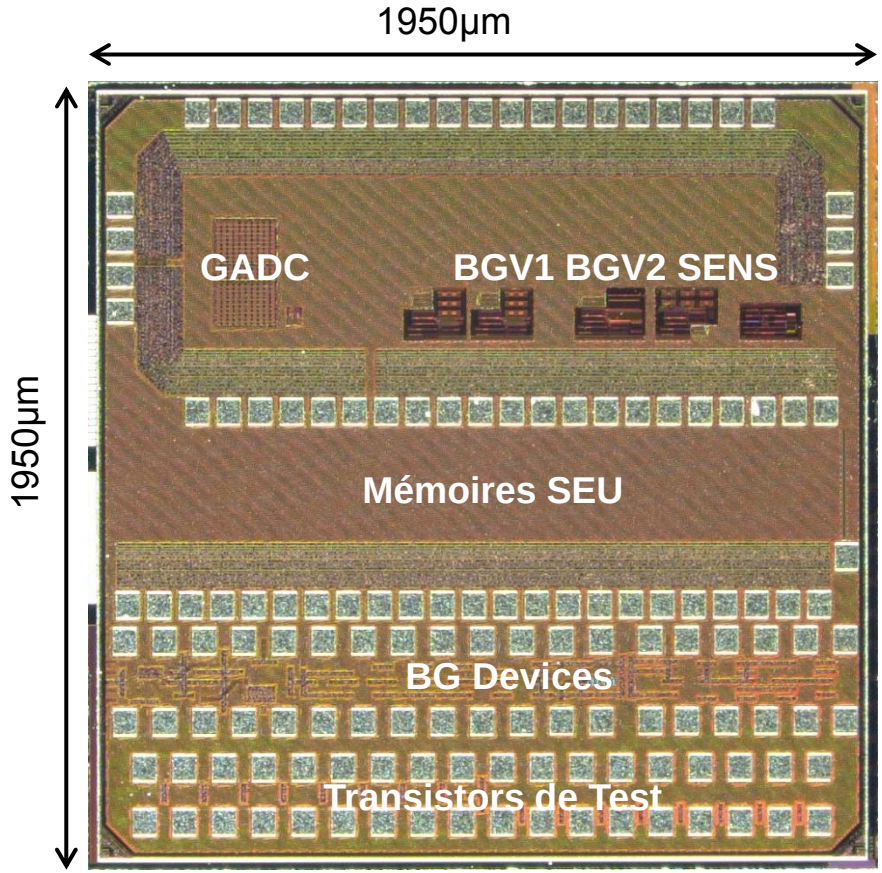
RD53 structure

- RD53 représente une centaine de personnes répartis dans environ 19 instituts (Bari, Bergamo-Pavia, Bonn, CERN, CPPM, FNAL, LBNL, LPNHE, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague, PSI, RAL, Torino, UC Santa Cruz)
- Divisée en 6 groupes de travail
- Spokesperson: Maurice Garcia-Sciveres (LBL) / Jorgen Christiansen (CERN)



: Activités CPPM

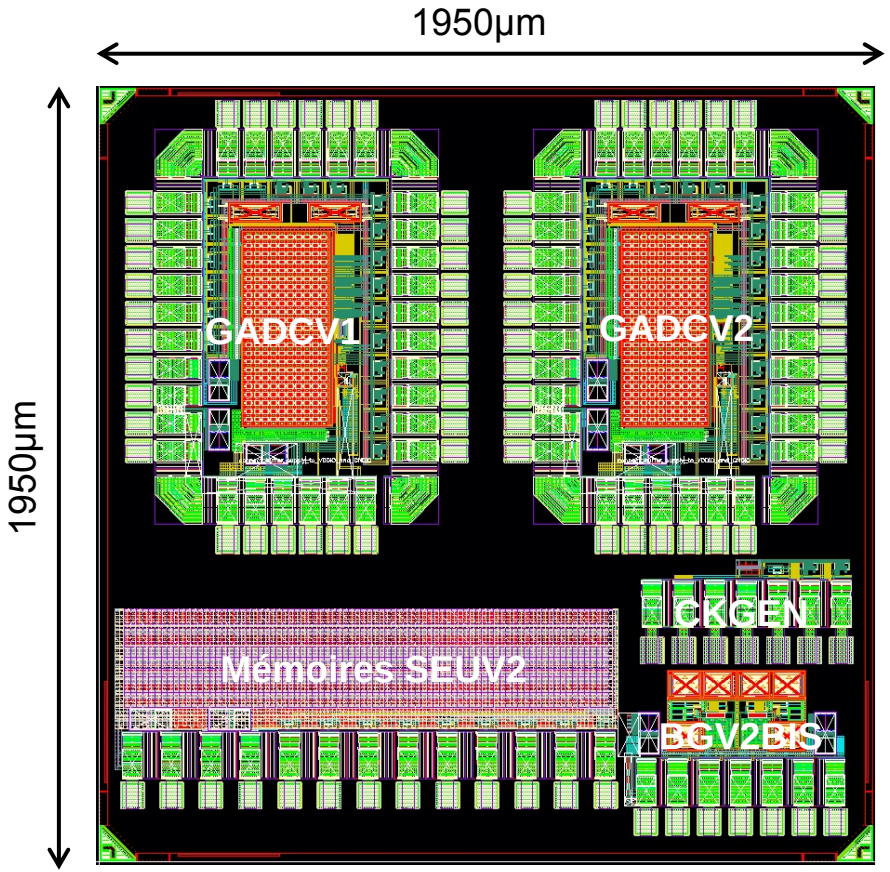
PROTO65V1



- PROTO65V1 (fin 2014)
  - Run TSMC 65nm mini@sic via europractice
  - Cell. digitales ARM

Block	Commentaires
GADC	Generic ADC type SAR (monitoring)
BGV1	BandGap (diodes Trans. Bipolaire)
BGV2	BandGap (diodes Trans. PMOS)
BG Devices	Diode BandGap's
Memoires SEU	- Triple redondance - DICE - HammingCode - Delai
Transistors de test	Matrice transistors (differents W/L)

PROTO65V2



- PROTO65V2 (début 2016)
  - Run TSMC 65nm mini@sic via CERN
  - Cell. digitales CERN

Block	Commentaires
GDACV1	Generic ADC type SAR (monitoring)
GADCV2	GADCV1 + registres W/L minimum
Mémoires SEU	- Triple redondance - DICE . Anneaux de garde . Interdigités
CKGEN	Générateur d'horloges non recouvrantes
BGV2bis	BandGap (diodes Trans. PMOS)

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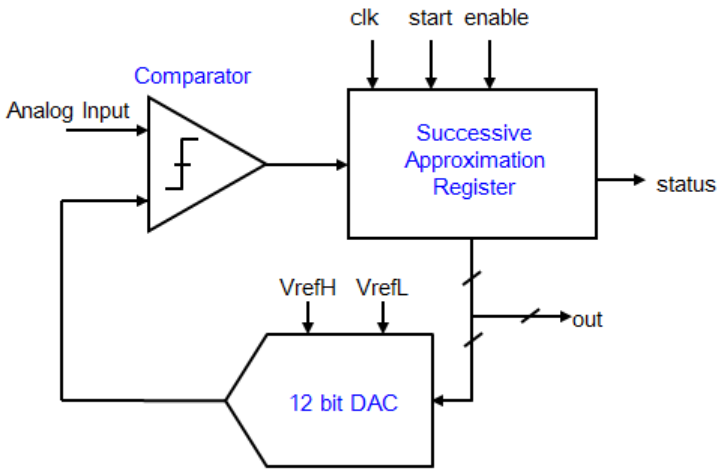
GADC

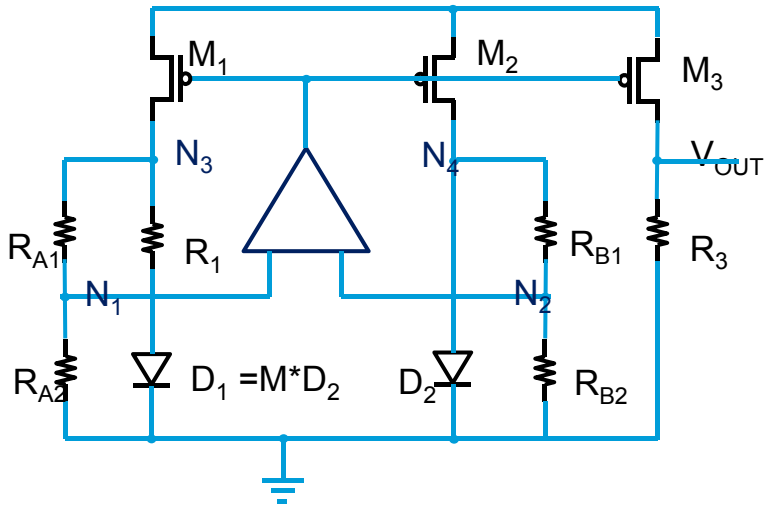
General ADC: monitoring, courant de fuite, T°C, références, …

Parameter	Value
Supply voltage	1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Architecture	SAR
Conversion clock	312 kHz (40 MHz CLK/128)
Resolution	12 bit
Input range	0 to 1 V (LSB = 244 µV)
Integral Non Linearity (INL)	± 1 LSB
Differential Non Linearity (DNL)	± 0.5 LSB
Capacitor	MIMCAP
Power	< 1mW (depends on frequency)
Trimming	Yes (6 LSB)
Status (end of December 2015)	Second prototype designed
TID	500 MRad
Designer (Email)	menouni@cppm.in2p3.fr awang@cppm.in2p3.fr renaud.gaglione@lapp.in2p3.fr



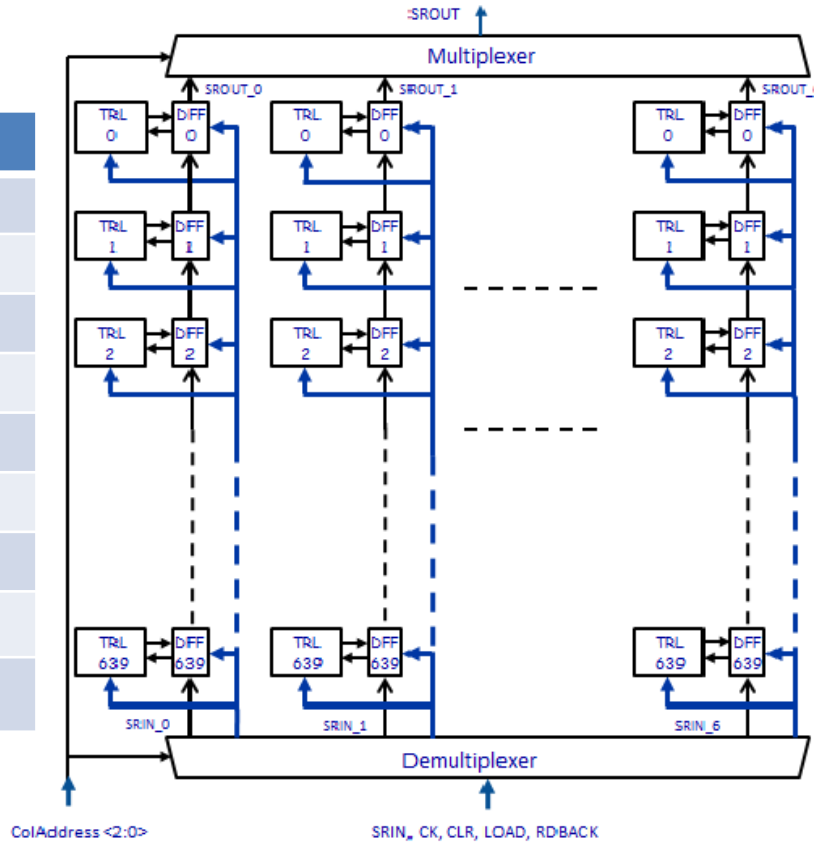
Référence de tension

Parameter	Value
Supply voltage	Typ 1.2 V (±10%)
Temperature range	-40 °C to +60 °C
Active element	V1: BJT_PNP10 V2:PMOS (DTMOS)
Bandgap voltage output	400 mV – 600 mV – 800 mV
Temperature coefficient	400 ppm/°C max
Noise	20 µV RMS max
Max variation (PVT, mismatch)	< 4 mV
Power supply rejection	TBD
Consumption	500 µW (main stage)
Startup circuit	Yes
Trimming	Yes (??)
Max variation (1GRad, 10^{16} n/cm^2)	<4mV
Status (end 2015)	2nd prototype under design
Designer (Email)	menouni@cppm.in2p3.fr



SEU

Parameter	Value
Column multiplexed	7
Column 1	Triple cell
Column 2	Column 1 (W/L min)
Column 3	DICE (guard ring)
Column 4	Interleaved DICE
Column 5	Delay (5ns +/- 1ns)
Column 6	Hamming Code
Status (end 2015)	2nd prototype under design
Designer (Email)	fougeron@cppm.in2p3.fr



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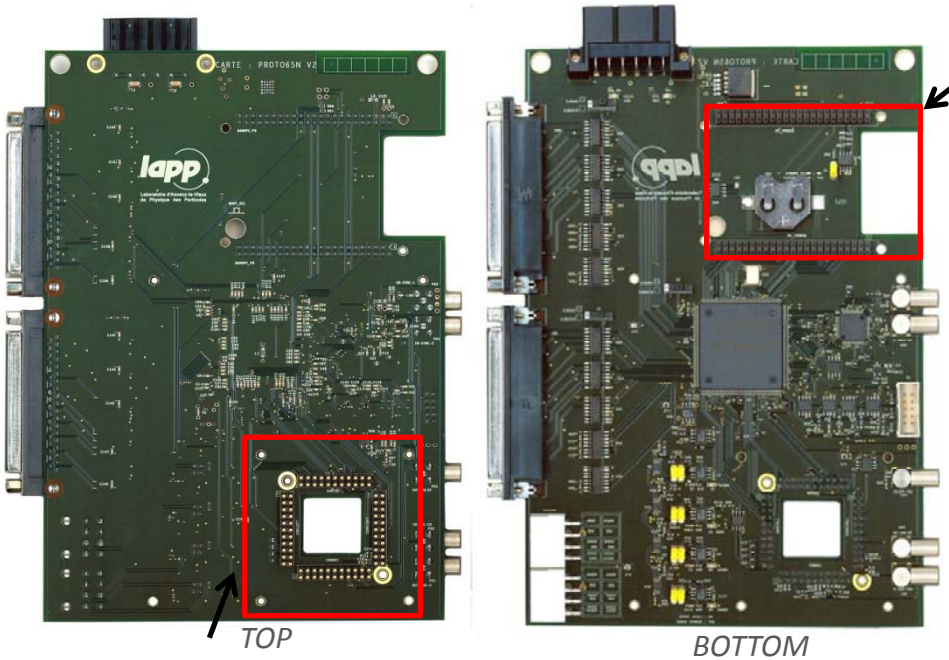
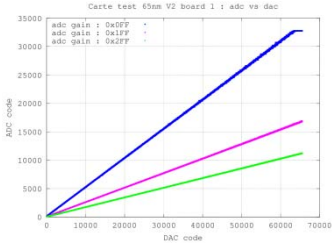
Banc de test (1/2)



carte fille échantillon

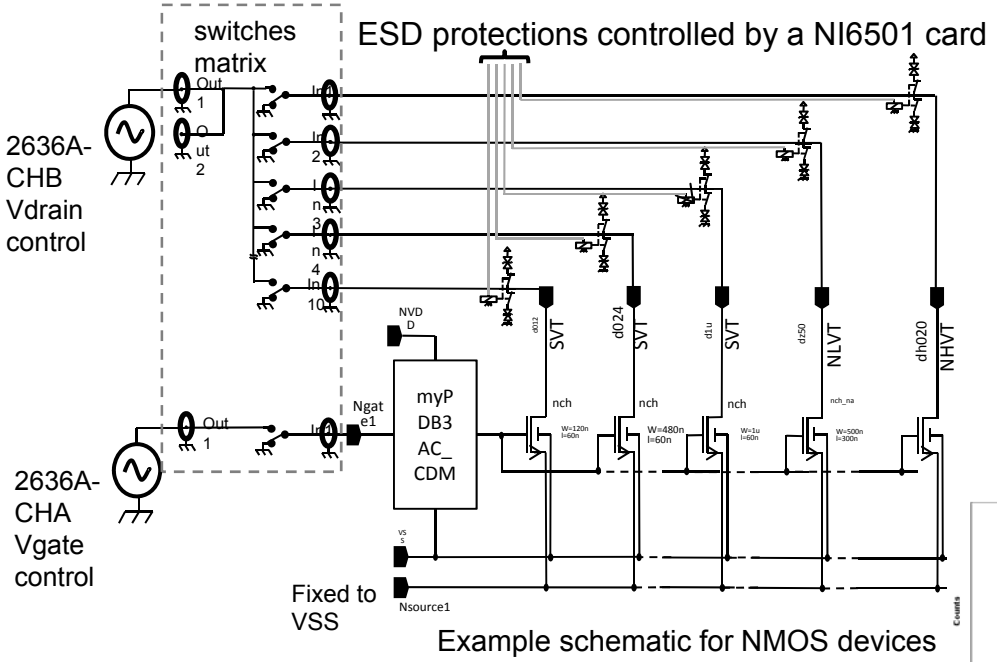
- Carte Beagleone associée à un FPGA
  - Interface Ethernet
  - Programmation flexible
  - Séquences de tests
    - FPGA (EP3C16Q240XXN)
- Fonctionnalités:
  - 40 voies digitales (TTL/LVDS)
    - 40 TTL
    - 30 LVDS
  - 4 voies analogiques
    - 4 DAC 16 bits
    - ADC 14 bits
      - 4 voies
      - 3 gains



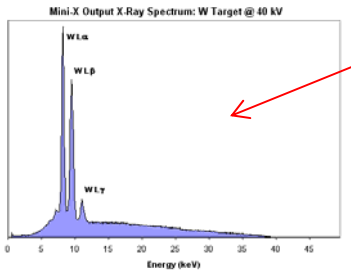
ADCout vs Gain

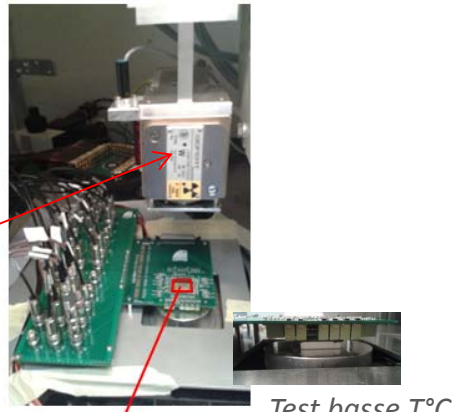
  - Monitoring alimentations, température
  - Compatible Irradiations (Source rayon X 10KeV, protons (PS CERN))

Banc de test (2/2)



- Banc de test transistors
  - Interface LabView
  - Séquences « ESD Safe »
  - Extraction Ion, Ioff, Vth, Gm
  - Compatible Irradiation Source X 10keV , proton (PS CERN)

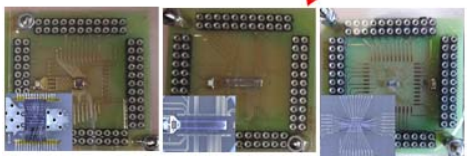




Test basse T°C

Setup source X

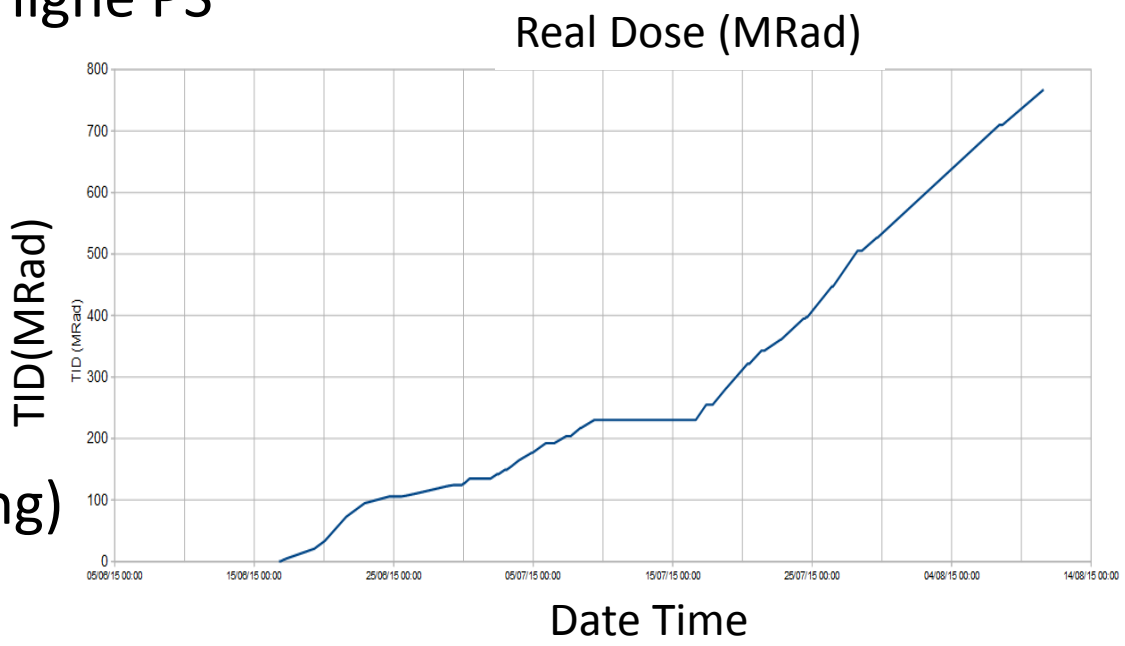
Dose rate : 2.5 kRad /s
Total dose: 1GRad
~1 semaine

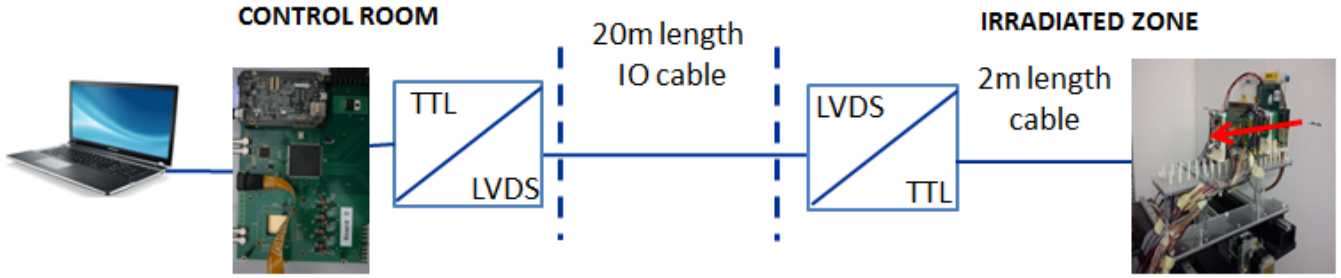


échantillons

Profil Irrad (PROTON PS – CERN)

- Faisceau protons 24GeV ligne PS
- Dose Totale:
  - 800MRad
  - ~ 2 mois
- Dose rate :
  - 400kRad/heure
- Arrêts faisceau (annealing)
  - Mesures intermédiaires
  - Réglage des installations





Setup proton PS CERN

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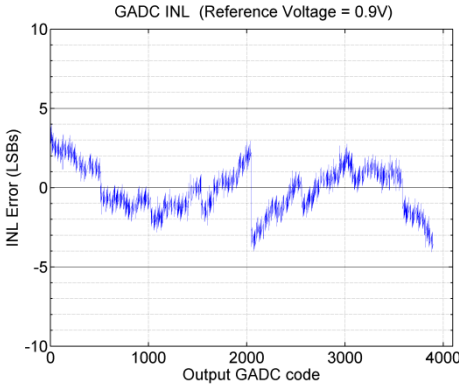
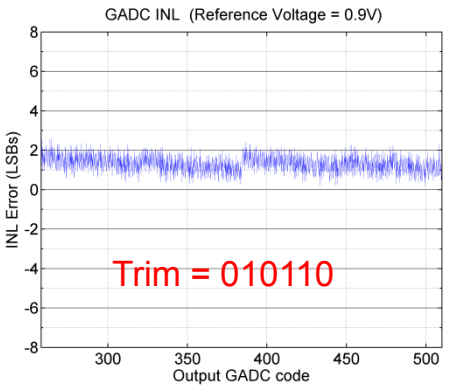
GADC

- Tension ref: 0.9V
- LSB = 220 µV
- The Global Non linearity :
  - INL =+/- 4 LSB
- Peak to peak noise < +/- 1 LSB
- Trimming compensation
  - LSB DAC 6bits (pas d' effet sur le MSB)
    - Trim = 111111 INL = 10 LSB
    - Trim = 000000 INL = 5 LSB
    - Trim = 010110 INL = 2 LSB
- Irrad (proton PS CERN):
  - 0-109 MRad
    - Offset < 10 LSB
  - 500 MRad
    - Offset élevé
  - 630 MRad
    - Plus de réponse

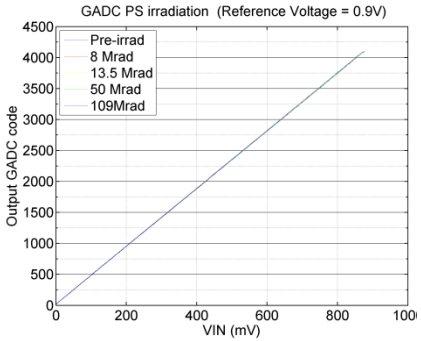


INL avant compensation

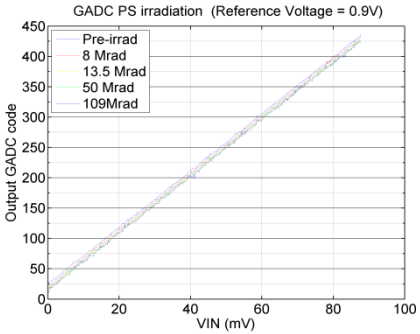


INL après compensation

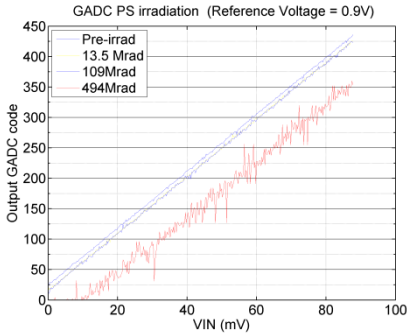
Test laboratoire



Linéarité Pre-Rad



Linéarité 109 MRad

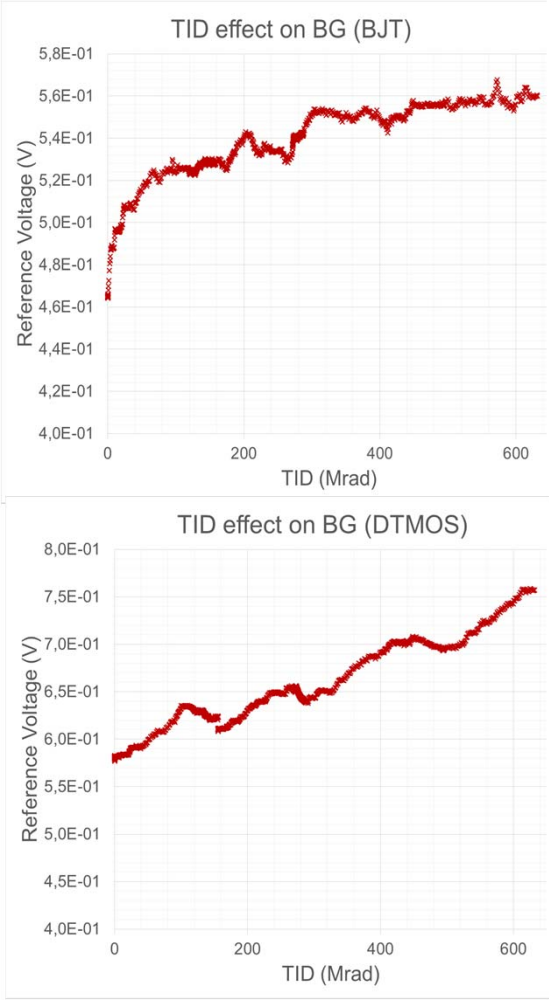


Linéarité 500 MRad

Test Irradiation

BandGap

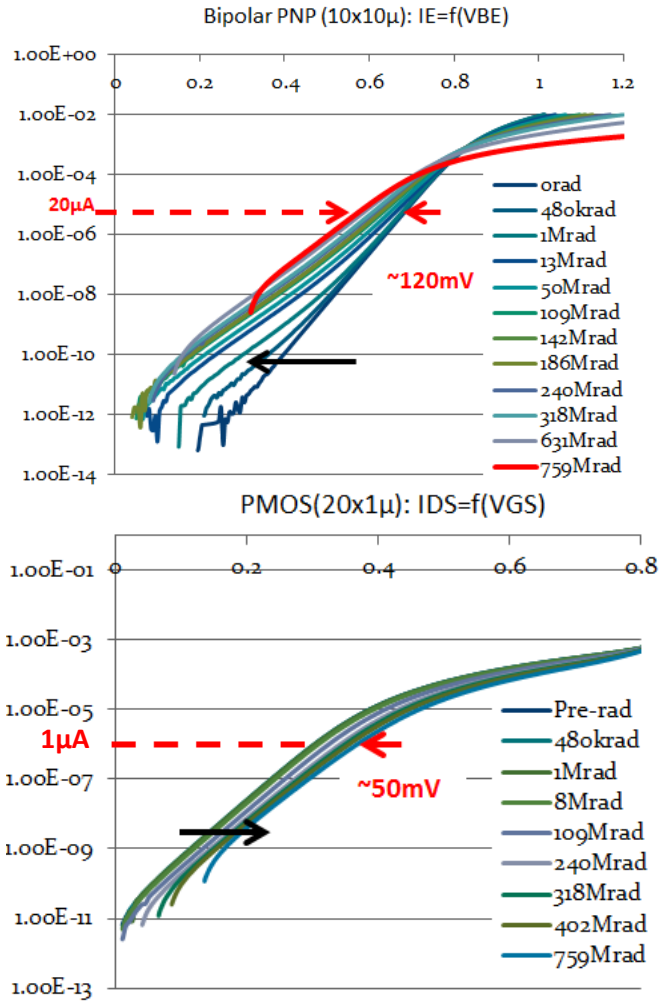
- Irradiation PROTON PS
  - BG version Bipolaire
    - 0 – 100MRad: Offset ~ 70mV
    - 200 – 600MRad: Offset ~20mV
  - BG version DTMOS
    - Déviation linéaire
    - Annealing pdt coupure faisceau significative
    - 0-630 MRad: Offset ~ 150mV



VoutBG vs dose

Diodes BandGap

- BJT
  - Ibias=20µA
    - 0-109MRad: Offset ~50mV
    - 200 – 630MRad Offset ~70mV
  - Offset équivalent au BandGap
  - Prochaine version Ibias ↗
- DTMOS
  - W/L=20µ/1µ (BandGap)
  - Ibias=1µA : Offset=45mV
  - Offset BandGap ↗
    - 2nd effet possible lié à la polarisation



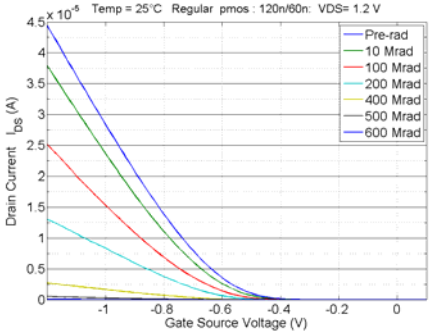
SEU

Architecture	device	surface	Error rate Nb err / spill		
			0 -> 1	1 -> 0	All
Delai	DFF for shift register	14.4µm²	5.6	2.9	4.2
	TRL for configuration	40µm²	0.082	0.04	0.06
	TRL + delai	54µm²	0.064	0.015	0.04
Hamming code	DFF for shift register	14.4µm²	6.07	1.72	3.89
	TRL for configuration	40µm²	0.06	0.015	0.037
	Hamming code 8b4b	50µm²	0.467	0.185	0.326

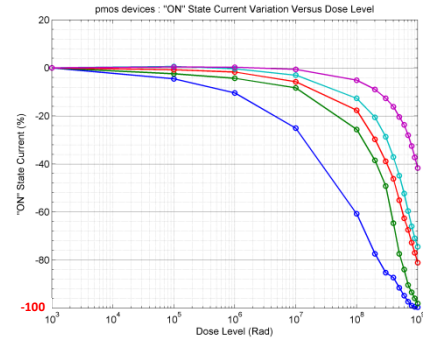
- Comparaisons :
  - TRL vs TRL délai : gain 1.5
  - Latch DFF vs Hamming code : gain 12
    - Moins intéressant que la TRL
    - Possible optimum bits Data / bits de parité

Transistors

- Transistors (≠ W/L) testés en rayon X et en protons
- Annealing: température ambiante + 7 jours à 100°C
  - NMOS:
    - IOFF ↗ 2 ordres de grandeur (120n/60n)
    - ION <50% après annealing
  - PMOS:
    - 120n/60n, 240n/60n ION ↘ 100%
    - ION ~80% après annealing



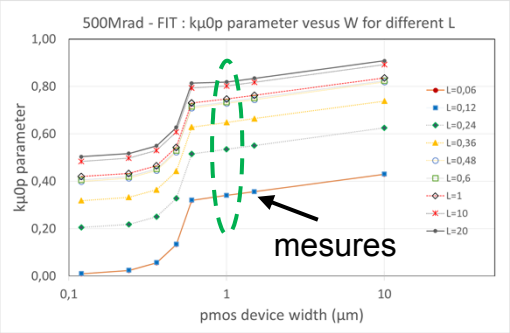
PMOS 120/60n vs dose



PMOS Ion vs dose

		Résultats irrad. 20°C		Résultats irrad. -15°C		Techno.B résultats irrad. -15°C	
shift		I_{ON}	V_{TH}	I_{ON}	V_{TH}	I_{ON}	V_{TH}
NMOS	120/60	-70%	0.35V	-65%	0.33V	-52%	0.08V
	480/60	-70%	0.35V	-48%	0.18V	-50%	0.18V
PMOS	120/60	-100%	-	-60%	0V	-52%	0.08V
	480/60	-88%	0.05V	-52%	0.023V	-63%	0.06V

Model Irradiation



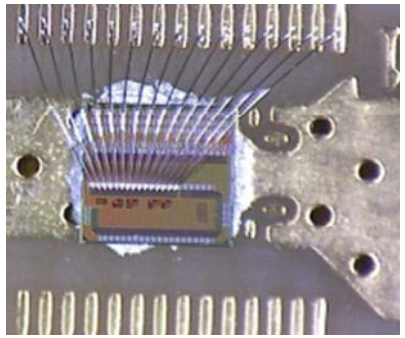
- Modification des models BSIM4 des transistors
  - NMOS: (variation du seuil, mobilité)
    - dvthn → vthn_prerad-vthn_rad
    - Kμ0n → μ0_rad/μ0_prerad
  - PMOS: (mobilité)
    - Kμ0p → μ0_rad/μ0_prerad
  - Chaque paramêtre est fonction du W/L du device
  - Manque encore des données (basse température, valeur petit W/grand L,…)
  - Création d'un corner supplémentaire 200 et 500MRad disponible pour la collaboration

INVD0	Time period (ns)					Frequency (MHz)				
Nb cell	Pre-Rad	200Mrad	% dev.	500MRad	%dev.	Pre-Rad	200Mrad	% dev.	500MRad	%dev.
1025	20.46	38.5	88.17	352	X16	48.87	25.97	-46.85	2.84	-94.2
2051	40.95	77.05	88.15	704	X16	24.42	12.97	-46.88	1.42	-94.2
3025	60.32	113.49	88.12	1037	X16	16.57	8.81	-46.83	0.96	-94.2

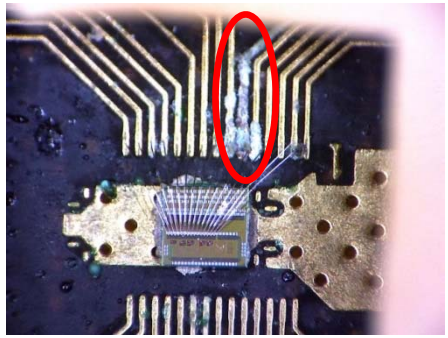
Simulation extracted corner 200-8500MRad (NIKHEF)

Retour d'expérience

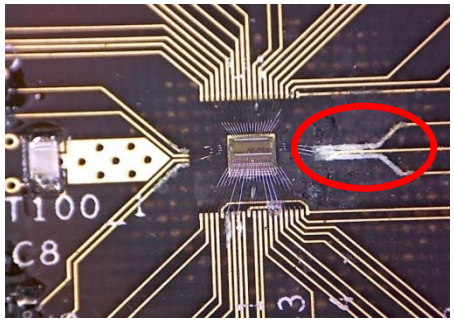
- Observation:
  - Pistes corrodées, bonding déconnectés ou en cc
- Causes probables:
  - traces d'Al(OH)3 (hydroxyde d'aluminium ≡ acide) produit par une réaction corrosive avec le chlore comme catalyseur,
  - Ambiance humide,
  - Pas de protection.
- Remède possible:
  - Protection des pistes (vernis épargne)
  - Changement de support polymide remplace le FR4
    - Résistance à la température (X2), prix plus élevés (X4)
  - Glob Top sur la puce
    - Contraintes thermiques, matériaux Rad-Hard….



PCB BanGap's pré-Rad



PCB BanGap's 800MRad



PCB GADC

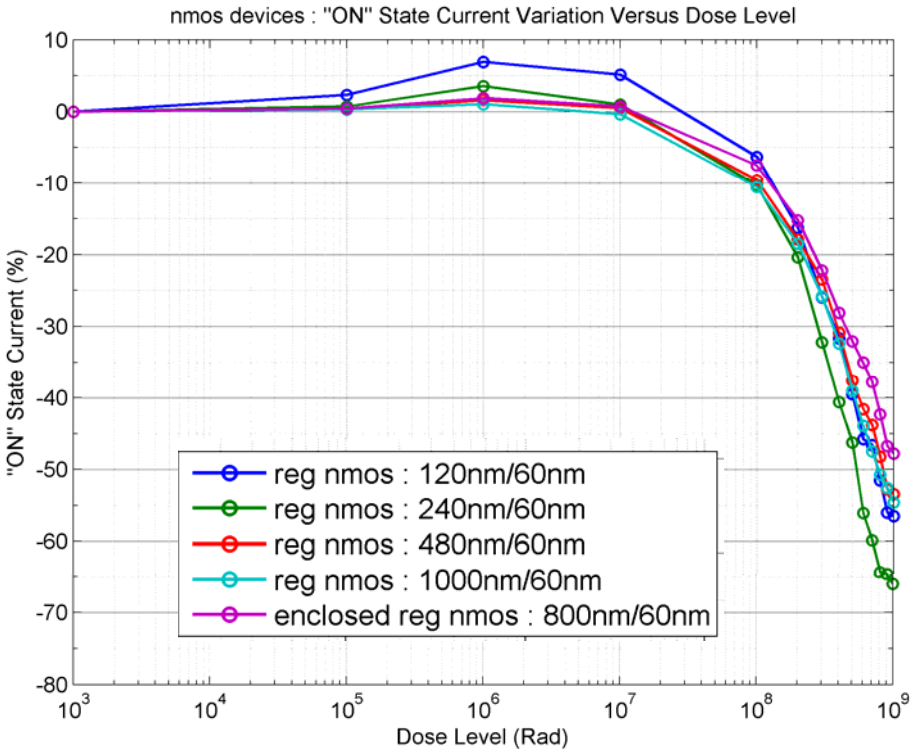
Perspectives

- 2016: réception du chip PROTO65V2
  - Mise au point de la carte mère « BeagleBon » quasi-finalisée
    - Séquence de tests, linéarité ADC, DAC,…
  - Câblage en cours
    - PCB « Rad-Hard » (sans halogen)
    - Test GADC
      - Layout DAC limitant les capacités parasites
    - Test BandGap
      - Polarisation interne, amélioration de la stabilité
    - Test SEU
      - Structure DICE, incidence de la structure interdigitée
  - Test en irradiation (PROTON PS)
    - SEU normalement en juillet
    - GADC, BandGap à l'automne
  - Possibles conceptions capteur de température, dosimètre

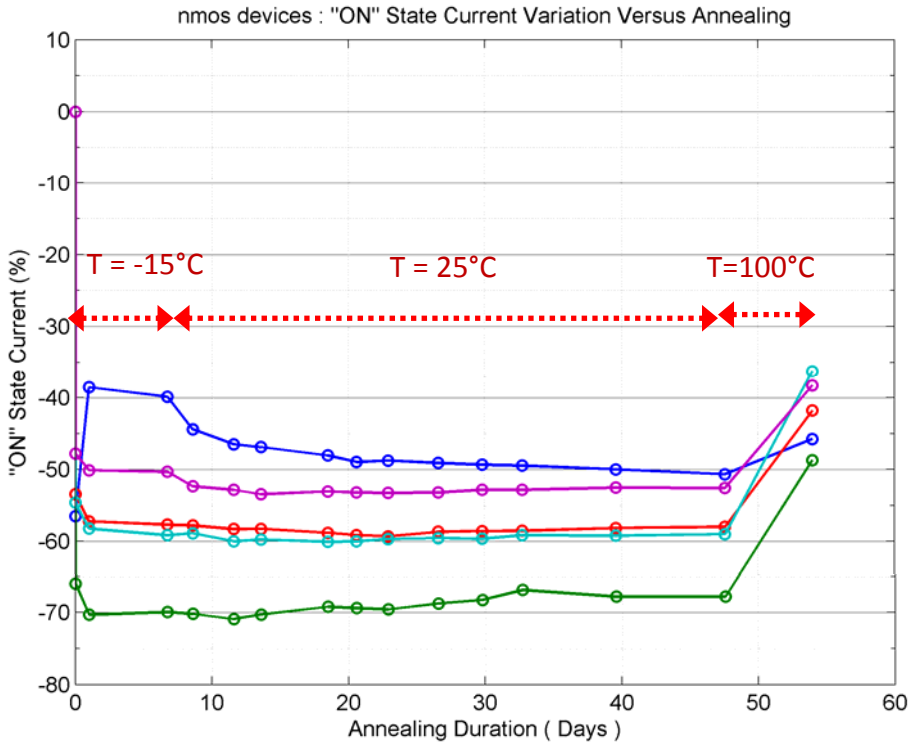
MERCI DE VOTRE ATTENTION

Backup

- NMOS: évolution du courant I_{ON}
  - -70% 240n/60n
  - annealing 7j à 100° Ion -40-50%, Vth ↘ <200mV, reverse annealing W=120n



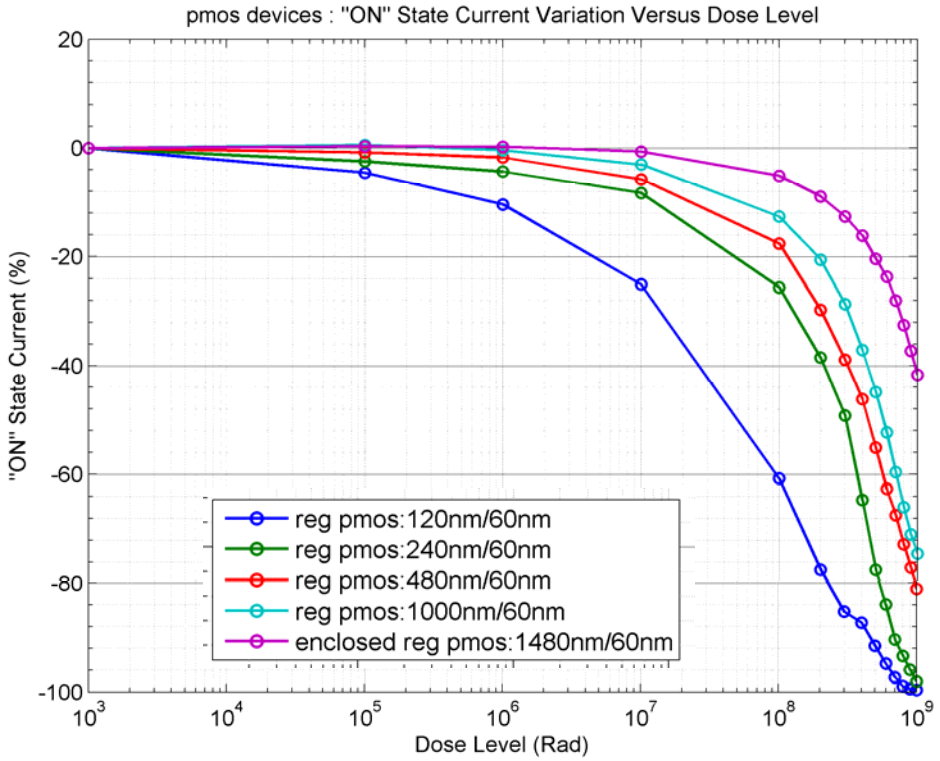
irradiation NMOS (ION)



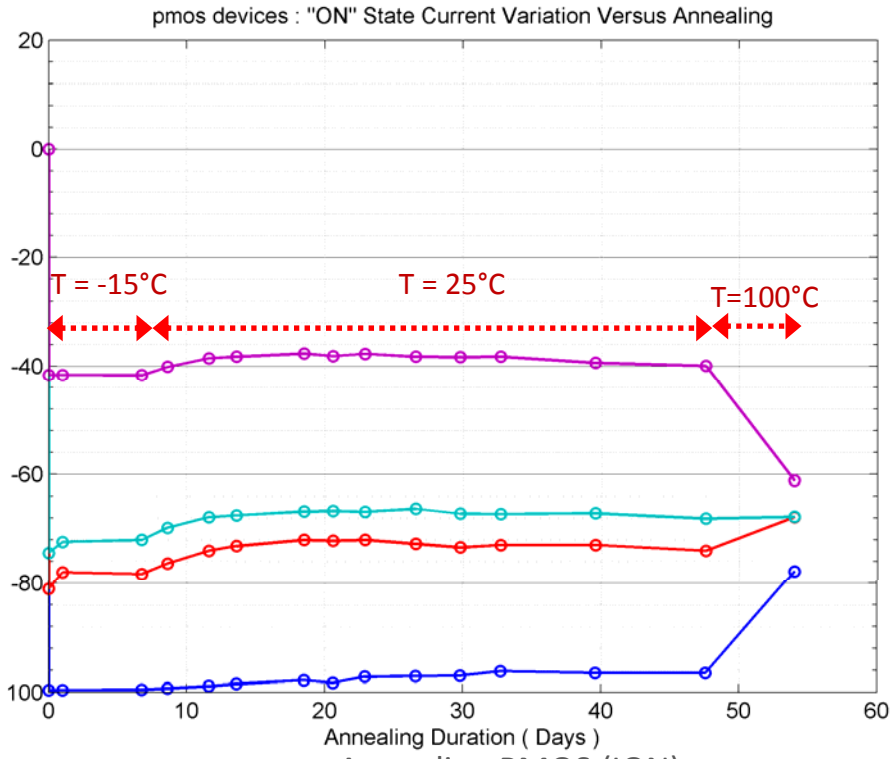
annealing NMOS (ION)

Backup

- PMOS: évolution du courant I_{ON}
  - -100% W=120n et 240n, annealing 7j à 100°-80-70%
    - Reverse annealing observé, Vth ↗ Gm quasi OK (-30%)



irradiation PMOS (ION)



Annealing PMOS (ION)