STEREO electronics overview

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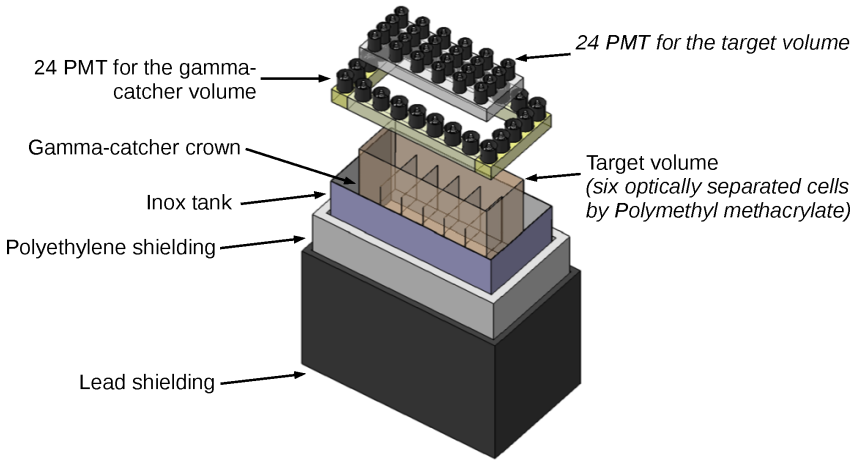
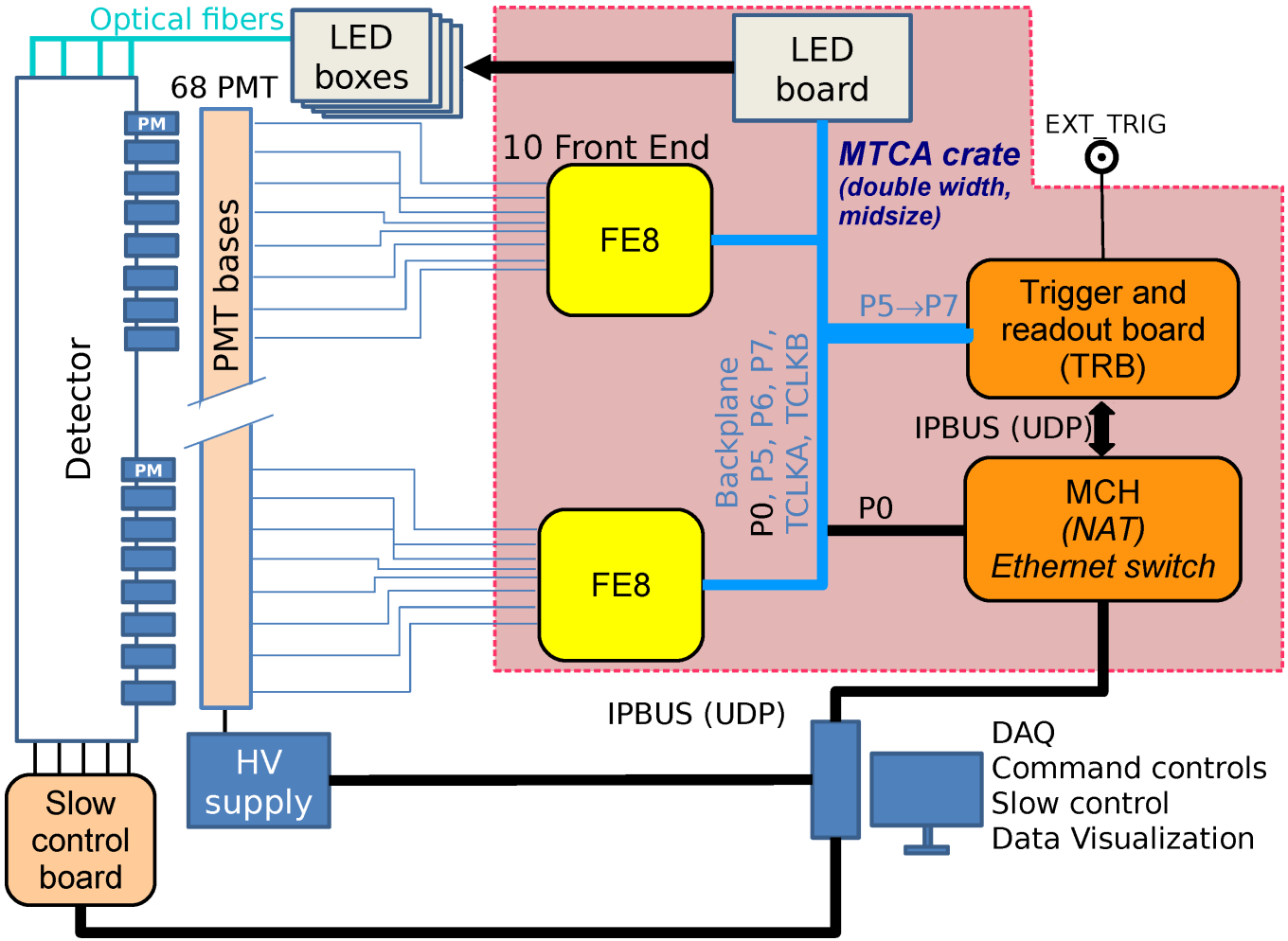
General requirements



- Monitor 68 channels required in 3 classes (for triggering)
  - 24 PMT for Gamma catcher
  - 24 PMT for target (gadolinium-loaded liquid scintillator)
  - 20 PMT for muon veto (Cerenkov detector)
- Withstand a **mean** trigger rate of 1 kHz
- Have no dead-time (pile-up excepted)
- Manage various trigger schemes and conditions (coincidence and anti-coincidence)
- Process signals on board: compute $\mathrm{Q_{tot}}$ and $\mathrm{Q_{tail}}$ for *Pulse Shape discrimination (PSD)*

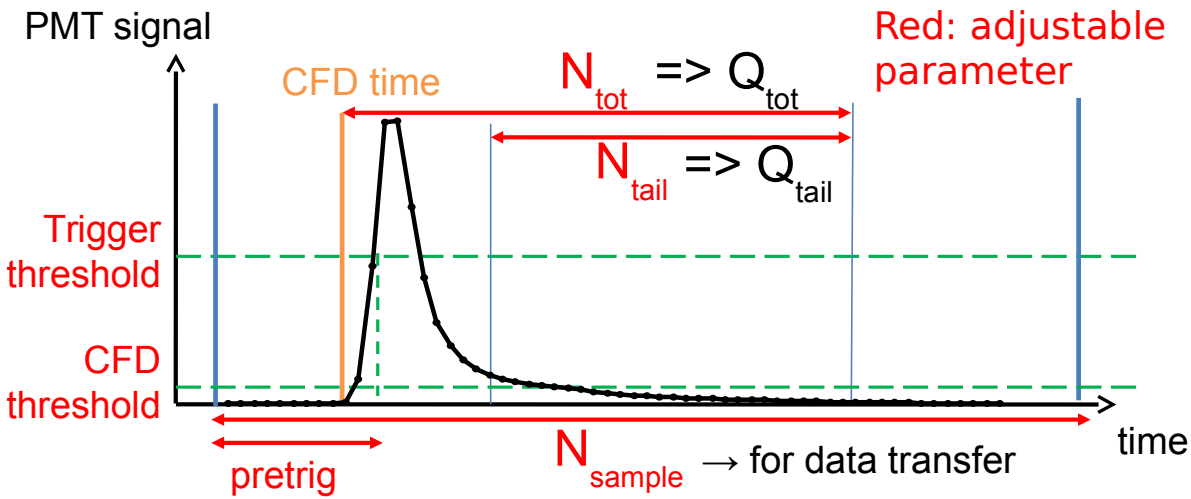
Electronics overview



- Trigger board (TRB) for: triggering, FE readout and LED control
- Communication FE $\leftrightarrow$ Trig Board with custom protocol
- Readout and slow control via IPBus (Secured UDP from CERN)

First level triggering (T1) and processing

1. FE emits a trigger when at least one PMT signal > trig threshold
2. Confirmed trigger (T1a) reception initiate PSD processing



- Beginning of signal is to be found with a *Constant Fraction Discriminator (CFD)* having its own threshold (above noise)
- Adjustable parameter defined prior to run
- $\mathrm{N_{tot}}$ represents typical pulse duration
- $\mathrm{N_{sample}}$ time window for analysis and samples to record in debug mode

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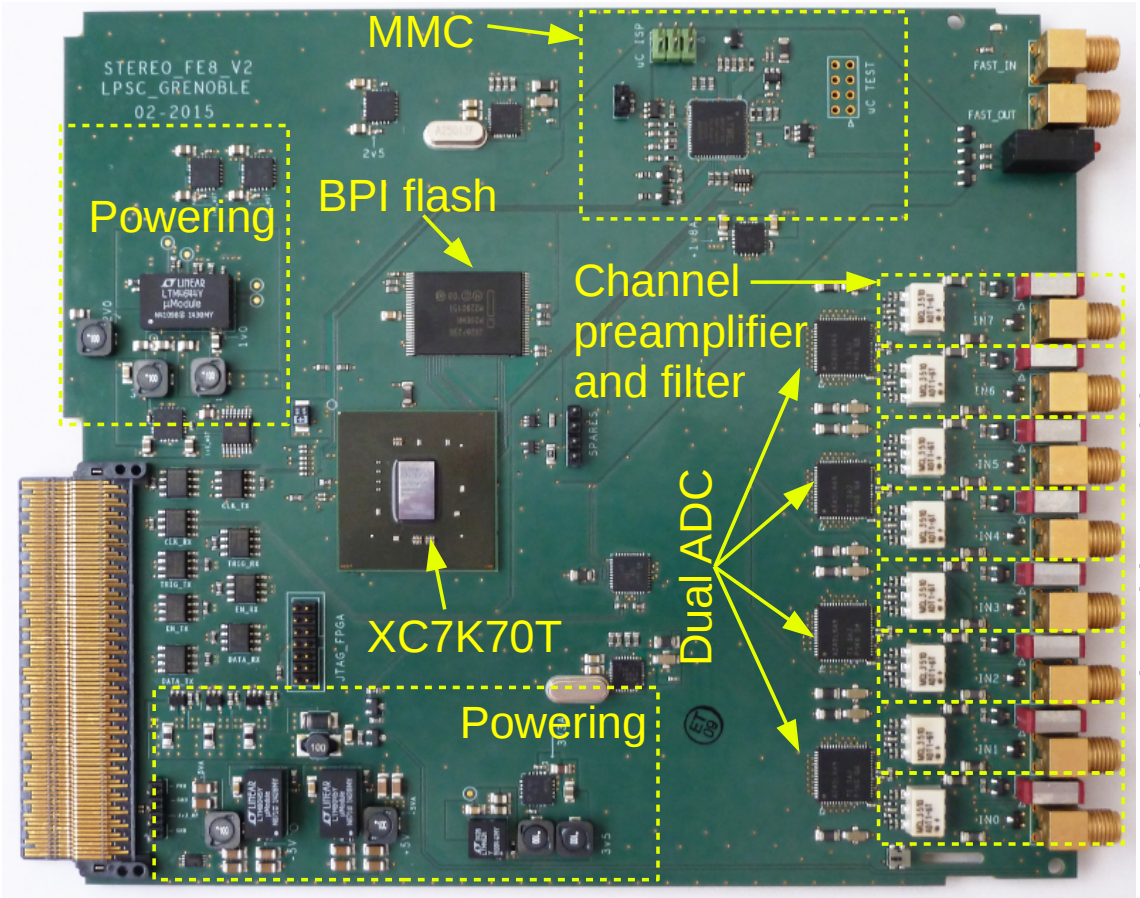
Front-end 8 (FE8) specifications

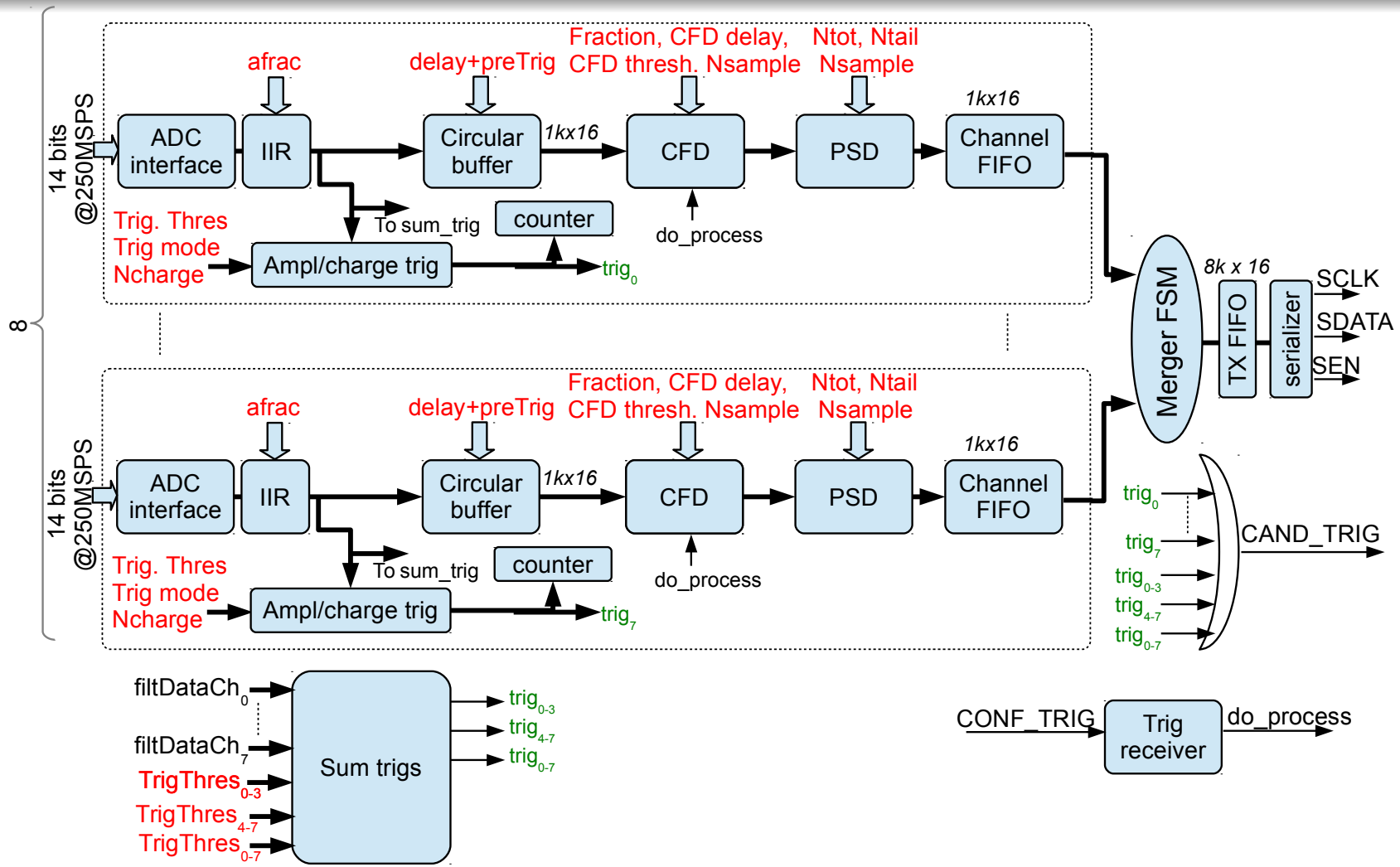
- 8 channels board (13 bit ADC @250 MSPS, dynamic range 1.0 V)
- Preamplifier + amplifier with 2 selectable gains, e.g x1 and x20
- The ADC input feature anti-aliasing filter (80 MHz)
- Readout by custom serial protocol, slow control by IPBus
- First level trigger on amplitude **OR** charge, selectable by mask :
  - Individual channel
  - sum of first 4 channels
  - sum of last 4 channels
  - sum of 8 channels
- Trigger bit inserted in the data flow
- Each channel has a high pass IIR to suppress pedestal
- Scalers for individual PMT monitoring
- CFD and PSD for each channel. $\mathrm{Q_{tot}}$ and $\mathrm{Q_{tail}}$ computed on board
- Transfer of $\mathrm{Q_{tot}} \times 8$, $\mathrm{Q_{tail}} \times 8$, zero crossing $\times 8$
- Optional debug mode to readout the $\mathrm{N_{samples}}$ used to compute CFD and PSD

FE8 hardware



- Main FPGA: XC7K70-2TFBG676,
- ADC: Texas Instrument ADS42LB49 (AC coupled, f_c >30 kHz)

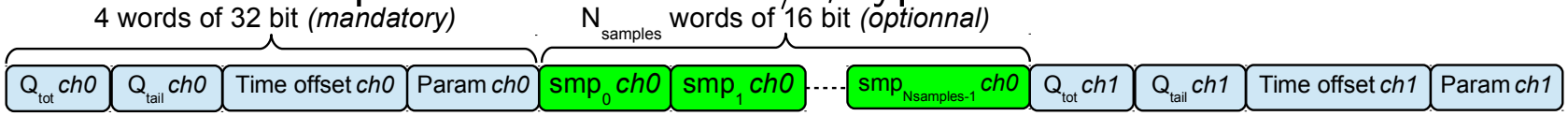
FE8 firmware overview



- Parameters are in red
- Pipelined processing: 1st CFD, then PSD, then data concentrated and finally serialized

FE8 ↔ TRB communication

- Serial link operated at 125 Mbit/s, typical frame content:



Average trigger rate limitation due to serial link

- In normal mode, rate limited at 125MHz/(4x32x8)=122 kHz.
- In debug mode, rate limited at 13.5 kHz (worst case, 64 samples).

- CFD time offset word contains:
  - N_ZC: relative offset of the CFD threshold crossing
  - Y1, Y2: CFD values before and after threshold crossing
- Param word contains:
  - ADC or IIR overflow: 1 bit
  - Trigger source bit (channel, sum4, sum8): 3 bit mask
- Triggering path at 250 MHz (to be sample accurate)

⇒ Delay from candidate trigger to confirmed trigger, a **circular buffer** is required in the front-end (about 120 ns or 30 samples)

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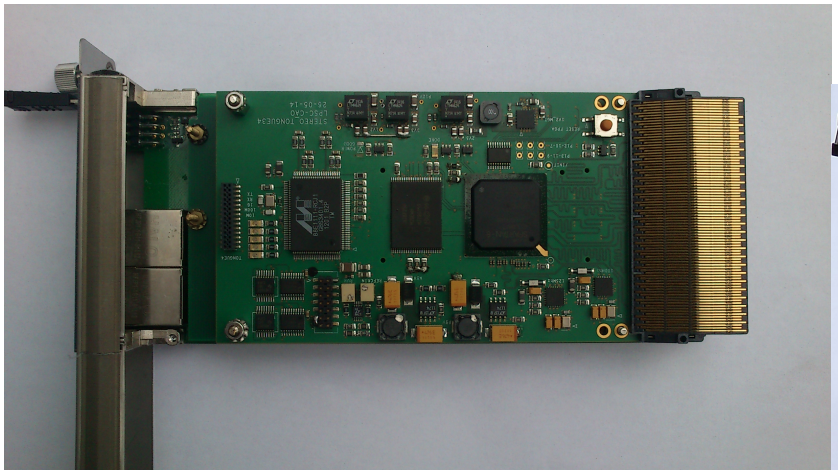
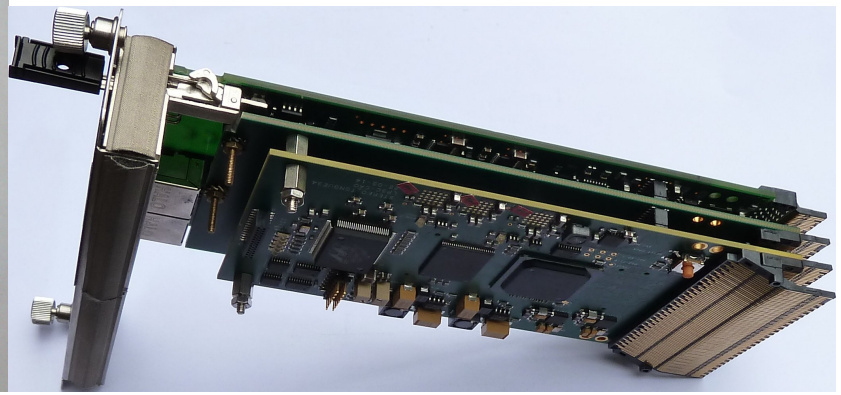
Trigger and Readout Board (TRB)

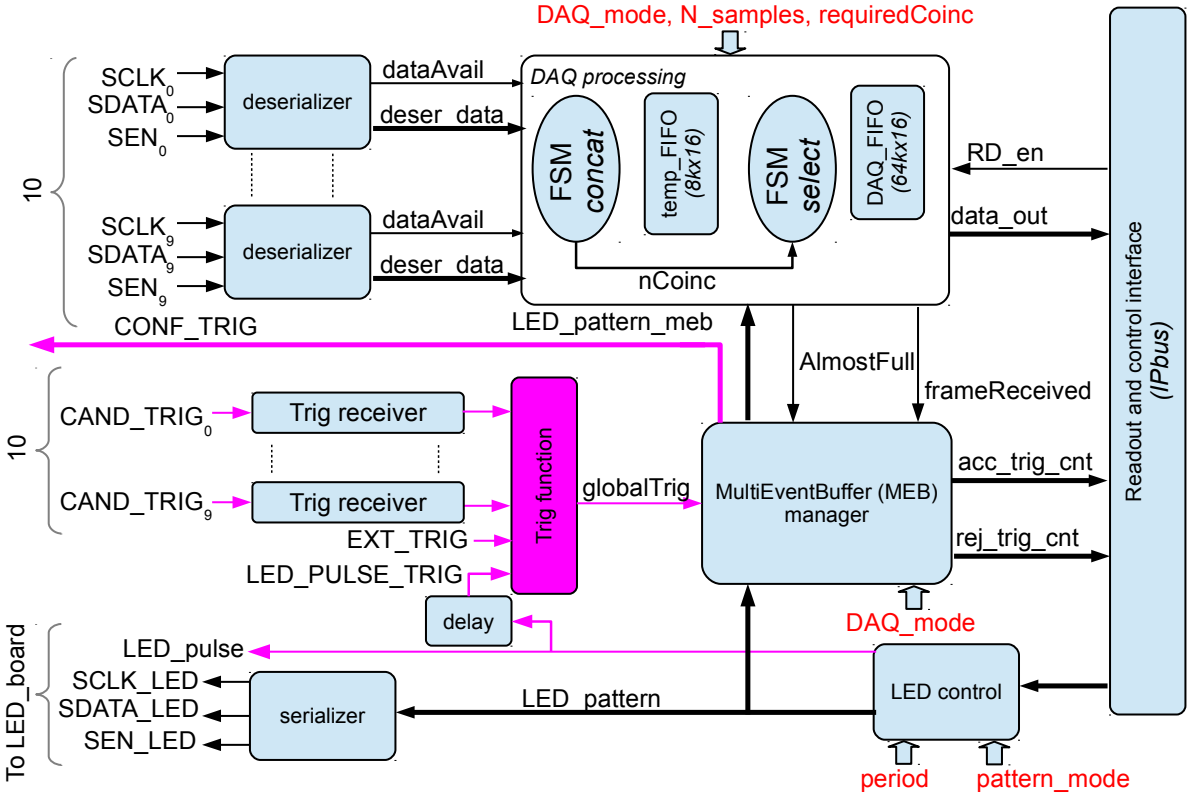




NAT-MCH and extensions (2 boards)

- Tongue 1: NAT-MCH featuring an Ethernet switch.
- Tongue 2: Clock trees (FCLKA, TCLKA), clock reception (TCLKB)
- Tongue 3: Main board with FPGA (XC6SLX45T-FGG484), power, Ethernet (GTP and spare phy)
- Tongue 4: Fast SMA inputs, RJ45 (spare Ethernet, LED box control)

TRB firmware



- MEB is implemented: up to 84 (normal)/6 (debug) consecutive triggers can be accepted (if separated by *N_samples* x 4 ns)
- T1 trig function.
- T2: event selection in hardware (FSM_select)
- In calibration mode (LED) several pattern sequences are possible.

Triggering

T1 trigger

- For now OR of the trigger issued by the FE8.
- FE8 triggers can be individually masked.
- Accepted and rejected T1 are monitored (32 bit counters).

T2 trigger

- Performed after T1 upon data reception in TRB.
- Event suppressed are not stored in DAQ_FIFO.
- For now T2 on coincidence is implemented: event is kept if the number of CFD thresholds crossed is above a programmed value for the whole system.
- Not monitored.

Typical readout frame

Common header:

- Word[0]: DATE LSB
- Word[1]: DATE MSB
- Word[2]: LED pattern
- Word[3]: T_VETO

Details:

- DATE is produced by a 32-bit counter incremented every 4 ns, recorded at T1a.
- T_VETO: time since previous veto trigger, resolution of 128 ns, 16-bit counter (max time 8.38 ms)

One channel data:

- Word[off+0]: Q_tot LSB
- Word[off+1]: Q_tot MSB
- Word[off+2]: Q_tail LSB
- Word[off+3]: Q_tail MSB
- Word[off+4]: CFD_time LSB
- Word[off+5]: CFD_time MSB
- Word[off+6]: Param word
- Word[off+7]: sample[0]
- Word[off+8]: sample[1]
- Word[off+...]: sample[i]

Trigger rate in normal mode above 1 kHz (related to the readout rate of the acquisition computer).

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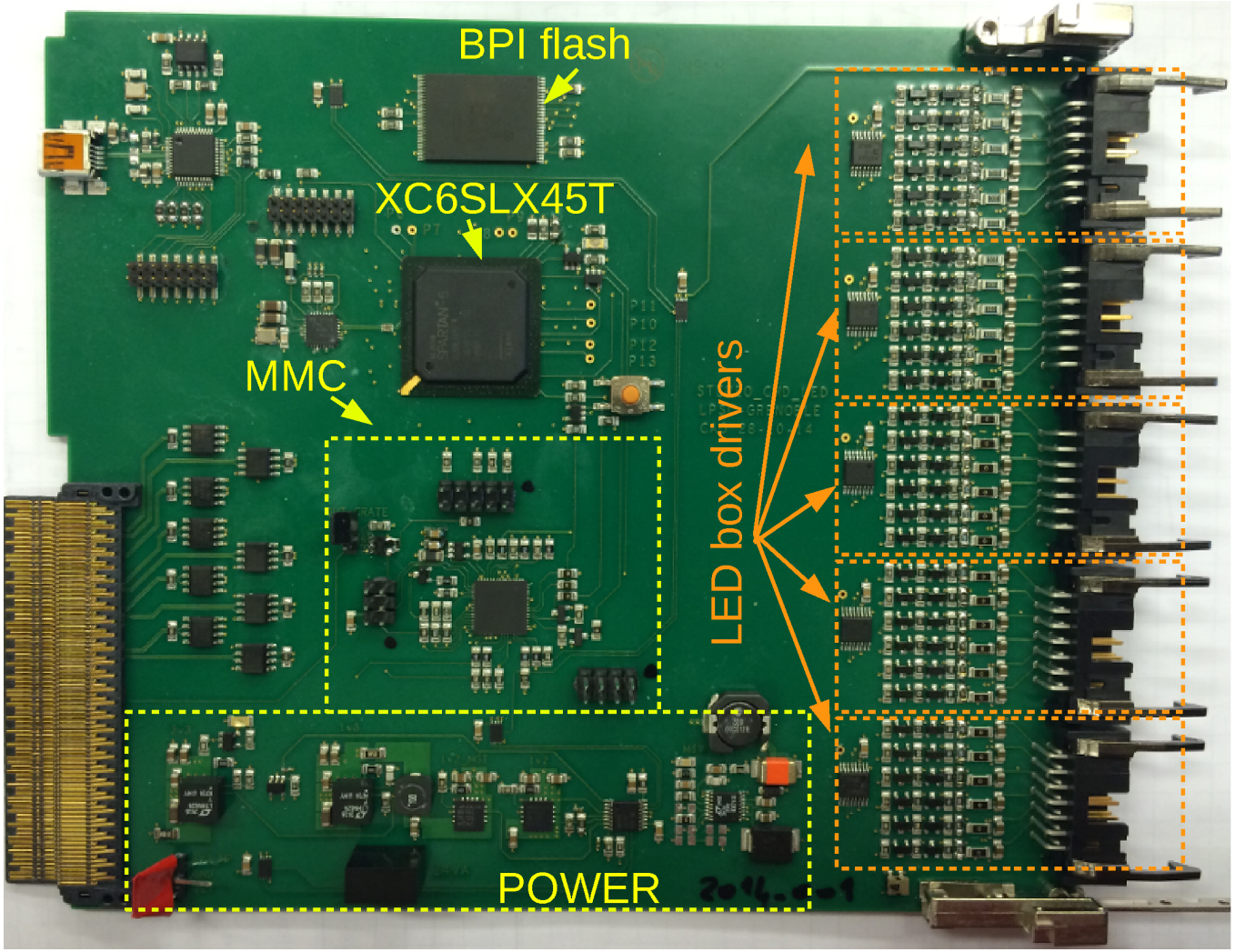
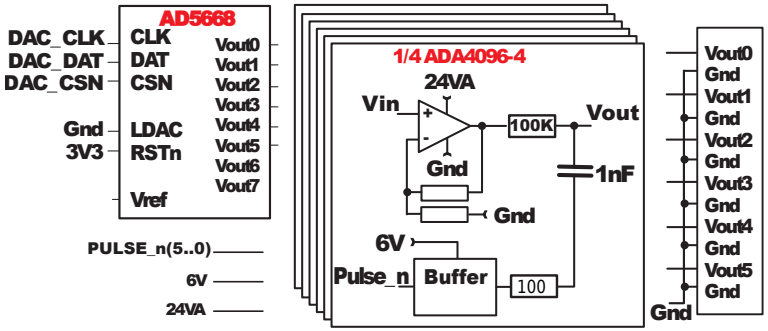
LED board hardware



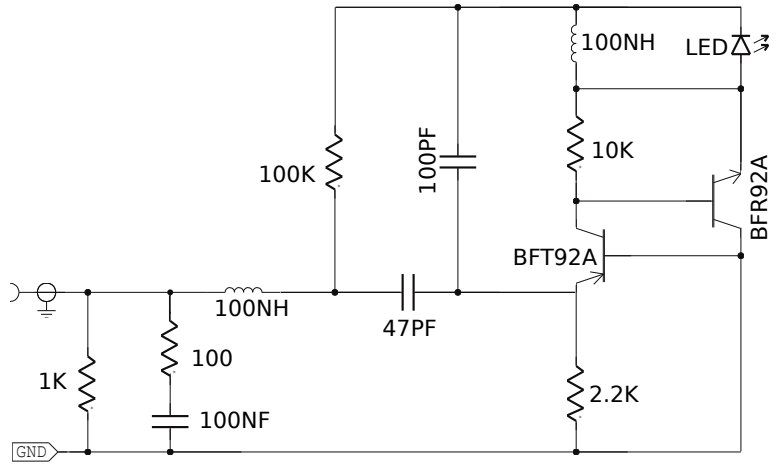
- Slow control by IPBus (for LED voltage level and BPI programming)
- LED pattern and timing are selected and driven by the trigger board.

LED box driver and led box

$\frac{1}{5}$ LED_box_driver from LED_board



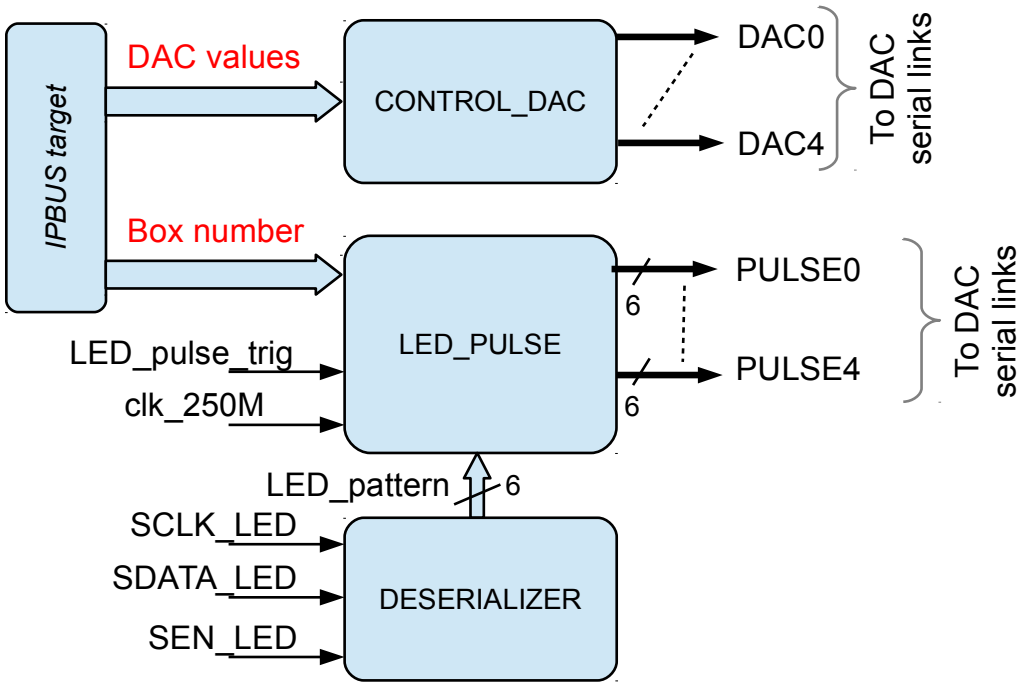
$\frac{1}{6}$ LED_driver from LED_box



Courtesy from G. Bosson

- Each LED box contains 6 LED and a discrete LED driver.
- LED light driver supplied and driven via a single coax cable:
  1. LED light level set by mean voltage (DAC setting via IPBus)
  2. Square pulse $> 2\,V$ fires the LED (generated by FPGA)

LED board firmware



1. Use IPBus to configure DAC and select the LED boxes to drive.
2. Serial data frame is used to set the required pattern (for instance incremental pattern).
3. After each serial frame, a led pulse trigger is sent by the trigger board to activate the LED pattern.

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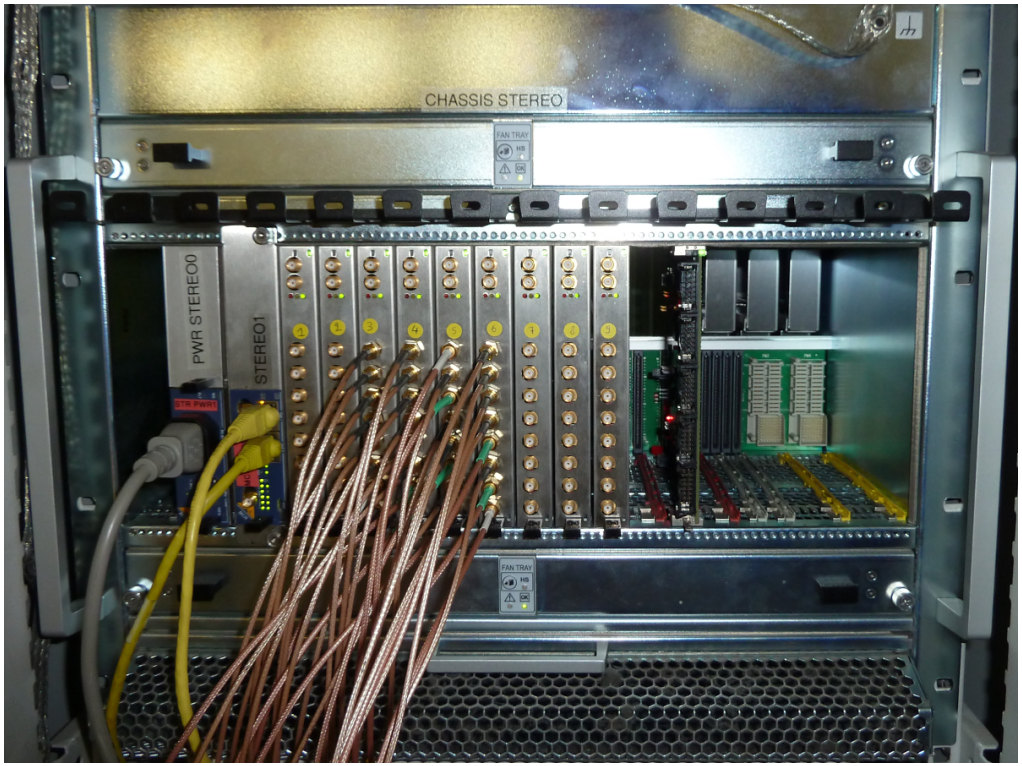
Summary



- FE8, LED_board and TRB validated on prototype experiment.
- Spare boards available: 2 FE8, 1 LED_board, 1 TRB
- Firmwares can be remotely updated, evolutions are possible, just ask.
- More details can be found in arXiv:1510.08238