Journées VLSI - FPGA - PCB et Outils CAO de l'IN2P3

Réalisation des complex gates du pixel du projet Alpide pour ALICE ITS

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Outline

- ALICE ITS Upgrade
- ALPIDE Description
- ALPIDE pixel logic
- Full custom digital circuit design
- Construction of CMOS complex gates
- Realization example - MEB
- Timing model extraction
- Conclusions

# ALICE ITS Upgrade

I. Introduction
- ALICE ITS upgrade project

The ALICE ITS will be replaced with an entirely new detector during LS2 (2019)

New Layout for improved resolution

- 7 layers, 12.5 Gpixels in ~ 10 m^2
- Inner layer radius 22 mm
- X/X_0 0.3 % (innermost layers)
- Spatial resolution ~ 5 μm
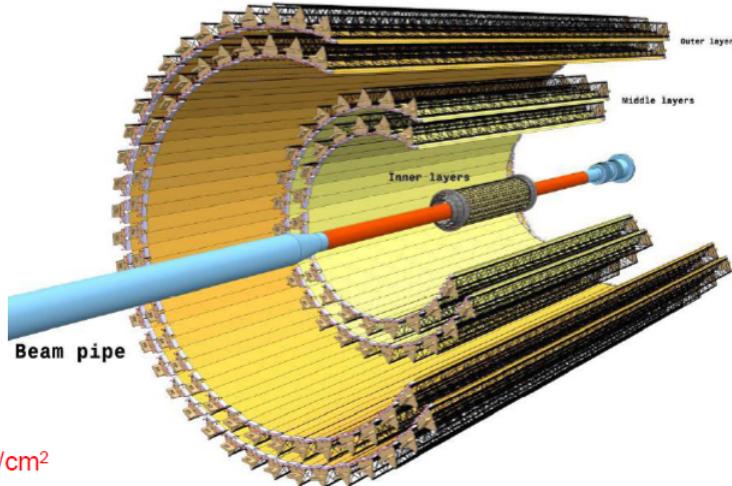
Requirements

- Chip: 15 mm x 30 mm x 50 μm
- Pixel size: O(30x30) $μm^2$
- Power density   < 100 mW/cm^2
- Integration time   < 30 μs
- Required radiation tolerance : TID 2.7 Mrad & NIEL $1.7 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2

Thin sensors, high granularity, large area, moderate radiation

→ Monolithic silicon pixel sensors

See L. Musa Thursday h.14 plenary talk

Daehyeok Kim – TWEPP 2015

ALPIDE Description
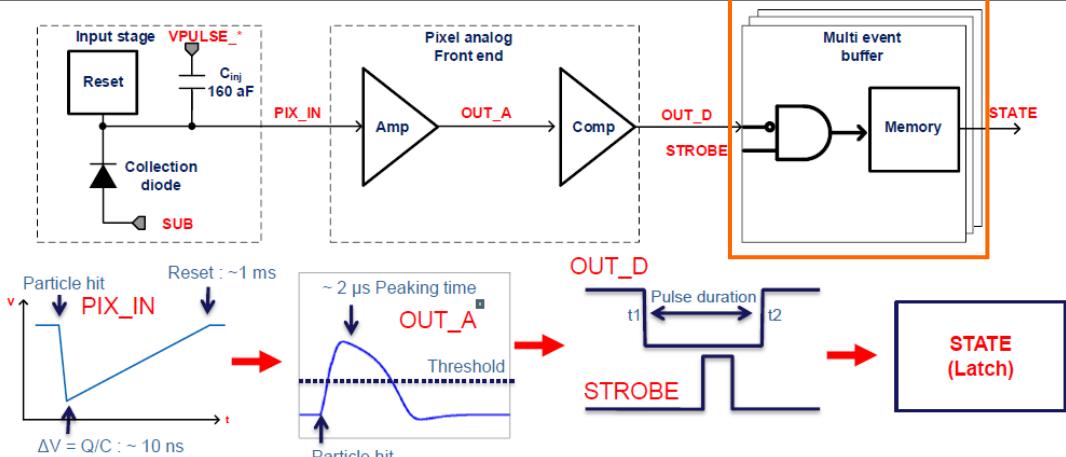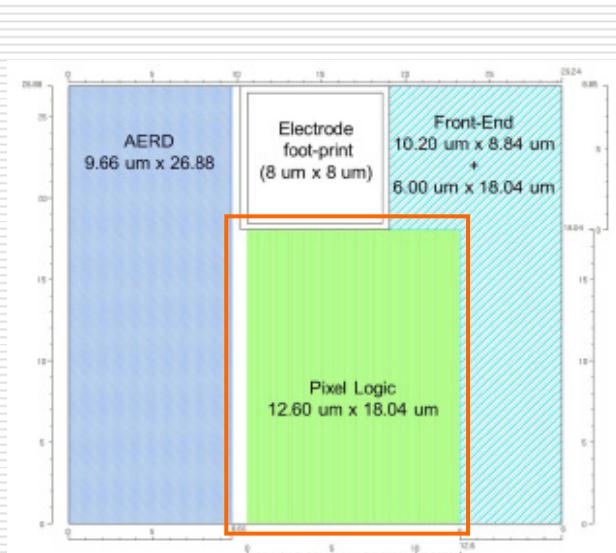
Daehyeok Kim – TWEPP 2015

ALPIDE Pixel logic
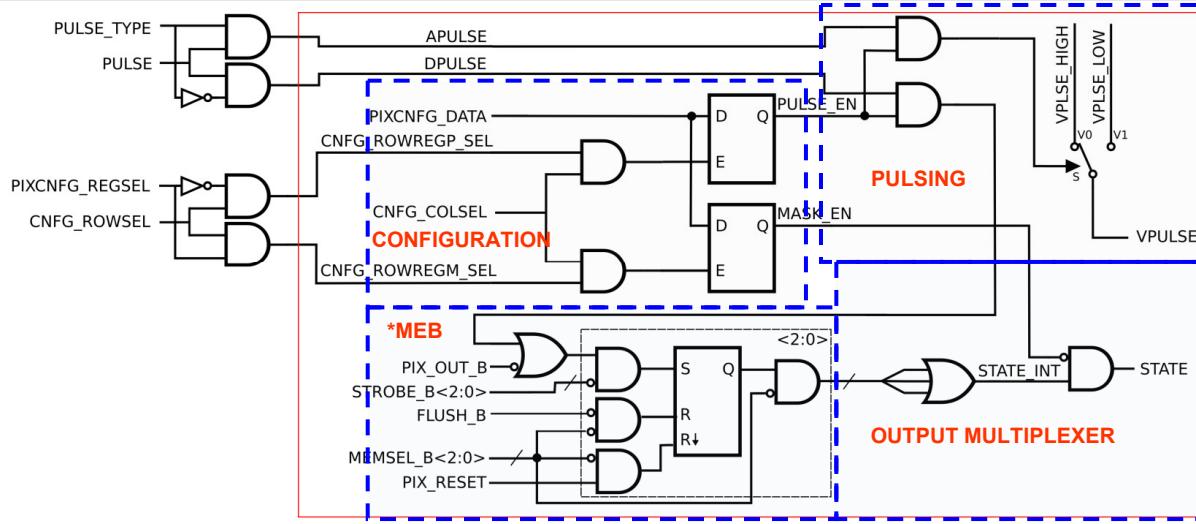
Pixel logic implementation constraints:

- Space limited by sensing node and pixel dimension

- 3 metal layers for routing (M4 is reserved for power routing)

- Integration to digital flow verification

→ **Full custom complex gate design to minimize the surface**

→ **Optimizing the dimension, element placements, signal path and modelisation**

→ **Timing model generation and verification**
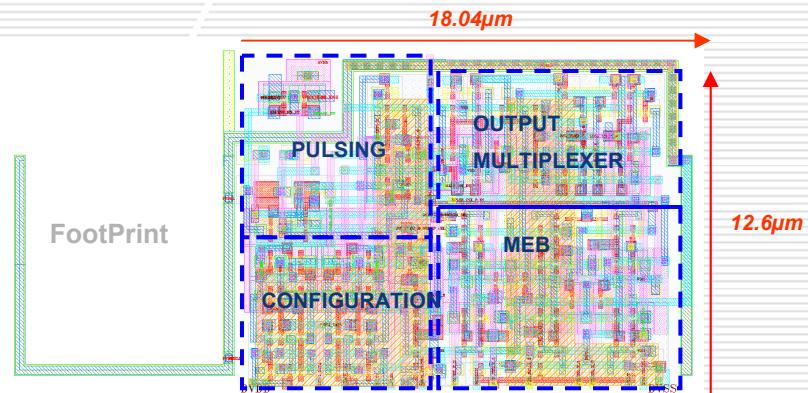
*MEB: Multi Event Buffer

Full custom digital design (1/2)

- ☐ Full custom digital are useful for designing small/repetitive logics that require optimization in: dimension, time, radiation hardening …
- ☐ Advantages:
  - ■ More compact
  - ■ Can use non standard logic such as: transmission gate, dynamic logic, radiation hardening …
- ☐ Disadvantages:
  - ■ More development time.
  - ■ Specific design and difficult to re-adapt to other circuit
 - ■ Difficult to integrate into standard digital verification flow

Full custom digital design (2/2)

- ☐ Sub-divide the circuit by group of function
- ☐ Develop the complex gates corresponding to the function
  - ■ Transistors level development: construction of NMOS and the complementary PMOS network
  - ■ Reduction of common input transistors if possible
  - ■ Simulation with arbitrary input to guaranty the original function
- ☐ Implementation of complex gates and circuit assembly:
  - ■ Define input/output pins orientation, metal layer and placement
  - ■ Optimizing transistor placement using Euler path & iteration
- ☐ Timing model extraction:
  - ■ Extraction of verilog description & timing model using Liberate tool
  - ■ Validate timing model by comparing with analog simulation

Construction of CMOS Complex Gate (1/2)

- ☐ Static CMOS logic are constructed based on serial (AND logic) & parallel (OR logic) transistors network
- ☐ The NMOS & PMOS network are complementary
- ☐ The output function is inverted from NMOS network

NOR GATE   NAND GATE
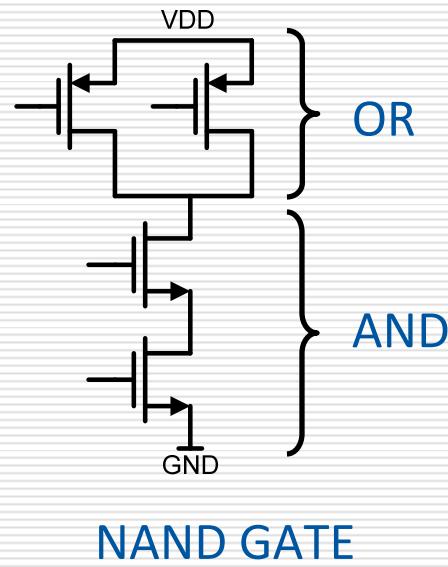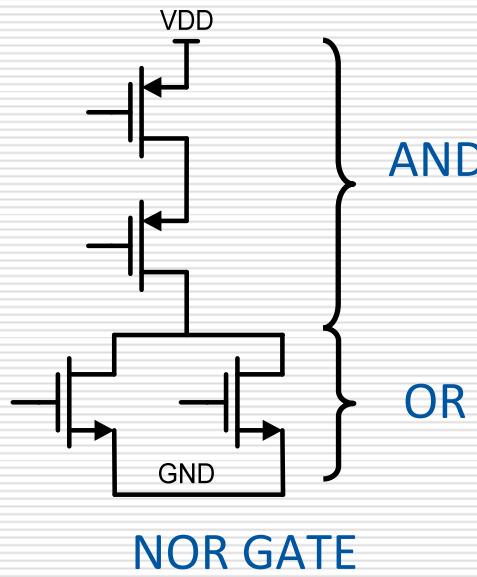
Construction of CMOS Complex Gate (2/2)

❶   Construction of NMOS network from derived function which includes only AND & OR logic

       -> The result will invert this function

❷   Derive PMOS network from the complementary of NMOS network

❸   Combine NMOS & PMOS network to form the output function

E.G : 2 ways to contruct the following function : $\quad F = A \bullet B + C \bullet D$

$$F \xrightarrow{\text{N/P network}} \overline{F} = \overline{A \bullet B + C \bullet D} \xrightarrow{\text{Invert } \overline{F}} \overline{\overline{F}} = F$$

$$F \xrightarrow{\text{Develop } \overline{F}} \overline{F} = \overline{A \bullet B + C \bullet D} = (\overline{A} + \overline{B}) \bullet (\overline{C} + \overline{D}) \xrightarrow{\text{N/P network}} \overline{\overline{F}} = F$$

Realization example (MEB) (1/4)
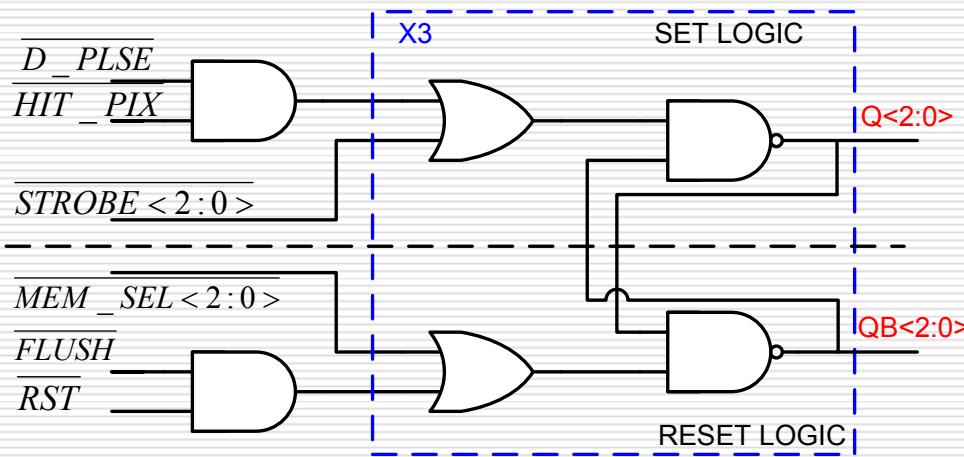

□ <u>MEB</u> : **M**ulti **E**vent **B**uffer

- 3 RS latches with control logics
- Receive HIT information from analog front-end (HIT_PIX) or calibration pulse from PULSING block (DPLSE)
- Receive CLEAR information from Priority Encoder (RST) and periphery (FLUSH)
- The STROBE<2:0> and MEMSEL<2:0> from periphery allow to select whether the corresponding registers is set or reset

Realization example (MEB) (2/4)

$$Q <i> = \overline{\overline{(\overline{D\_PLSE} \bullet \overline{HIT\_PIX} + \overline{STROBE <i>}) \bullet QB <i>}}$$

❶ Construction of NMOS network from the function that contain only AND & OR logic
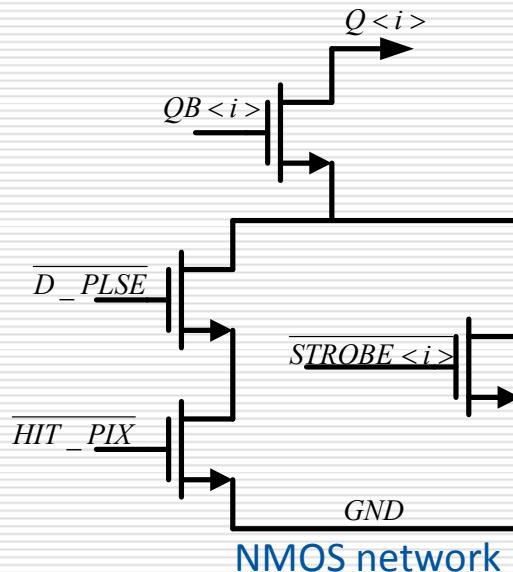
❷ Complementary PMOS network is deducted from NMOS network

$$F = \overline{(\overline{D\_PLSE} \bullet \overline{HIT\_PIX} + \overline{STROBE <i>}) \bullet QB <i>}$$

NMOS network

PMOS network
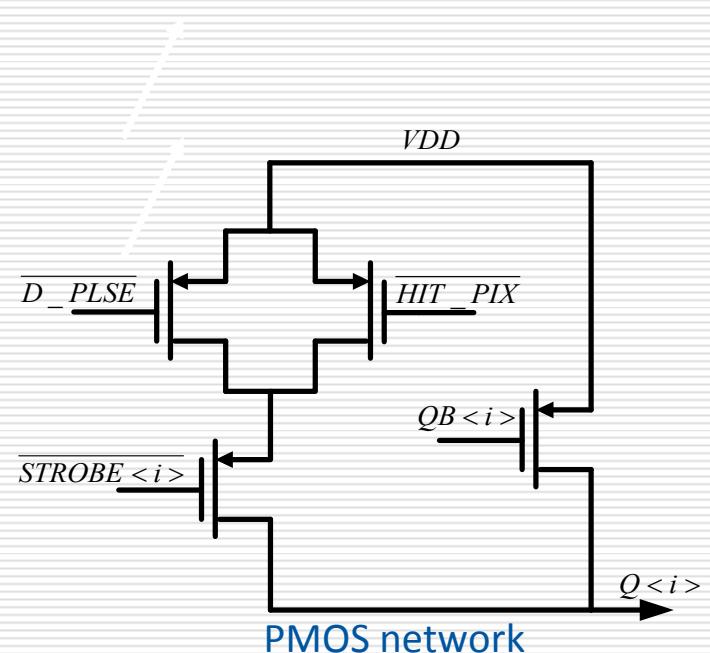
$$\Rightarrow Q <i> = \overline{F} = \overline{(\overline{D\_PLSE} \bullet \overline{HIT\_PIX} + \overline{STROBE <i>}) \bullet QB <i>}$$

Realization example (MEB) (3/4)

❸ Transistor reduction

Common input of 3 Memories
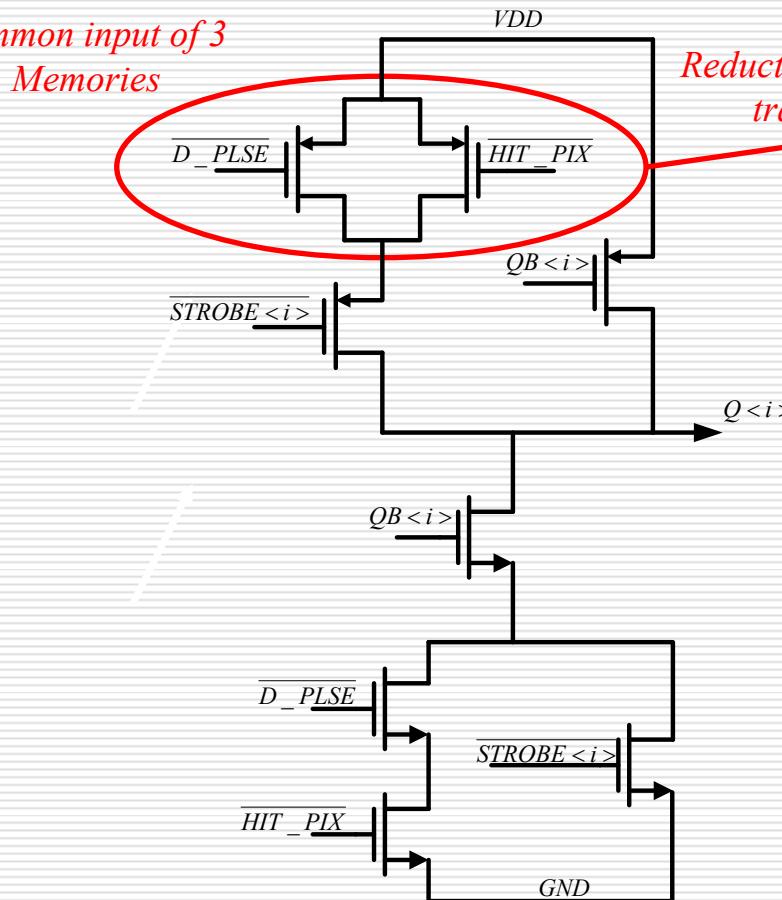
Reduction of 4 transistors

Journée VLSI-FPGA-PCB et outils
CAO de l'IN2P3
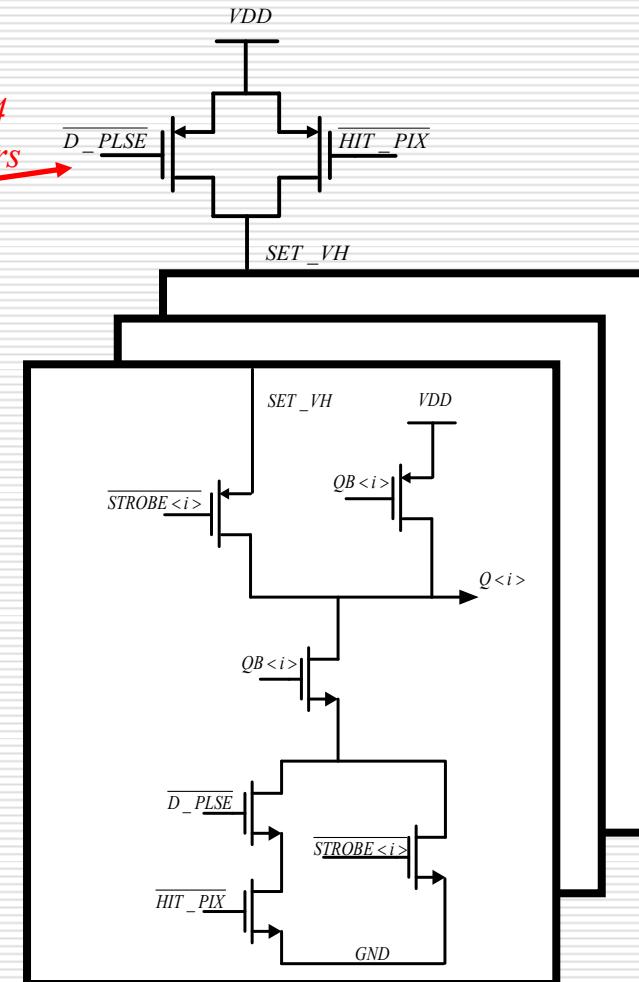
Realization example (MEB) (4/4)

7.6μm

9.3μm
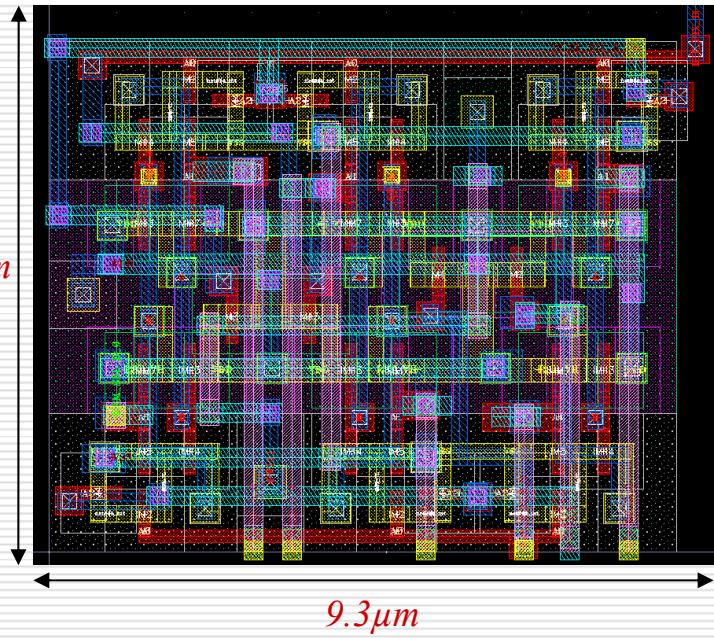
|	Complex gates	Standard cells
Transistor number (NMOS/PMOS)	24/16 (40 trans)	36/36 (72 trans)
Surface (μm²)	71	180

Timing model extraction (1/2)

- ☐   Tools: Cadence Liberate
- ☐   Input files:
  - ■ Extracted netlists
  - ■ Foundry device model
  - ■ Liberate command file in Tcl format (cell definition, template definition, leakage definition …)
- ☐   Output files:
  - ■ Verilog file (.v)
  - ■ Synopsys Lib file (.lib)
  - ■ Data sheet (.pdf, .html …)
  - ■ Database for post processing (.ldb)

Ref: Characterization of digital cells – Xavier Llopart (CERN)
http://www.in2p3.fr/actions/formation/microelectronique15/LibCharctSeminar_short.pdf

Timing model extraction(2/2)
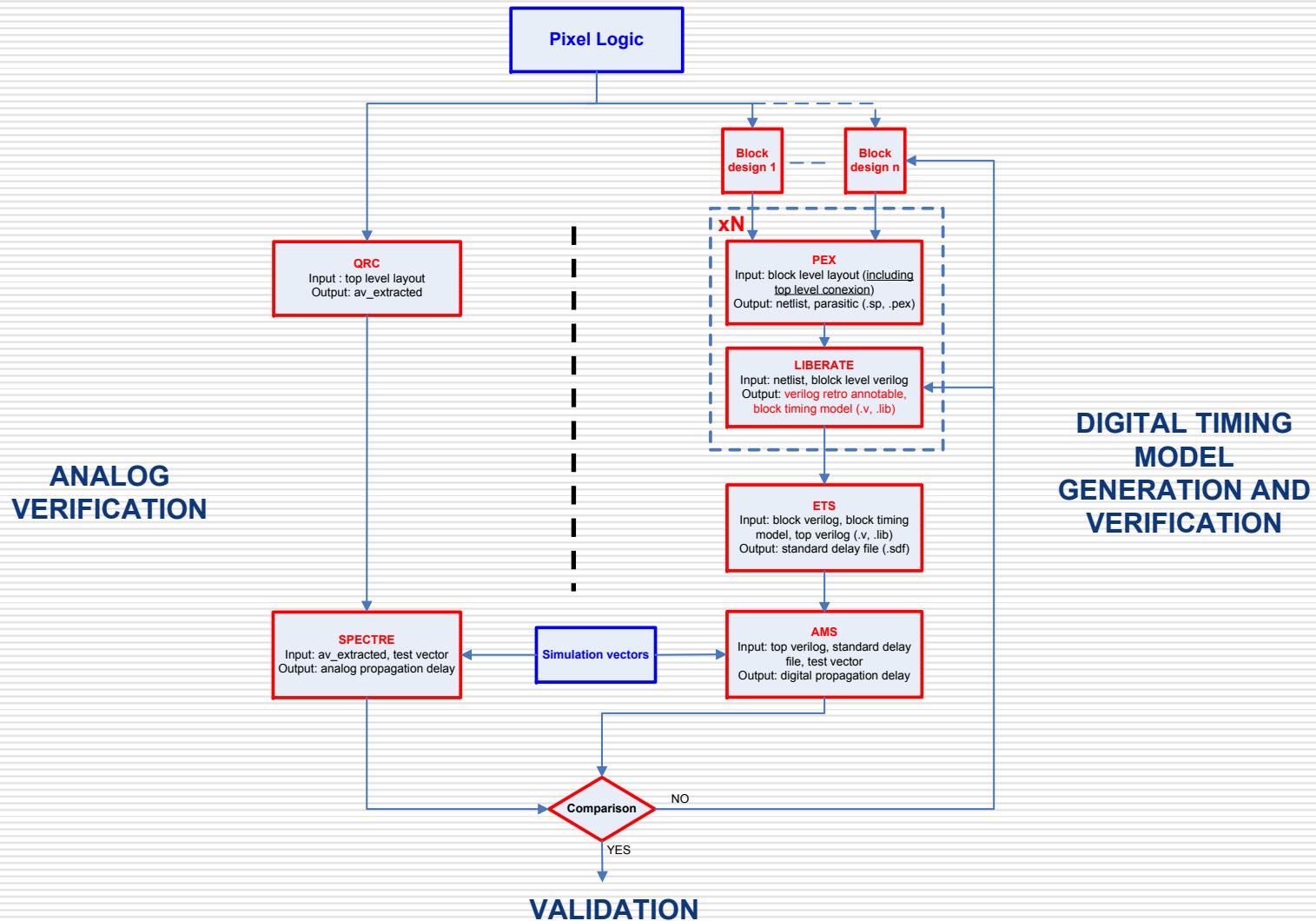
Conclusions

- ☐ A compact in-pixel logic based on complex gates has been realized for ALPIDE chip allows to host different logic functions (108 transistors) in a limited surface ~230µ²

- ☐ Full custom digital is practical for small logic that requires particular optimization

- ☐ The construction of complex gate allows to optimize the number of transistor and circuit dimension.

- ☐ Cadence liberate tool allows to generate standard timing model that required by digital simulation, place & routing tools