CALICE-France: a snapshot

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JCL'2016
Chimie PariTech
24/03/2016

Synoptic: recent activities

VFE Readout

- Omega ROC's

SiW-ECAL's

- Prototype Building & plans for BT
- Long SLAB's
- R&D
  - COB ↔ Korea
  - (Wafers design)
- Thermo-Mechanical studies
- Outreach: CMS-HGCAL & ATLAS-HGTD

Micro-Megas for Calorimeters R&D

RPC-SDHCAL

- BT program
- Analysis & first results: (Energy weighting)
- HR3 & Large Surface implementation
- Gas system

(Simulations: DD4HEP)

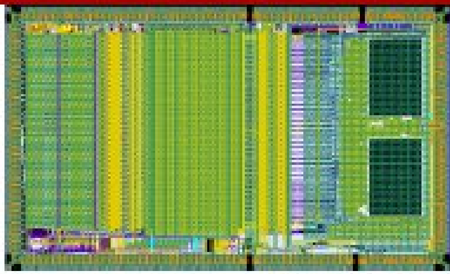
DAQ

- 'Common DAQ'
- PYRAME/CALICOES
- Data Quality: DQM4HEP

What next ?

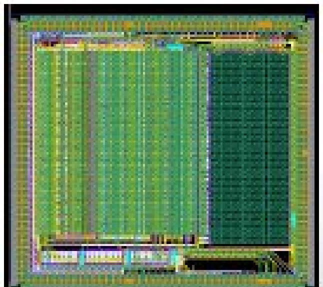
Readout ASIC

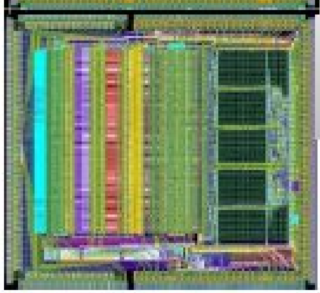
ROC chips for ILC prototypes



SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
June 07, June 08, March 10, Sept 11

ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (Eudet/Aida funded)

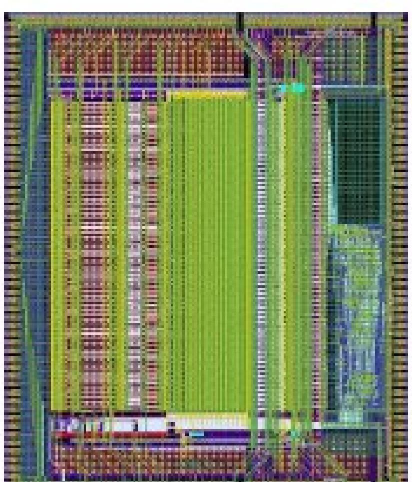


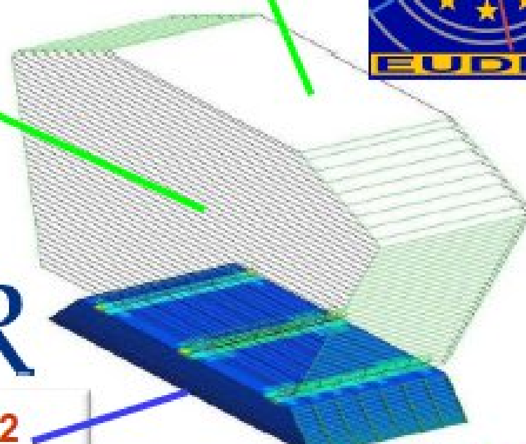


HARDROC2 and MICROROC
Semi Digital HCAL (sDHCAL)
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06, June 08, March 10

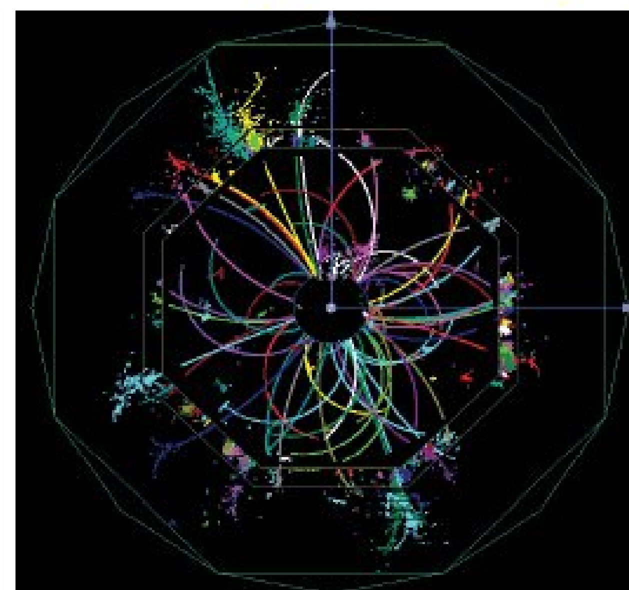
Requirements for electronics

- Large dynamic range (15 bits)
- Auto-trigger on ½ MIP
- On chip zero suppress
- **10^8 channels**
- Front-end embedded in detector
- **Ultra-low power : 25µW/ch**





SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
March 10



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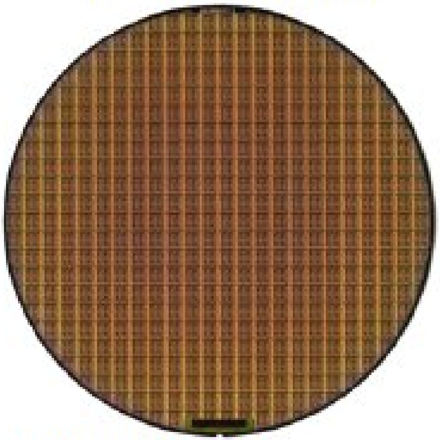
Engineering run 2016

- CITIROC1A
- CITIROC2
- DOPIROC
- GEMROC
- MAROC3A
- PHOTOROC1A
- SKIROC2A (PIN)
- SKIROC2-CMS
- SPACIROC3A
- SPIROC2E (SiPM)
- 1 other chip



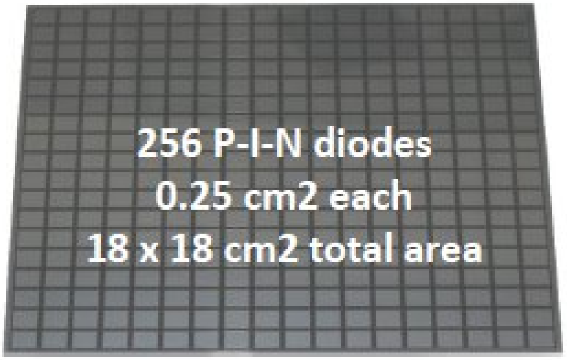
Schedule : Chips expected for middle of May 2016

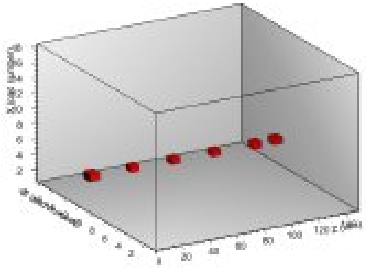
Dicing and packaging : June 2016

SKIROC2A

by S. Callier, C. de la Taille

- BUG CORRECTIONS
  - Some « Zero events » during digitization : **DONE** (added delays, cf. SP2C)
  - Substrate Shielding, Inputs Shielding : **IMPROVED** (added connections)
  - Test mode for naked dies (voltage drop off & missing pads) : **CORRECTED**
  - Trig Ext path no more thru delay cells to store the analog data : **DONE**
- IMPROVEMENTS
  - 4-bit DAC for trigger level adjustment : **OPTIMIZED**
  - Bandgap : **CHANGED** (from HR3)
  - Delay Cell : **Slightly IMPROVED**
  - AutoGain Selection : **CHANGED** (from SP2C)





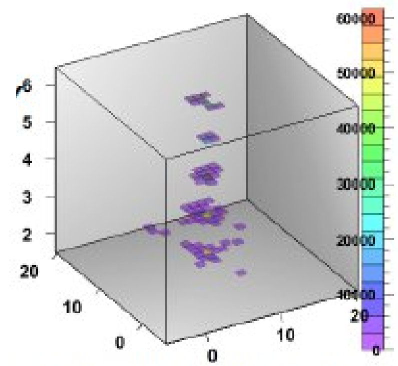
Production possible through CMS-HGCAL collaboration

SPIROC2E

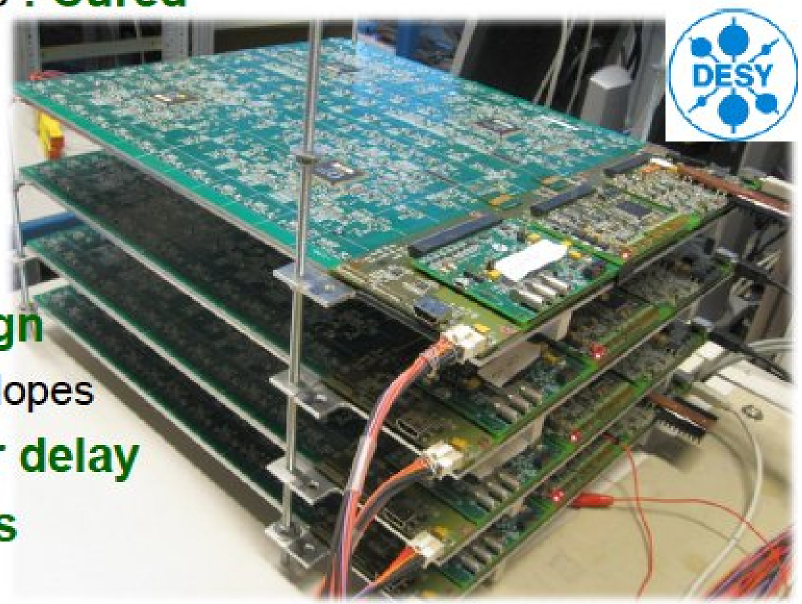
- Starting from SPIROC2D
  - - SPIROC2D included many improvements but...

- BUG CORRECTIONS
  - Fast Shaper & Threshold on discriminator : **Fixed**
  - Reset on Delay cells (column 0, 10, 14) : **Fixed**
  - Gain dependency on last channels : **Cured**
  - 5V DAC Probe Register :
    - **uses 5V pads & probes**

- IMPROVEMENTS
  - TDC : **CHANGED for a new design**
    - 1 unique current source for both slopes
  - TDC : **Delay ADDED to fit trigger delay**
  - Delay cells : **Noise Improvements**



Shower in 5 AHCAL layers (DESY testbeam)



SPIROC used by
- **AHCAL**
- **ScW-ECAL**
- **T2K**
- **...**

SiW-ECAL

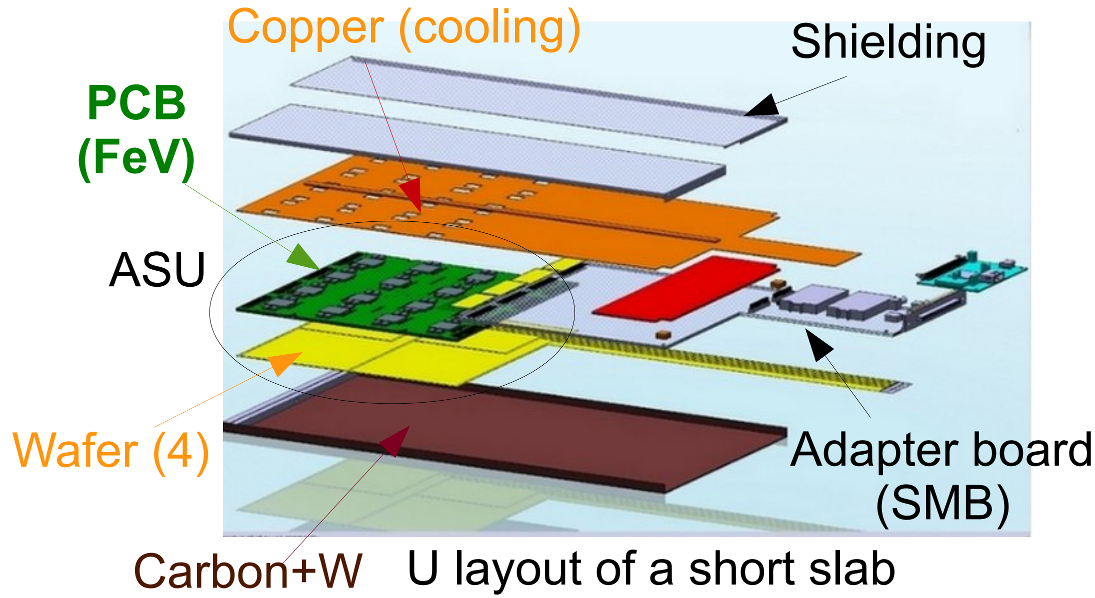
SLAB's

R&D for "mass production" and QA

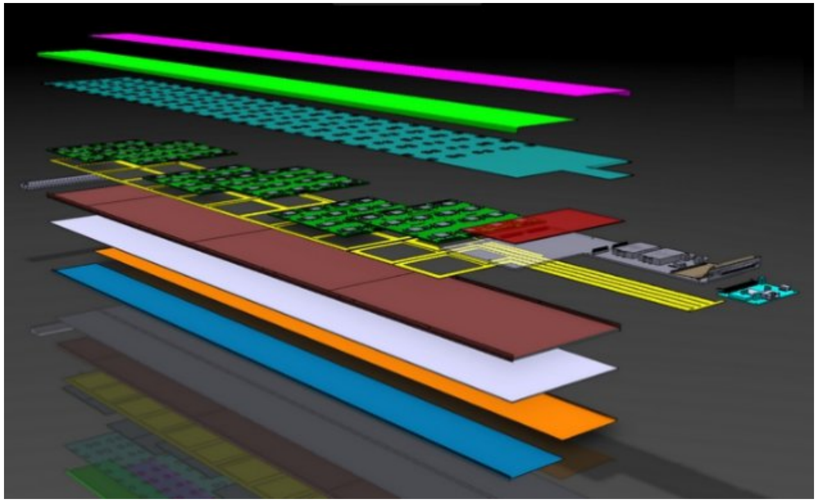
- Quality tests & preparation of large production
- Modularity → ASU & SLABs
  - Choice of square wafers (≠ from hex: SiD, CMS HGCAL)

Numbers (R_{ECAL} = 1,8 m, $|Z_{Endcaps}|$=2,35m) (likely to be reduced by 30–40%)

- **40** Barrel modules: 40 (as of today all identical)
- **24** Endcap Modules: 24 (3 types)
- **9600** Slabs = 6000 (B) + 3600 (EC)
  - many ≠ lengths
- **~75K** ASUs
  - **300K** Wafers (2500 m²)
  - **1.2M** VFE chips
  - **77M** Channels

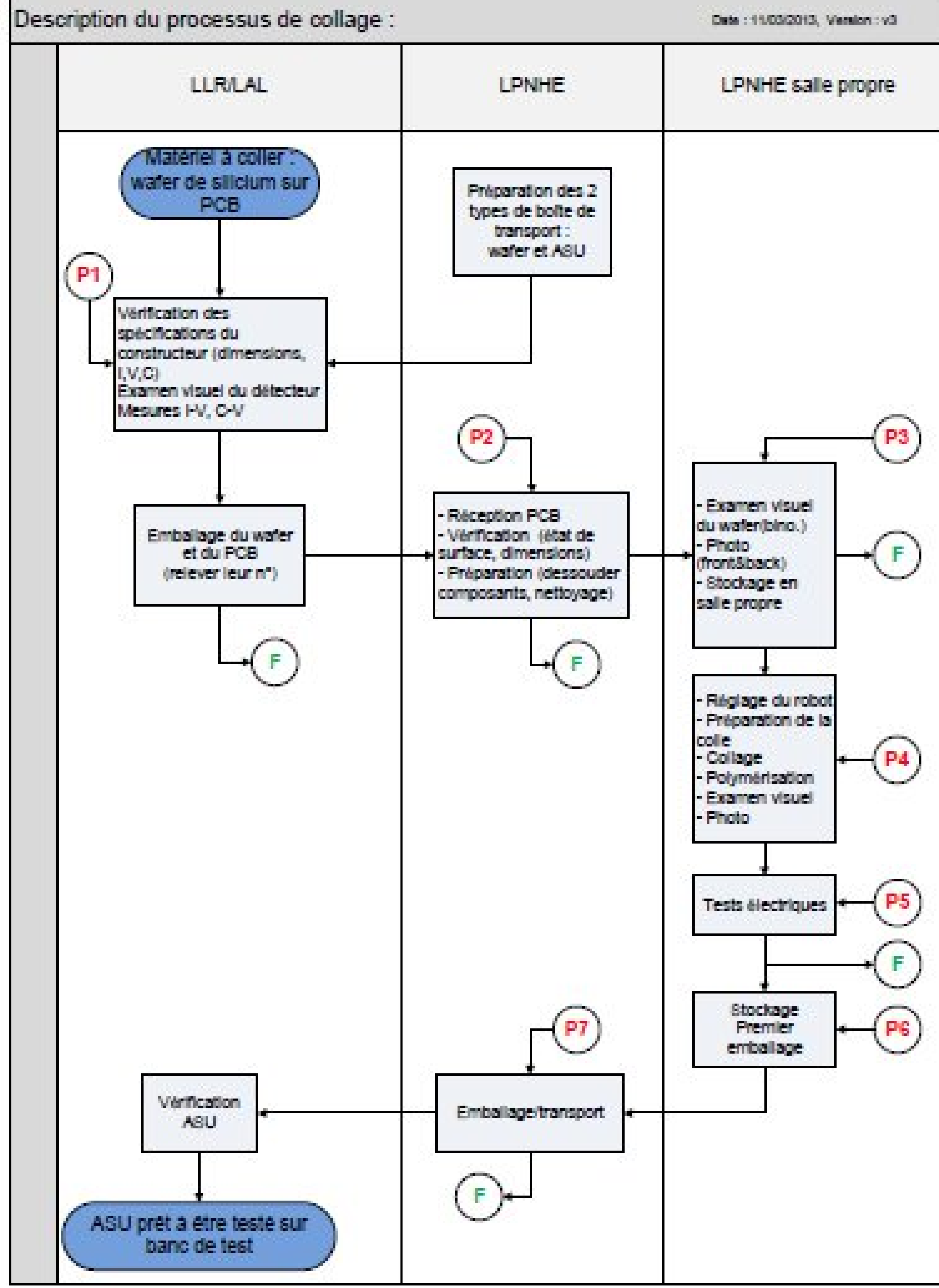


U layout of a short slab


U layout of a long slab

Quality insurance

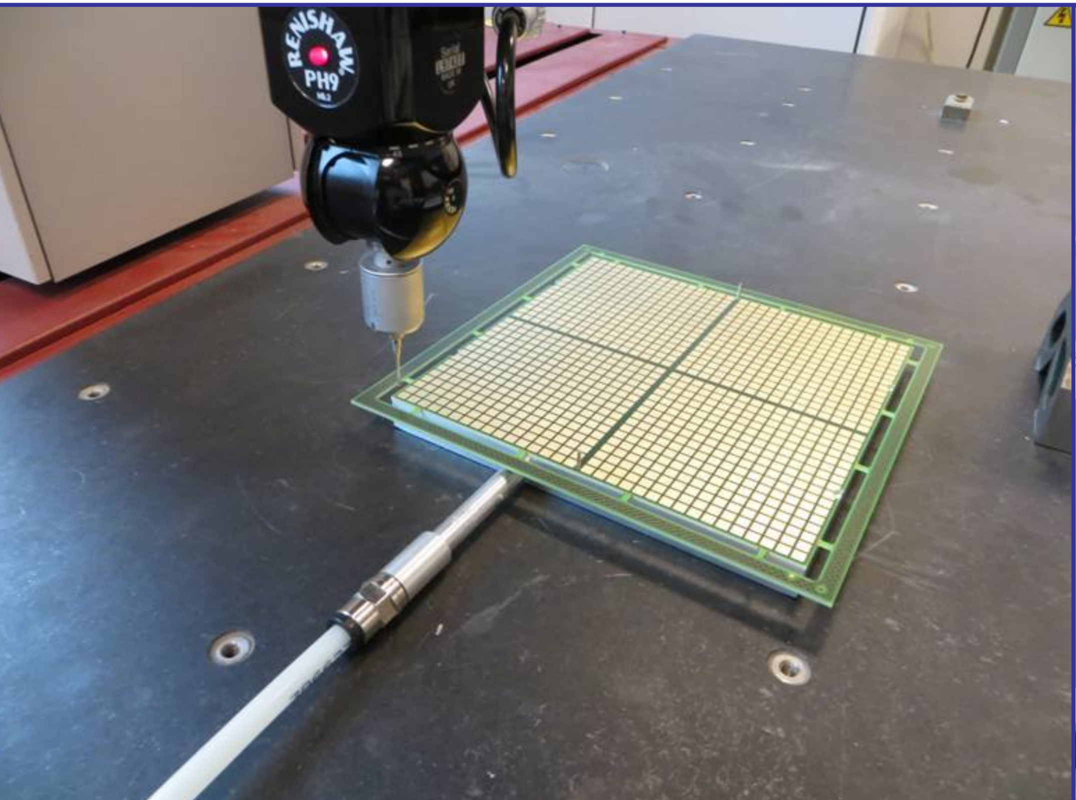
- Task flow completed
- Reception and gluing procedures for 1 and 4 silicon sensors written
- Operation on PCB monitored (follow up)
- Gluing tests registered
- ….



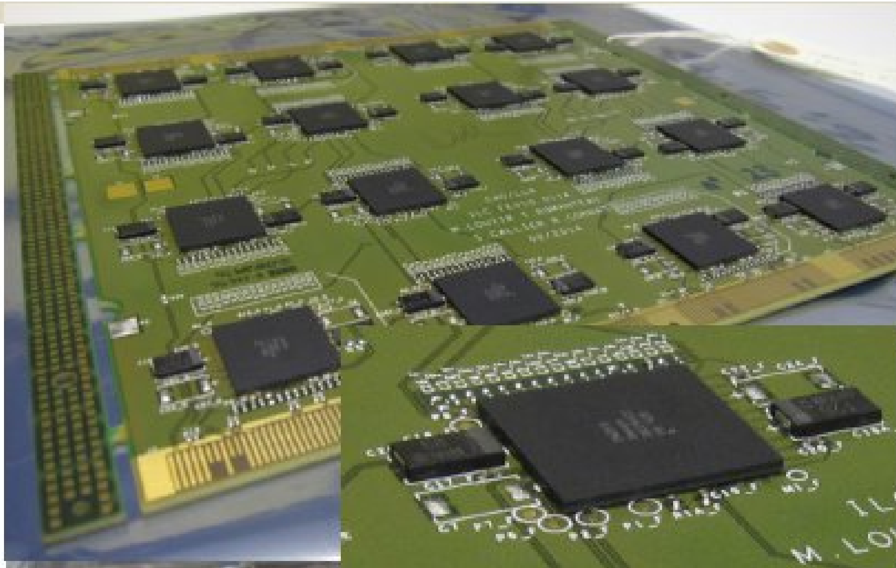
Px : Procédure à mettre en place et à documenter F : fiche de suivi du wafer

PCB Metrology

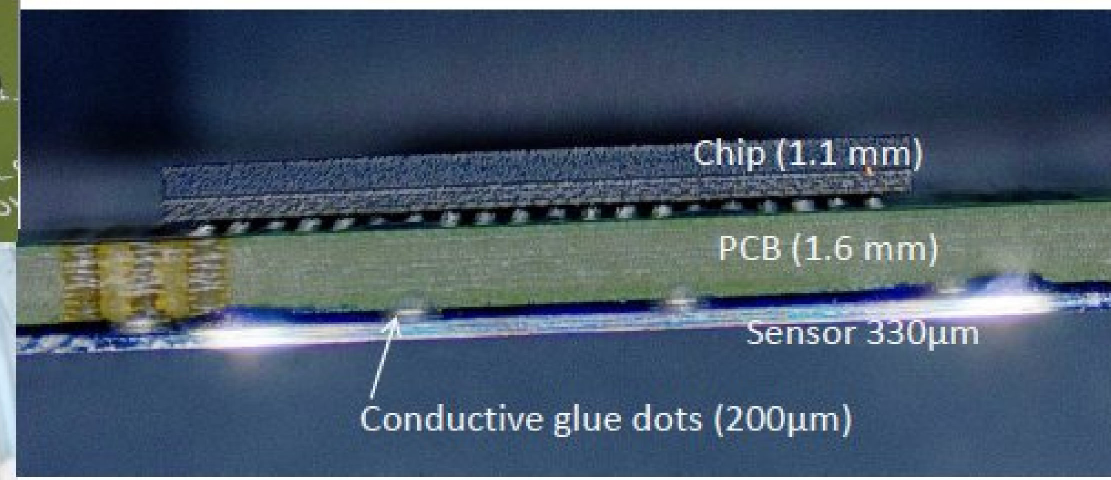
- Development of an automatic process using a coordinate measuring machine (tri-dim machine)
- Before cabling :
  - Squaring
  - Parallel edges
  - Size
  - Thickness (flatness in depression)
  - Flatness
- After cabling : flatness and thickness

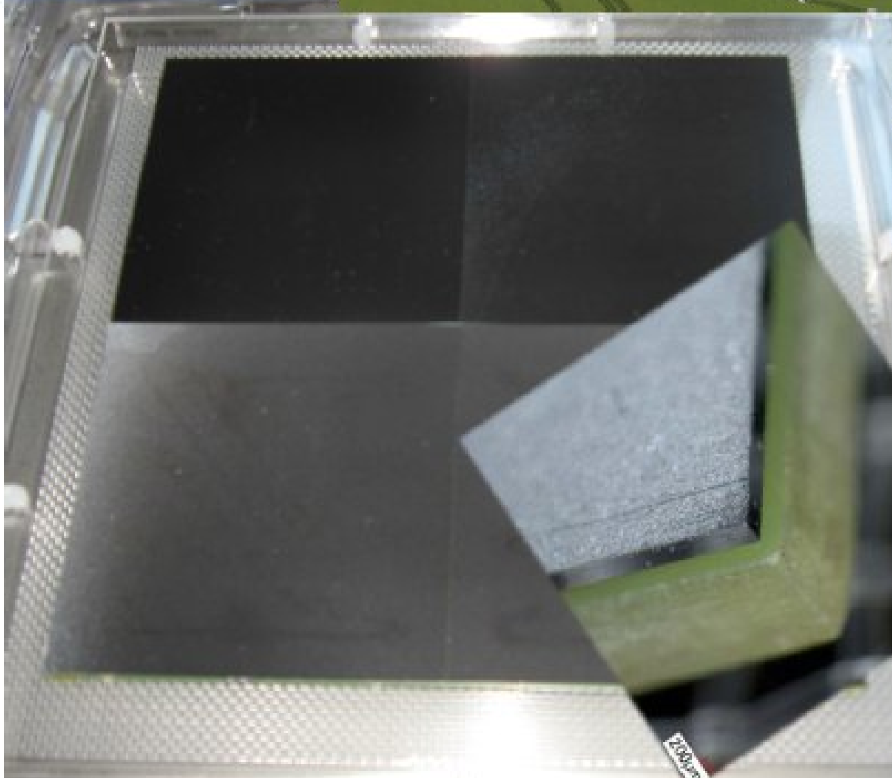


Detector module assembly



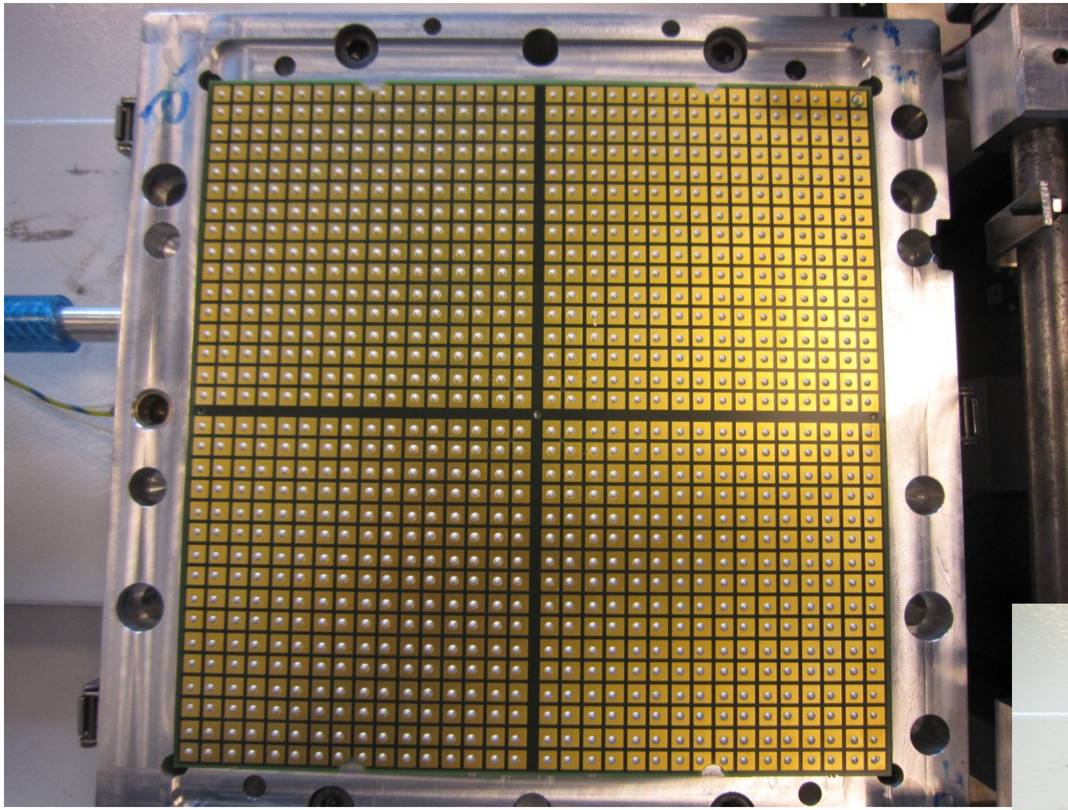
Robots for gluing sensors are developed
Manual tools for the assembly of a short slab are existing





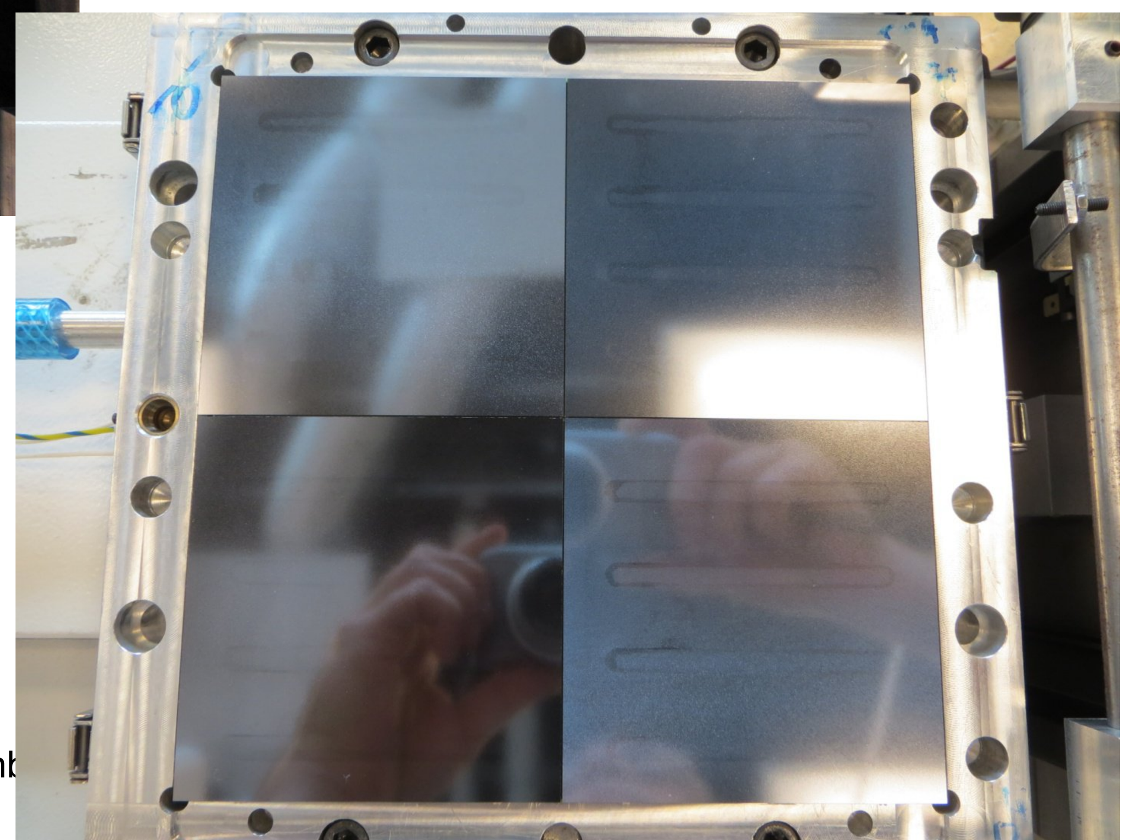
4 wafers 9cm x 9 cm wide can be glued with a 20 µm precision and reproducible process.
Glue is dispensed in order to form 200 µm thick dots

Second step : 4 wafers per PCB



- Deposit of glue on the PCB

  256 X 4 = 1024 dots

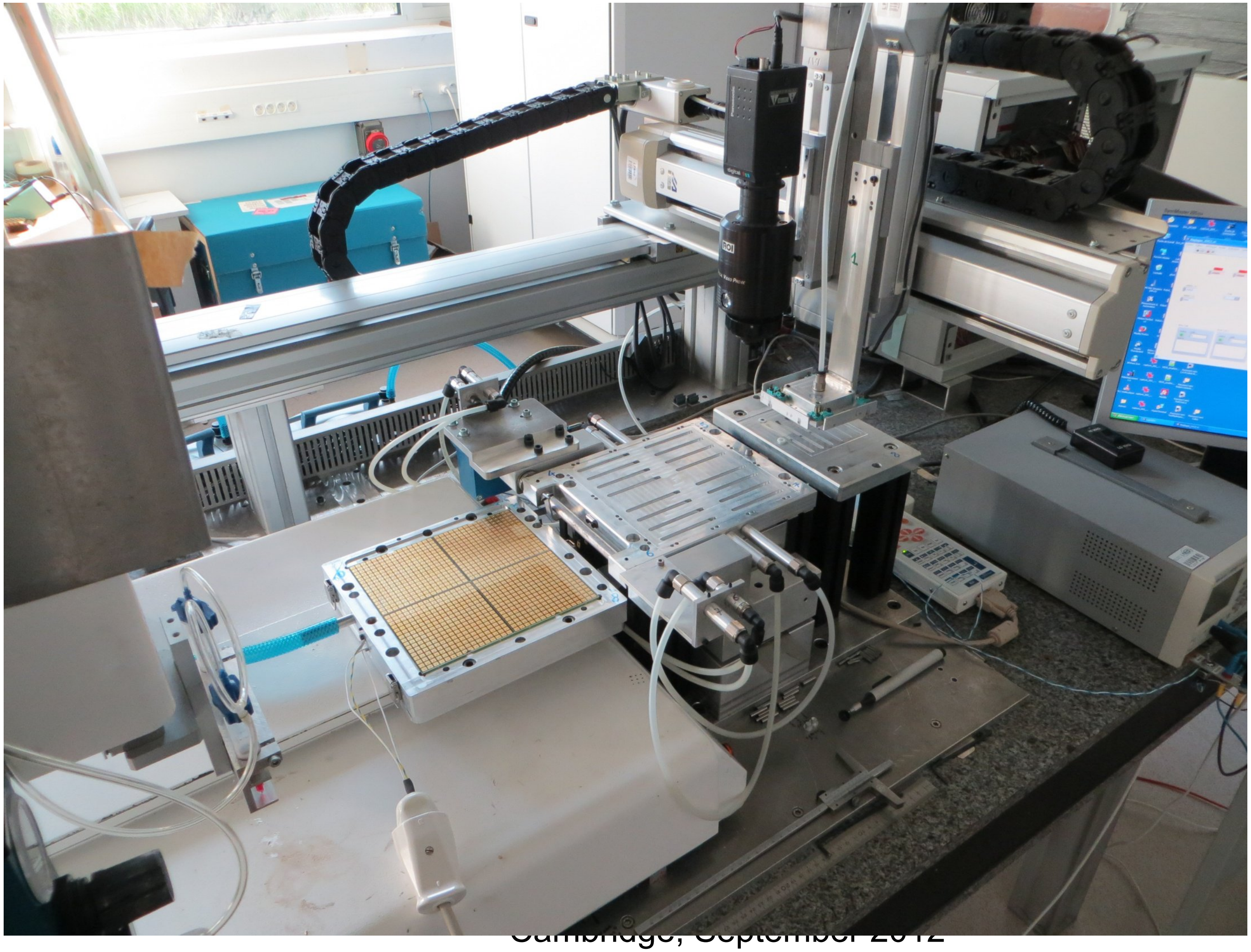


- Move the plate with the 4 wafers on the PCB

- The alignment is fundamental :
  - PCB = 180.3 mm maximum
  - Wafer = 90 mm

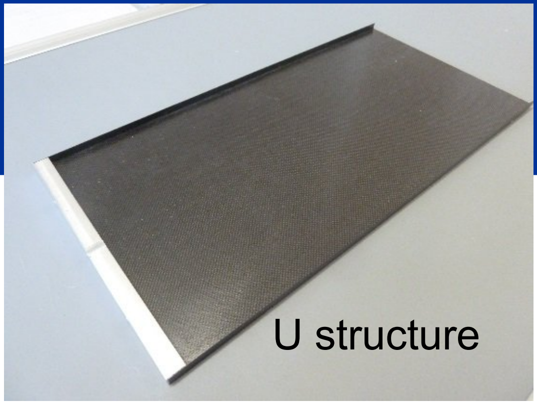
Gluing and positioning automated process

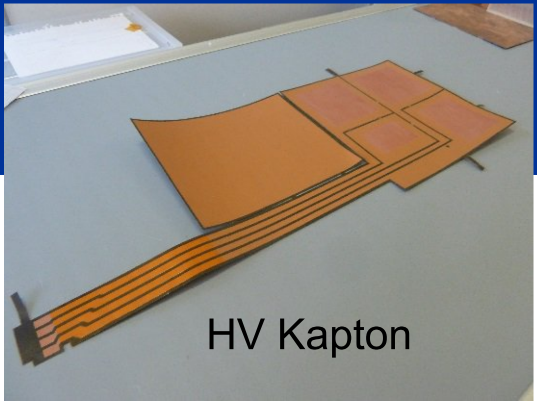
- Software (Labview) for the gluing robot has been implemented
- The second robot for positioning, alignment, and handling has been assembled and its software developed

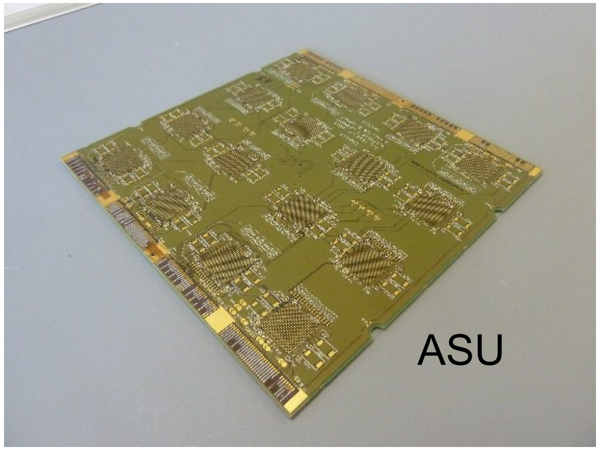


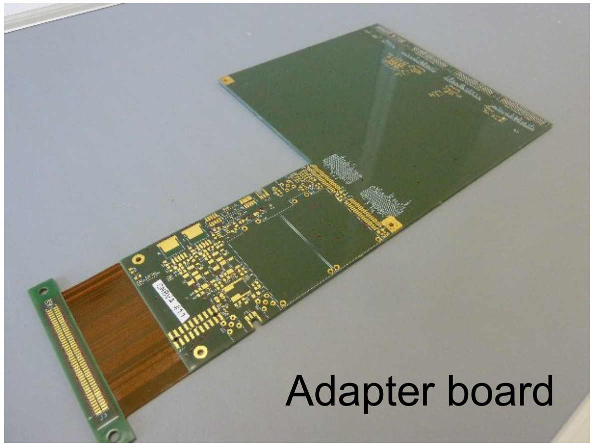
Integration
by LAL group

Integration
in 13+ steps
- **Backing for 1 night**

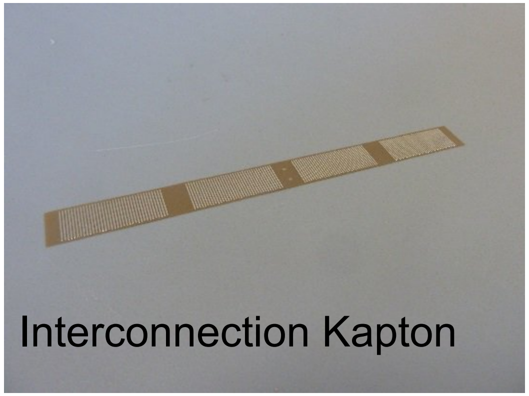


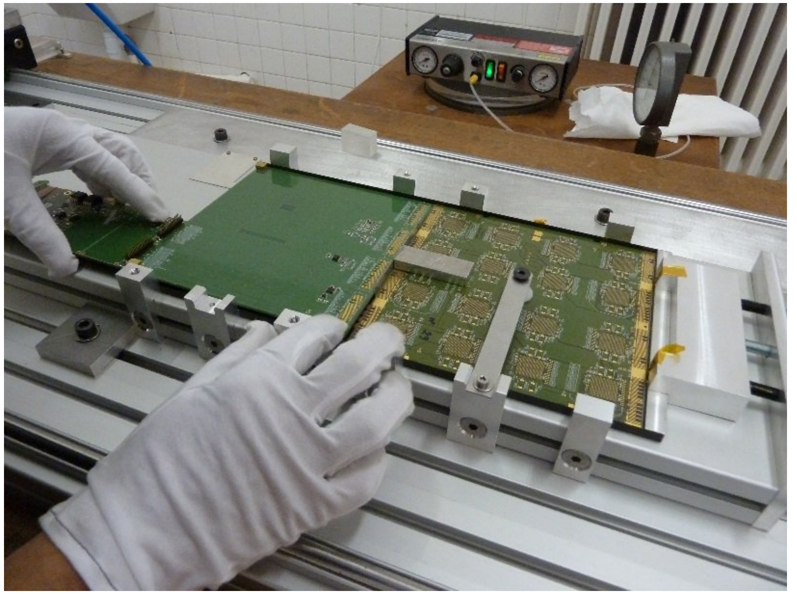




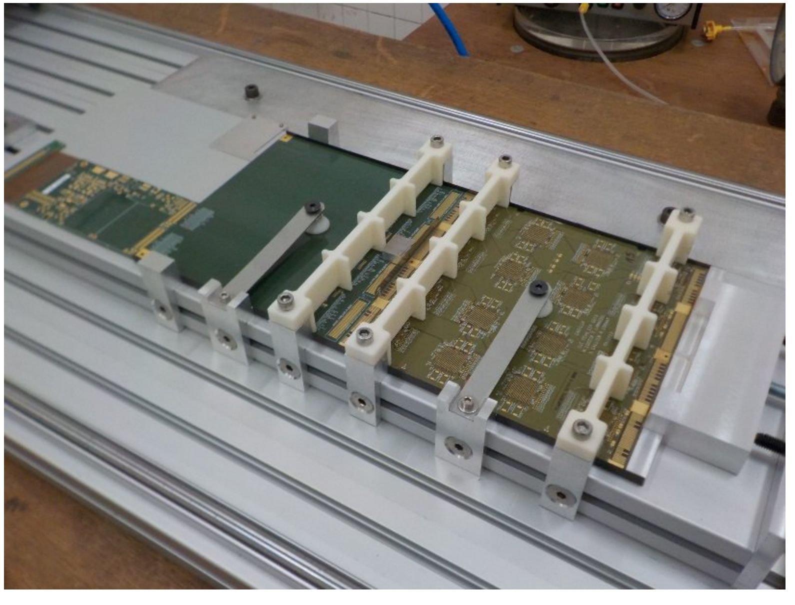


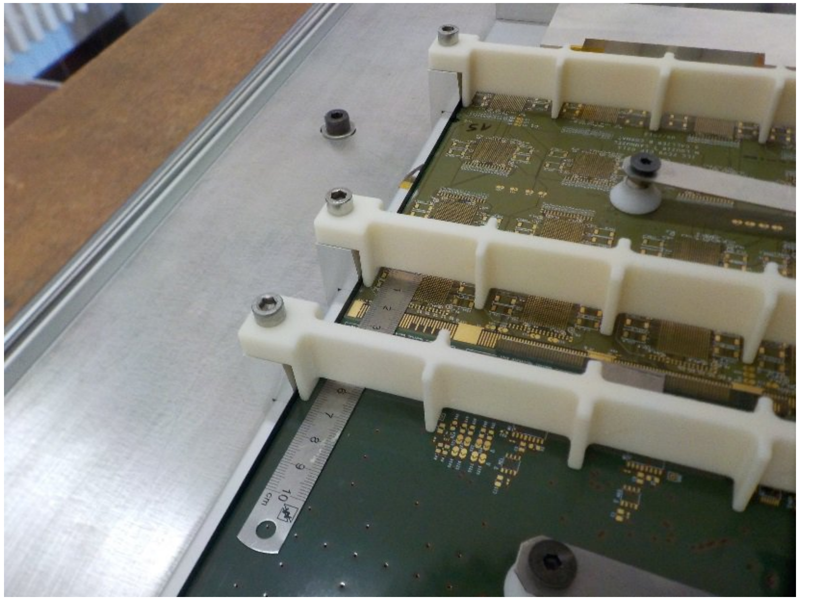
Parts



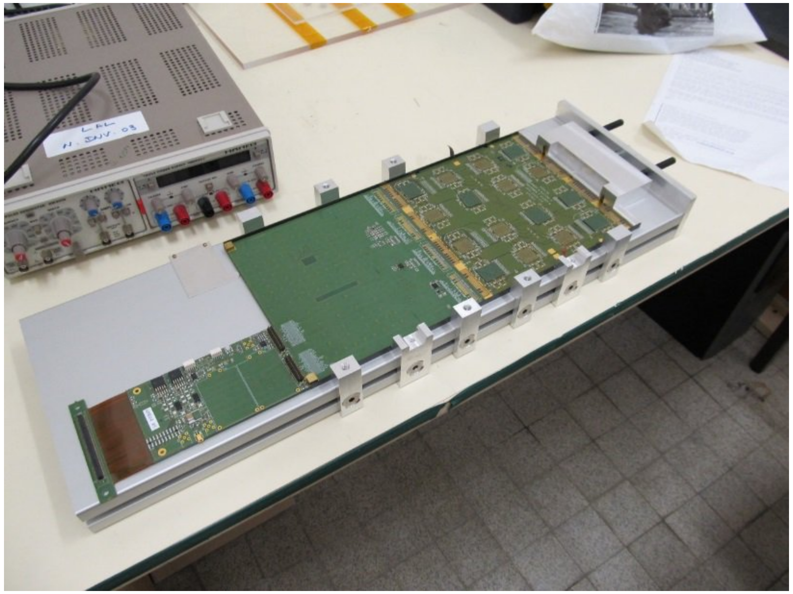


Adapter board integration

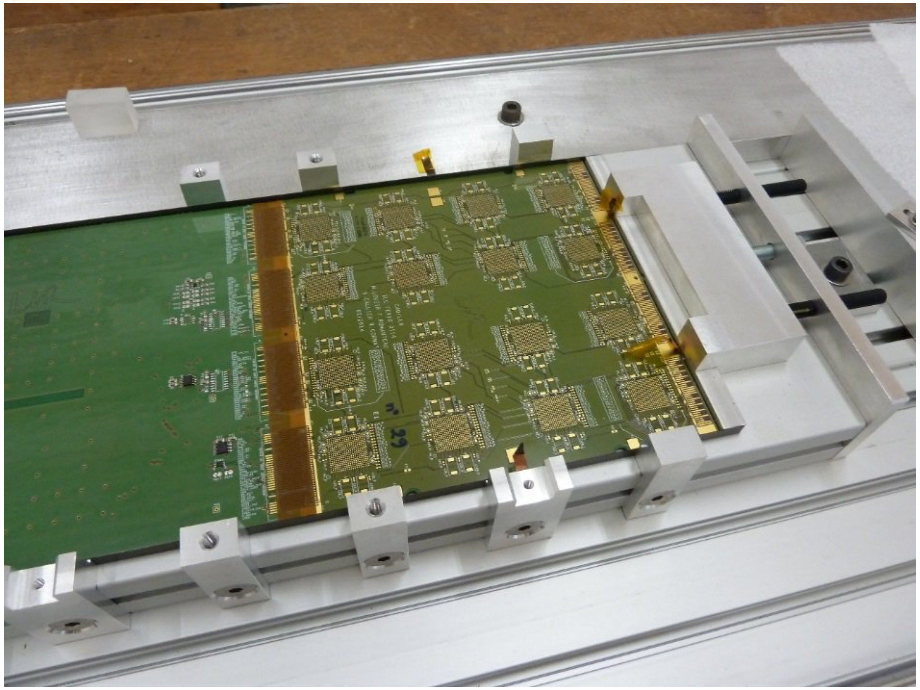




Flanges for flatness



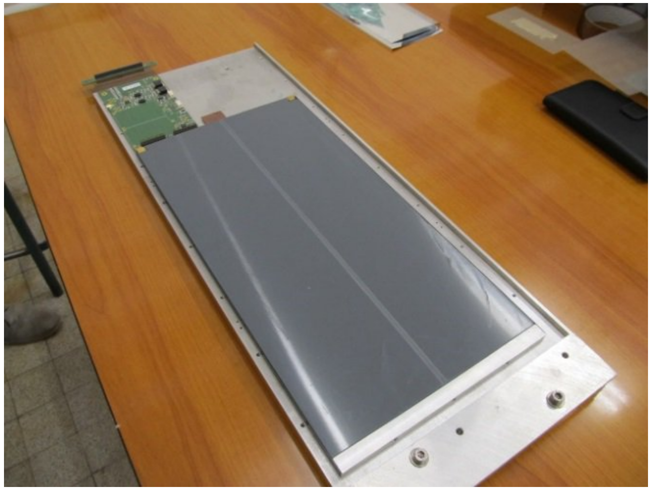
Ready for interconnection



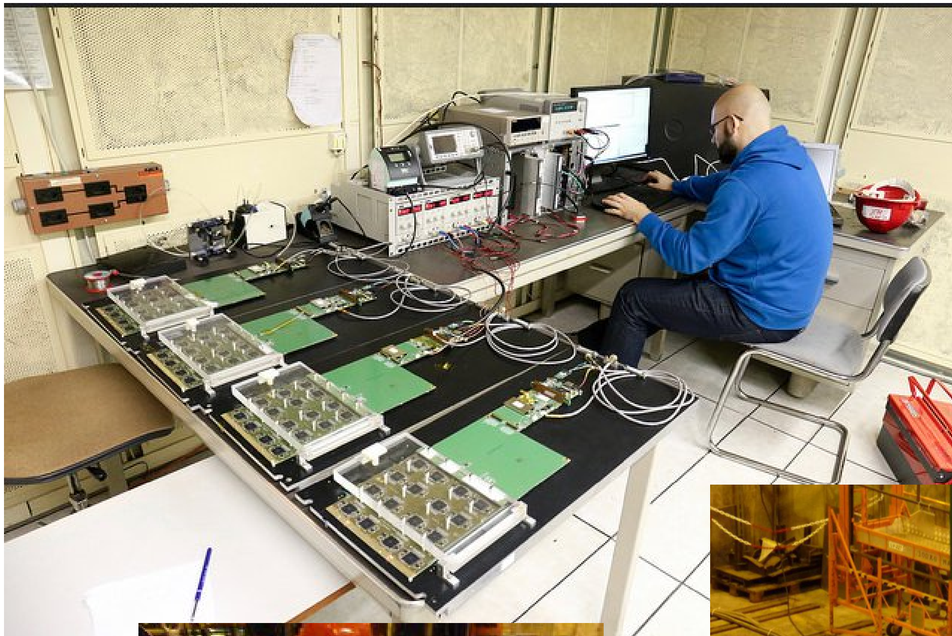
Interconnection completed

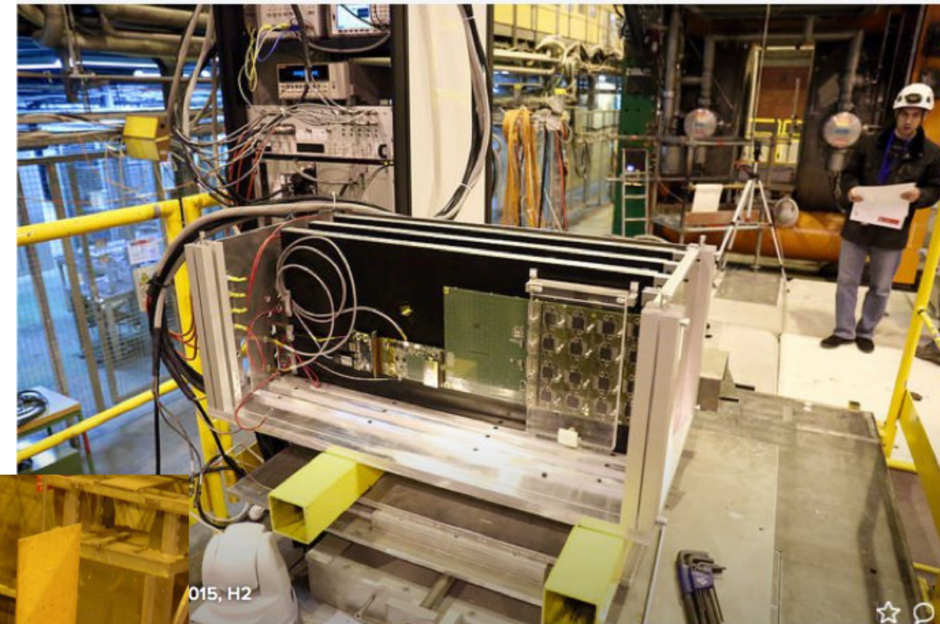
Slab Assembly Planning
2 slab in march
3 slab in april

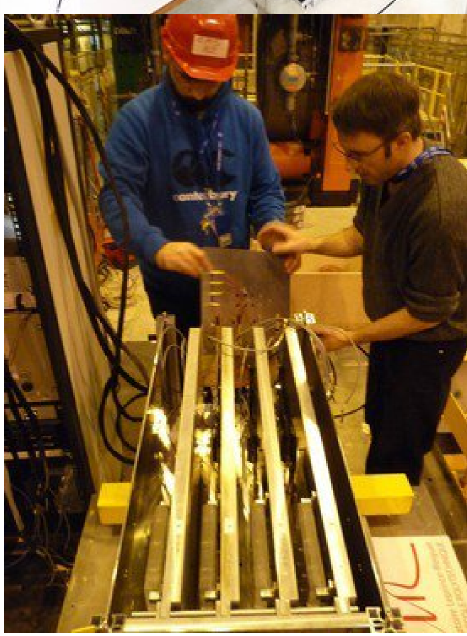
1st two SLAB's in tests
7 expected for June
⇒ in BT

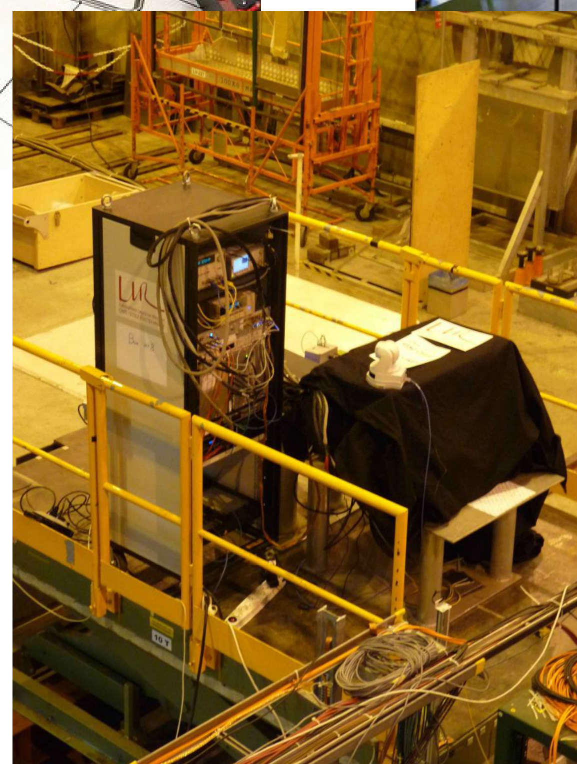


Beam test at CERN nov 2015
2–16th of november









Running conditions

4 layers ready for TB on test plates and put in the setup, the last layer was not operational (faulty HV) and was not used.

- Position of layers: beam → DIF1, DIF2, DIF0
- Each layer had 4 x 256 pixels / channels.
- All layers were always **power pulsed.**

Spills: Several settings tried,

- mainly long spills (eg. 200 + 50 msec = data taking + readout/dead time) to increase statistics with SPS spills of a few seconds, so, effectively corresponding to quasi-continuous mode.
- Also, some special runs with short spills 2.5 + 247.5 msec (no BX clock cycling)

DAQ: No problems with configuration of the setup.

High Gain: All data have been taken with feedback C=1.2 pF (nominal value is 6 pF)

- 5 times higher gain and better S/N (unexpected), but lower dynamic range

Selected **trigger threshold** = 230 after suppression of noisy cells

- much better than in cosmic runs one year ago (~290) but ≥ 220 (used for 2013 cosmic runs PCB (FEV8)).
- Special runs with a few triggering cells in showers

Very smooth running

DAQ: single crash (due to unchecked scripting)

Many data taken (but “only” ~85 GB)

- Beam structure + ACQ for ILC (bursts of 50ms × 4Hz)

Muons runs

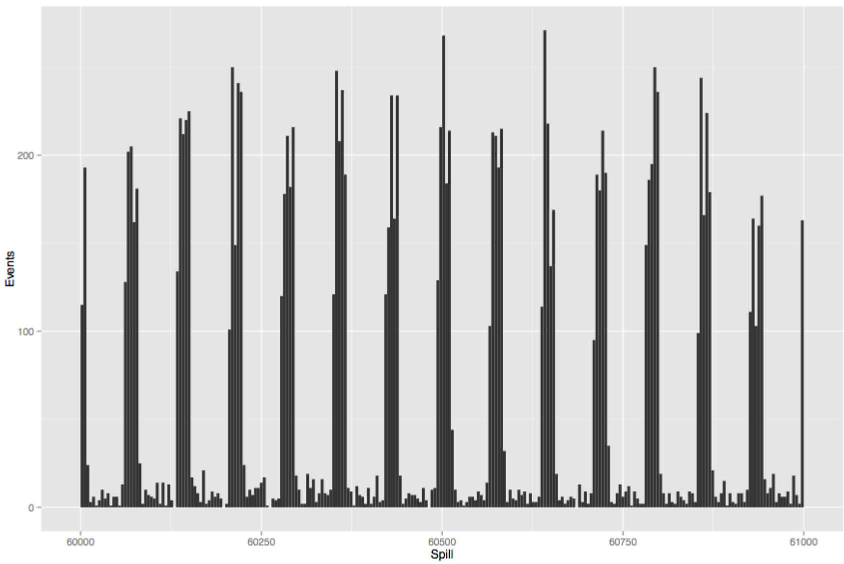
- Calibation first @ high threshold
- variation of threshold, and angles (49°, 90°)

Electrons of 15, 30, 50, 100, 150 GeV

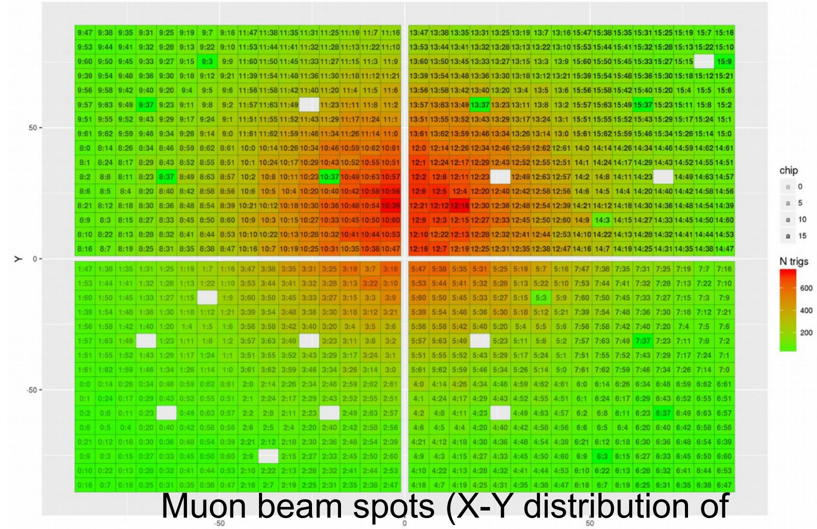
- with 8.5 X0
- with mini-cal option this WE

Pions of 50 and 150 GeV with 1.75 λ

- Check non un-conventionnal events



Masking : 2.2% of all channels

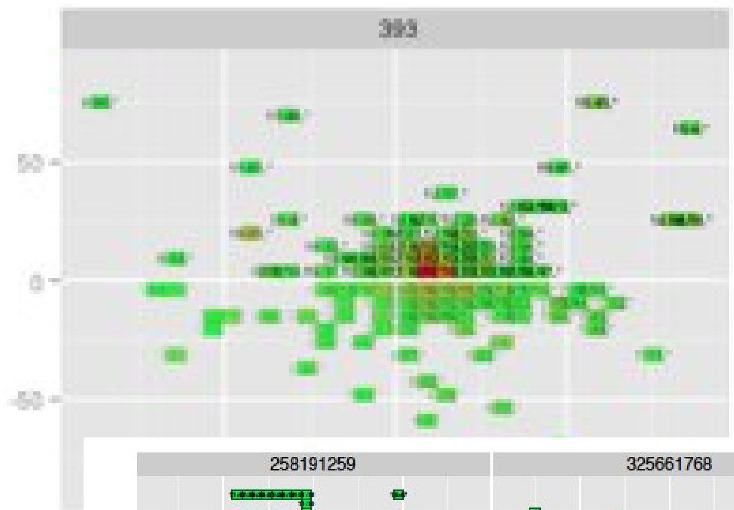


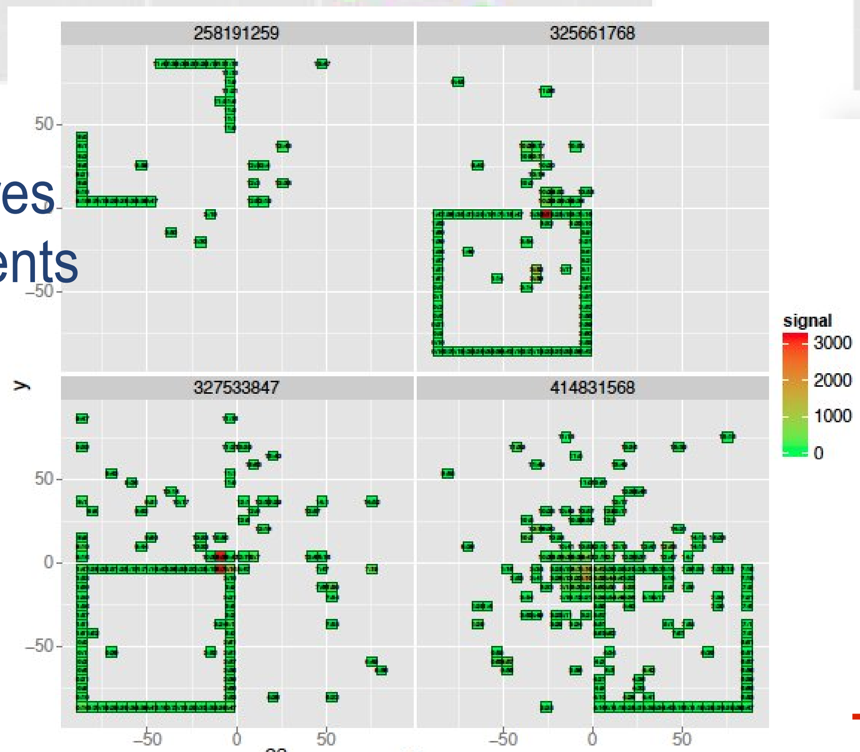
Muon beam spots (X-Y distribution of N triggers, requiring ADC-pedestal>10) from typical muon run 361 as example

Square events

by Kostya Shpak

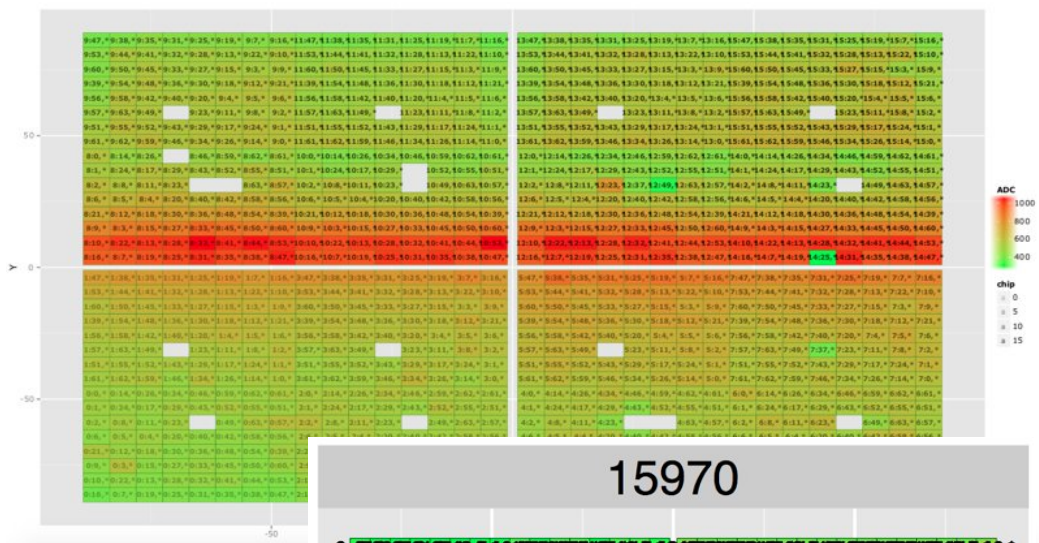
Normal event



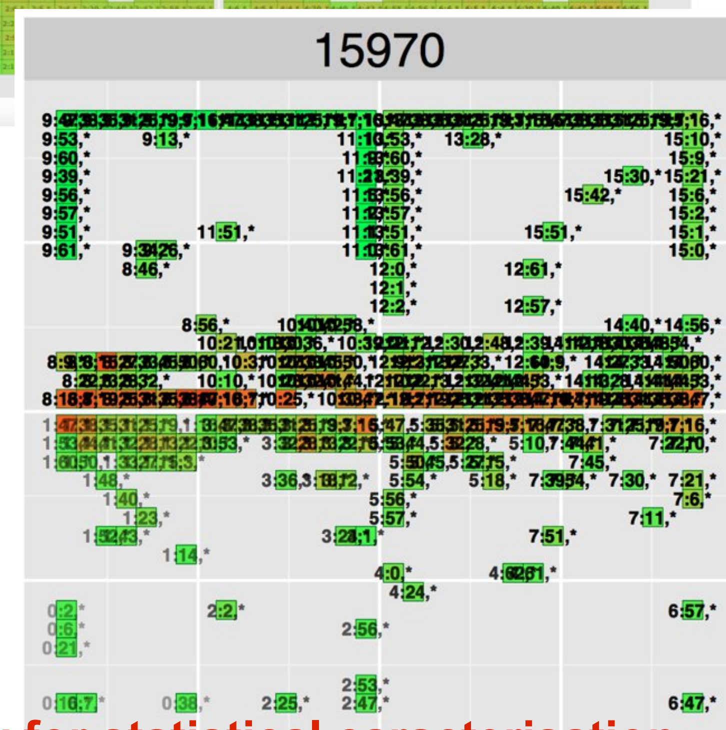


5 squares in 4 events

Shoot @ 90°



4 Sq in 1 event



Tools ready for statistical caracterisation

Others (not developed here)

Masking verification: some issues

Data corruption

- in case readout time wasn't sufficient
  - corrected by DAQ settings

Negative signal (ADC=4)

- located near the DIF connectors

Pedestal stability

- Slow drift after power one on long period

Split and delayed triggers

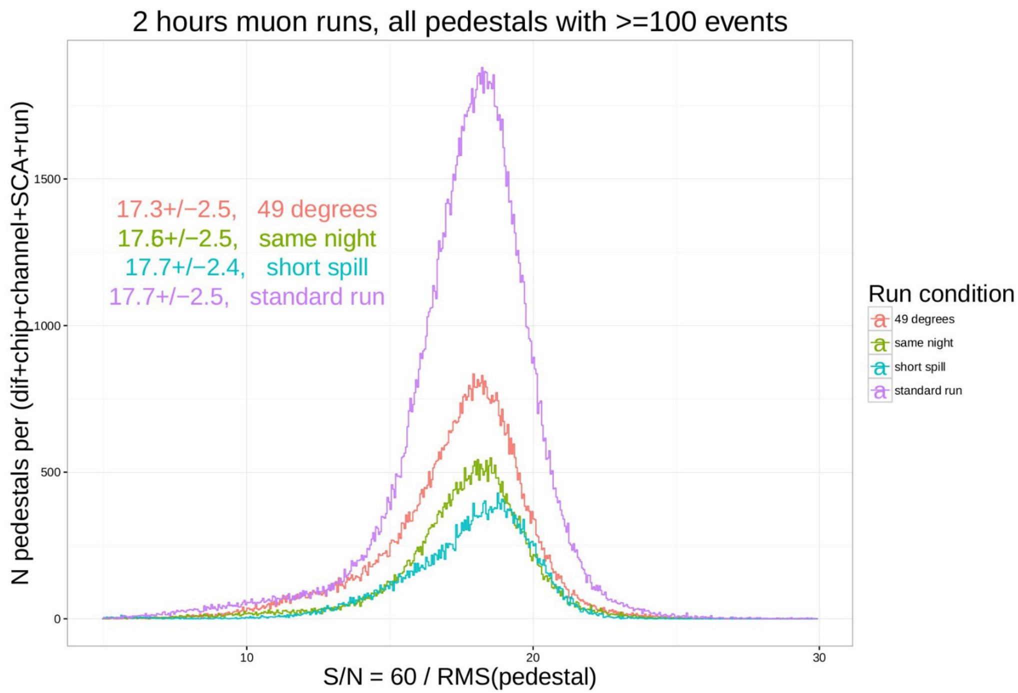
- "High intensity" delays trigger

Chip full events

Un-operationnal chips if SCA=15 in ACQ-1

Pedestal width:

- S(MIP) / RMS(pedestal) =17..18.
  - Good even for short spills with "real" power pulsing and drift effects



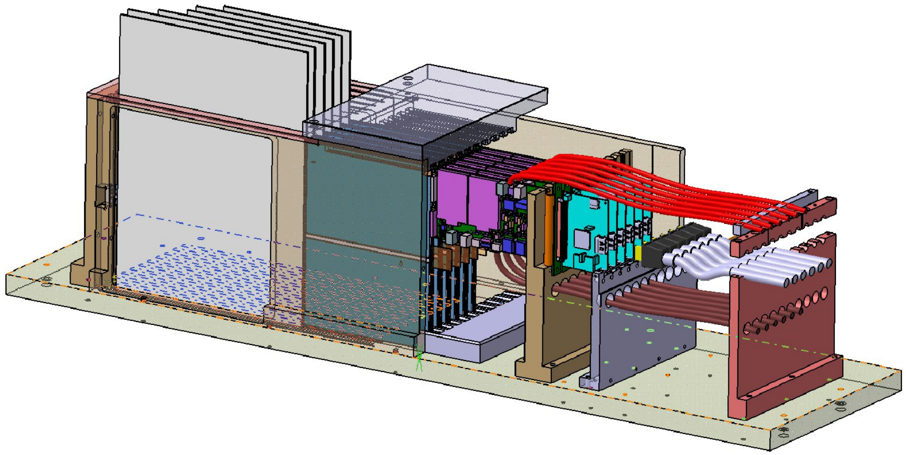
Beam test in 2016

Real calorimetric tests with 7–12 SLAB's in coordination with SDHCAL

- 7 ASU ready; production should resume in april
- real SLAB's (no more test plates) prod started this month
  - improved S/N ratio, robustness
- dependant on beam period (still under discussion)
  - eventually could re-use some of the CMS time in sept/oct.

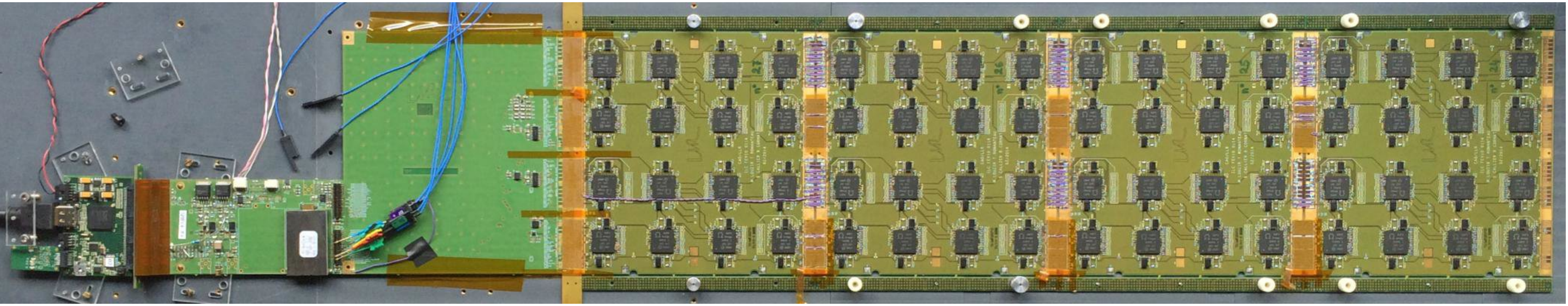
Flexible structure to accommodate

- variable number of SLAB's
- be in "real conditions" for PFA tests:
  - 24 X_0 of W + 3 cm gap before SDHCAL



Long SLAB: chaining ASU in cassette

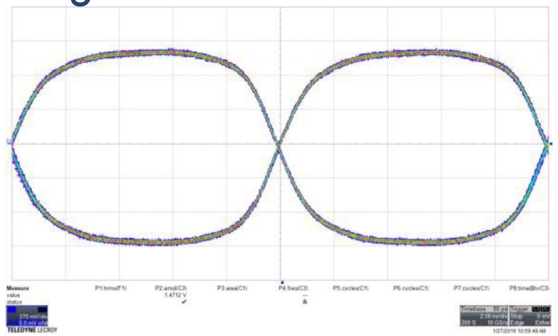
by J. Nanni & M. Louzir (LLR)

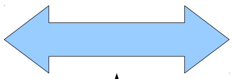


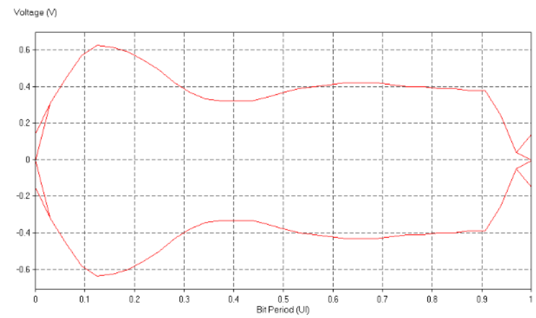
4 ASU connected correctly (✔ Control & Command, Config, Clocks, ✘: only 3 readout)

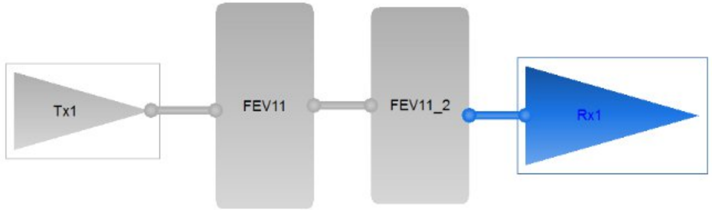
- debugging: interconnection (after many trials) Kaptons ⇒ Wire if not OK.

Clock spreading measurement & simulation:









After 4 ASU: Skew: 400ps; Jitter: 150ps;
Eyes well opened
⇒ 100Ω termination resistor needed

Long SLAB: chaining ASU in cassette

by J. Nanni & M. Louzir (LLR)

Check of short circuits on power lines

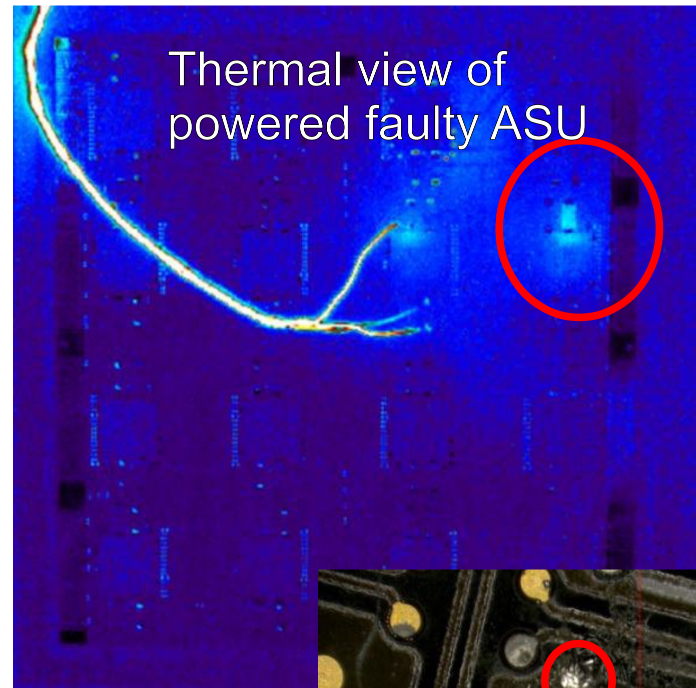
- 2 with out of 5 ASU (FEV11) received March 2015

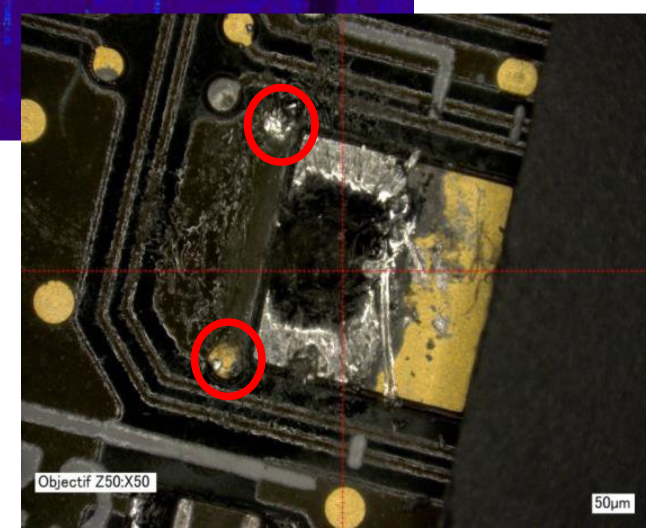
Goal: demonstrate validity of the feasibility of a long SLAB of 8–10 ASU's

- Instrument (baby wafers) ends Equipped (ASIC) in between
- Do full signal check
  - with power pulsing
- Mount with "real set-up" HV capton + Carbon Cassette

Key element of the SiW-ECAL concept for ILD.

- *tools available, still much work to do...*





2 vias of gnd! too close from vddd! capacitance connexion.

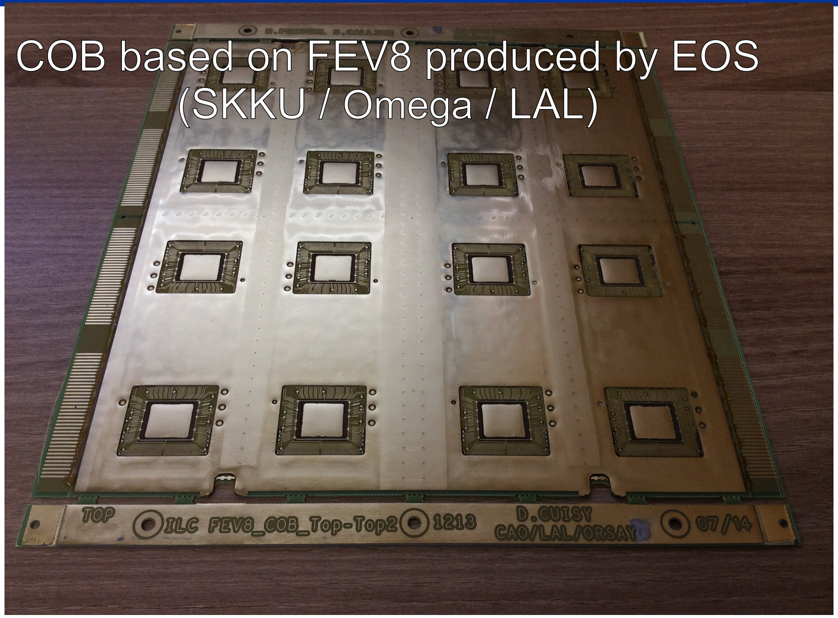
Chip on Board

by R. Poeschl (LAL), J. Chai (SKKU)

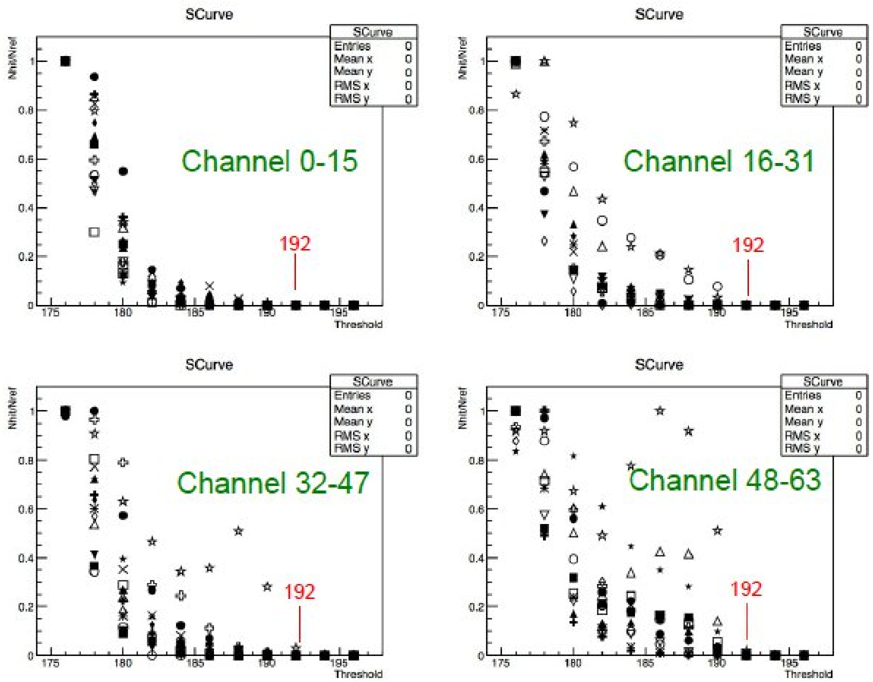
For lower X0 and improved PFA:

Embbed chips in board ⇒ **COB**

- Mechanical & Electrical challenging
- 10 boards produced, bonded @ CERN
  1st debugging fall 2015



Chip0 after disabling of 7 channels: No charge injection



First noise S-curves fine

- to be checked with signal injection

Next (ST to LT plans)

- Continue test
  new boards using FEV11 design
- upgrade DAQ
- Check with Wafers (⊃ mechanics)

Integration in ILD: thermal studies

by Denis GRONDIN / Julien GIRAUD (LPSC)

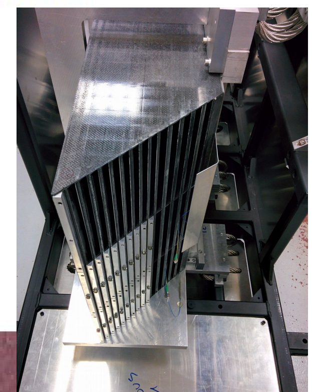
Tests and simulation on detector (EUDET module)

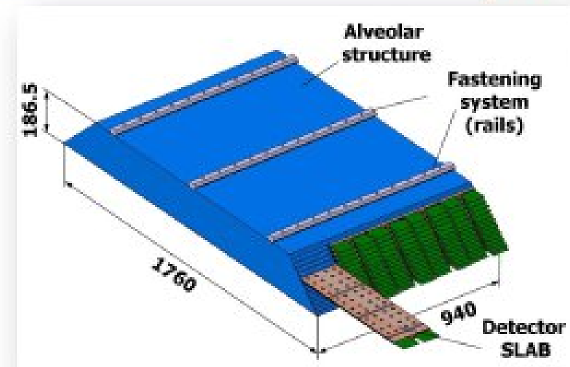
CALICE
Calorimeter for ILC

Dummy SLAB with heater to simulate power dissipation :

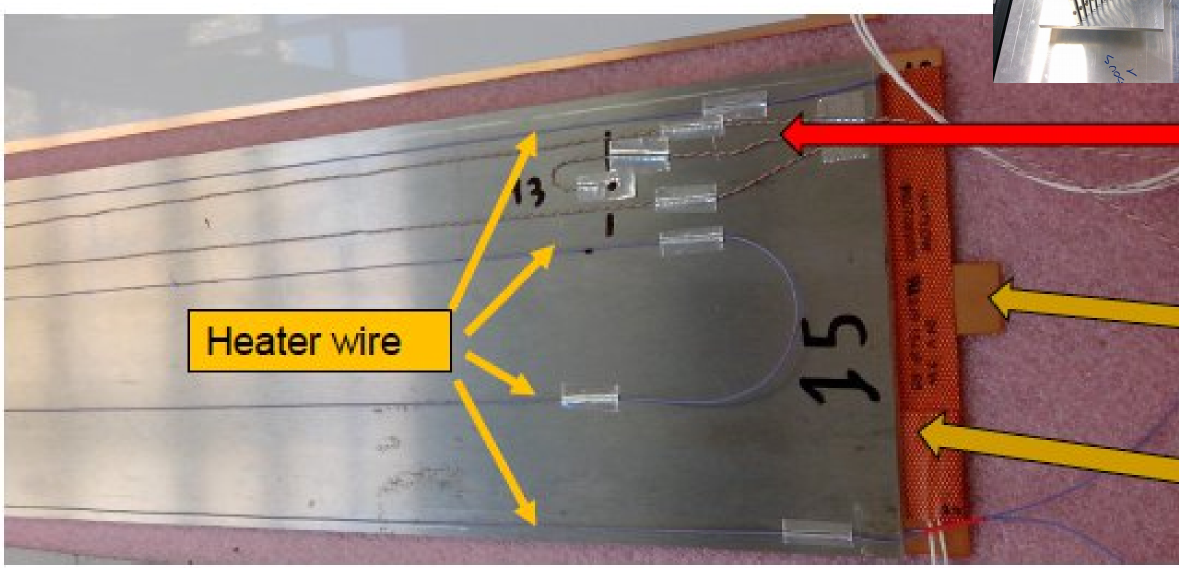
- ASU => 0.5 W to 1 W per ½ SLAB
- Front => 0.3 W to 3 W per ½ SLAB
- Cooling effect.

Realization of 15 SLAB (Aluminum / copper / Plastic)



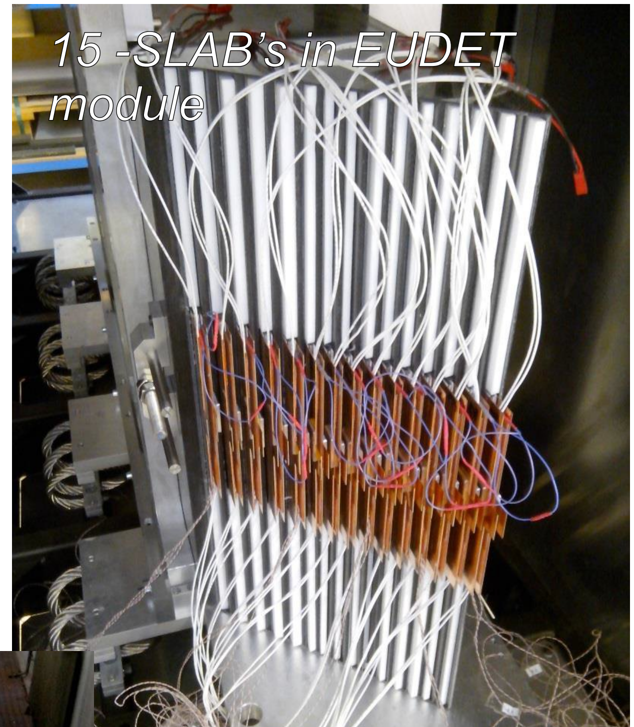


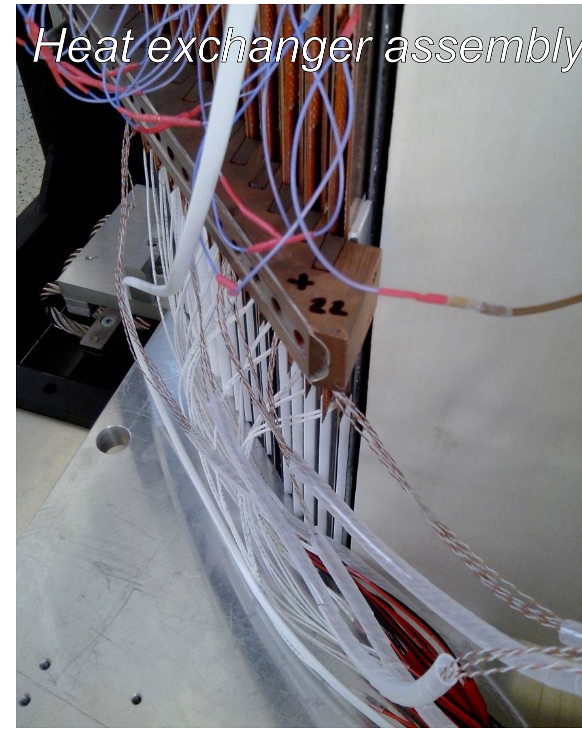
3 x Thermocouple P class 1
(±0.5°C de -40 à +125°C)
Inside 4 SLAB



Integration in ILD: thermal studies

by Denis GRONDIN / Julien GIRAUD (LPSC)



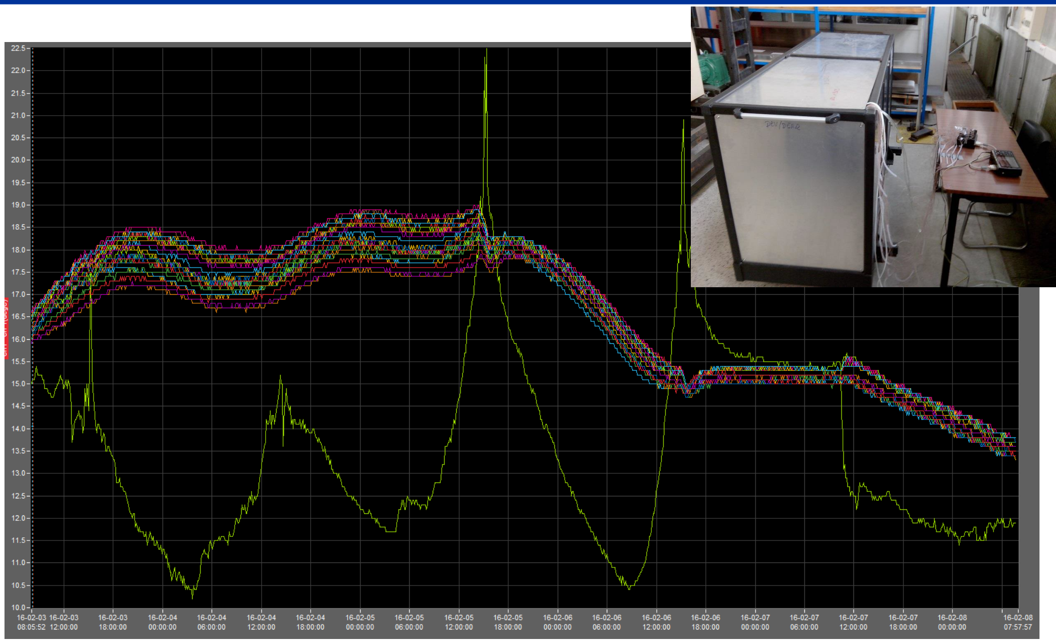


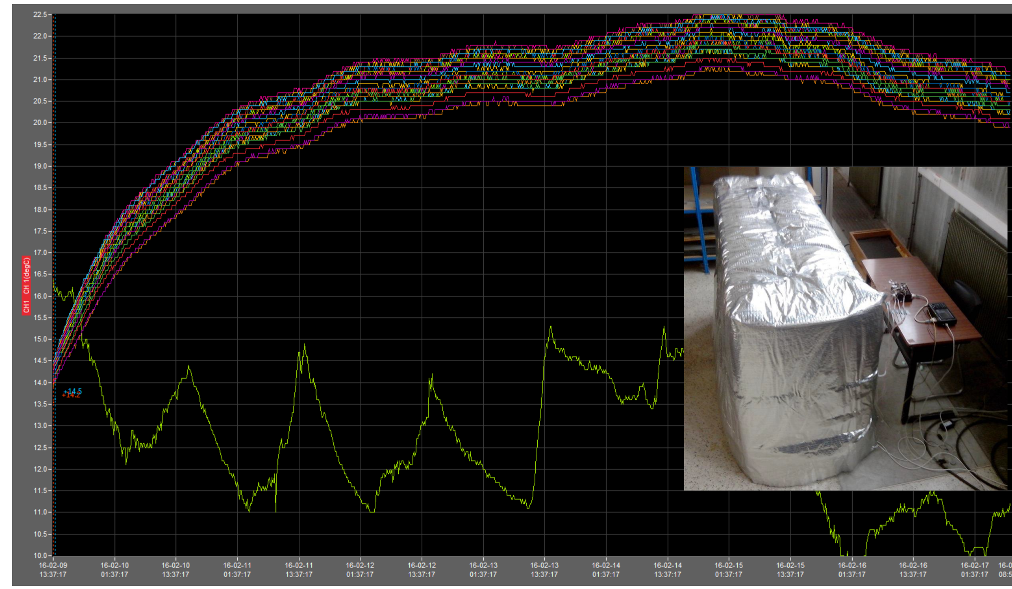
Puissances ASU / SLAB (W)	1	2	1	2
Puissances Front / SLAB (W)	1	1	2	2
Total ASU SLAB (W)	15	30	15	30
Total FRONT SLAB (W)	15	15	30	30
Total (W)	30	45	45	60

Important thermal inertia => 4 days minimum of stabilization

Integration in ILD: thermal studies

by Denis GRONDIN / Julien GIRAUD (LPSC)





3 day period

Power without cooling

- P= 15.476 W

Peaks in **external temp** due to direct sunlight

8 day period

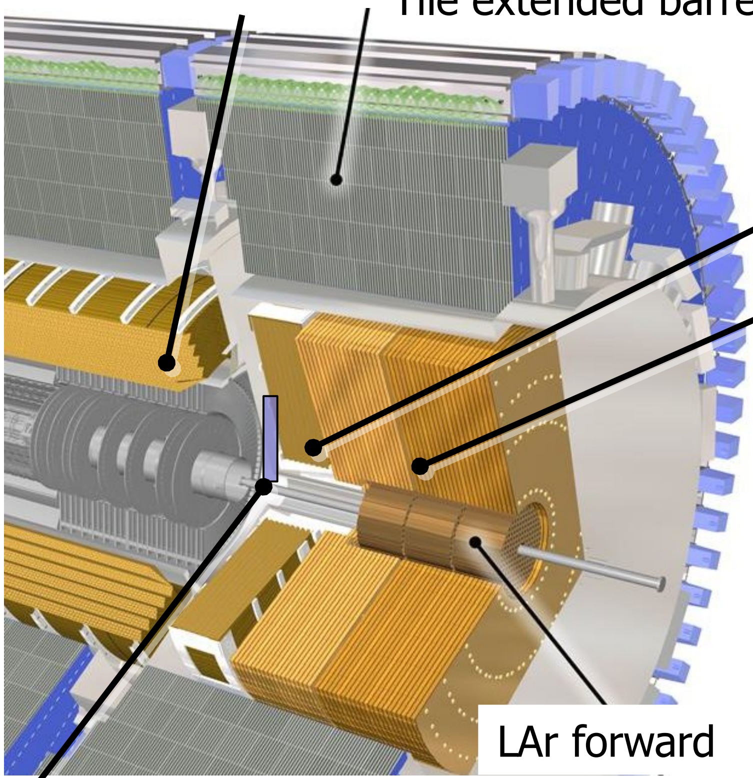
Conclusion:

- Efficiency of ex. isolation ✔
- Thermal test takes time…

Ready for cooling tests...

LHC Upgrades at Paris-Saclay ATLAS-HGTD

- A dedicated "timing" forward detector device is envisaged for ATLAS at HL-LHC to cope with the very large collisions pile-up
- A Silicon High Granularity option is proposed by France (LAL, LPNHE, Omega, CCPM), US (Santa Cruz, BNL), and CERN

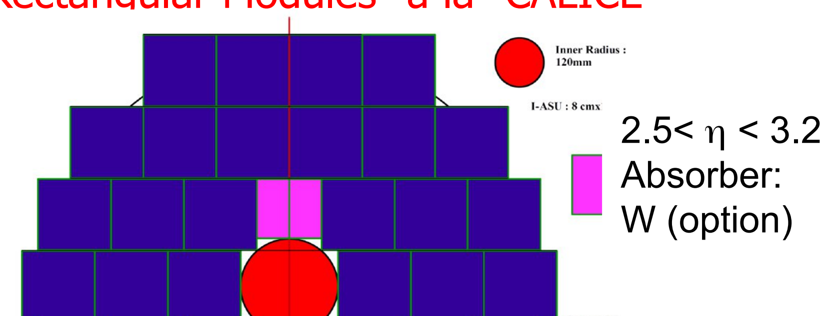


The HGTD project aims to achieve the required 20-30 ps timing precision for ($2.5<\eta<4.3$) actually covered by the so-called Inner-wheel of the LAr forward e.m. calorimeter

The HGTD needs a fine transverse granularity (~5x5 mm^2), to optimize the timing resolution versus the cell occupancy, and will have 4 layers in depth.

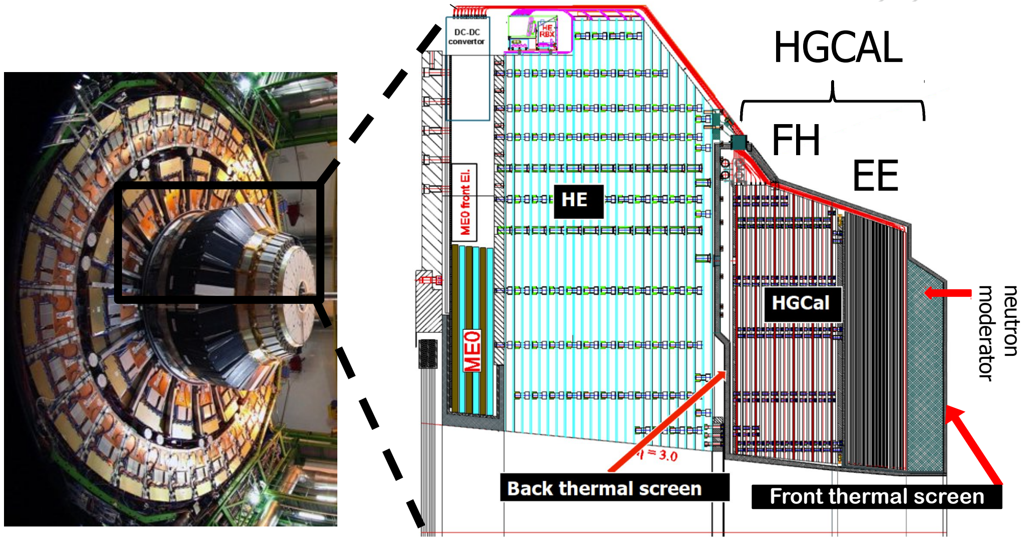
HGTD Reference design

Rectangular Modules "à la" CALICE



LHC Upgrades at Paris-Saclay
CMS-HGCAL

- A “HGCAL” SiW calorimeter, inspired by the pioneering work of CALICE, has been adopted for the CMS forward calorimeter at HL-LHC



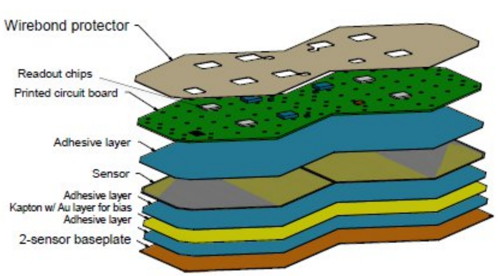
HGCAL EE+FH Highly granular:
- **312** Cassettes, **44k** Wafers
- **100k** FE ASICS, **6M** Channels

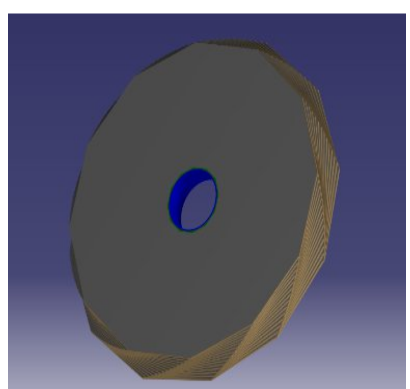
The CMS-LLR group, with help from Omega lab., is at the origin* of this ambitious CMS project

* LLR polytechnique, CERN, U. Minnesota, IC London, UC Santa Barbara,

The CMS HGCAL project has ~ 100 members from 20 institutes among which 3 French IN2P3 and IRFU labs.

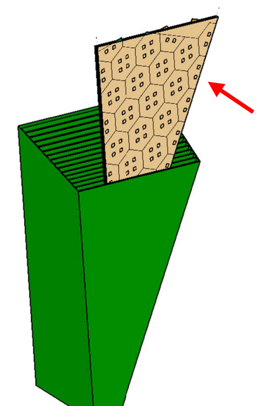
Modules with two 6” sensors





HGCAL Reference design
[CMS Technical Proposal]

C-fibre/W Alveolar 30° “petals”
12 Petals assembled together



Cassettes
(heaxagonal Si active element,
FE, Cooling plates)
inserted in alveoli.

Micro-Megas HCAL & ECAL

Micromegas calorimetry

Alternative for SiD HCAL

Pros : proportional mode, high-rate, narrow avalanche, simple gas, low-noise

Constructed : 4 prototypes of 1x1 m^2 (in 2012)

Shower measurements to validate technical choices & Geant4 simulation

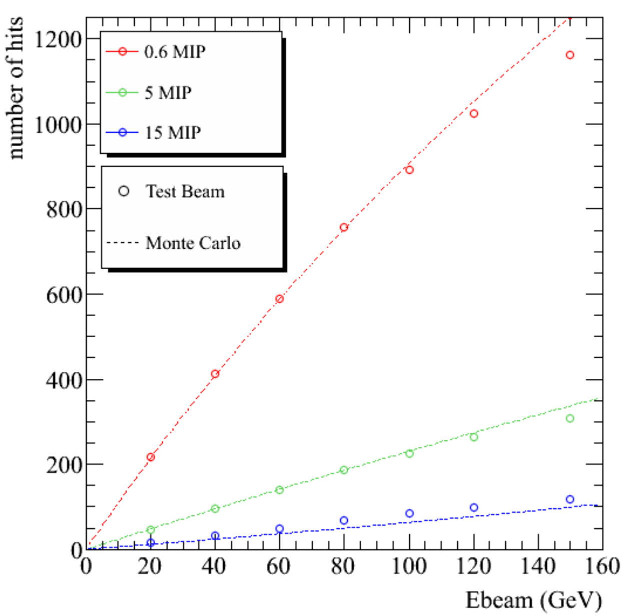
* Hadron sample recorded inside SDHCAL with 4 Micromegas + RPC (SPS, 2012)

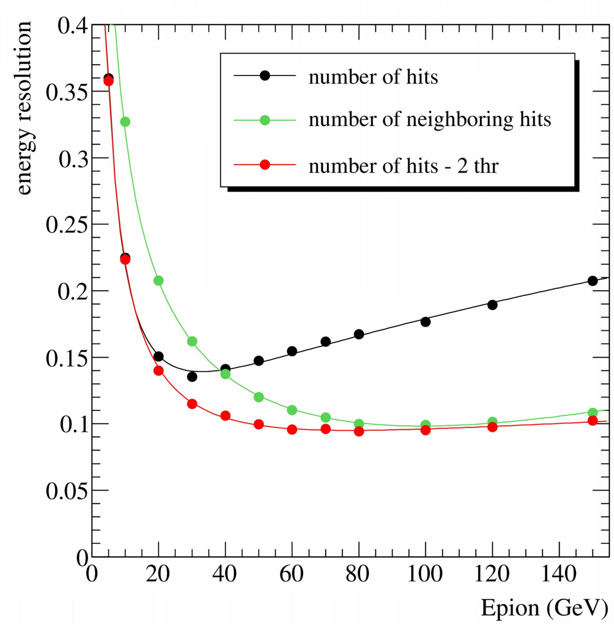
→ response of a virtual Micromegas SDHCAL well reproduced

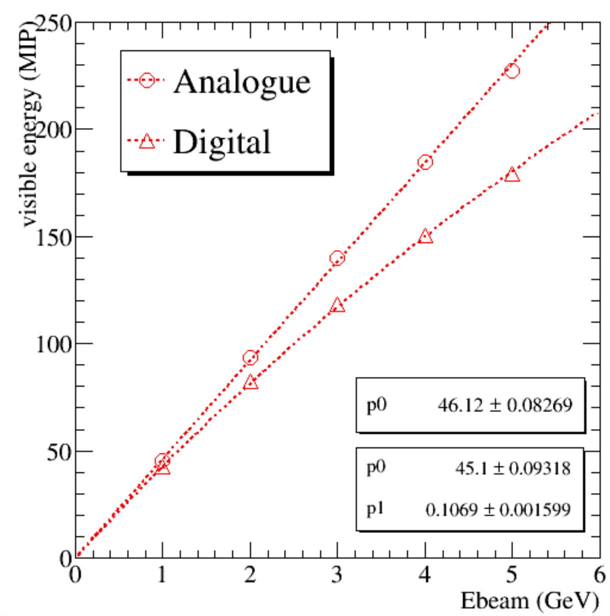
* For the energy resolution, we rely on Monte Carlo

→ saturation term can be mitigated by means of threshold or hit density info.

* Electron sample (DESY, 2013) : comparison between analog & digital readout







Present : resistive prototypes

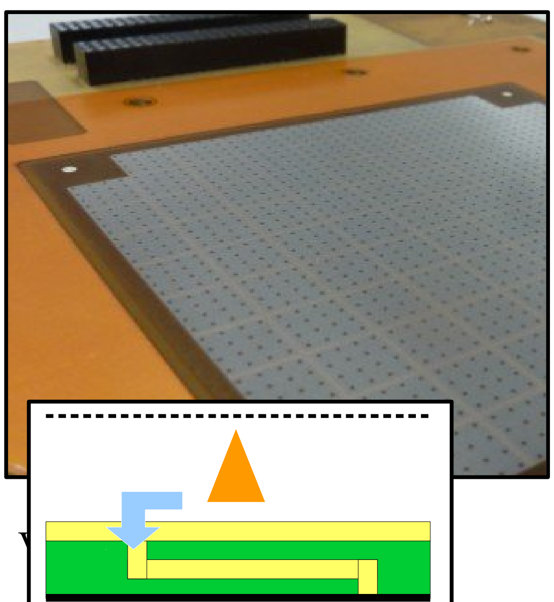
Sparking

Occurs rarely (10^-5 / shower) but causes deadtime of ~ o(1) ms
+ requires passive components on PCB to protect ASIC (2 diodes/channel !)
Resistive anode : advantage of RPC (no sparks) w.o. drawbacks (high-rate)

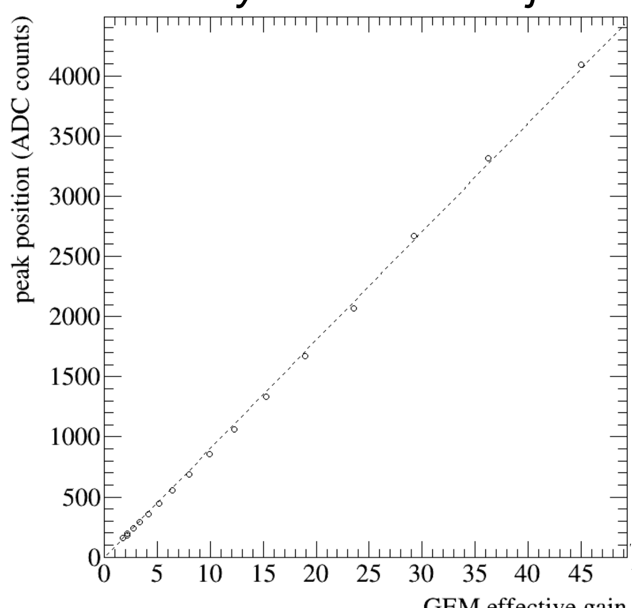
Prototypes with : segmented resistive pads and burried resistors (10x10 cm^2) (2014-15)

* Good compromise between fast charge evacuation & full spark suppression
* Primary electrons at the mesh within 50 ns → last ones feel reduced Efield
→ Preservation of the proportionality of the response was checked.

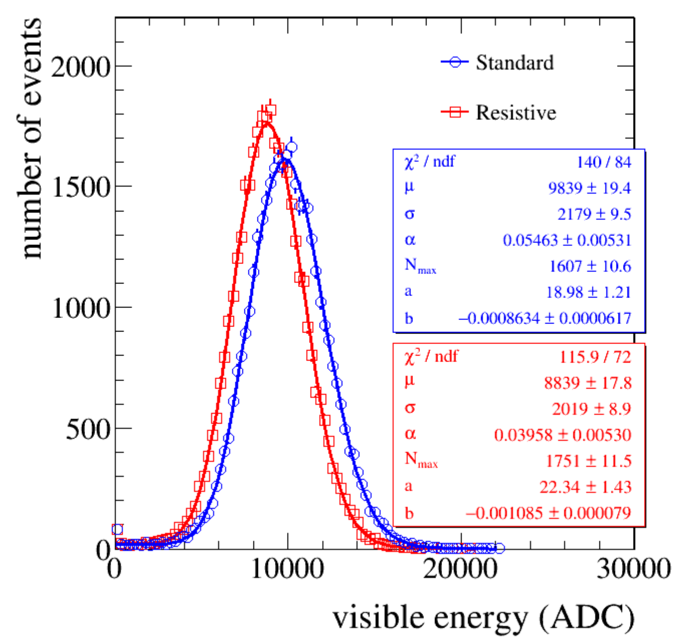
LAPP-Irfu-Demokritos



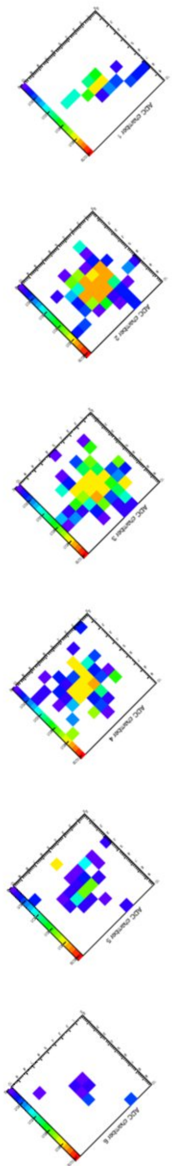
^{55}Fe X-rays after GEM injector



200 GeV e^- behind 8 X0



Present & prospects

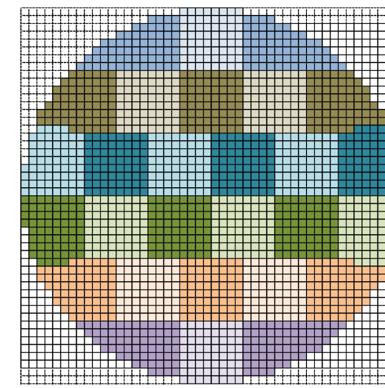


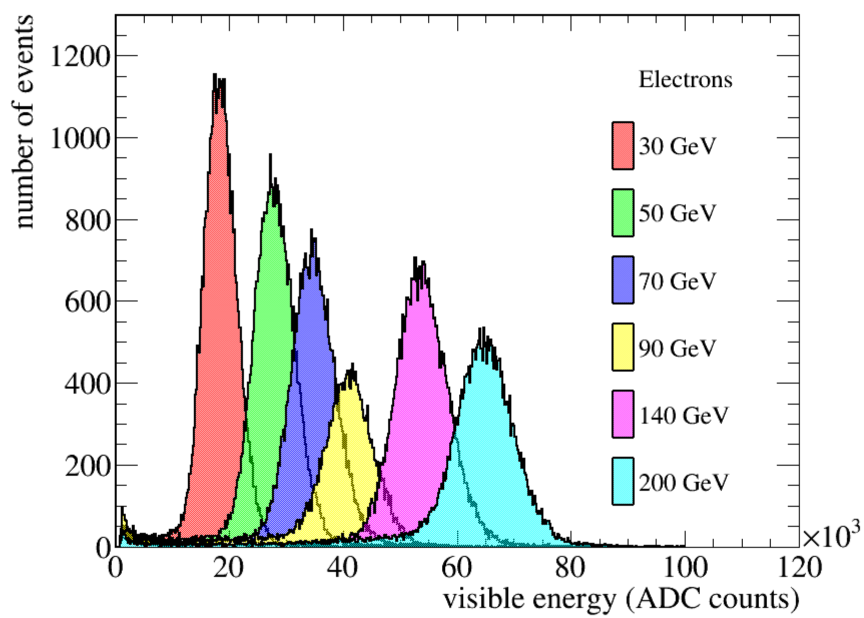
Mini-ECAL : 6 R-prototypes and 20 X0 (SPS, 2015)

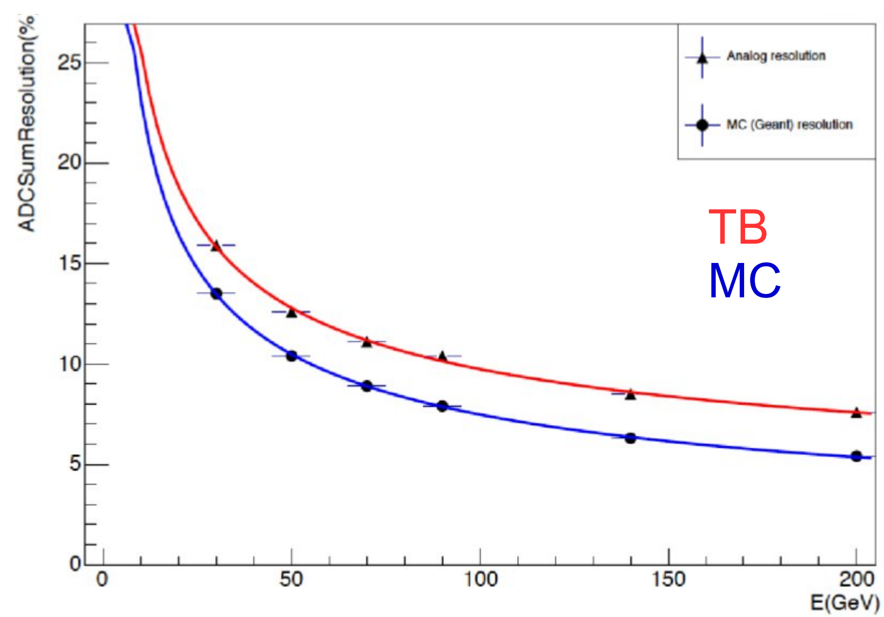
Sampling obviously not optimised but
→ Running from 30 to 200 GeV without 1 spark
→ Stochastic term well reproduced by simulation

Future plans

* Validate burried-R techno. on 48x48 cm2 ASU →
* PCB design on-going, fabrication of 10 units in 2016
* To be shared with Weizmann
* Possibility to evolve towards small calo. if funds allow







RPC–SDHCAL

SDHCAL activities

Articles

→ **The SDHCAL prototype conception and construction paper** is published

→ **First SDHCAL result paper accepted for publication (18/03)**

→ **A note on the SDHCAL simulation is published and a paper is being finalized**
→ **A paper on track segments finding using HT in SDHCAL is almost finalized**
→ **A note on SDHCAL ARBOR is published. A paper in preparation.**
→ **A paper on comparison of different hadronic shower models**

→ **A note on energy reconstruction using NN techniques**

SDHCAL activities

Beam tests 2015

2 weeks on H6-SPS +1 week on PS + **2 weeks at H2 (offered by the SPS….**.)

→ Use of USB2 protocol : DAQ Dead time reduced by a factor of 2

→ HV control according to T,P. Attempts to use Cerenkov detectors

→ Energy scans, different angles : important for simulation

→ **Gain correction, threshold corrections, gas purifier…**

Analyse activities

→Hadronic shower models comparison with SDHCAL data finalized (**A. Steen Thesis**).

→SDHCAL ARBOR (Rémi Eté). Simulation is now included (see B. Li Talks)

→MVT for energy estimate and electron/pion separation (S. Mannai &G.Garillon)

→Electron pion separation (work initiated by M-C. Fouz& A. Pingualt)

R&D activities

Electronics (CIEMAT, **IPNL, OMEGA**) , detector (**IPNL, OMEGA**, GWNU) and mechanics (CIEMAT,IPNL), DAQ and monitoring (**IPNL**)

3 periods of TB

1- SPS-H6 27 April-13 May 10-80 GeV
2- PS 25 May – 3 June 2-12 GeV
3- SPS-H2 15-31 October 10-80 GeV

Corrections :

→ Use **temperature –Pressure correction**.
Energy scan to compare with data without this correction.: **analysis to be done**

→ Apply **electronic gain correction** (using noise maps)
→ homogenous response and to reduce the DAQ dead time (factor of 2). Energy scan with this: **analysis partially done**

Filtering

→4 **Tungsten** plates provided by Wolfgang **to eliminate electrons** (50m upstream)

→Cerenkov was used but was successful only in PS**: analysis being worked out**

FilteringExtended Data sets

→Three angles (0, 10, 20 degrees) of exposition. Energy scan for each angle

→For Neural Network tests a scan of 1 GeV step was performed between 40 and 50 GeV. **analysis being worked out**

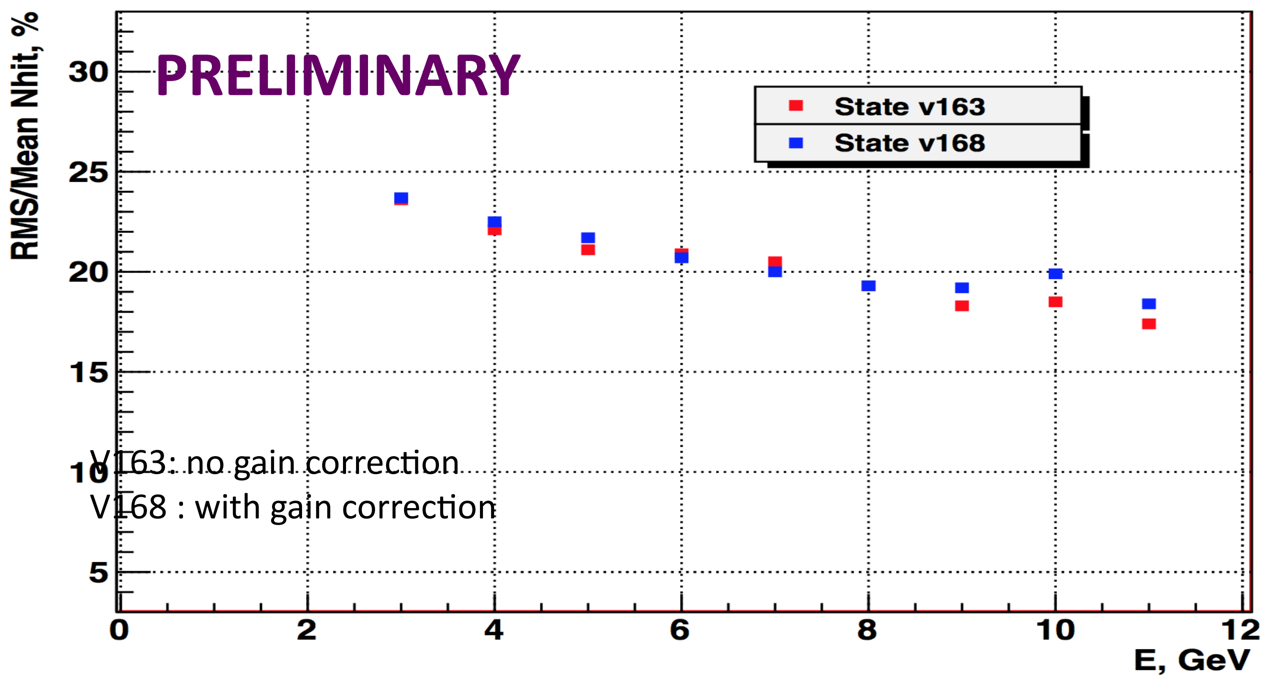
→ Two different values of the first threshold are tested (114 and 142 fC)

→ At PS 1 GeV step scan was performed for all configurations. 5 GeV step in the case of the SPS **analysis to be done**

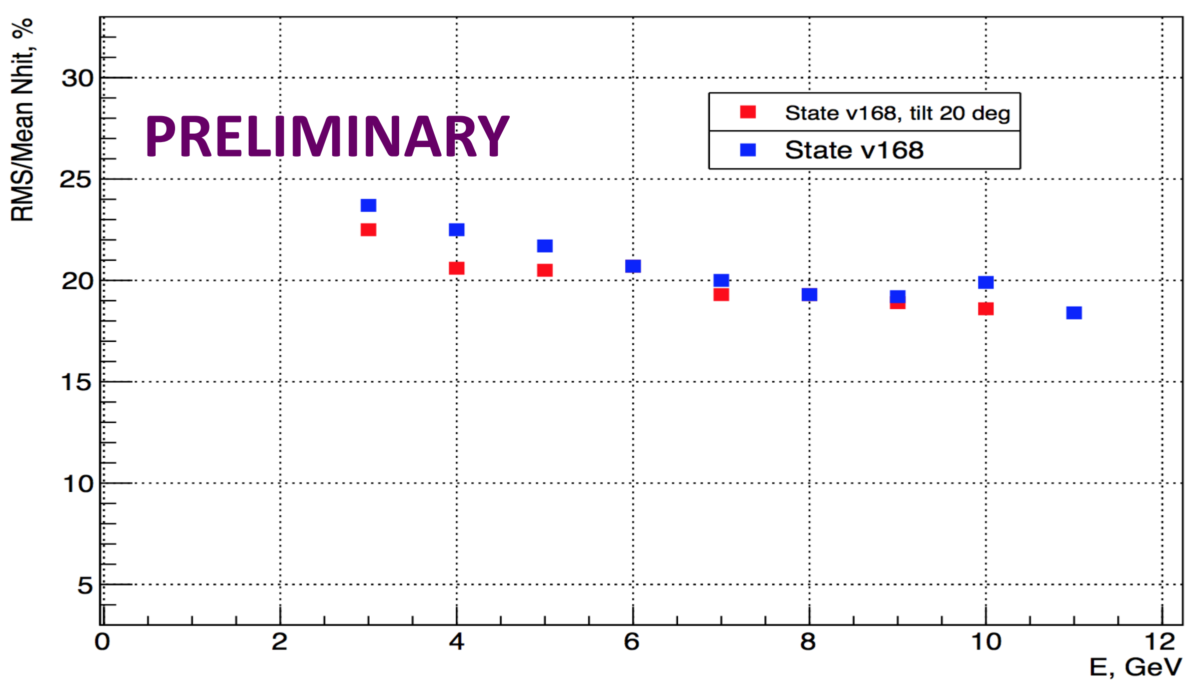
→ Use threshold as a parameter to homogenize the SDHCAL response **analysis partially done**

Technical :

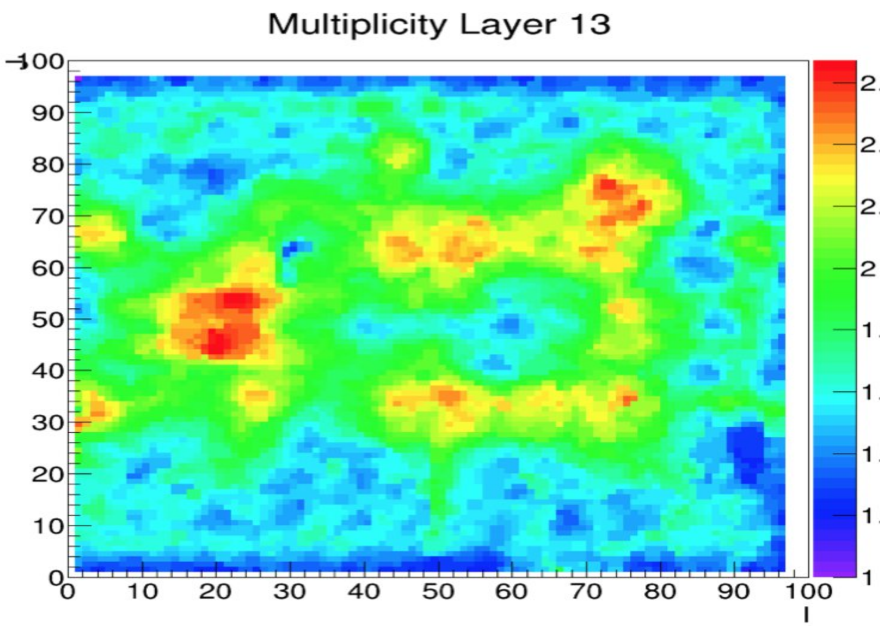
→ First test of the gas purifier **: problem during TB, now problem understood.**

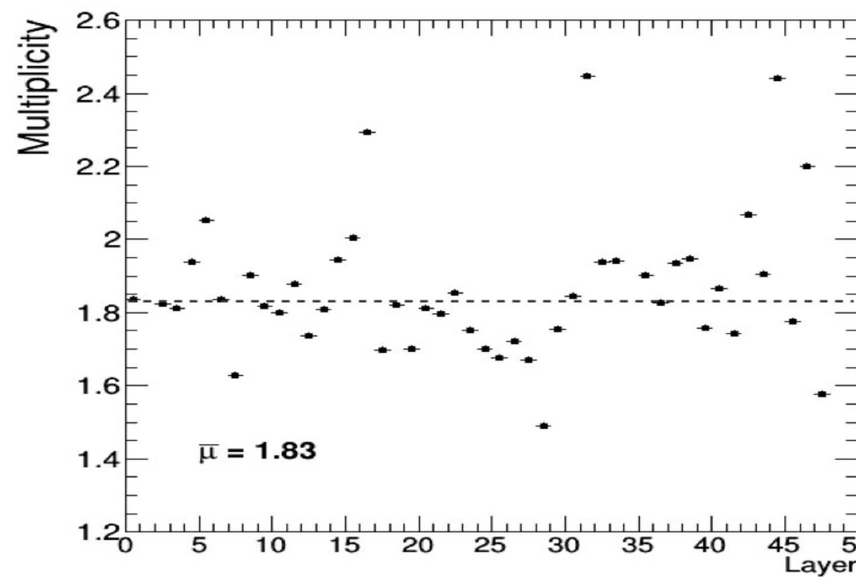


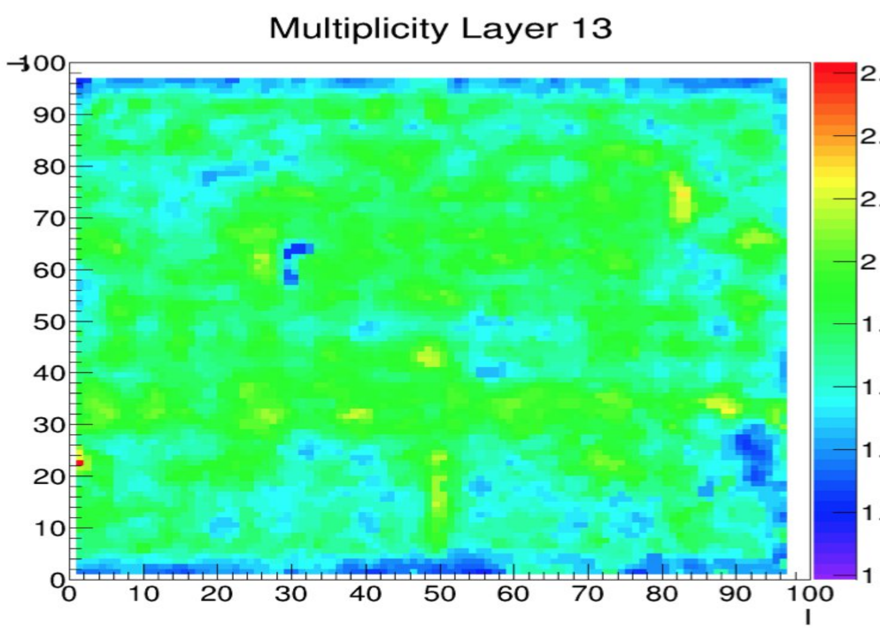
Collected data are being analysed. Preliminary results are consistent with those of 2012

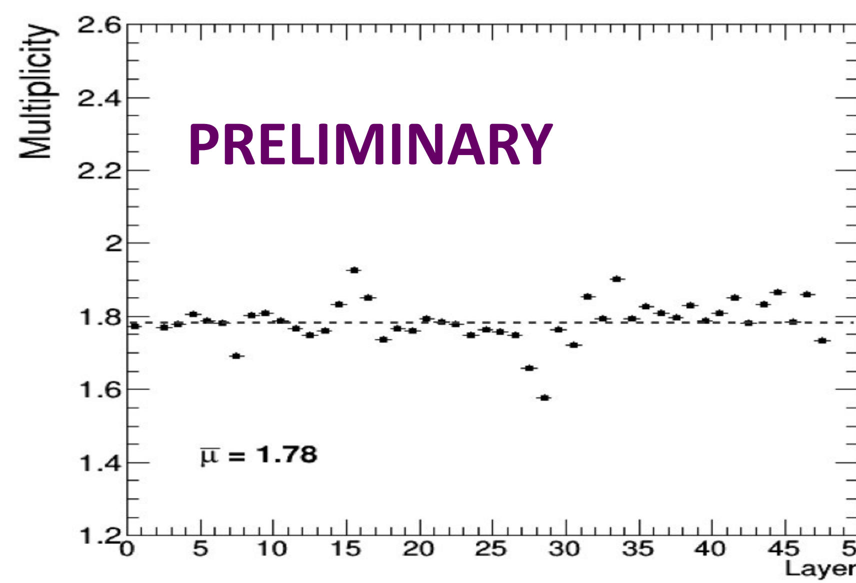


Establishing homogeneity by varying the threshold value



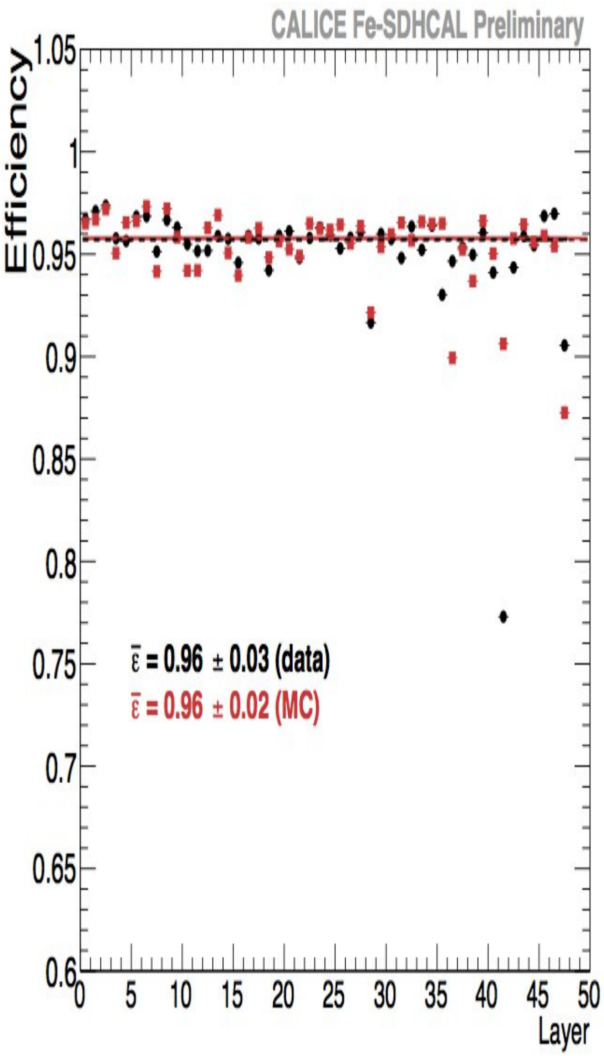


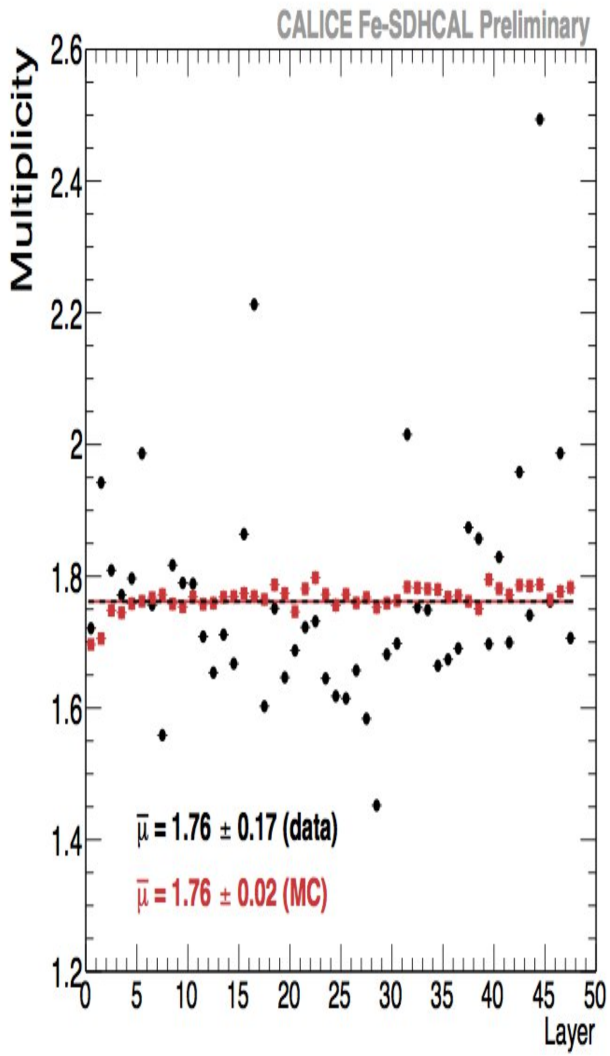


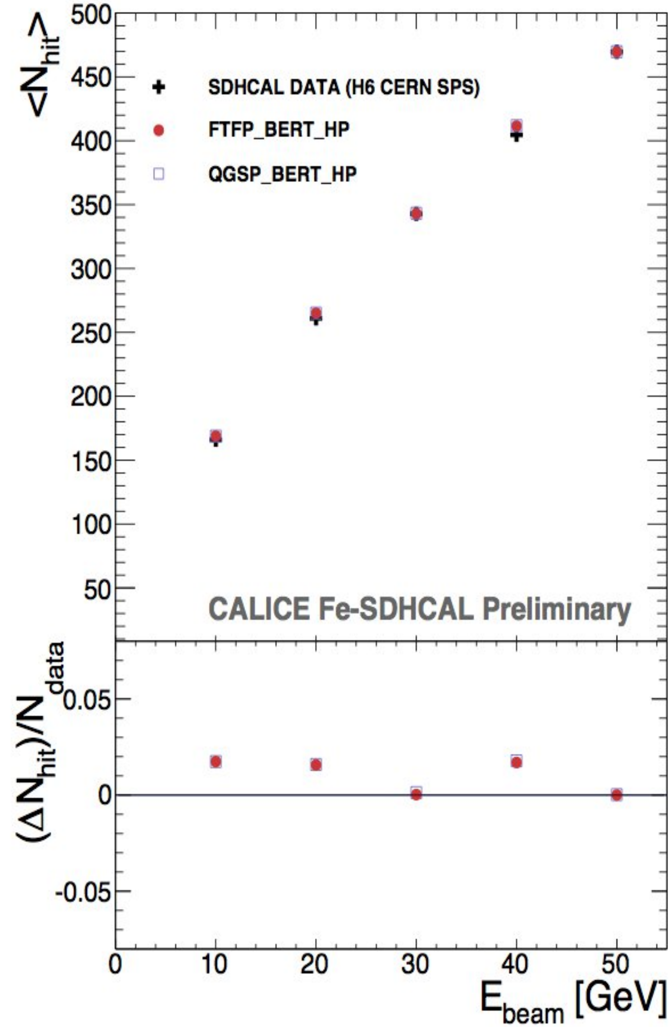


Simulation

The digitizer is finalized. Parameters tuned using muons and electrons. Detector inefficiencies (dead channels) are included.

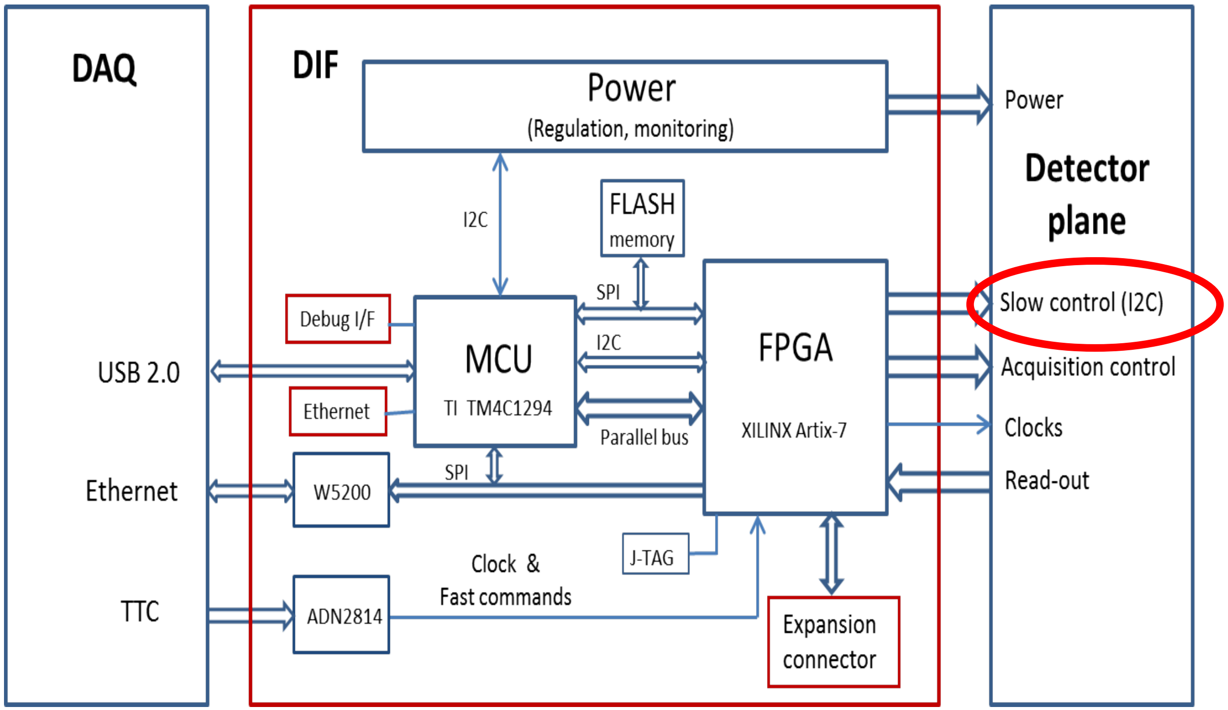






Hardware R&D of next generation: full zero suppression & large surfaces

HARDROC3: Preliminary results confirm that all functionalities are. Test of the 600 HARDROC3 is under preparation at IPNL.
DIF : design is in an advanced stage

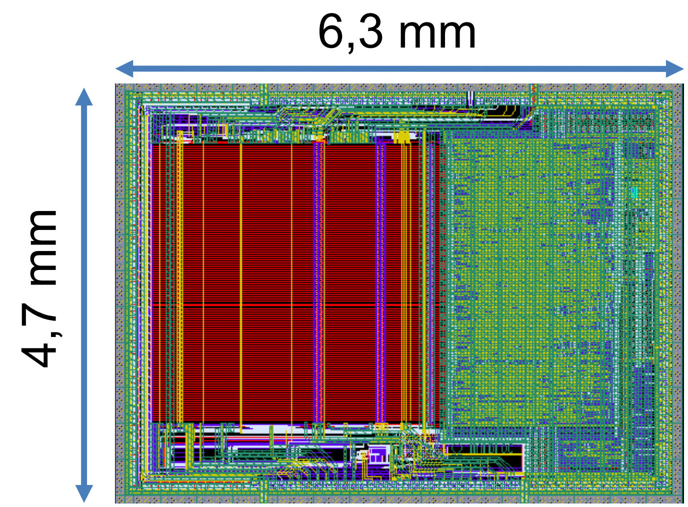


PCB : Rooting is finalized. ~~Baseline is 50x33 cm² PCB (24 ASICs)~~. **Large PCB of 100×33.3cm²**
Mechanics : Important progress
Detectors : Design of 2 m² is being discussed. First construction attempt will come soon after readout design is finalized

ASIC: HARDROC3

HR3 main features:

- Independent channels
- Zero suppress
- Extended dynamic range (up to 50 pC)
- I2C link with triple voting for slow control parameters



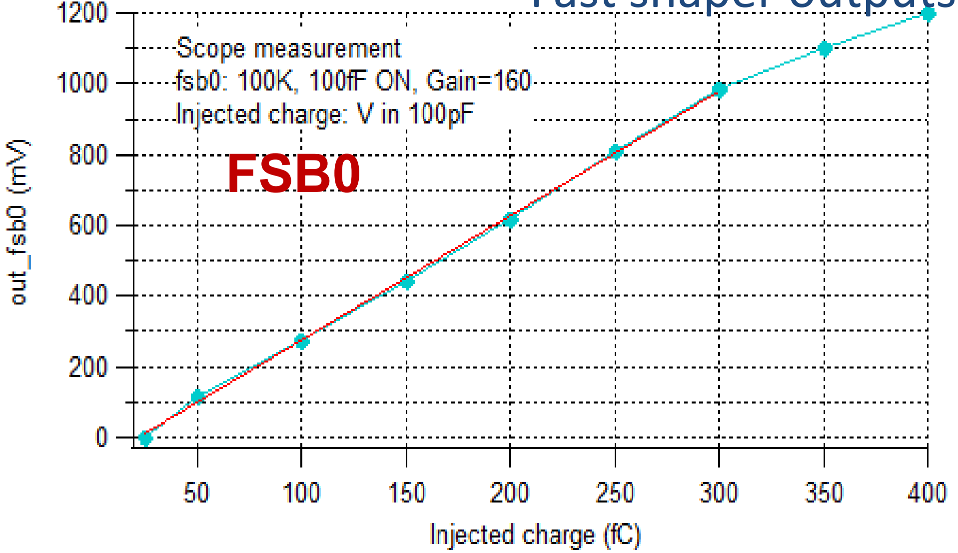
HARDROC3:

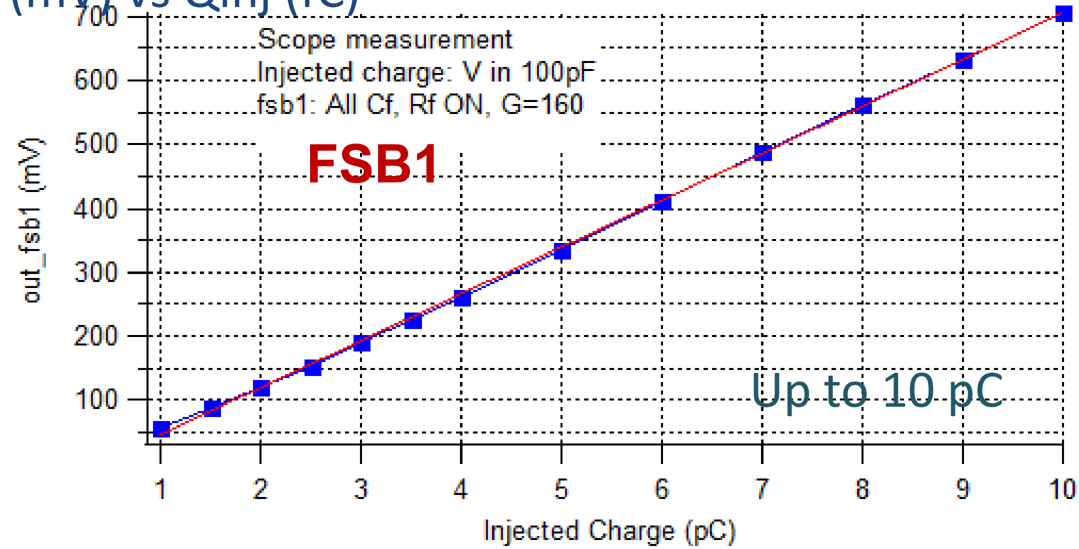
- Production run submitted mid February 2015 (AMS SiGe 0.35µm)
- Naked dies expected in May 2015
- Chip will be available in June 2015 after packaging in QFP208
- Die size ~30 mm^2
- Around 600 chips will be available

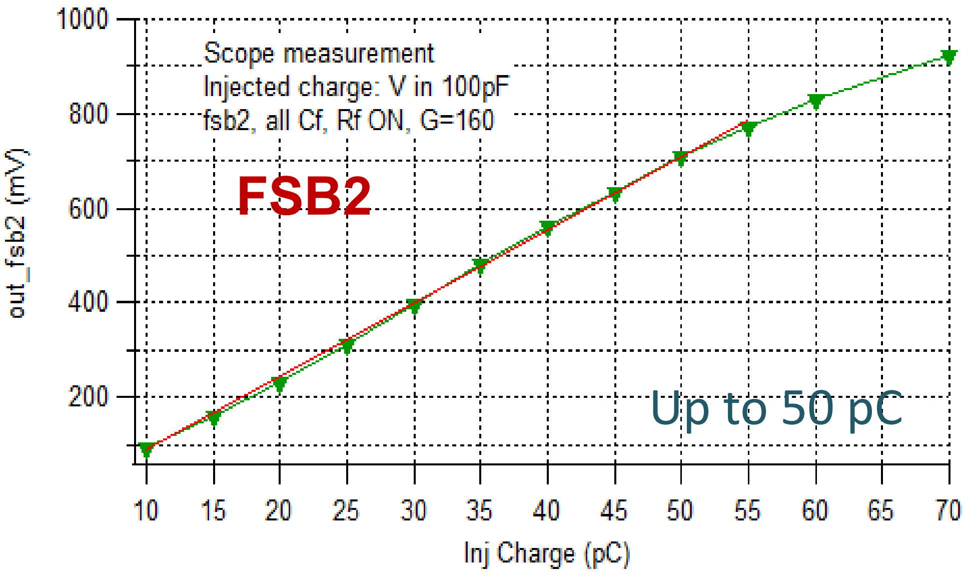
Vincent.Boudry@in2p3.fr

HR3: Analog linearity

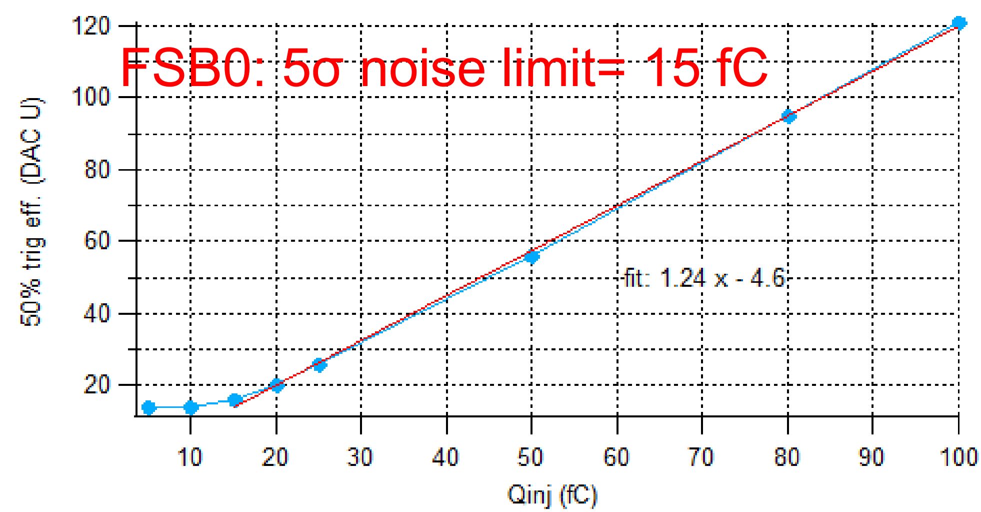
Fast shaper outputs (mV) vs Qinj (fC)







50% trig. Eff. (DAC units) vs Qinj (fC)



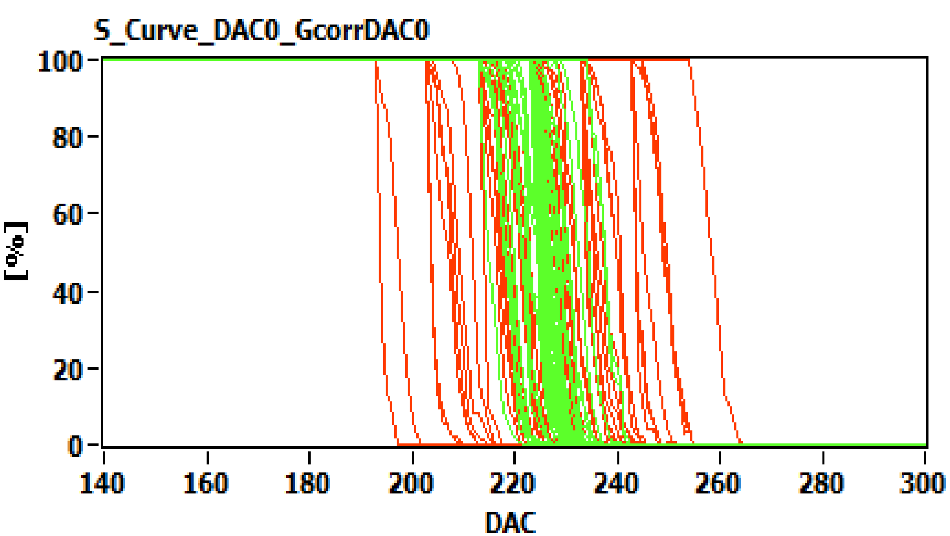
Dynamic range: 15fC - 50 pC

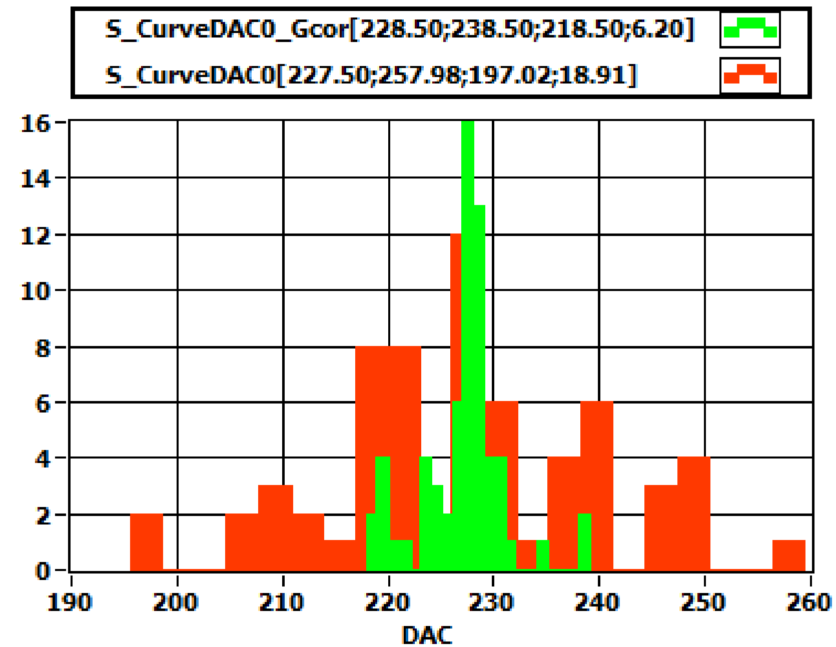
Laser engraving with a robot

H3B TESTED : 786
Yield : 83.3 %

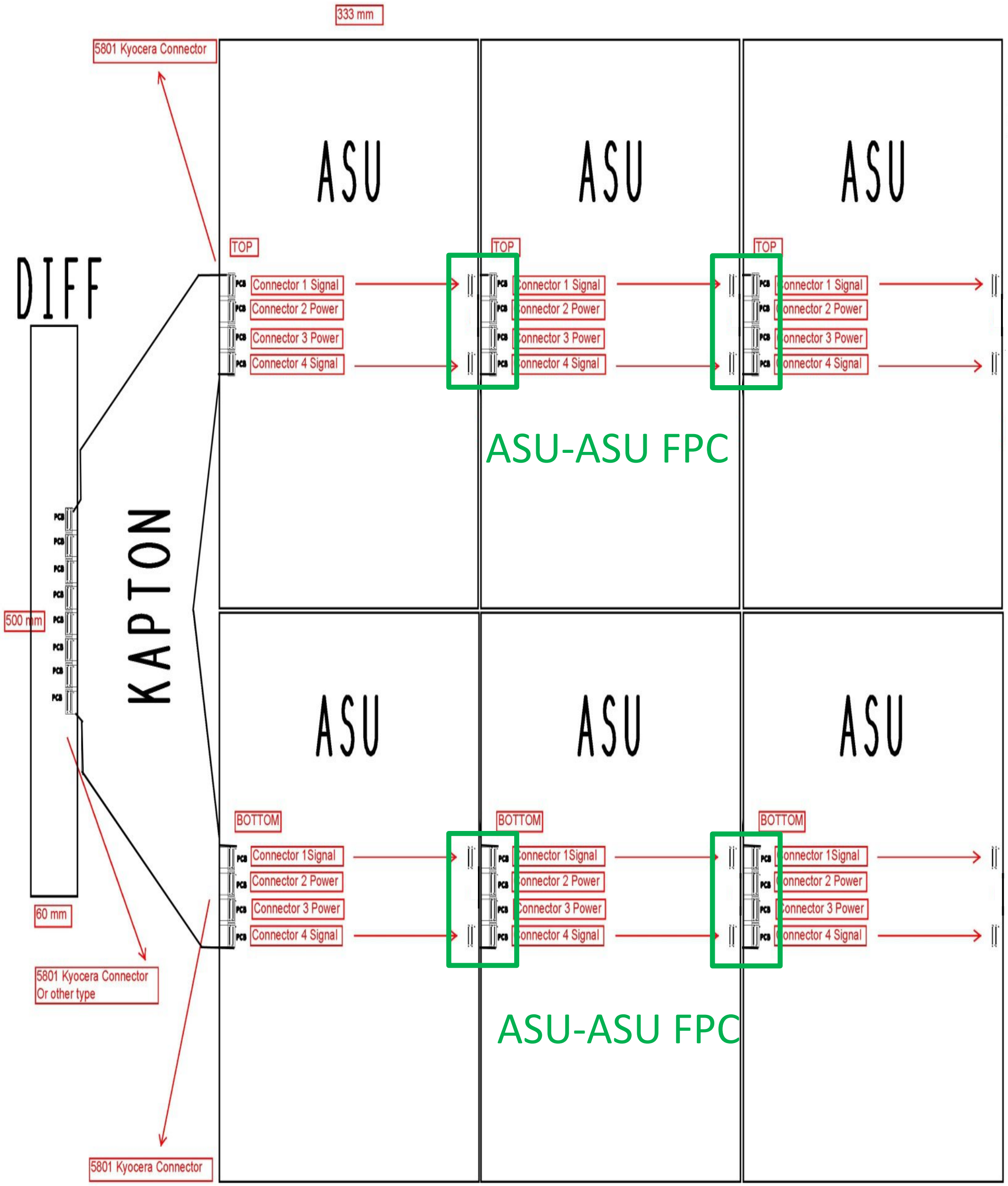
The majority of discharges :
Dead Channels

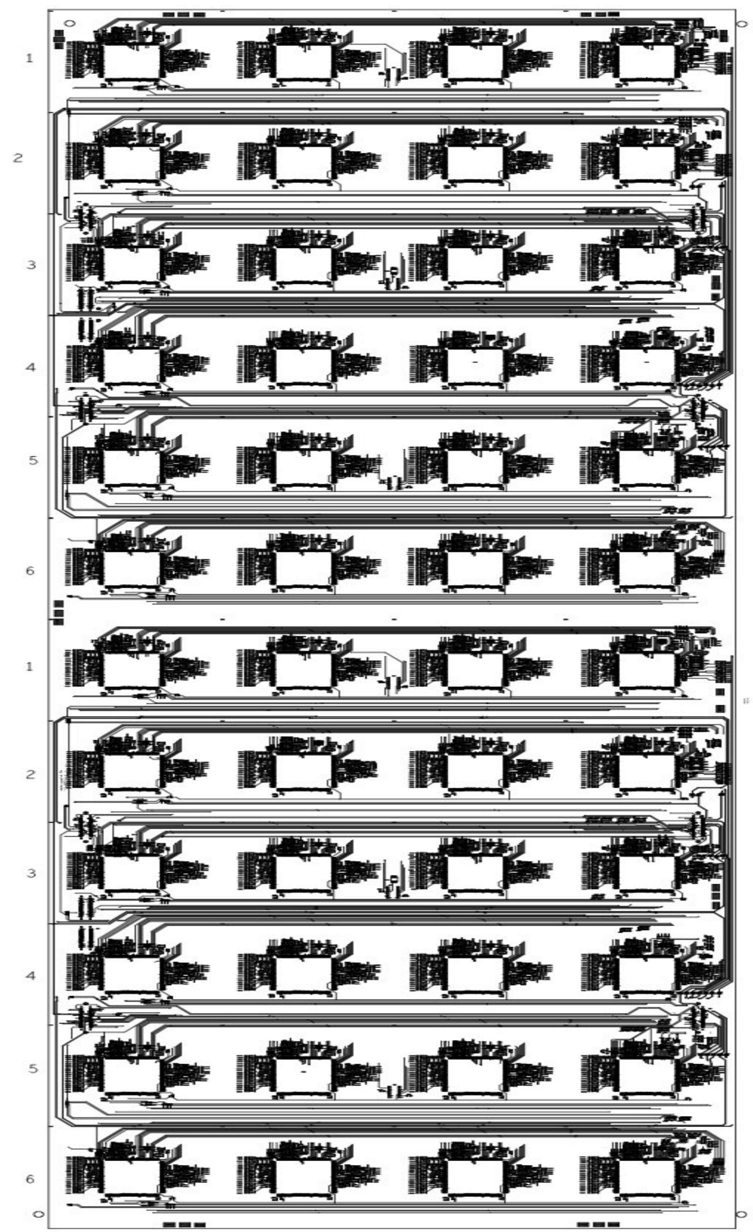
Injection : 100 mV on Ctest (64 Ch)
Gain = 144



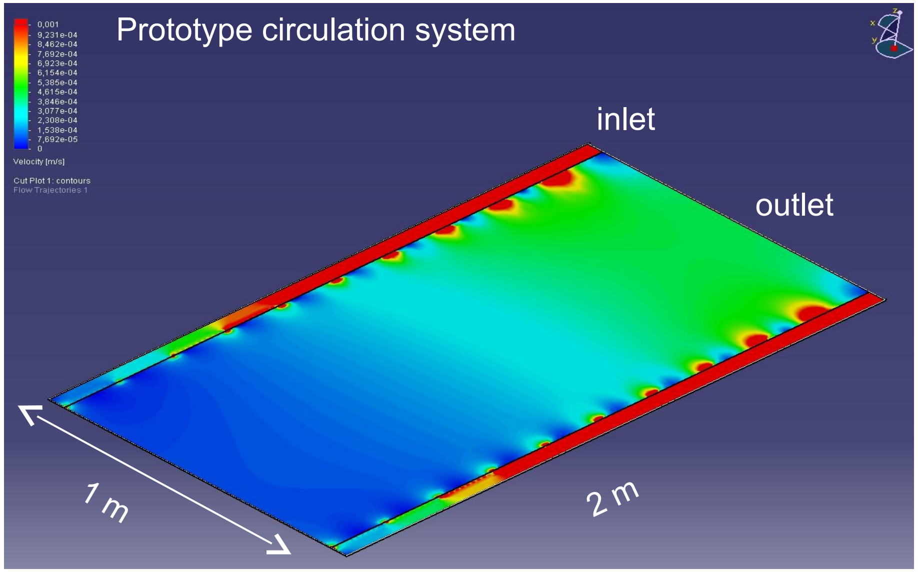


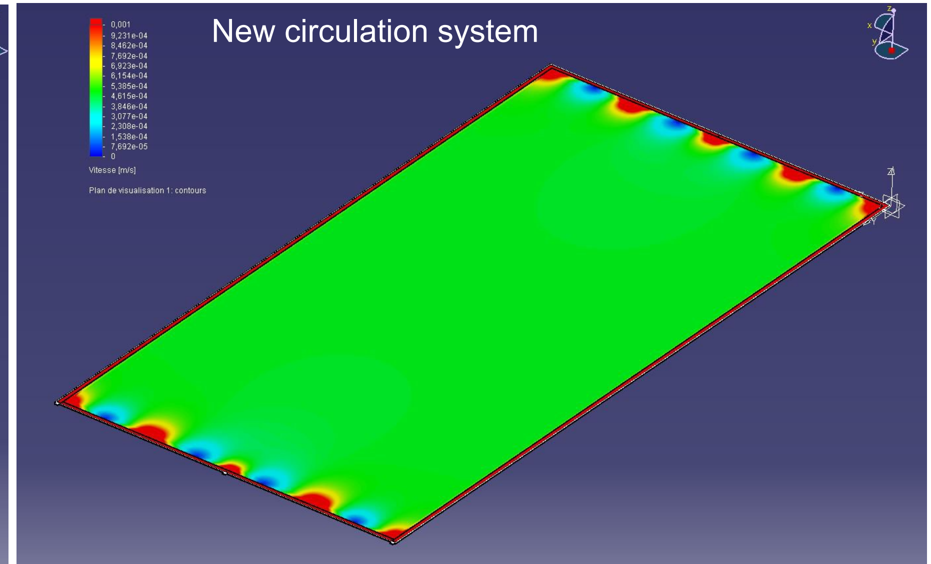
Large PCB of 100×33.3cm² design

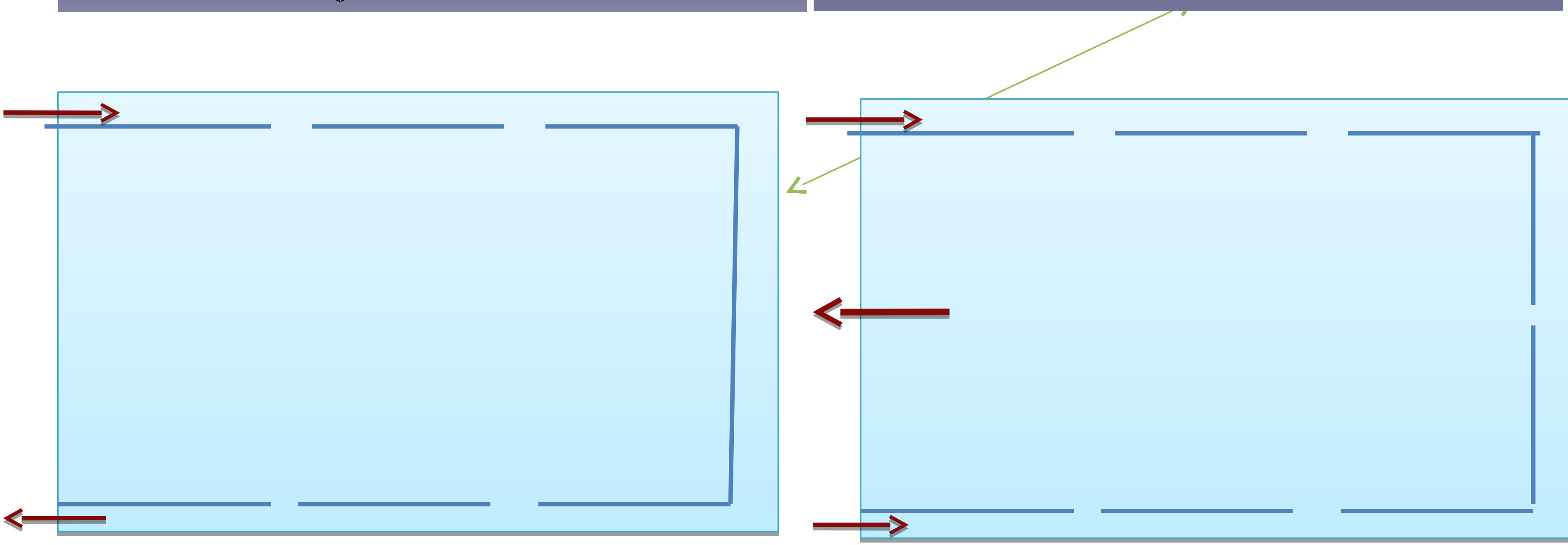


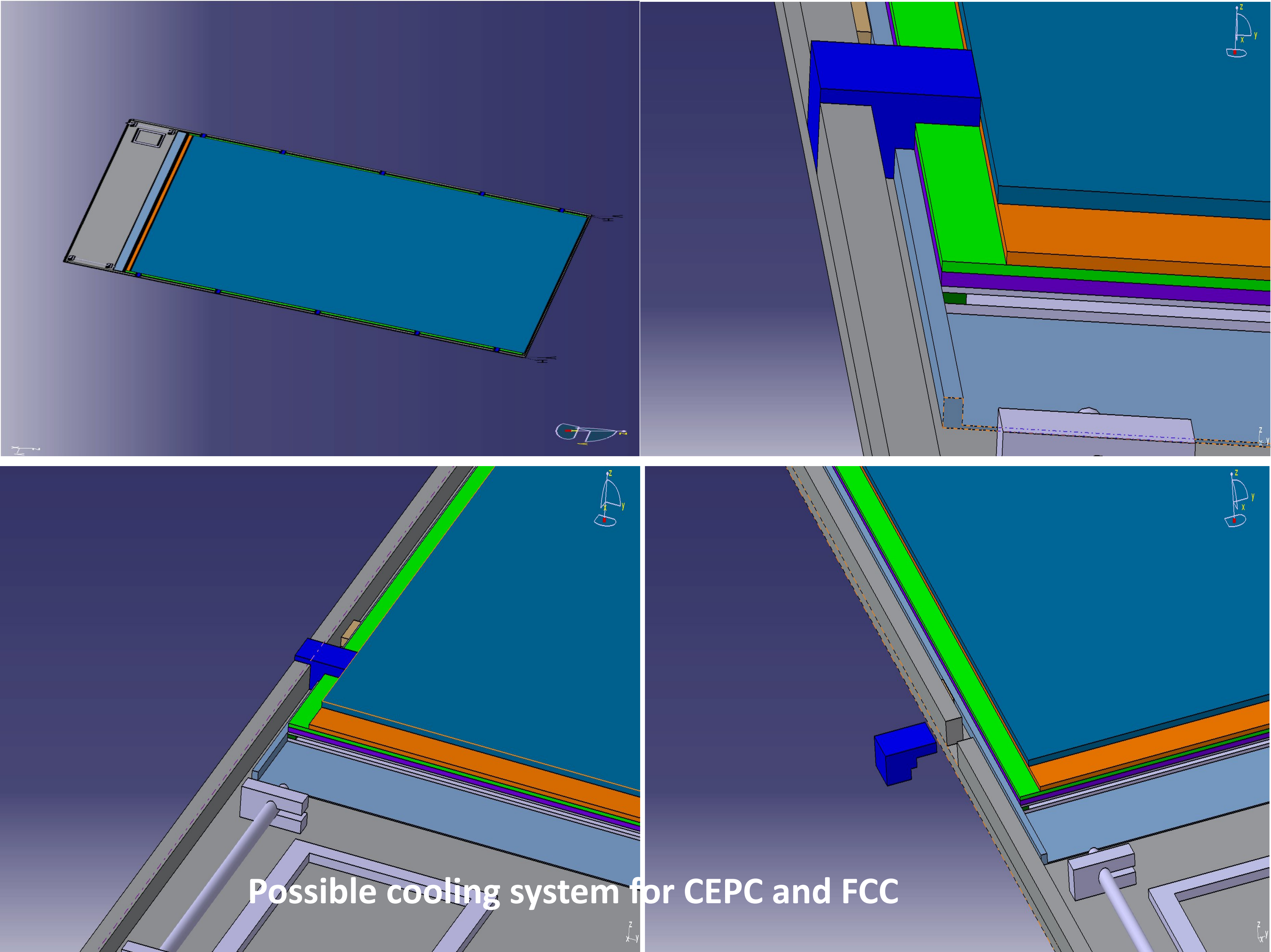


Detector conception : Single gap



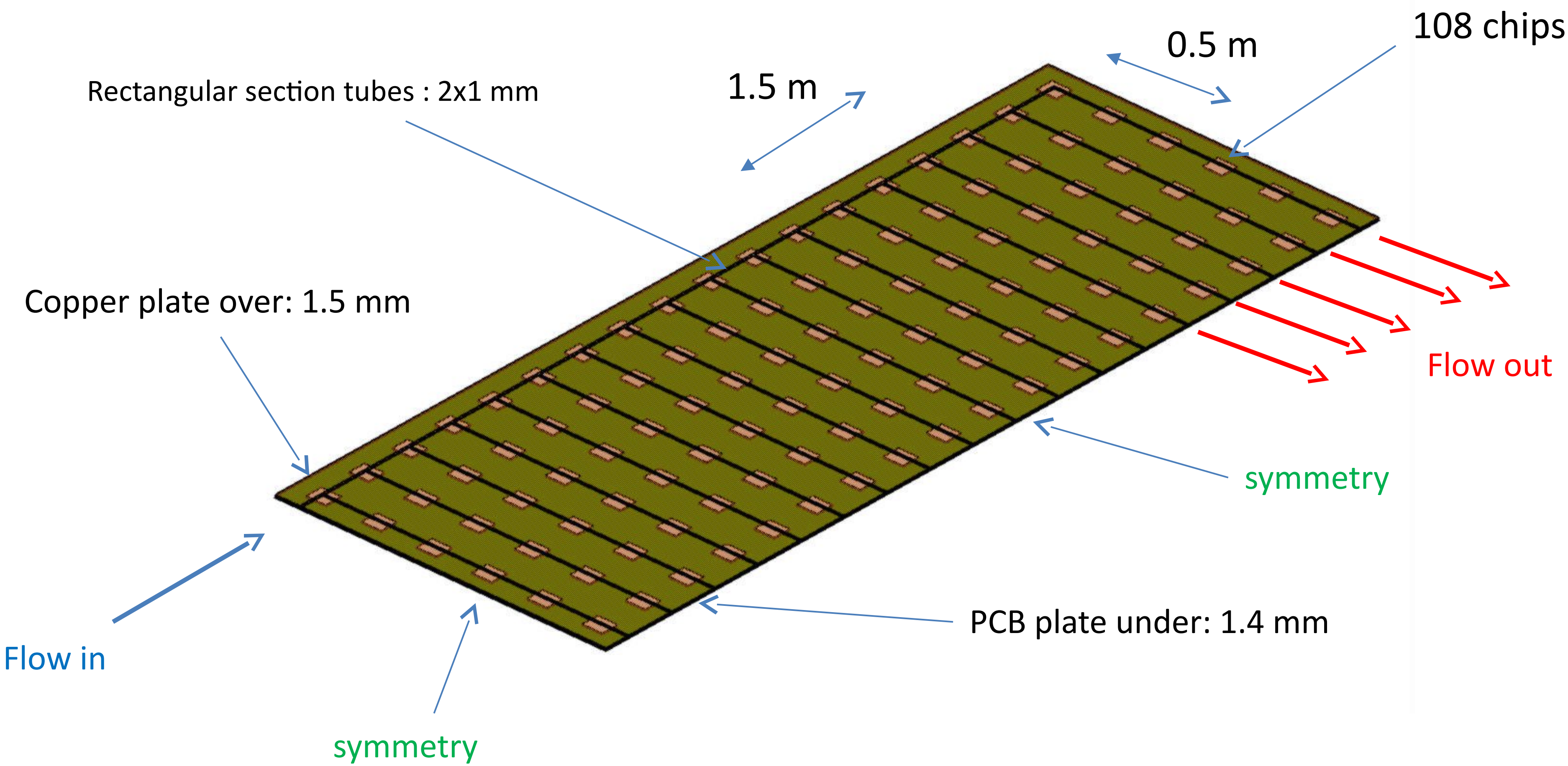






Possible cooling system for CEPC and FCC

Simulations thermiques GRPC 3m²

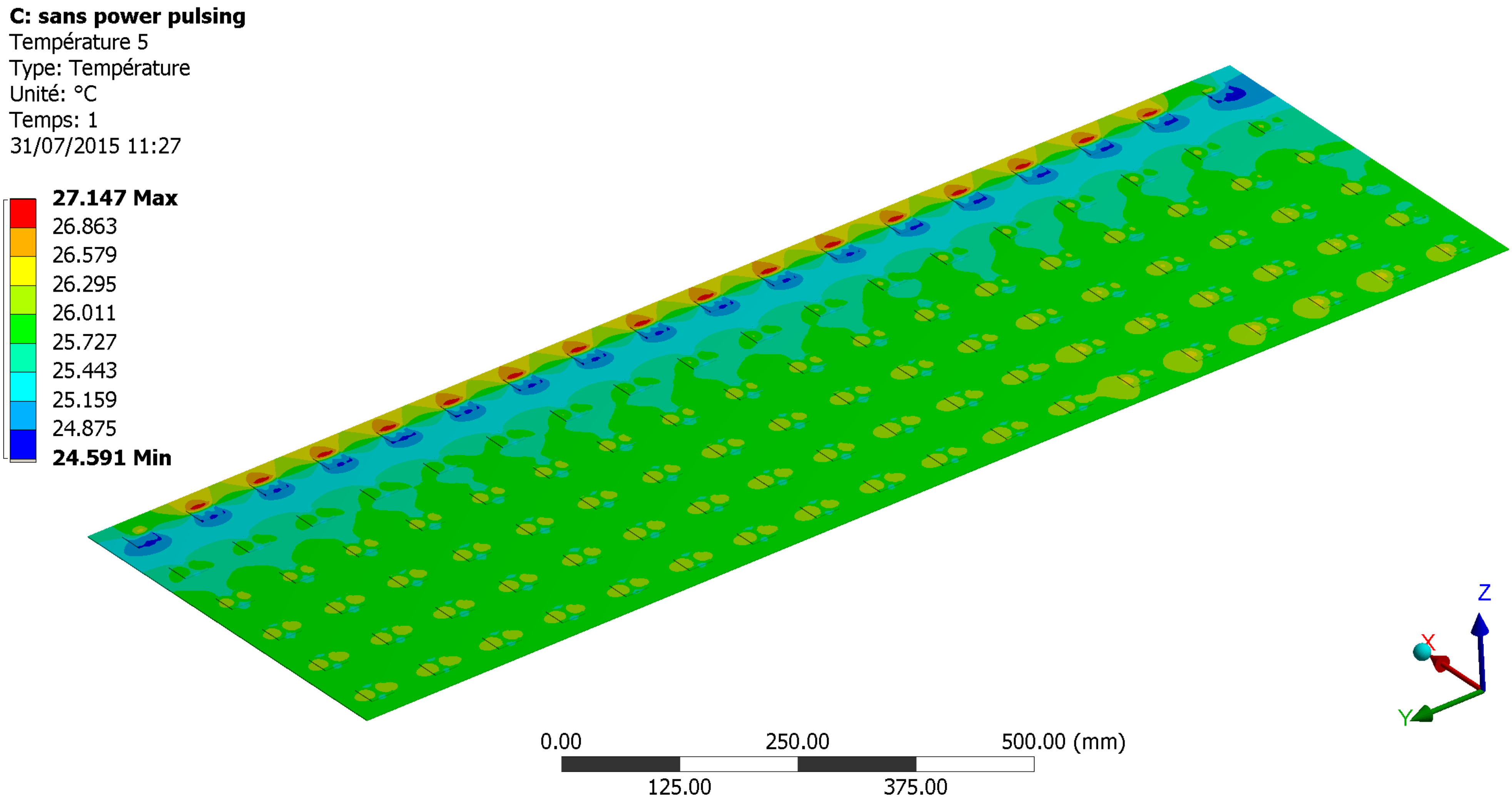


Water cooling : h = 10000 W/m²/k

thermical load : 0.8 mW/chips with power pulsing, 80 mW/chips without power pulsing

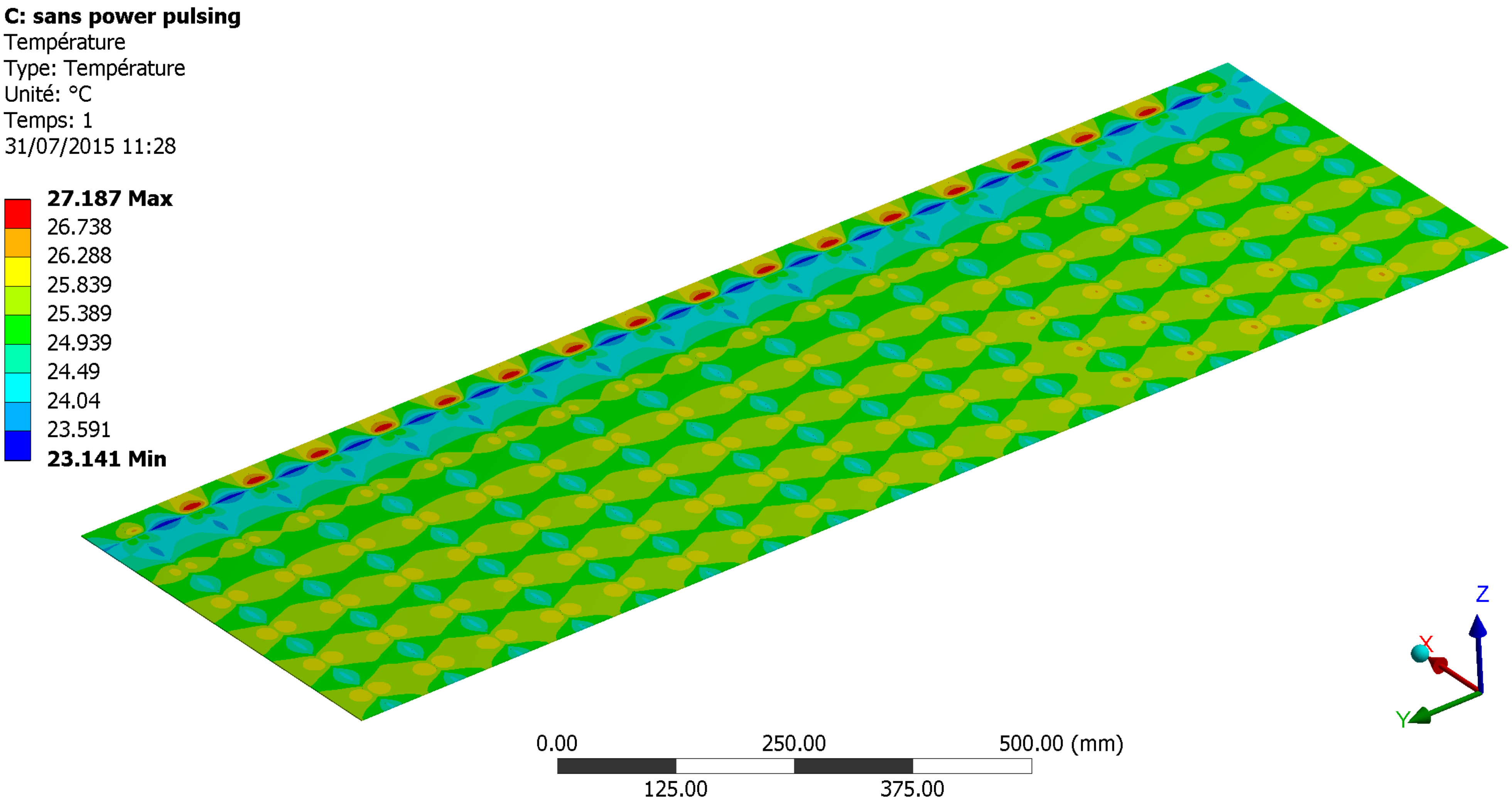
Simulation ¼ structure

Simulations thermiques GRPC 3m² without powerpulsing



Simulation ¼ structure pcb + chips

Simulations thermiques GRPC 3m² without powerpulsing

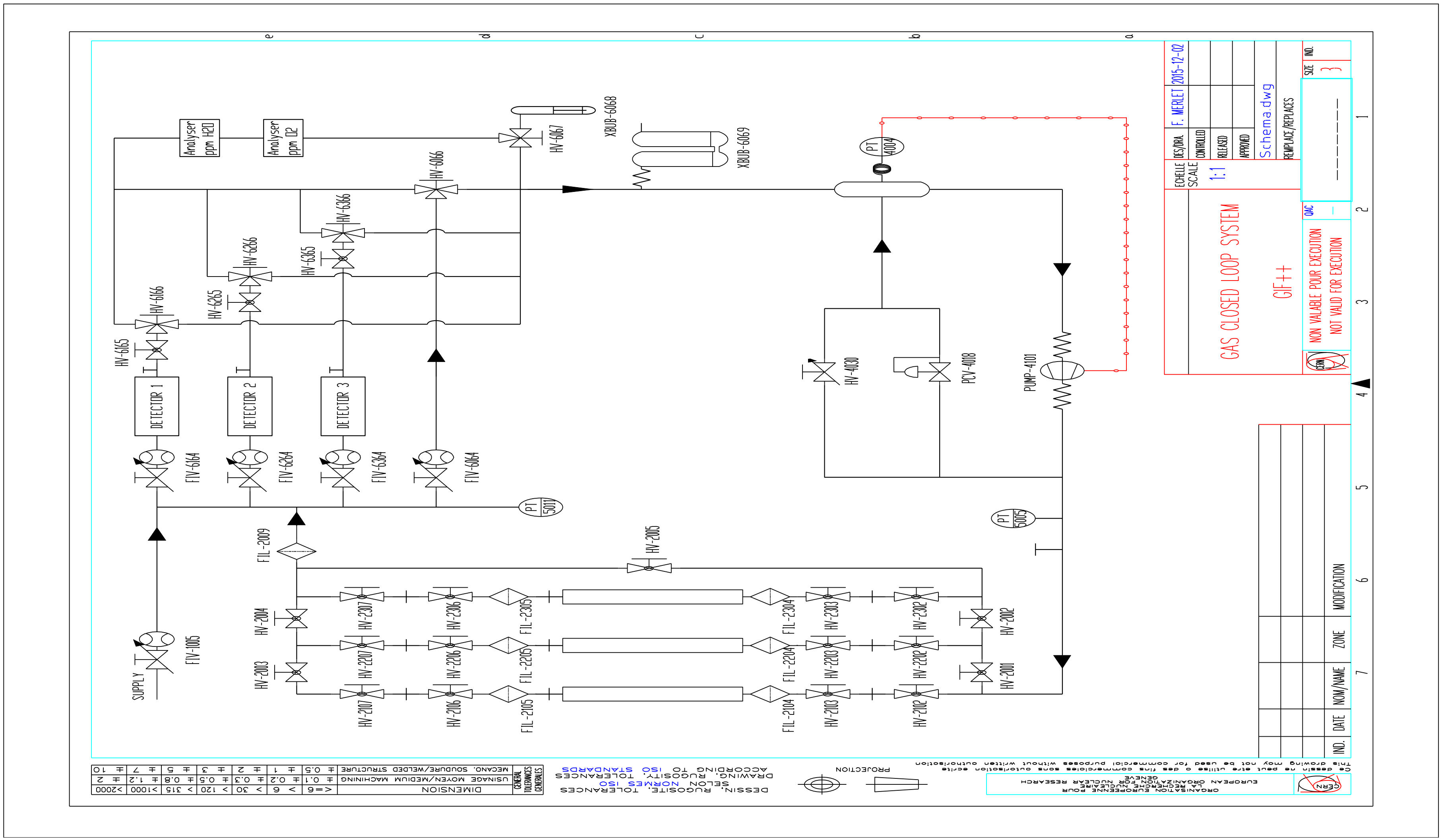


Simulation ¼ structure copper plate

Gas purifier

Goal: reduce the gas consumption to reduce the cost.

Gas renewal of 5-10% rather than 100%

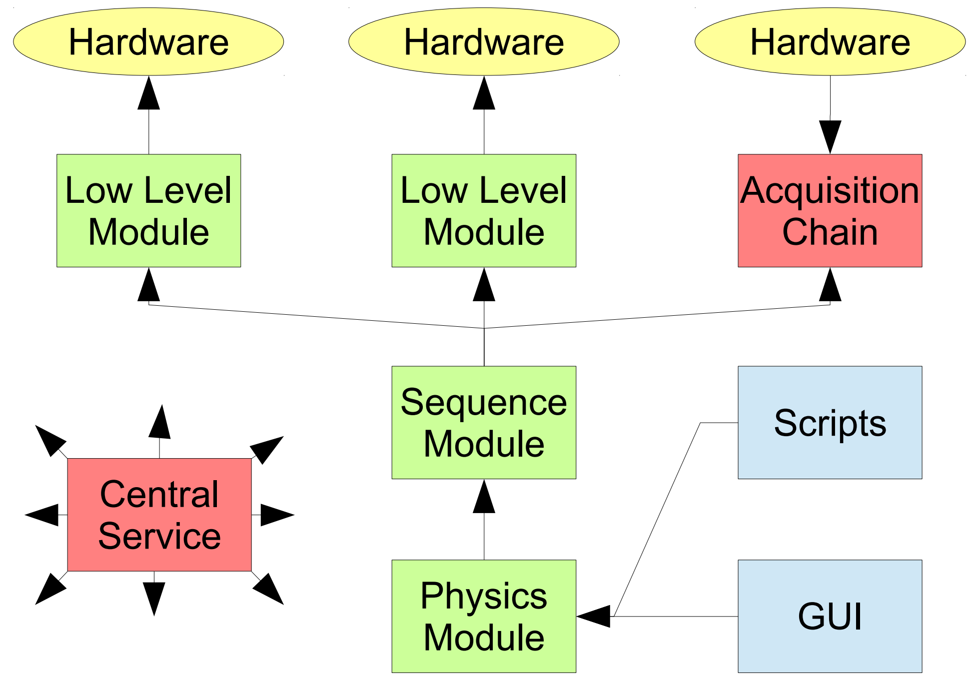


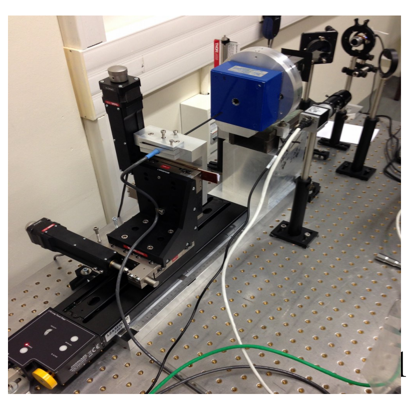

FIV-6064
FIV-6164
FIV-6264
FIV-6364
FIV-1005
HV-6066
HV-6166
HV-6366
PT4004
PT5011
H2O
PT atmo
PT5005
O2
SPARE
HV-2307
HV-2207
HV-2003

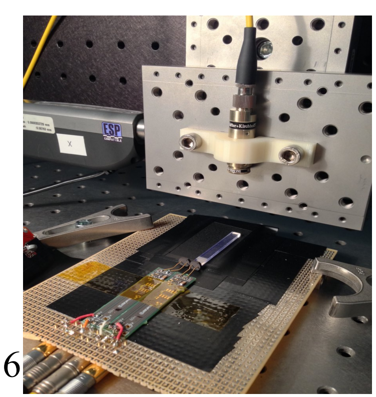
DAQ

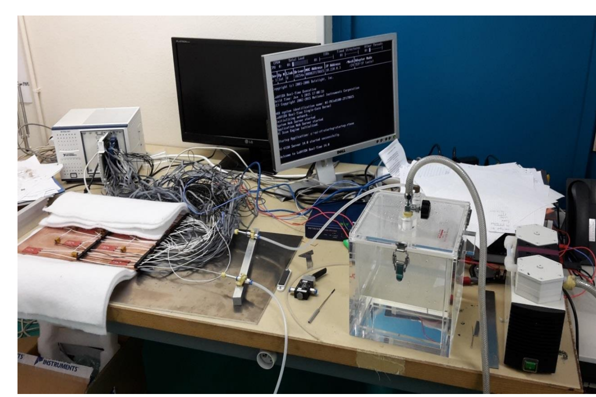
Pyrame online system for HEP

- Online Programming Framework
- High performance data acquisition and monitoring
- Distributed over TCP network
- Numerous hardware drivers
- Evolutive : from basic test-bench to real detectors
- Easily scriptable
- Multiple language and SCADA bindings









http://llr.in2p3.fr/sites/pyrame/

Frédéric Magniette, Miguel Rubio-Roy, Floris Thiant

DAQ activities
from SDHCAL

Implementation of a GBT based communication for Roc chips

- GBT CERN standard aims at Fast Timing Distribution, Data link, and bidirectionnal Slow Control

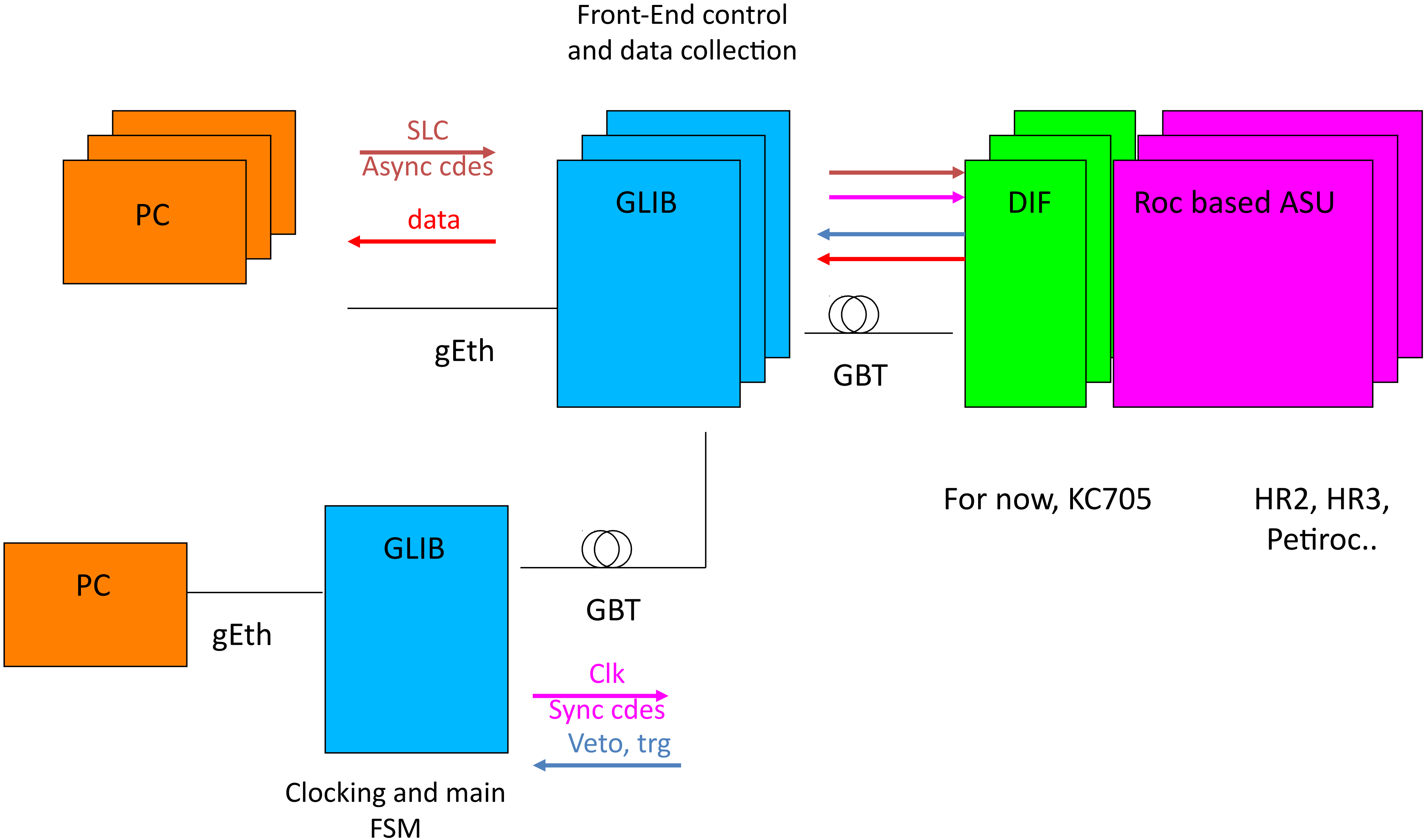
Primary design for Hardroc 2 & 3, Petiroc

- But easily adaptable to any Roc chip

Hardware platform : DIF2 (CIEMAT) when available, Glib(CMS) or Xilinx KC705 development board before

Goals : ILC SDHCAL (LP GBT) and CMS Muon chambers (LP GBT or full GBT)

Global system architecture



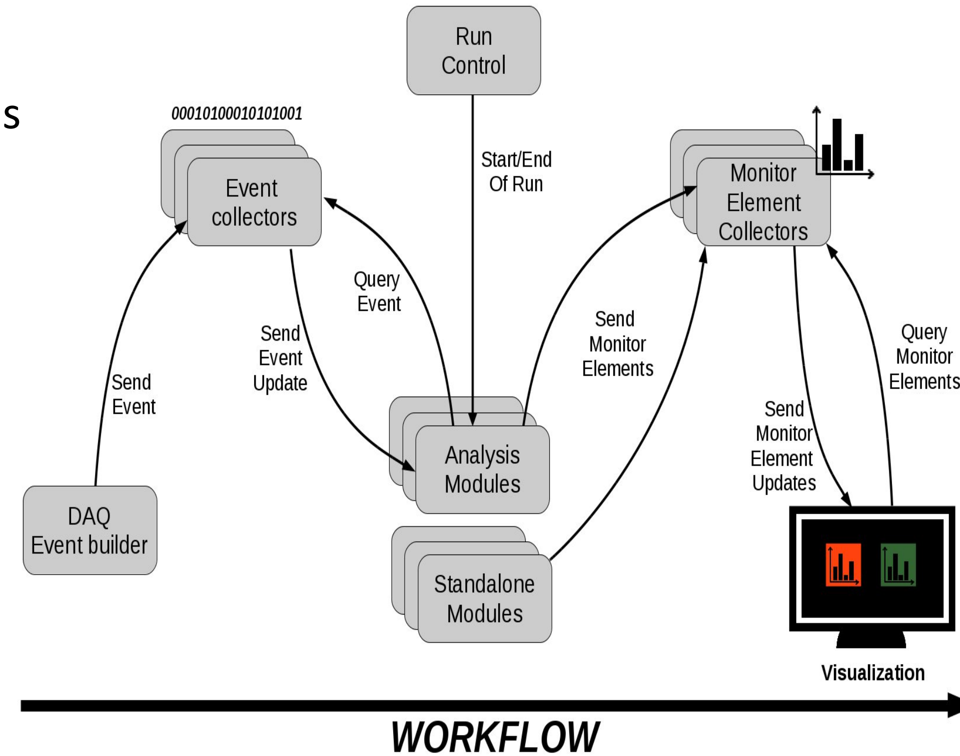
DQM4HEP

Data Quality Monitoring for High Energy Physics

This is a generic C++ framework to perform online data analysis and data quality report. It deals with online application workflow, inter-process communication and memory management.

Main features :

-Event distributed system (client / server architecture)
-Set of user interfaces designed for data quality analysis
-Monitor element distributed system
-Graphical user interface for data visualisation (Qt Gui)
-Large scale remote process management
-Generic IO support for different experiment
-Designed for simple prototype monitoring up to complex systems like ILD or LHC detectors
-Logbook interface (ELog)



Combined beam test SiW-ECAL & SDHCAL

→ First combined tests of two technological prototypes
→ First attempt to have a common DAQ system
→ Use of a common framework to control and to collect data (EuDAQ if possible otherwise SDHCAL or ECAL based DAQ)

First attempt to run SDHCAL with one SiW slab is very promising. Some problems found and solved or being solved.

A slot of **two weeks was allocated but in June**. Discussion with SPS coordinator and CMS to have the TB in September or October so more SiW-ECAL slabs could be available.

Goal : test of HW in common conditions, of PFA

What next ?

Test of PFA's

ECAL standalone

- separation of showers studies (γ's, e's) ⇒ tracking in front ?
  - e+γ beam (thick target with a magnet in front ~10 m)

ECAL + HCAL

- **SW** superposition of showers γ/e + h
- **Physical** superposition of showers (h+γ ?)

Test of PFA in B field

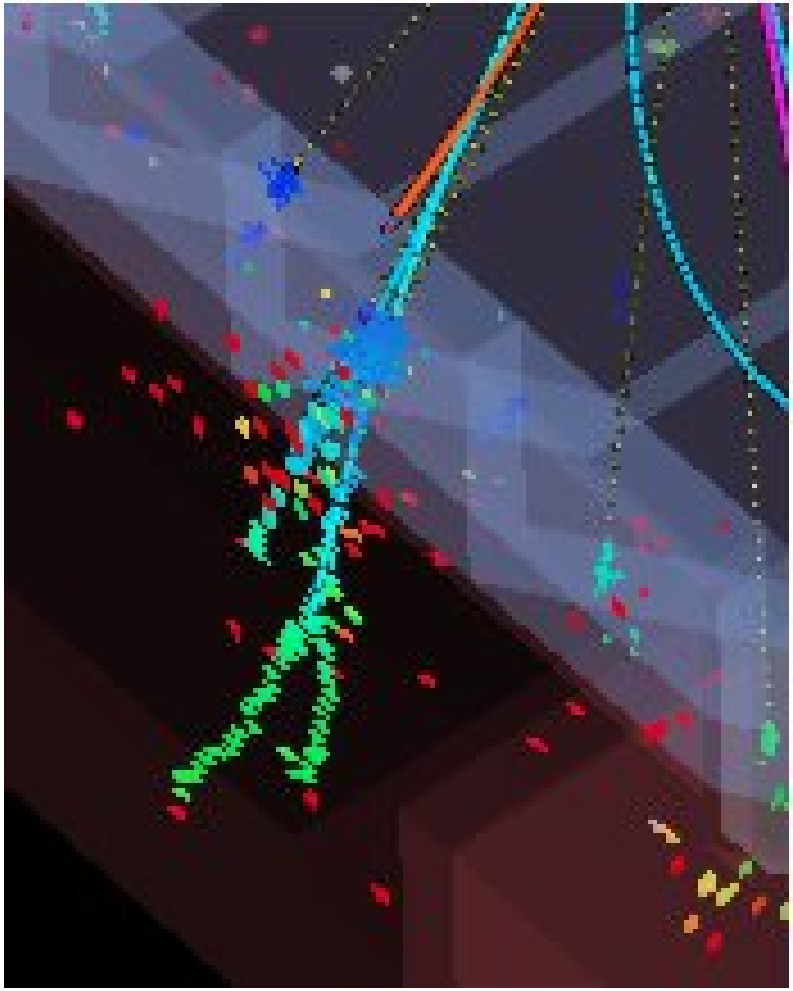
- Tracking,
  B effect in RPC's (?)
  on mechanics with PP,

- ⇒ Reduction in size of the SHDCAL (last 10 layers) to fit in the M1 magnet in H2B ?
  - (~30 cm missing) ?

Timing ?

CMS-HGCAL and ATLAS-HGTD are investigating precise time for vertex separation

- 50ps timing precision for single cells
- ➘ ~10 ps for EM shower
- electronics (CEA / Omega) is being developped for this: distribution & FE



Benefits in terms of PFA ?

- Certainly in HCAL : ns enough ?

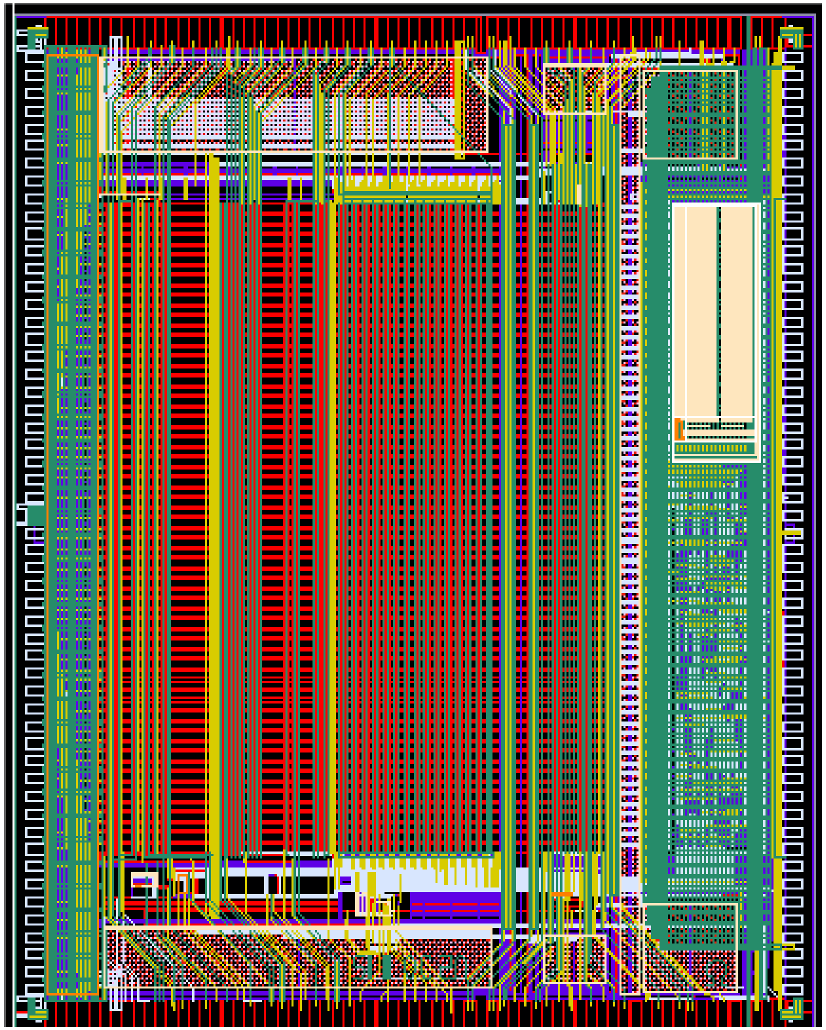
  in ECAL ? to be studied...

But do we have time (and ressources) for time ?

Thank you

SKYROC2-CMS

- **SKIROC2-CMS chip submitted mid-January**
  - Expect chips back in ~ 3 months
    - 400 chips
    - **Available for Fall test-beams at CERN**
    - Also 400 chips of SKIROC2_CALICE
    - 50 chips assembled in BGA (e-tests)



- **Modified to include “HGC-like” front end**
  - ~20ns shaping time and 40MHz sampling
  - ADC + TOA(~50ps) + TOT
  - P-on-N and N-on-P read-out options