DAQ(s) pour le Semi-Digital Gas HCAL & développements ILD

Vincent Boudry

SOCLE'08

8-9 décembre 2008
LAPP Annecy

ÉCOLE POLYTECHNIQUE

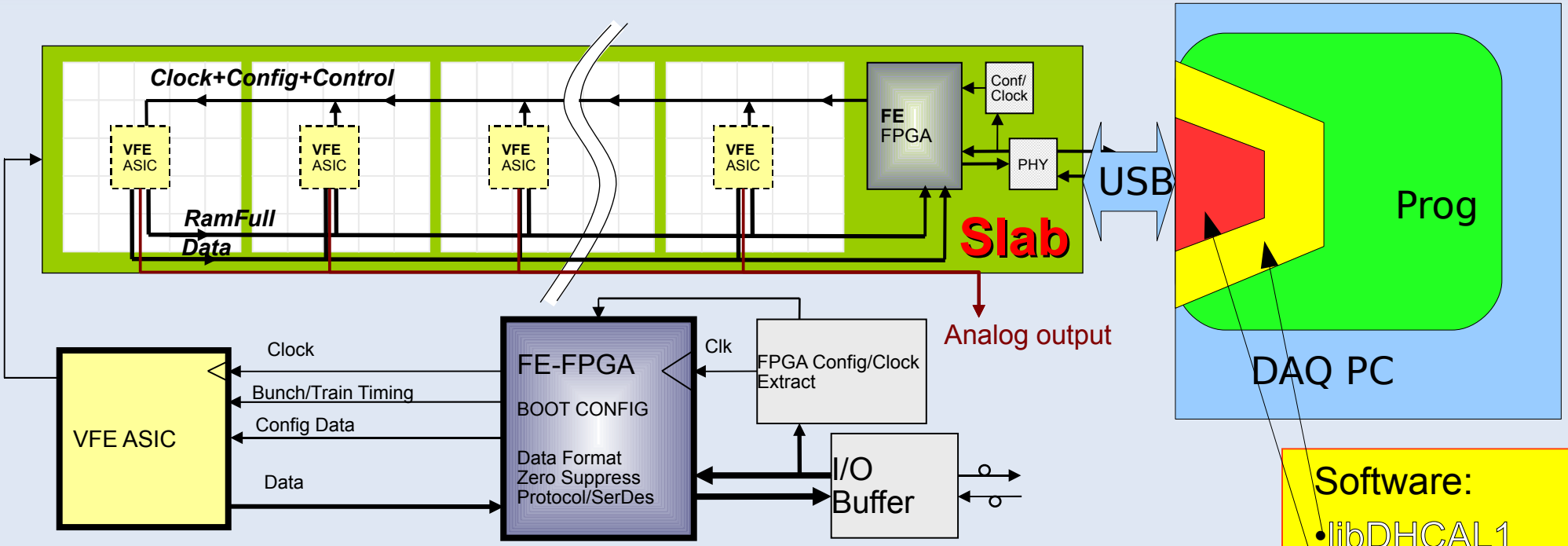
Synoptique

- DAQ TB Mini-DHCAL
  - Premières analyses de l'électronique en faisceau
  - Analyses « bas niveau » de trains de données
- DAQ pour le m^2
- DAQ pour le m^3
- Simulation & Intégration dans l'ILD

Testing Embedded electronics

- 1 m²
  - 10k channels
- 1 m³ (40 layers)
  - 400k channels

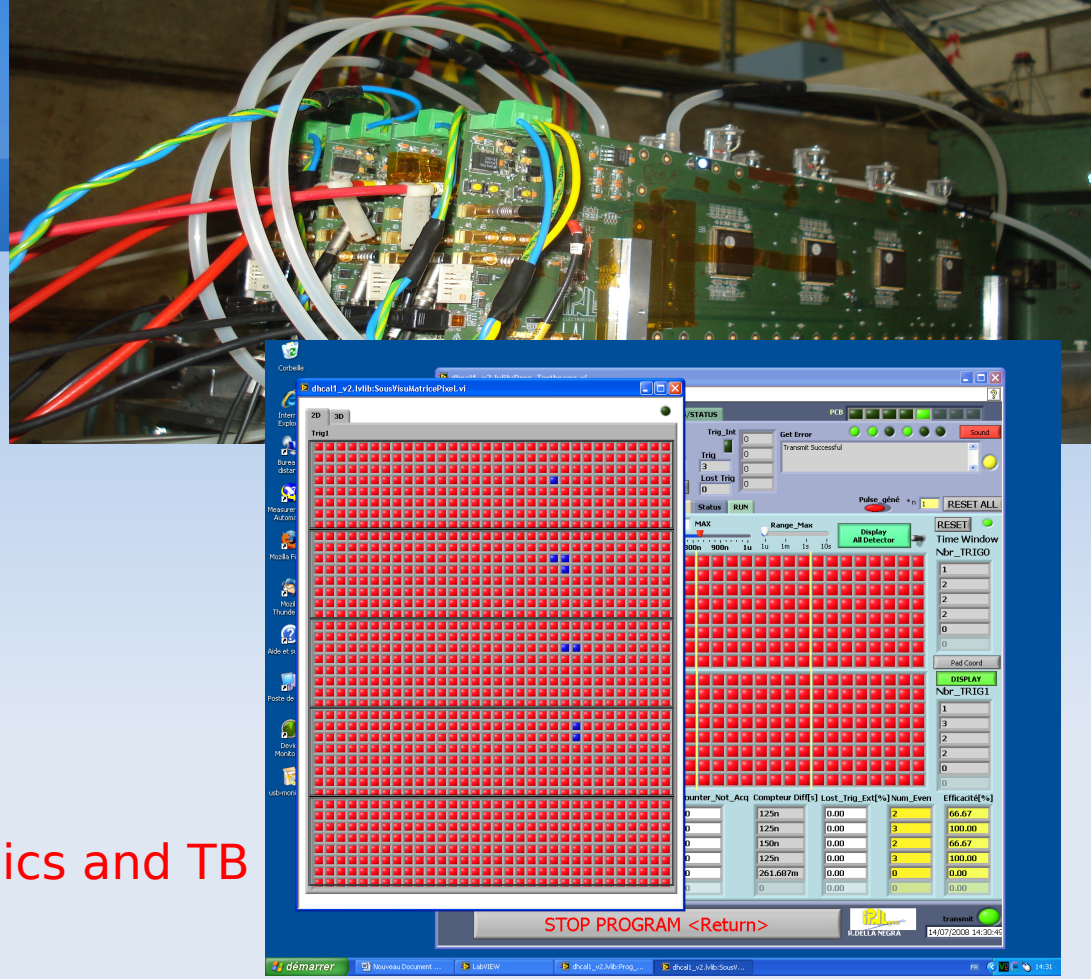
- Embedded Readout chips
  - 64 channels
- Daisy Chained
  - Control & readout



FirmWare: Comm FPGA ↔ HR, Gestion ACQ, Comm USB

Software:
- libDHCAL1
- **Driver USB**

Data taking (DAQ)



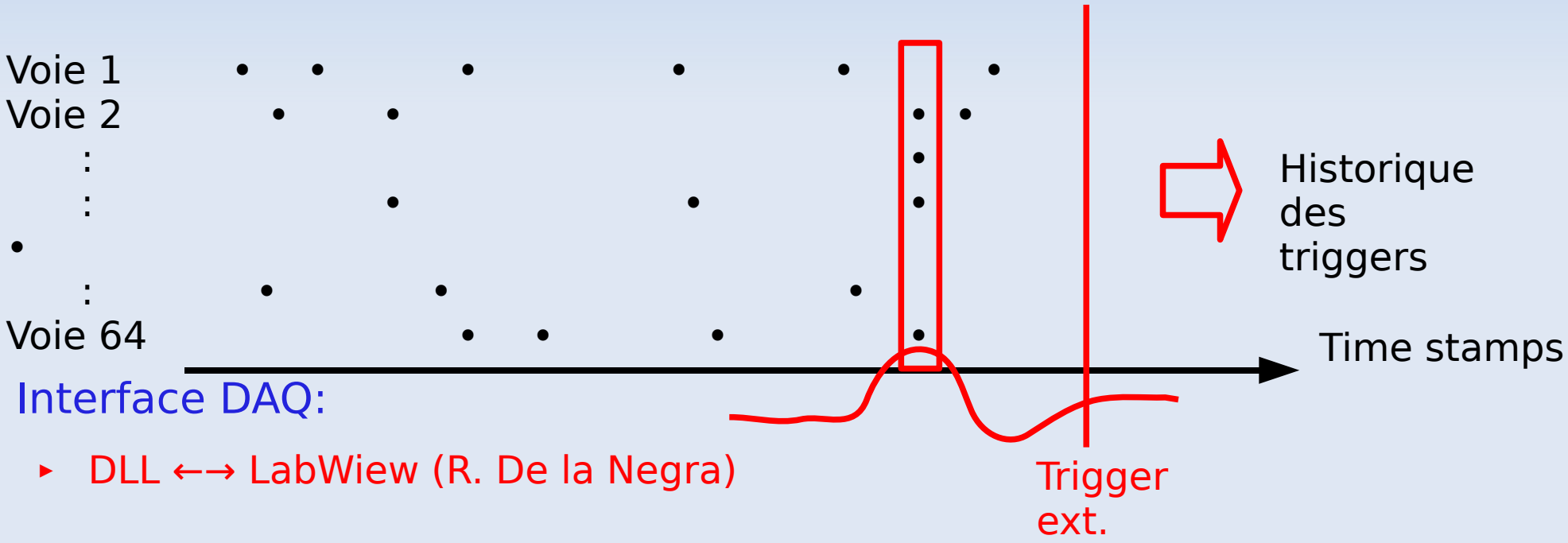
- CERN PS: **400 ms** spills every 48 or 33s (day/night cycles).
  - low multiplicity: low part. density, mostly punch through π's
- 3-5 Cartes “DHCAL1”
  - 4 HardRocs managed by 1 FPGA
  - “Debug card & DAQ” used for cosmics and TB
- USB readout: LabView (**R. Della Negra**) + libDhcal (**C. Jauffret**)
  - asynchroneously RO of all cards (”LabView thread”)
- Running mode: **single event with auto trig** + BUSY logic & automatic RAMFULL recovery (⊃ BUSY signal)
  - Acquisition rates: 5-20 Hz

Soutenance de thèse le 22 décembre au LLR

Dev^t de la DAQ-FE (suite)

Socle 2007

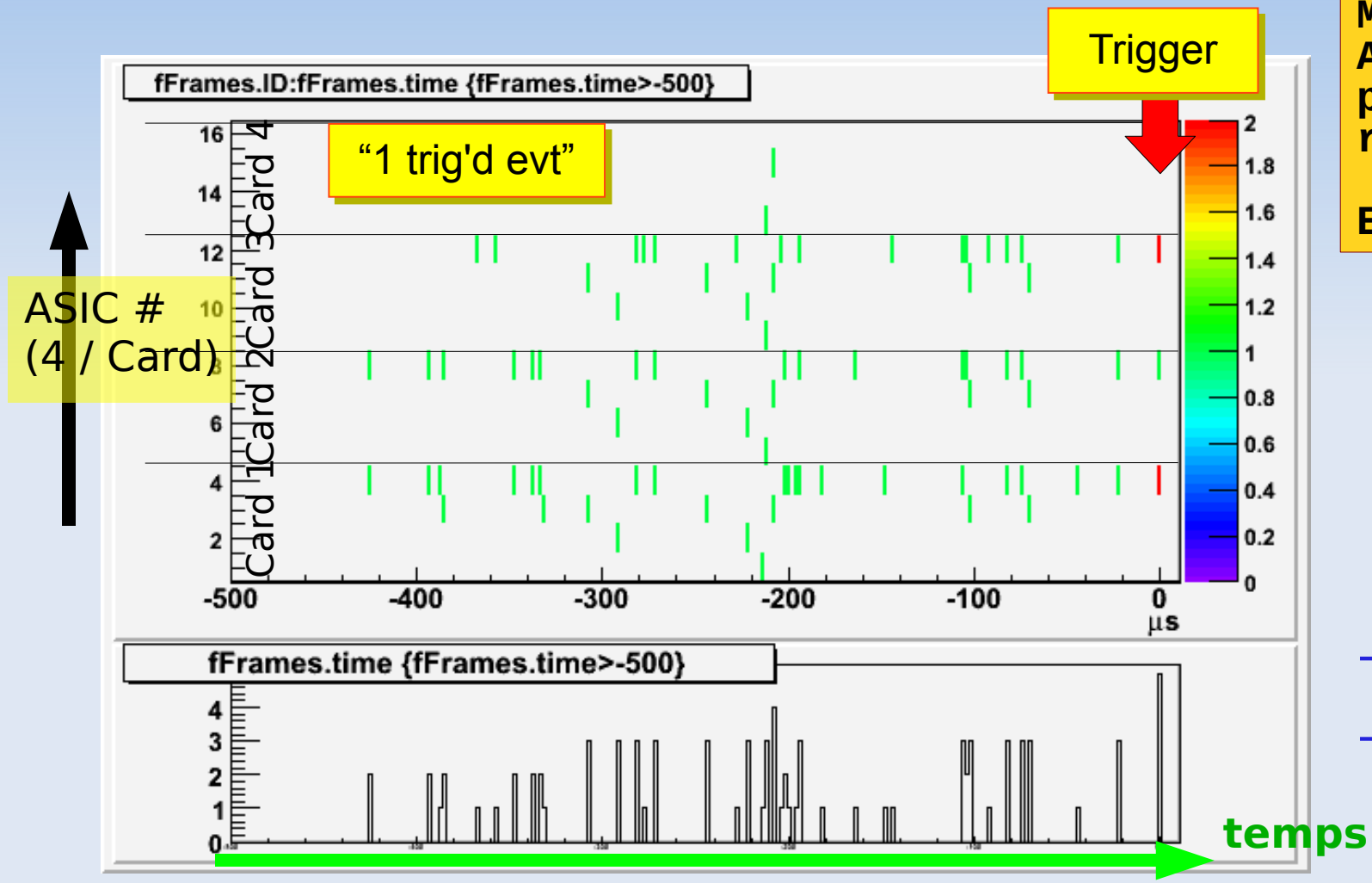
- Lecture numérique
  - Jusqu'à 128(-1) trigger par chip avec timestamp
  - Pour TB & cosmique: ref. donnée par trigger externe



- Interface DAQ:
  - DLL ←→ LabWiew (R. De la Negra)

Maintenant réalisé

Histoire d'un évènement



Many More stat Available with proper time reconstruction

Expt'd: (30

- 2 "lots" de données
  - Triggées
  - Mémorisées "ILC like"

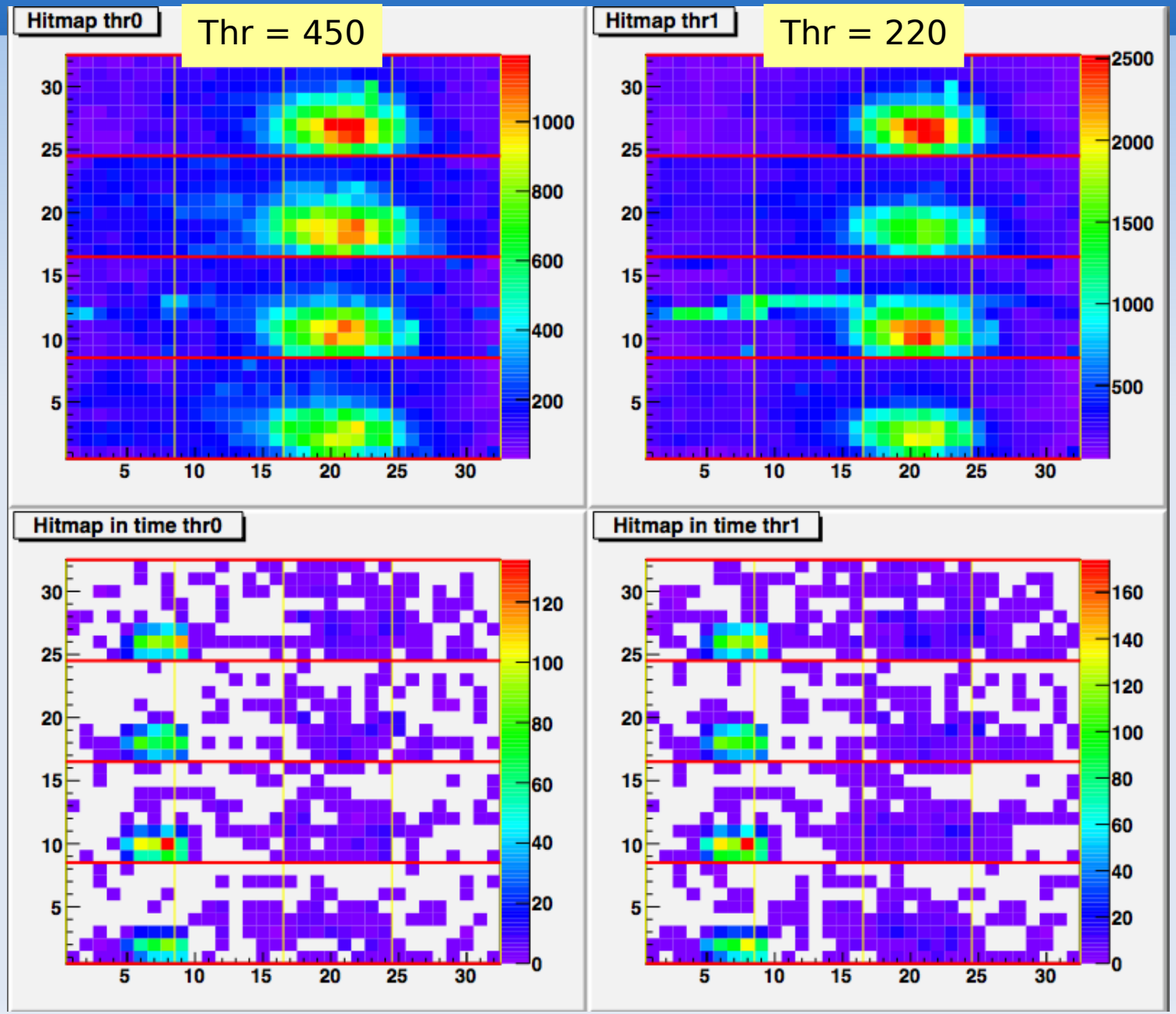
→ Historique

→ Conditions physiques

ICI Synchronisation sur le trigger ext. →

time = (BC-LastBC) × τBC – DiffCounter × τDiffCounter

Lots de données trig vs mem

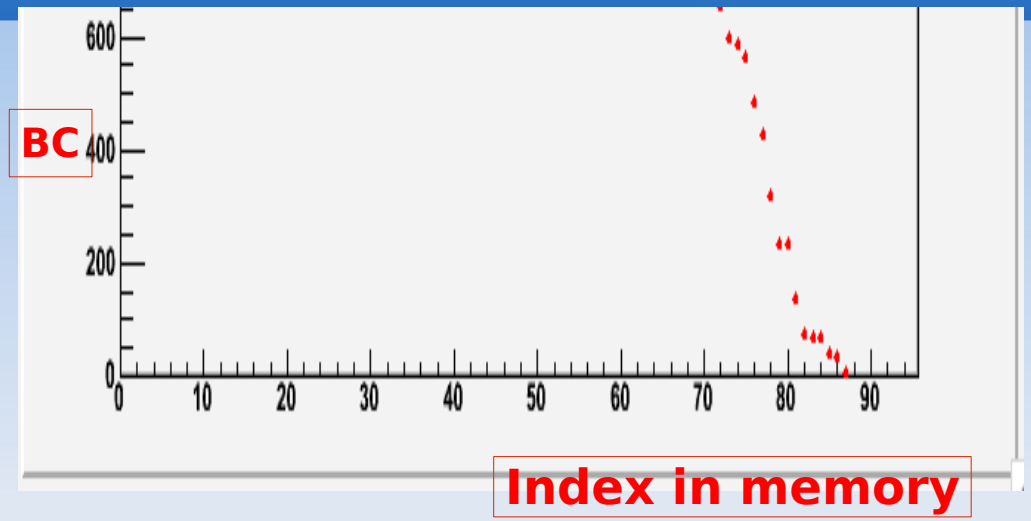


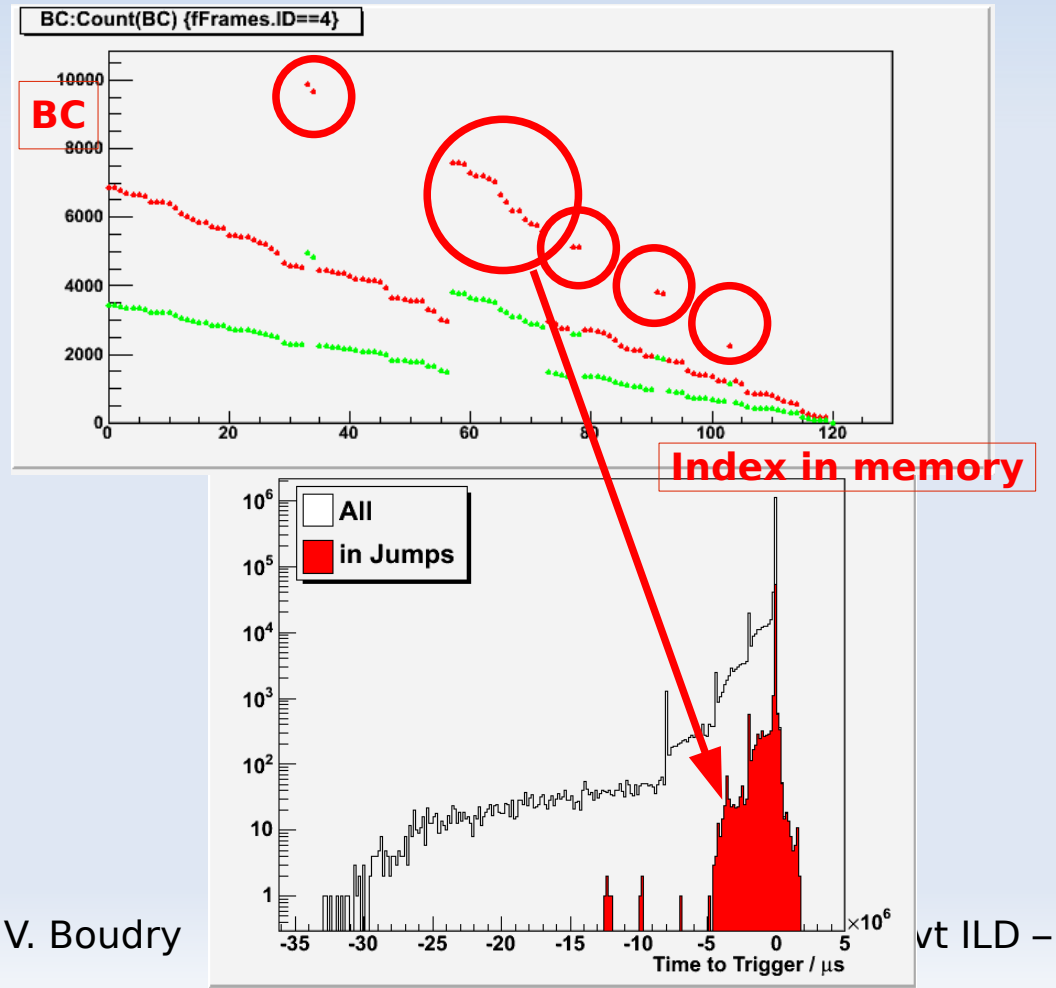
All Events

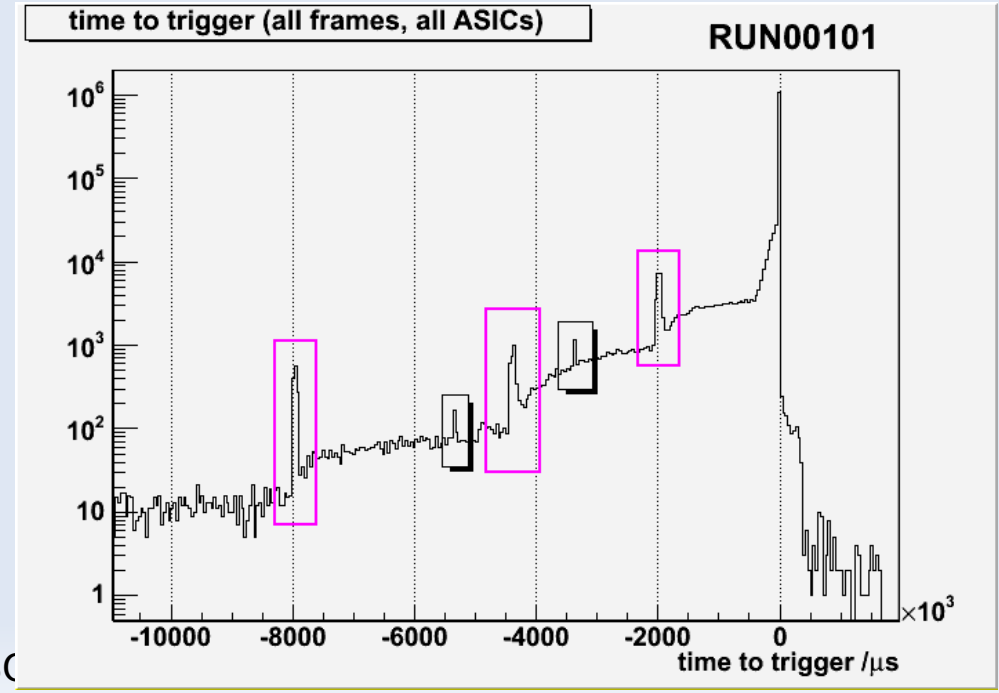
in time
With ext.
trigger

Reconstruction du temps

- BC + sync → temps
  - Dépassement du compteur 24bits (~ 3s)
  - Timing jumps observed (1%) evts







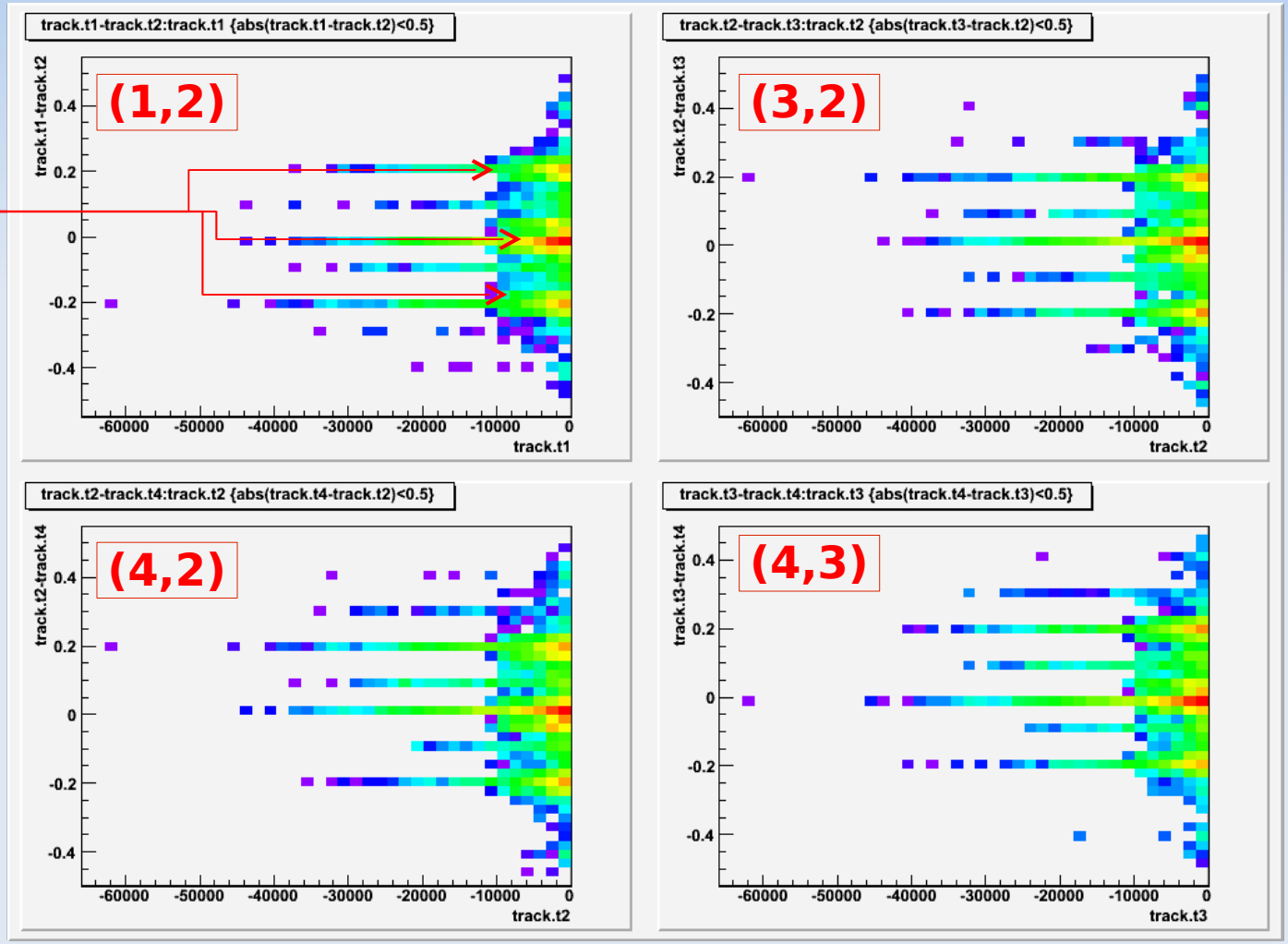
Calibration en temps

Corrélation en temps entre les différents ASICs

Pics à ±200ns (et ±100ns)

Intercalibration inter-carte:

$\delta f/f \leq 0.5$ ppm



Δt (ASICs)

Khaled Belkadhi

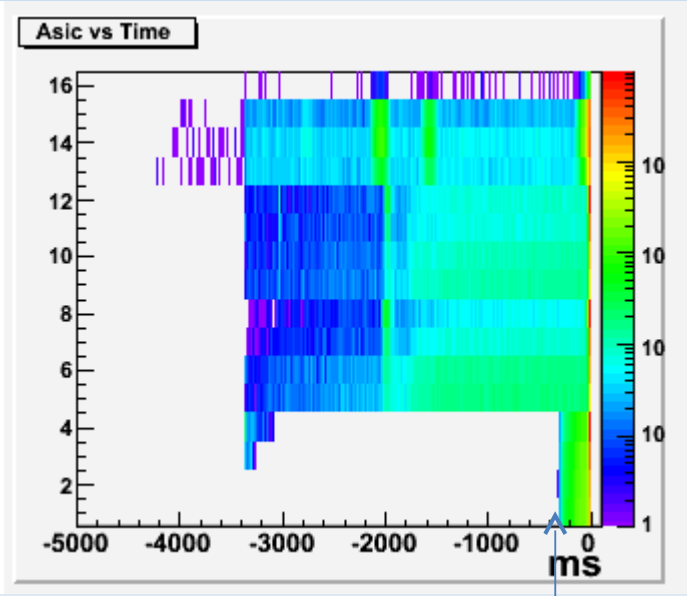
Time → trigger/ µs

Efficacité avec evts memorisés

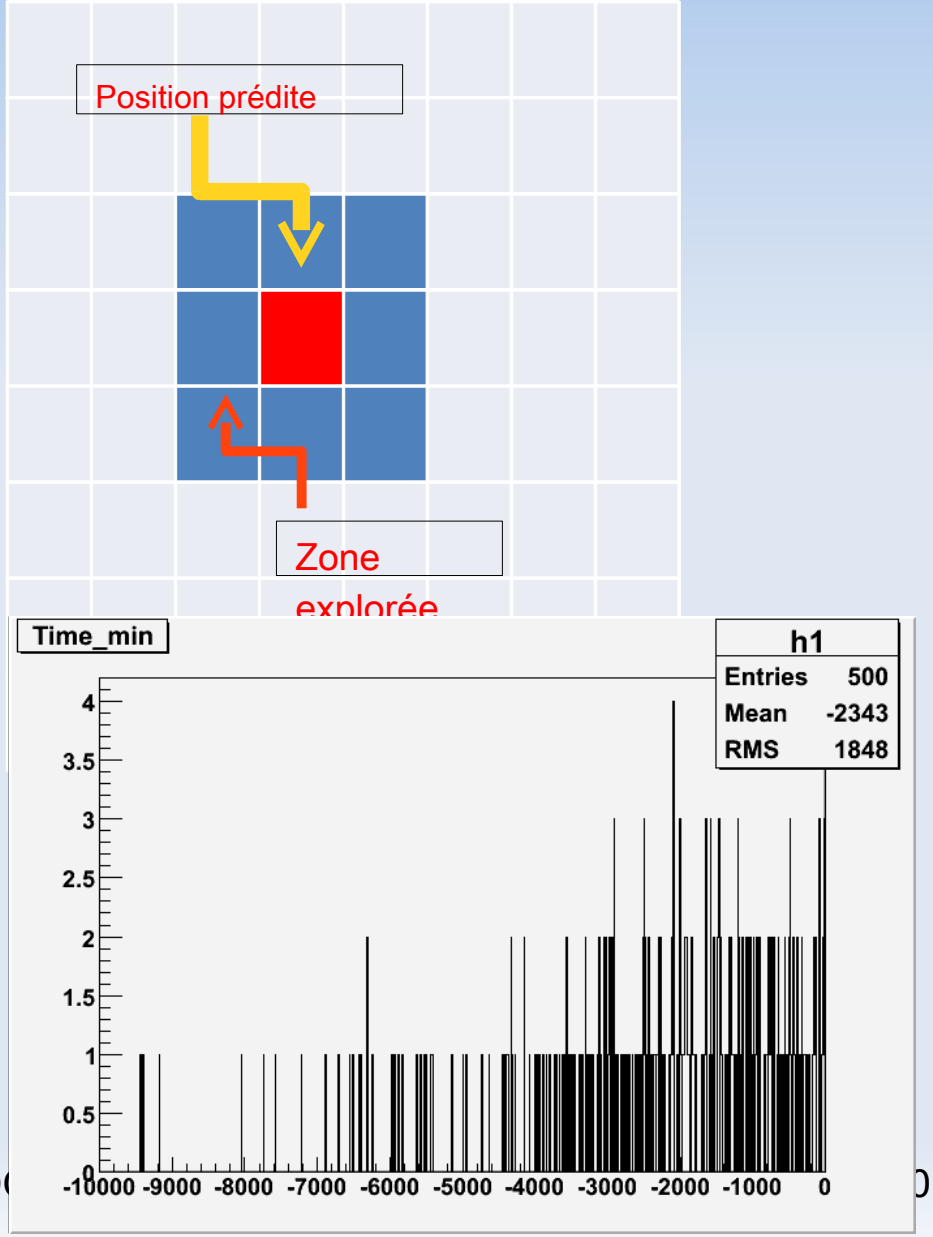
1ère reconstruction d'évt en train de « type ILC »

Sélection en position: ±1 pad en X et Y.

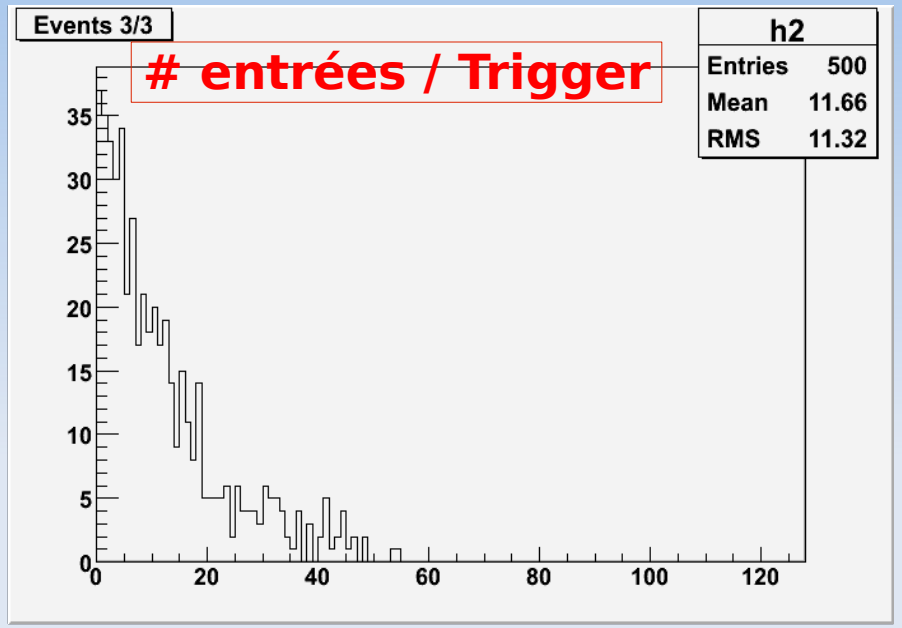
Sélection en temps:
- δt< 5%
- disponibilité des cartes.

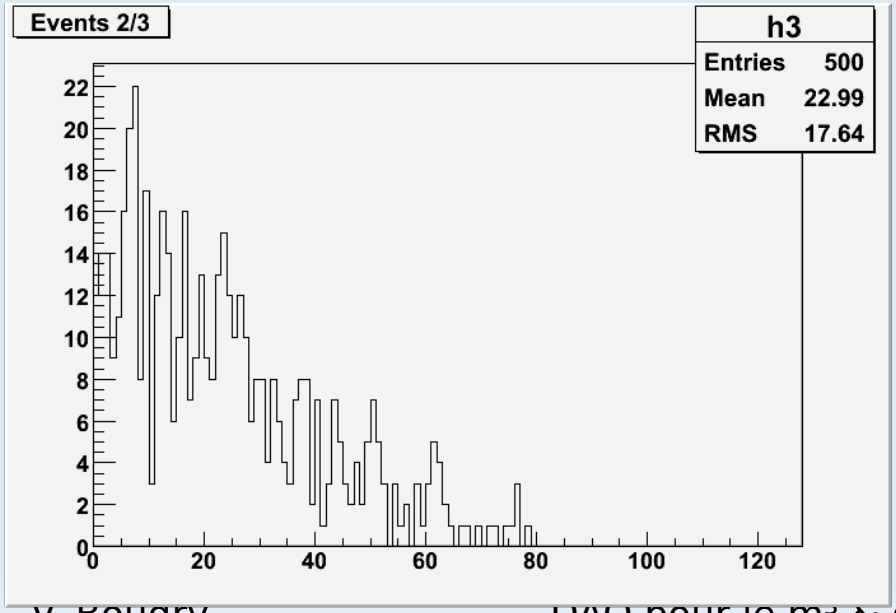


Temps de référence pour la dernière carte



Efficacité avec evt mémorisés

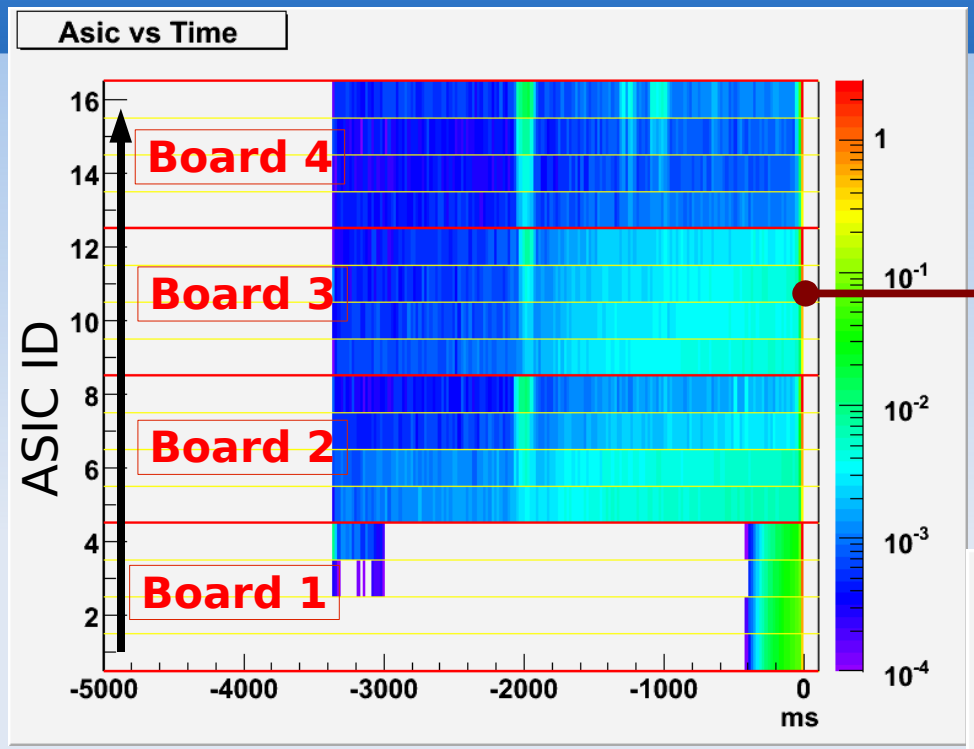




Très préliminaire

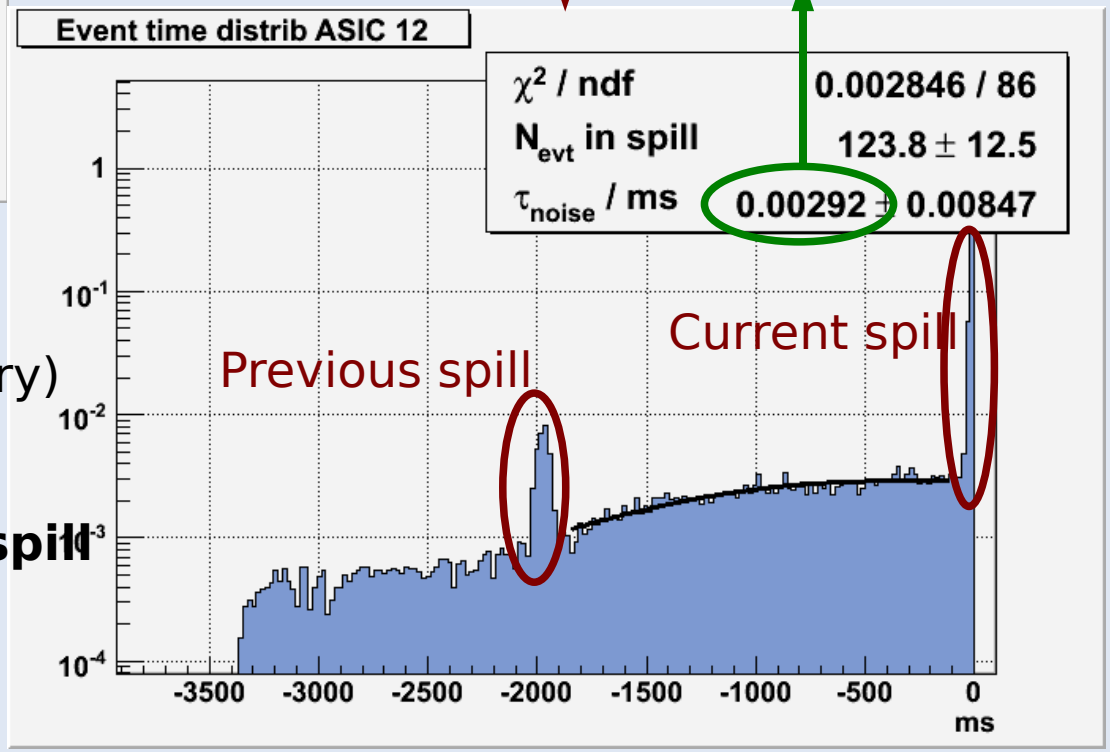
Quelques premiers résultats: RUN101 ; HV=7.4 kV	
Efficacité à 3/3 coïncidences (all events)	83.66 %
Efficacité à 2/3 coïncidences (all events)	77.70 %
Efficacité à 3/3 coïncidences (t>-300 ns)	88.07 %
Efficacité à 2/3 coïncidences (t>-300 ns)	79.60 %

Noise & ROC study



Run00101
Hit rates for each triggered event

2.9 Hz / 64 cm²
= 0.045Hz/cm²
= 0.27 hit/BC sur 30M chan



Shape:

- flat noise+event rate **τ**
- modified by RAMFull (Loss of memory)
- probability at **-t** =
  - (1- P(avail. mem, t × τ))
  - avail. mem = 128 evts – **N_{evt} in spill**

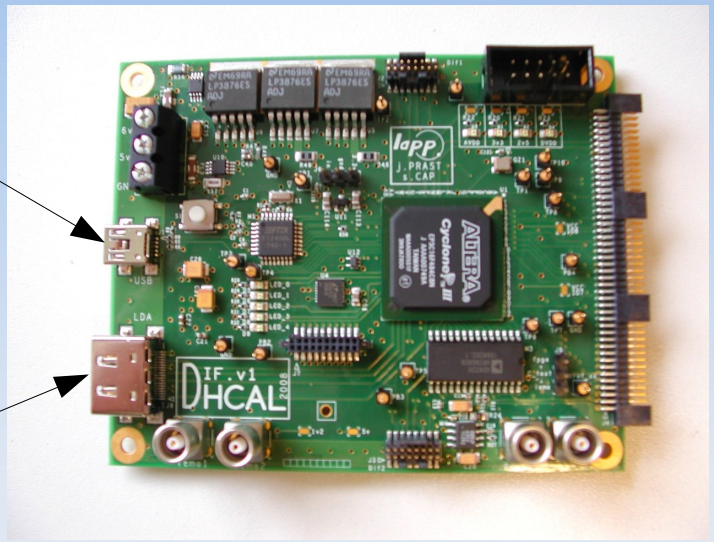
$$P(a, x) = \frac{1}{\Gamma(a)} \int_0^x t^{a-1} e^{-t}\, dt$$

The 1 m² electronics

Julie Prast & Guillaume Vouters

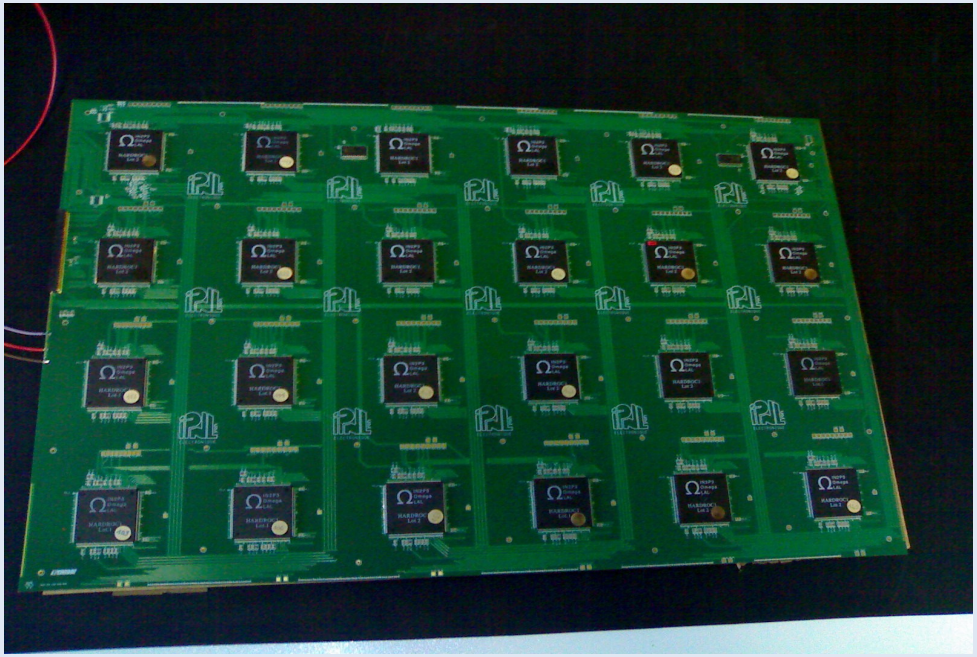
DIF

- 10-layer board (6 for signals) designed and prototype produced
- FirmWare & SoftWare operationnal and **tested in beam** (with 4 HR µMegas card)



ASU

- 8-layer board designed and produced
- 500×33.3×1.2 mm³
- Connections between adjacent PCB foreseen
- ASICs were tested and plugged



Software

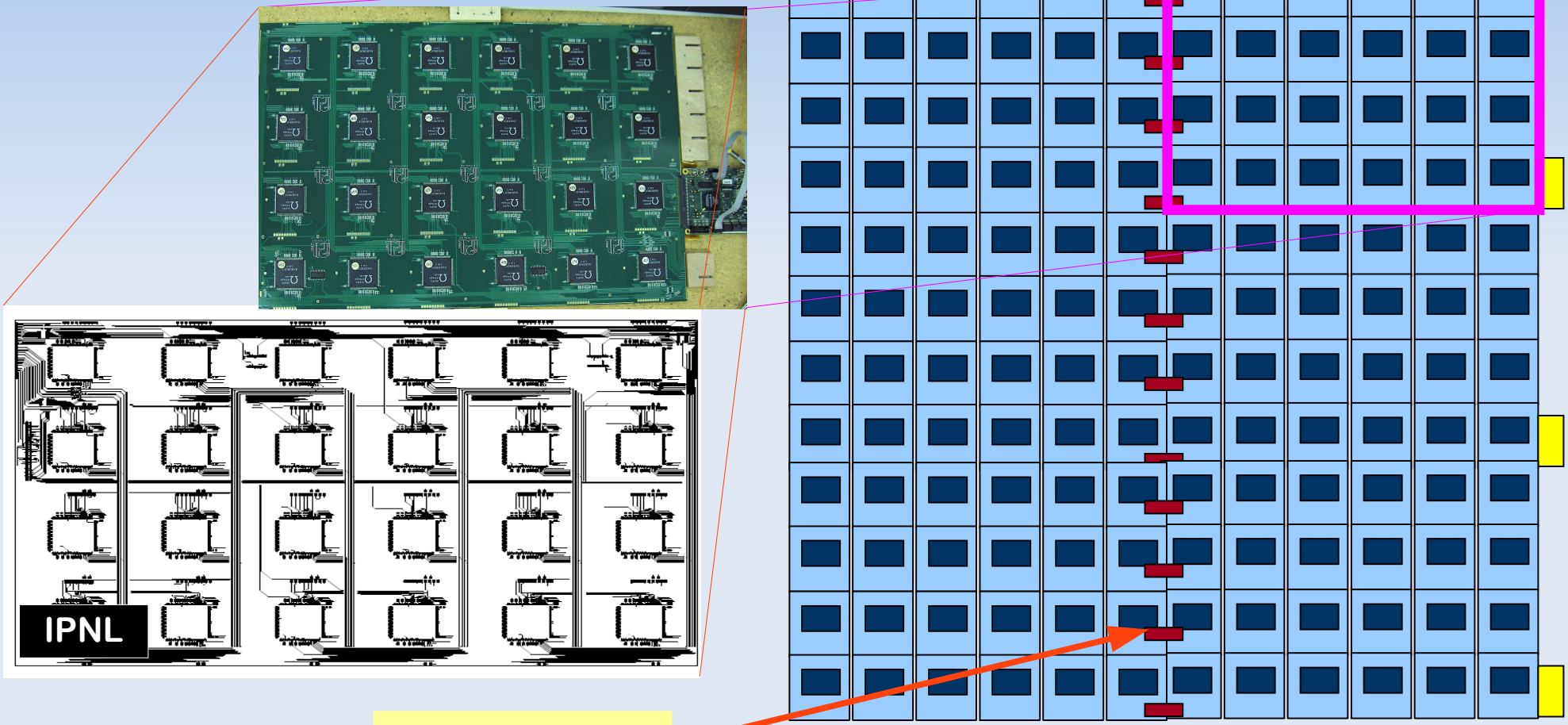
Acquisition software based on US/**XDAQ** developed

Ch. Combaret

Données μMEGAS disponible ⇒ doivent être validées

Next steps: m²
ASIC support Units

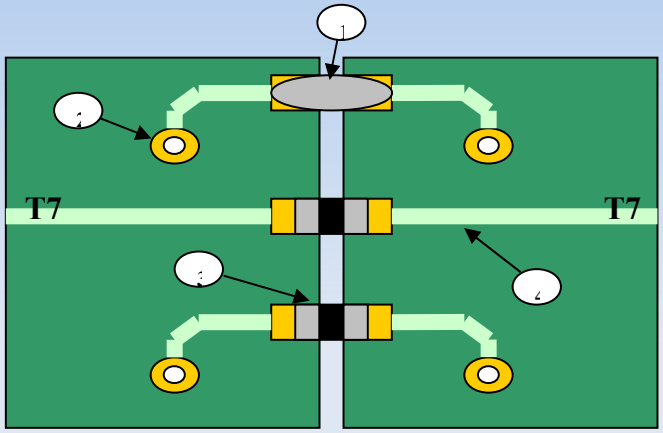
1 ASU → 6×4 chips

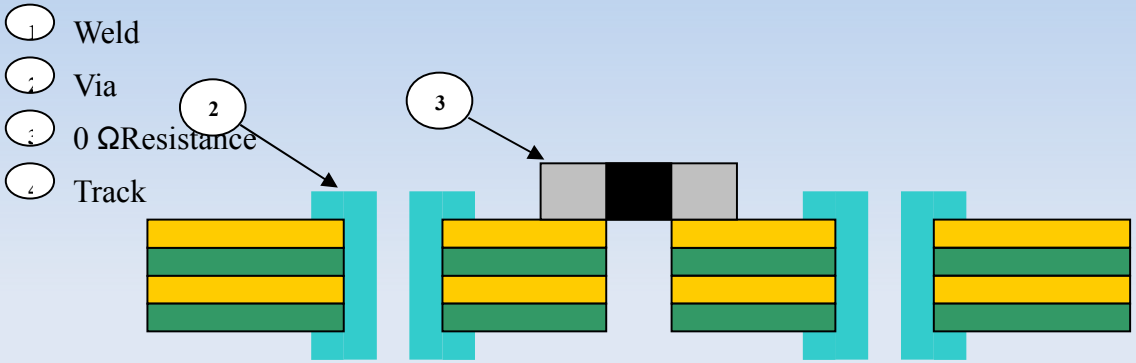


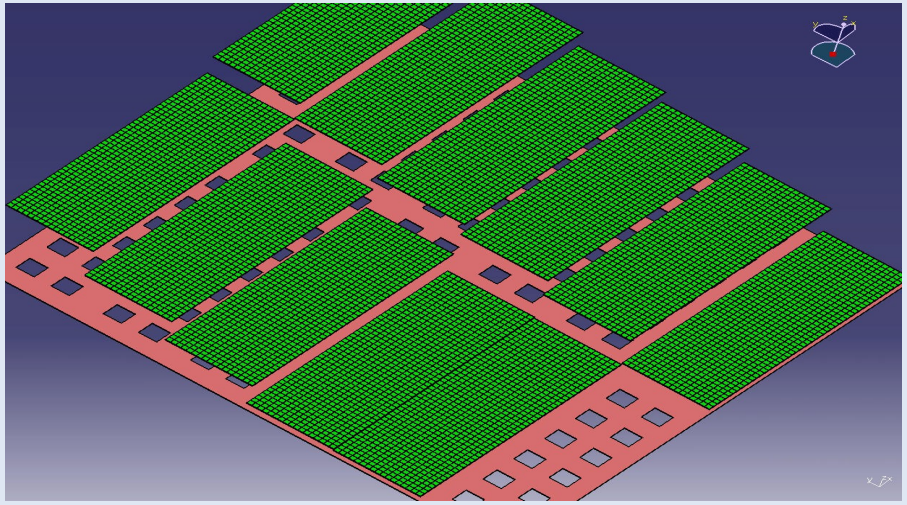
pcb-connector

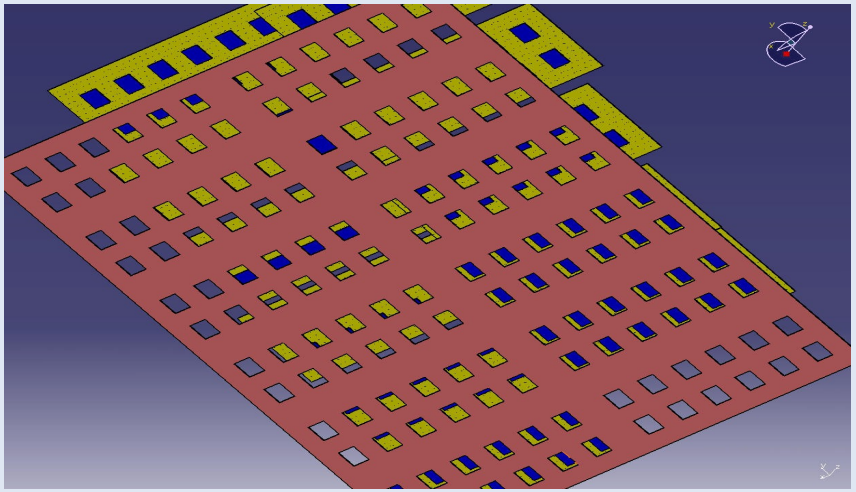
ASU hosting 24 HARDROC chips produced and being tested

Connection between the different ASU is under study: signal transmission+ mechanics (IPNL+CIEMAT)



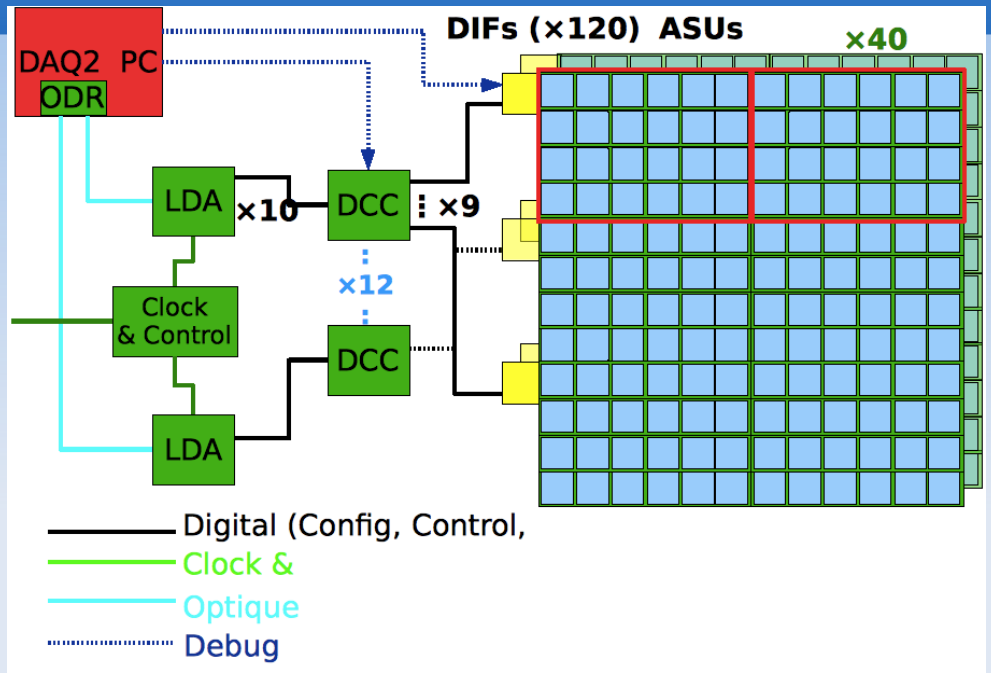






Besoins pour la DAQ du 1 m³

- ***ASICs***
  - 460 HR2 prêts,
    besoin d'un banc test
  - ⇒ 5760 pour le m³
- DAQ2 EUDET
  - ***DIF Annecy***: proto prêt et fonctionnel
    - Testé en TB (nov).
    - Code en cours d'adaptation HR2
    - Bloc lect DIF à implementer
  - Cartes UK
    - PC + ODR
    - Clock and Control
    - LDA
  - ***Carte Concentratrice***



DIF Task Force & eDAQ meetings:
- ***Rémi Cornat***
- ***Julie Prast/G. Vouters***
- ***Bart Hommels***
- ***Mathias Reinecke***

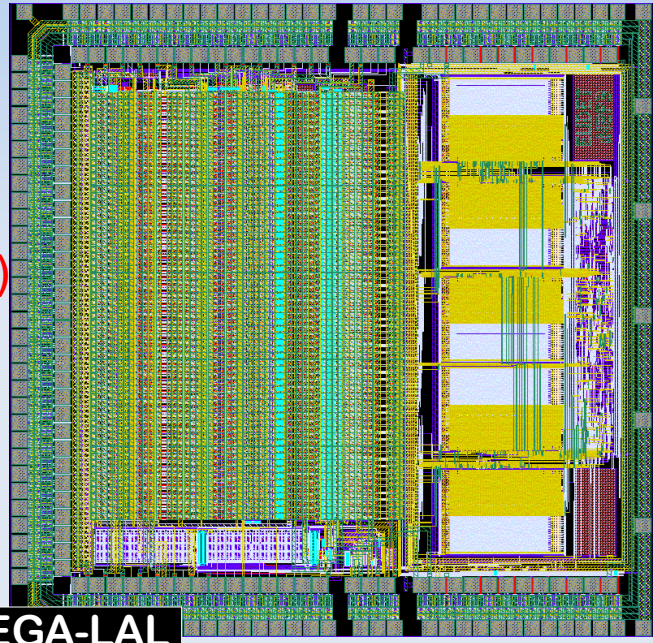
- Format de données
- Distribution
  - Horloges
  - Signaux rapides
  - Commandes
  - Configs

HArDROC2

2nd gen in electronic tests

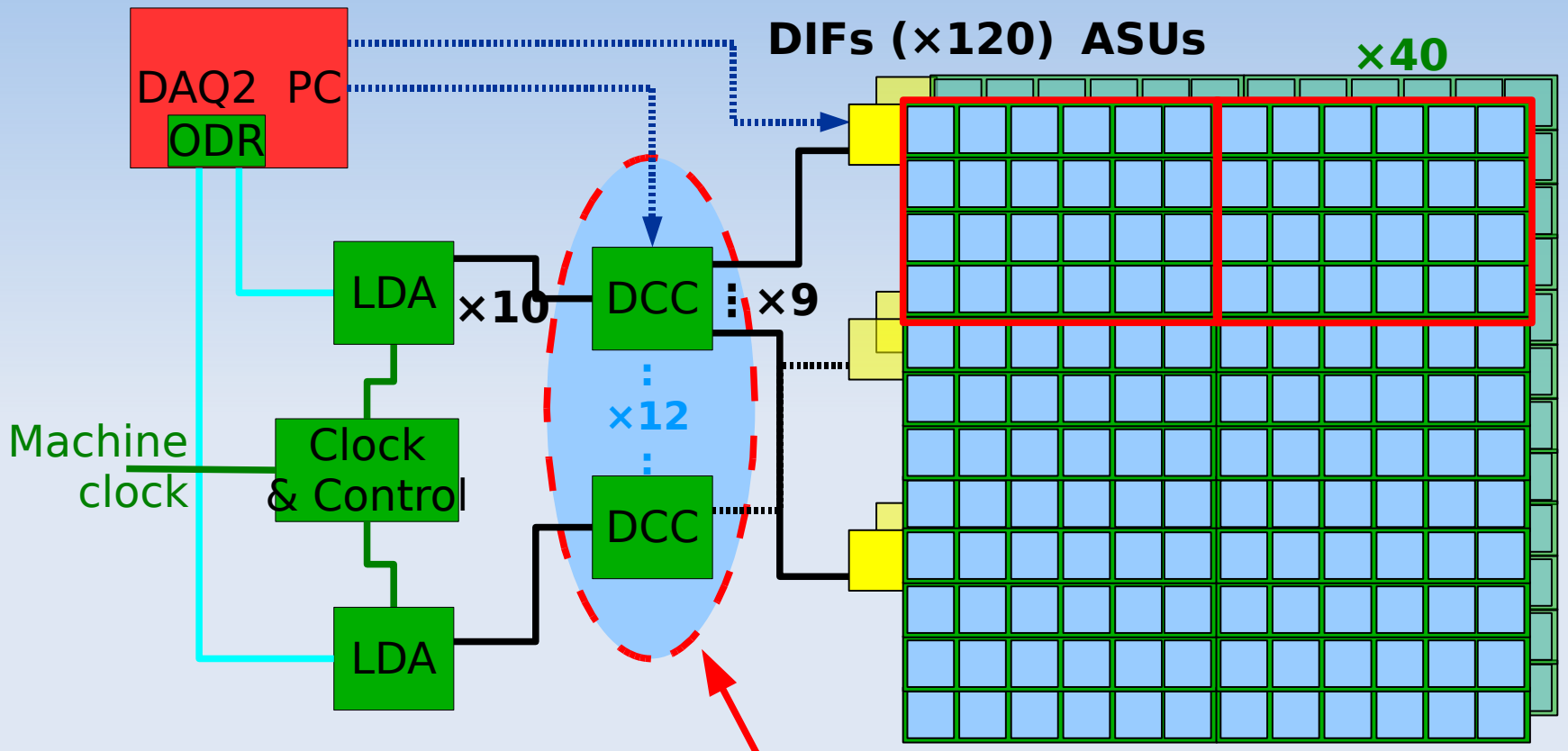
- First batch (460 chips) produced and being tested
  - Will be used for the m^2
- Correction of the minor bugs of HR1
  - Mask, memory pointer (dummy frame)
  - Shift registers improvment (configuration loading)
  - Bypass on critical signals
- Improvement on Power Pulsing
  - Now also digital part

    ⇒ consumption ≤10µW/chan
- Dynamic range extension
  - Gain correction: 8 bits instead of 6
- 3 shapers and 3 threshold (3 indep^t DAC) coded on 2 bits
  - 10 fC, 100fC, 1pC (for µMEGAS)
  - 100 fC, 1pC, 10pC (for GRPCs)



OMEGA-LAL

DAQ2 EUDET pour le sDGHCAL



Digital (Config, Control, Data)
Clock & Sync
Optique GigE
Debug USB

Carte DCC en développement au LLR

1 PC: 2 k€
1 ODR: 4-5 k€
1 LDA: ~1.3 k€

Rappel: 40×100×100 cellules = 400k canaux!!!

Flux de données

N DIF/LDA	N DIF/DCC	LDA-DIF Dclk [MHz]	LDA-DIF FLUX [MB/s]	LDA Dclk [MHz]	LDA FLUX [MB/s]	ODR FLUX [MB/s]	Disk Flux [MB/s]
10	**9**	**80**	*10*	**1000**	*125*	**1000**	**170**
Detector	**DHCAL**	Evt Size	Mem Size	ASIC Dclk [MHz]	ASIC FLUX [MB/s]		
		20 B	**128**	**5**	0,63		
Mode	Calib/Noise Single	Calib/noise Burst	TB Single	TB Burst	Demo		
N ASIC/DIF	**48**	48	**6**	6	6		
ASIC	20 B	2 560 B	20 B	2 560 B	2 560 B	note de JCB:	
R/O time 1	*32 µs*	*4 096 µs*	*32 µs*	*4 096 µs*	*4 096 µs*	Moyenne	4,8
R/O time ALL	***1 536 µs***	***196 608 µs***	***192 µs***	***24 576 µs***	***24 576 µs***	sigma	2,6
DIF	960 B	122 880 B	120 B	15 360 B	15 360 B		6,54
R/O time	*96 µs*	*12 288 µs*	*12 µs*	*1 536 µs*	*1 536 µs*		
LDA w/o DCC	9 600 B	1228 800 B	1 200 B	153 600 B	153 600 B		
R/O time	*77 µs*	*9 830 µs*	*10 µs*	*1 229 µs*	*1 229 µs*		
DCC	8 640 B	1 105 920 B	1 080 B	138 240 B	138 240 B		
R/O time	*864 µs*	*110 592 µs*	*108 µs*	*13 824 µs*	*13 824 µs*		
LDA w/ DCC	86 400 B	11 059 200 B	10 800 B	1 382 400 B	1 382 400 B		
R/O time	*691 µs*	*88 474 µs*	*86 µs*	*11 059 µs*	*11 059 µs*		
ODR	17 280 B	2 211 840 B	2 160 B	276 480 B	276 480 B		
1000MB/s	*17 µs*	*2 212 µs*	*2 µs*	*276 µs*	*276 µs*		
Disk	17 280 B	2 211 840 B	2 160 B	276 480 B	276 480 B		
170MB/s	*102 µs*	*13 011 µs*	*13 µs*	*1 626 µs*	*1 626 µs*		
Max R/O time	***1 536 µs***	***196 608 µs***	***192 µs***	***24 576 µs***	***24 576 µs***		
Max Freq	0,65 kHz	0,01 kHz	5,21 kHz	0,04 kHz	0,04 kHz		
Max evts Freq		0,65 kHz		5,21 kHz	5,21 kHz		

Mode Acq

Nombre d'ASIC touchés par 1 π de 100 GeV

Facteur limitant

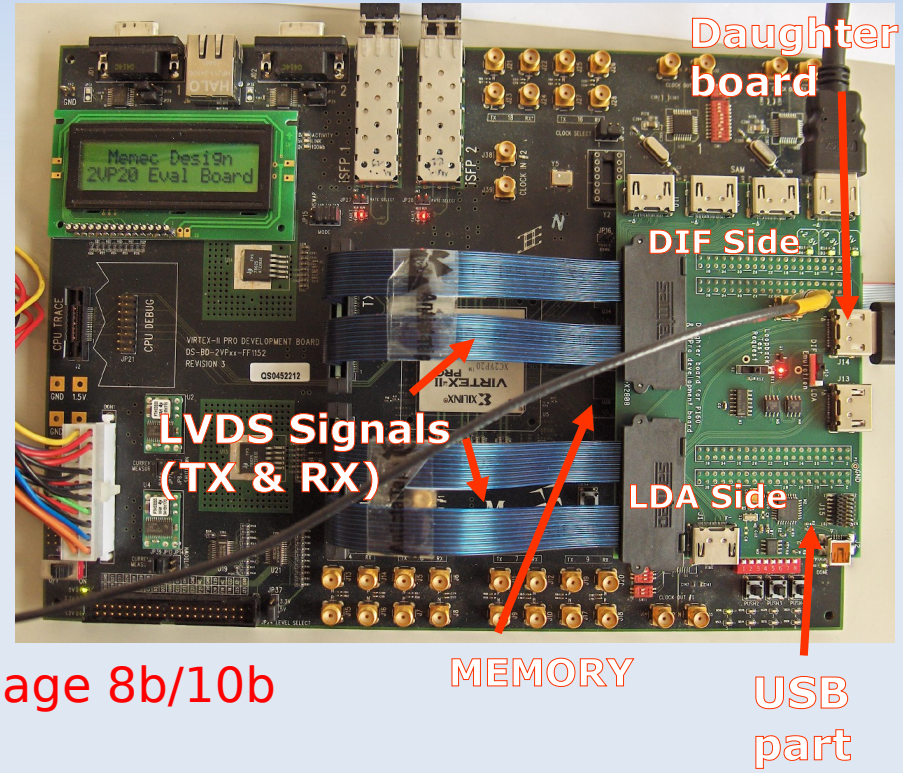
Vitesse Attendue

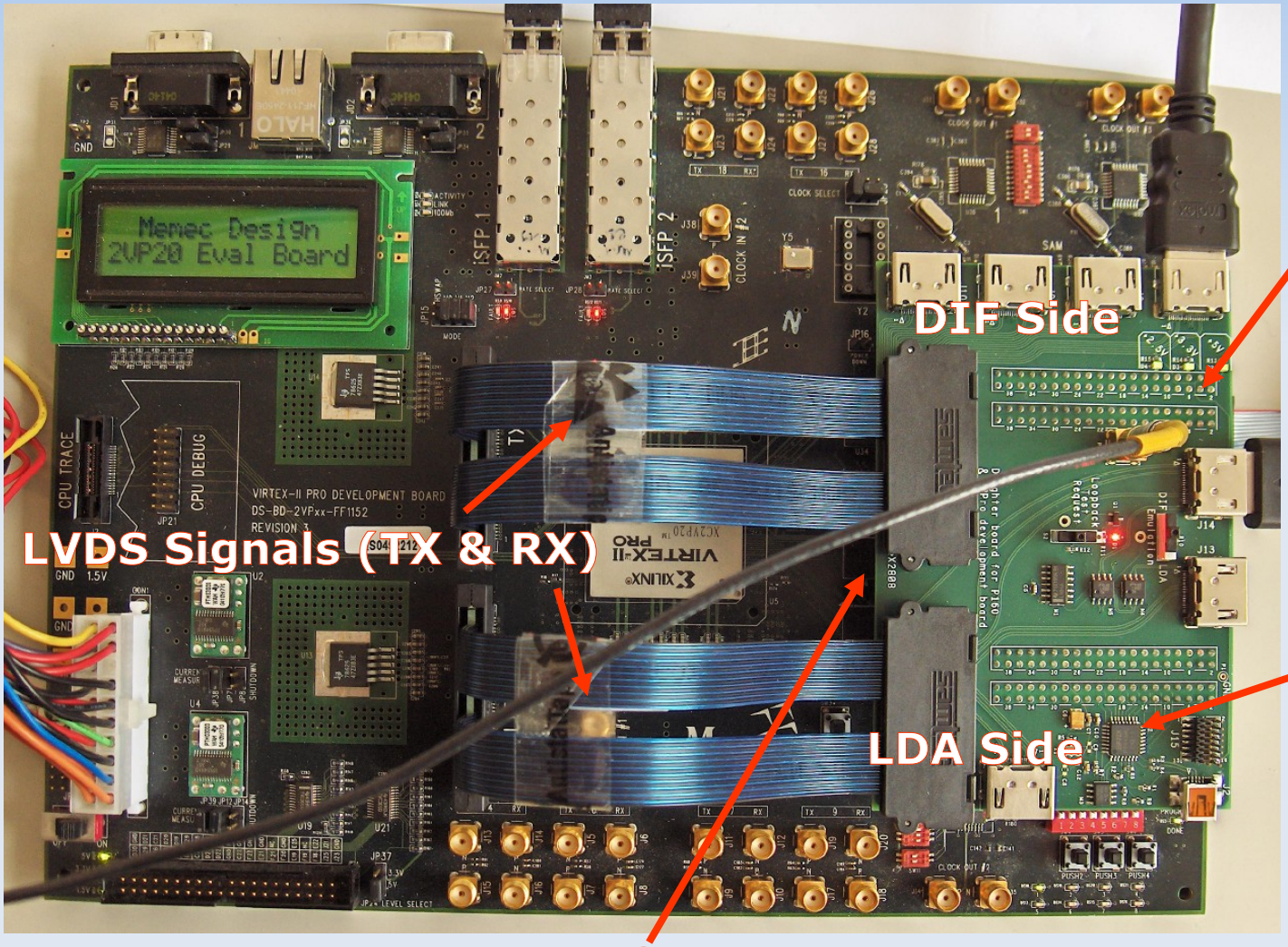
Carte DCC

Attendus:
- Transparence
- Optimisation du flux
- Faible coût
- Sécurité de la DAQ

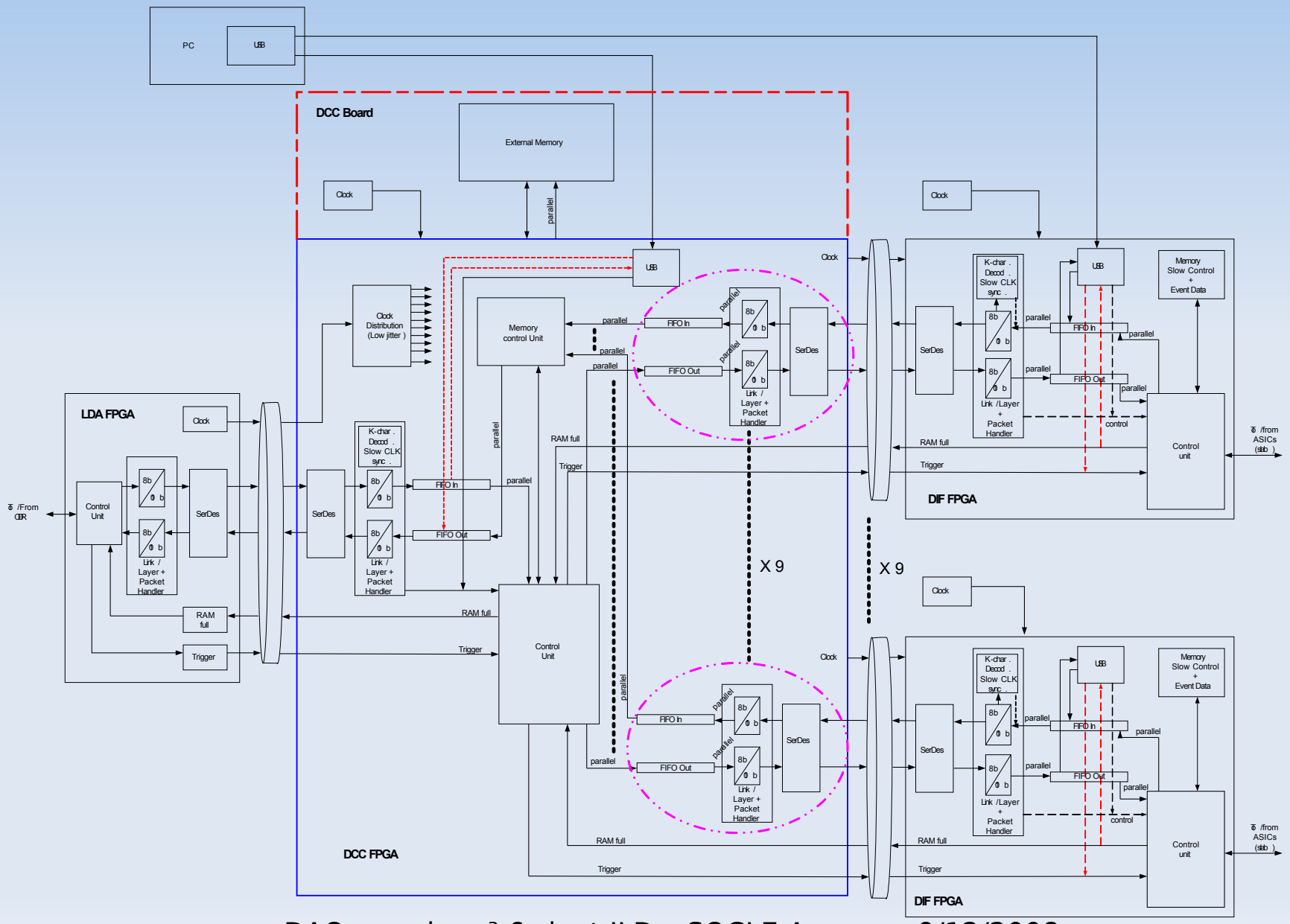
Franck Gastaldi & Antoine Mathieu

- Pre-proto (proto-0)
  - Lecture de 4 DIFs
  - Implantation et tests du code VHDL
- Utilisation d'une carte d'évaluation XILINX:
  - 128 Mbits SDRAM
  - Carte fille:
    - connecteurs HDMI
    - bloc USB
- **Développements**:
  - Marc Kelly (U. Man) : blocs Ser-Des, codage 8b/10b
  - Bloc USB (Clément Jauffret)
  - Blocs VHDL propres:
    - Contrôleur mémoire, blocs commandes, buffers (FIFO),.....)




Memec Design
2VP20 Eval Board
VIRTEX-II PRO DEVELOPMENT BOARD
DS-BD-2VPxx-FF1152
CPU TRACE
CPU DEBUG
ISFP 1
ISFP 2
CLOCK IN #2
DIF Side
LVDS Signals (TX & RX)
LDA Side
Daughter board
USB part
MEMORY

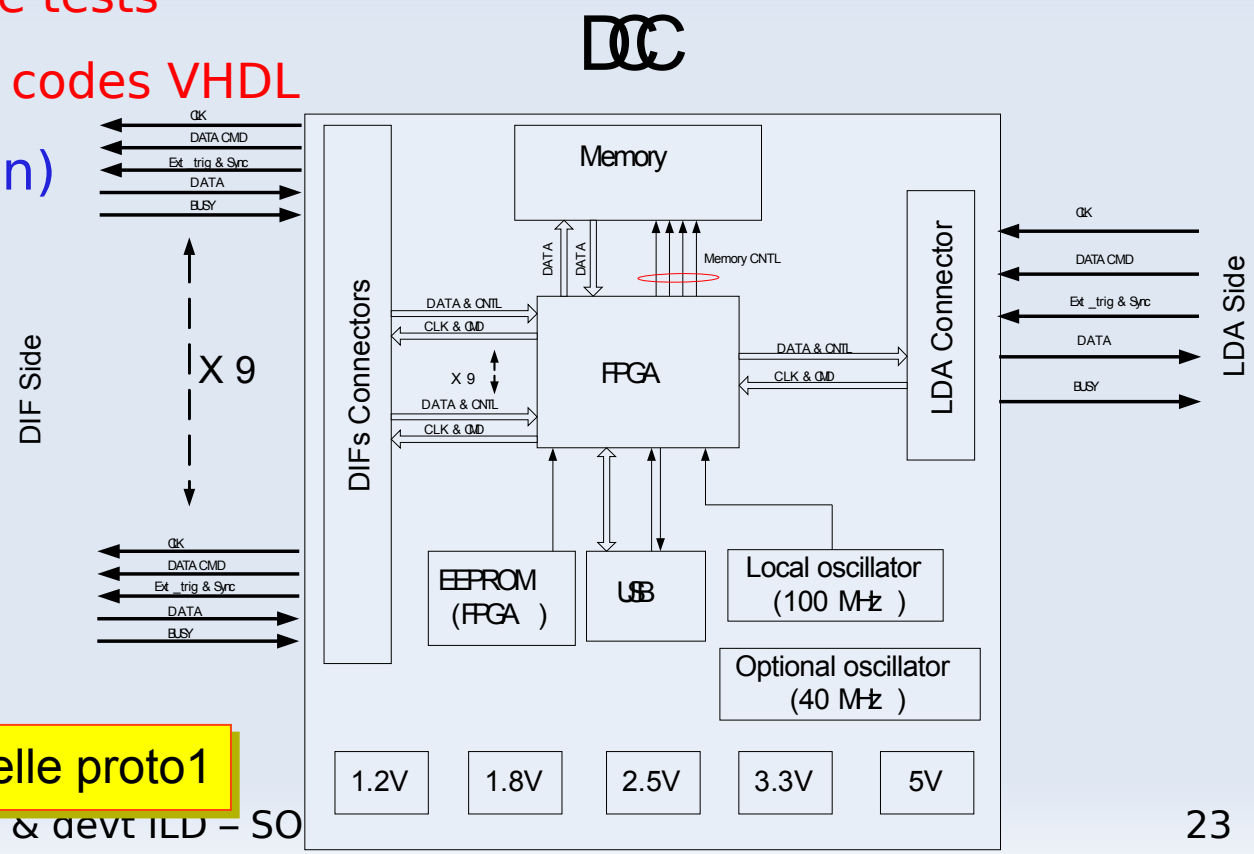
Chaine d'acquisition prototype DCC



Planning DCC

- Janvier 09:
  - Finalisation Schématique et Routage PCB DCC
- Janvier - Avril 2009
  - Fabrication prototype DCC
  - Mise en place du banc de tests
  - Validation des différents codes VHDL
- Mai – Juin 2009 (estimation)
  - Production des cartes pour le m³

- Bouclage DCC-DIF / DCC-LDA
- Connection avec la DIF (code sur la DIF)

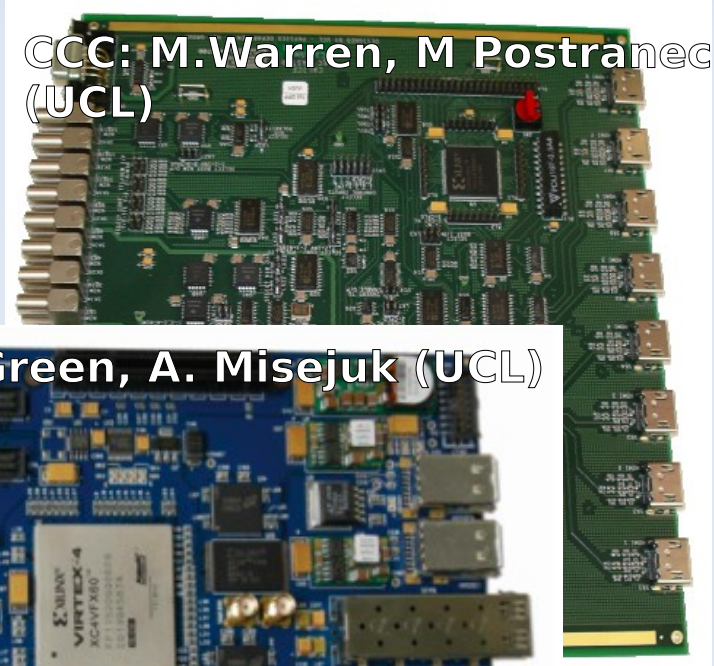


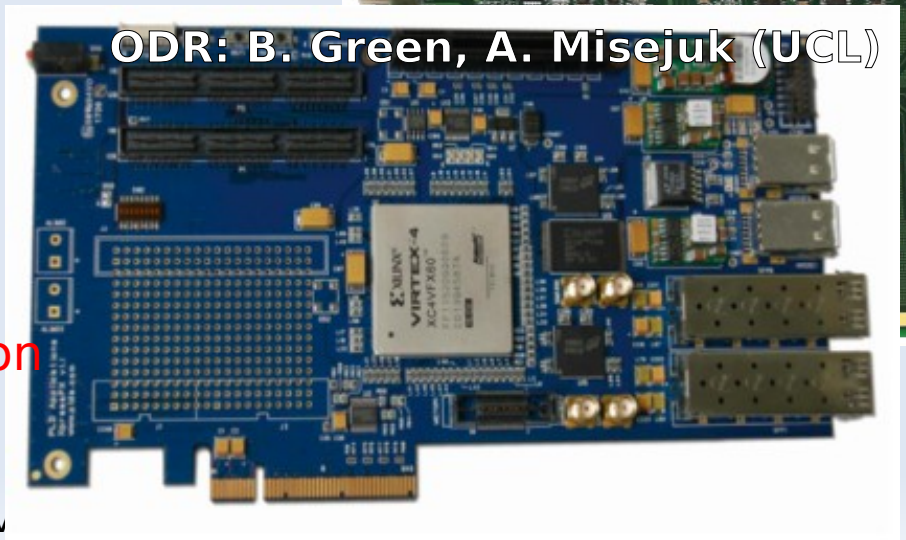
Implementation fonctionnelle proto1

Banc test & intégration de la DAQ

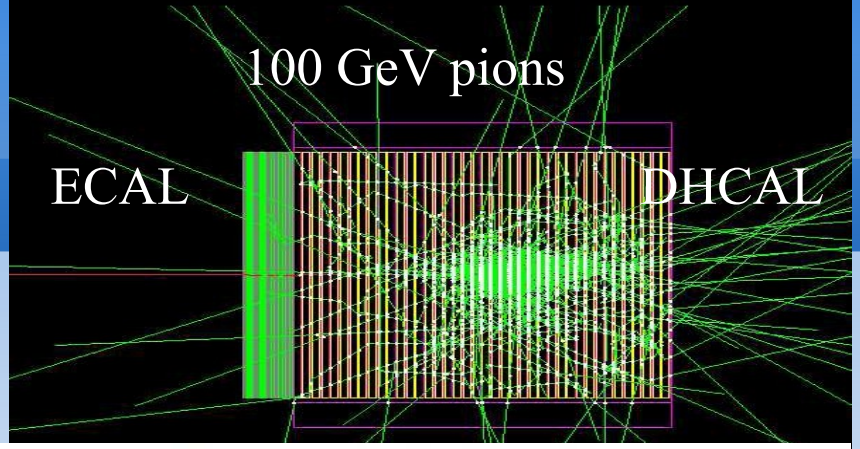
- Matériel:
  - 1 Proto-DIF ✔,
    - Integration code LDA-DIF
  - 1 LDA (✔? fin déc),
    - HW pbm resolved ?
  - 1 CCC ✔?
  - 1 ODR + 1 PC DAQ ✔
  - 1 proto DCC (mars ?) ou proto-0
- Code DAQ : DOOCS
  - Demo disponible
- → Mars 09
  - Intégration pour un m³
  - Besoin d'aide pour intégration vrai détecteur

LDA: M. Kelly (U. Manchester)


CCC: M.Warren, M Postranecky (UCL)

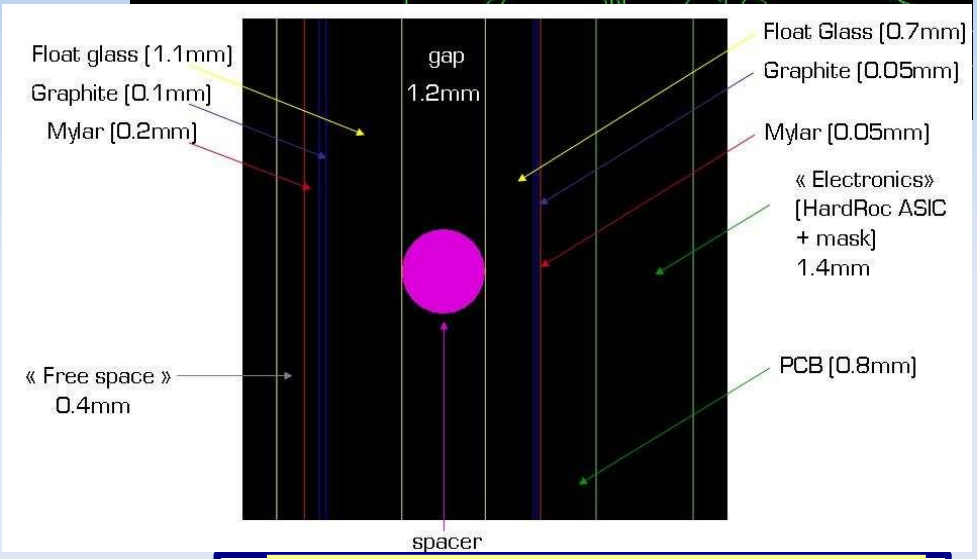

ODR: B. Green, A. Misejuk (UCL)

Simulation des TB

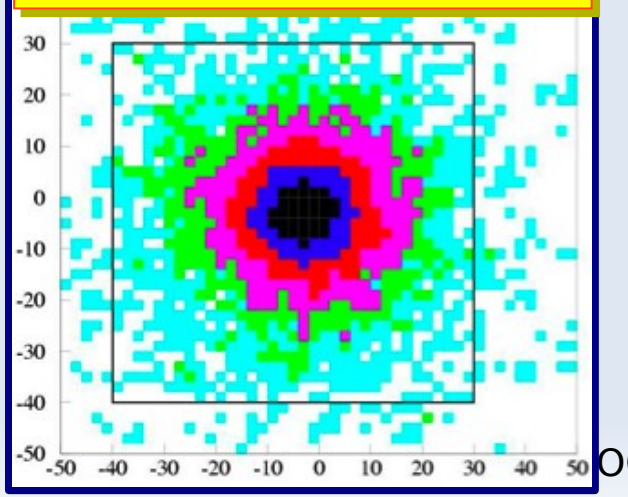


- Simulation détaillée
  (amenée de gaz, entretoise)

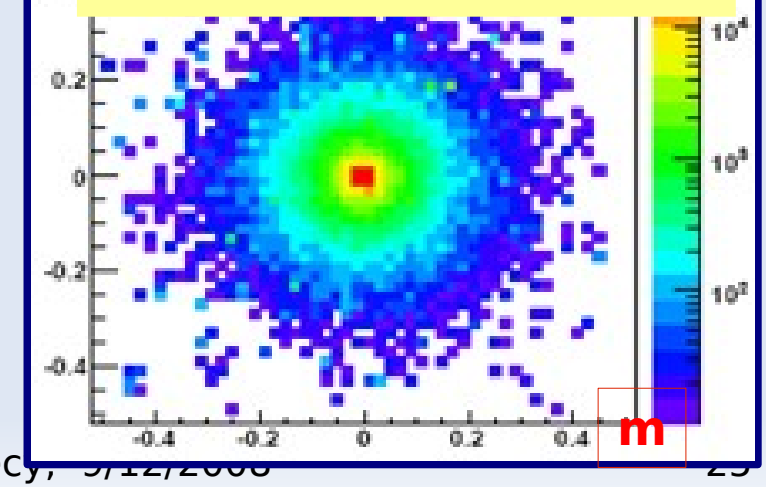
Emmanuel Latour,
Gérald Grenier,
Muriel Vander Donckt



note LC-DET-2004-029



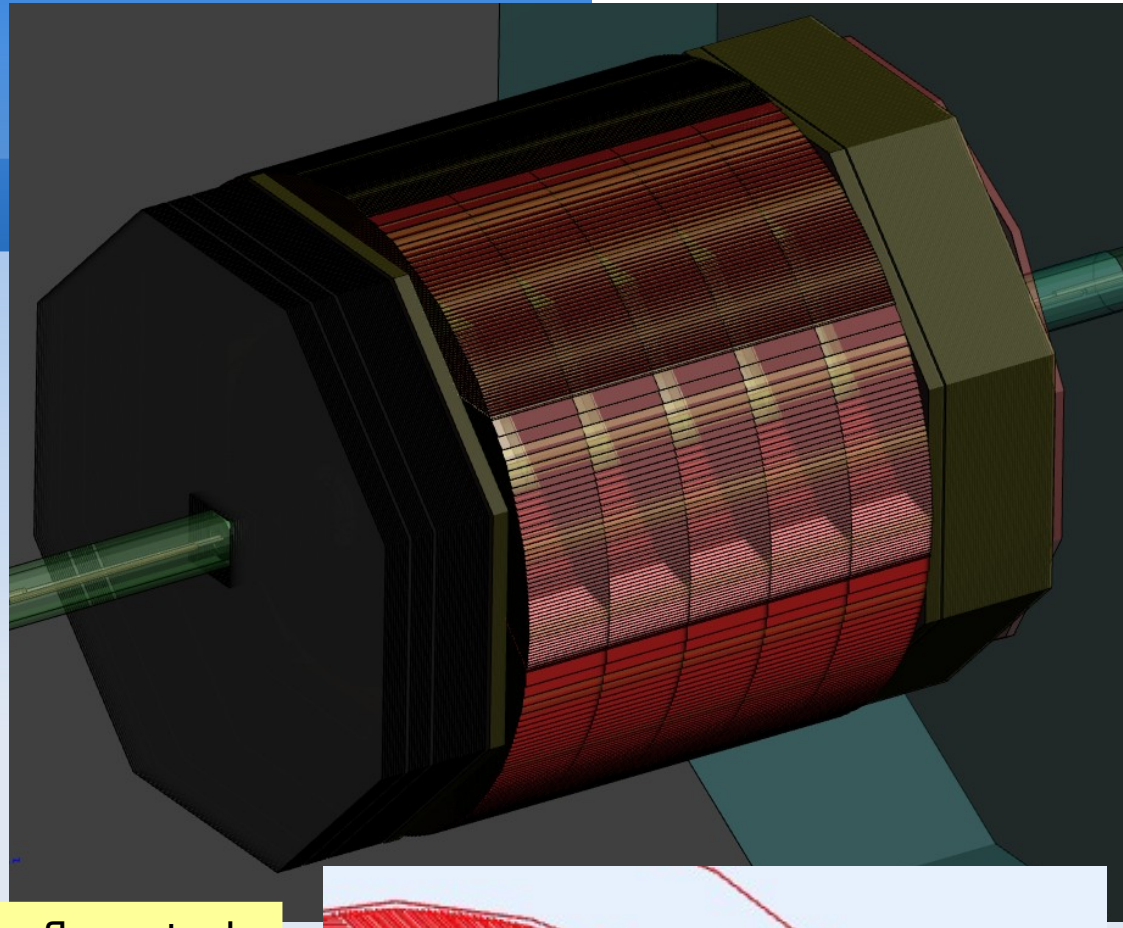
Transversal hadronic showers



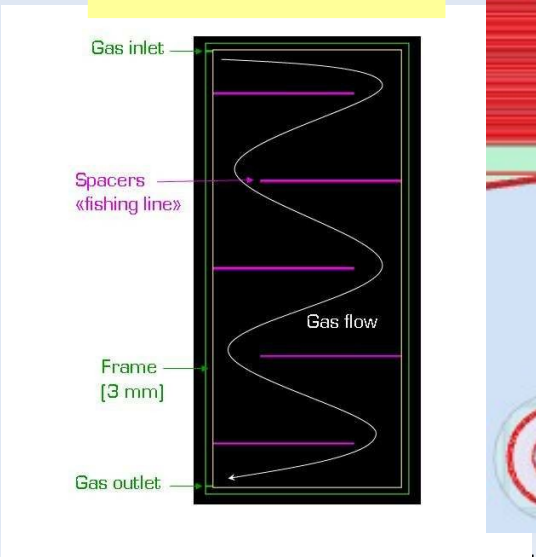
Intégration ILD

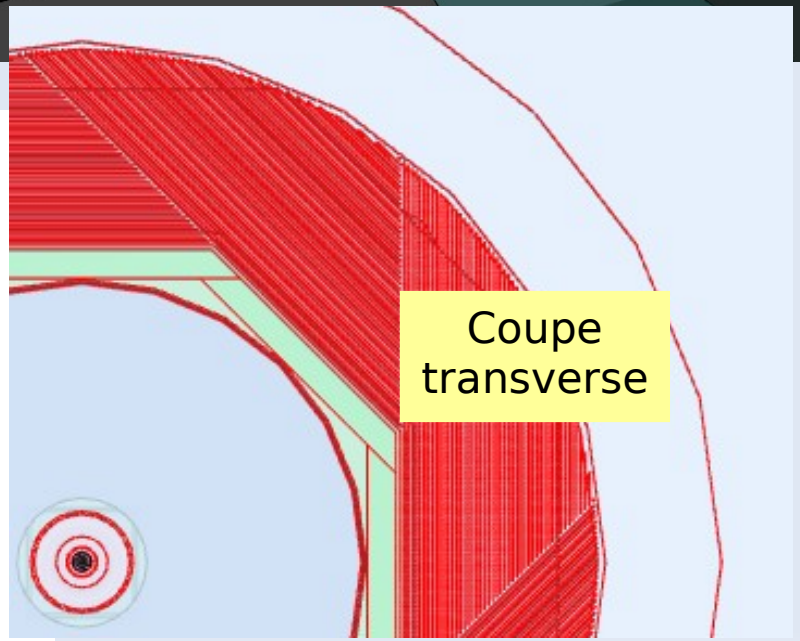
- Structure mécanique « à la Henri » rigide & non projective
- Géométrie dans la simulation
  - 5 roues + bouchon
  - 8 Modules/roue
  - 48 couches/module
- Electronique, gaz and refroidissement à la périphérie
  - Baril & bouchons quasi-jointifs
- Intégration de slabs RPCs détaillés

Emmanuel Latour, Paulo Mora de Freitas, Gabriel Muşat



Gaz flow study

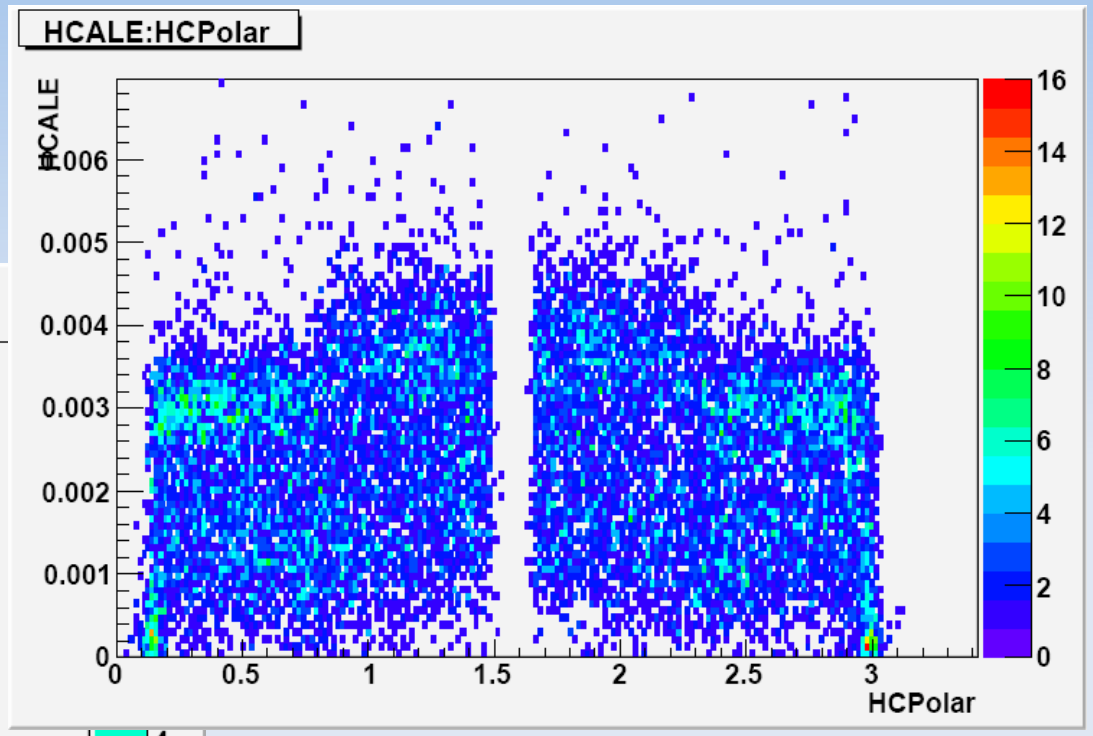


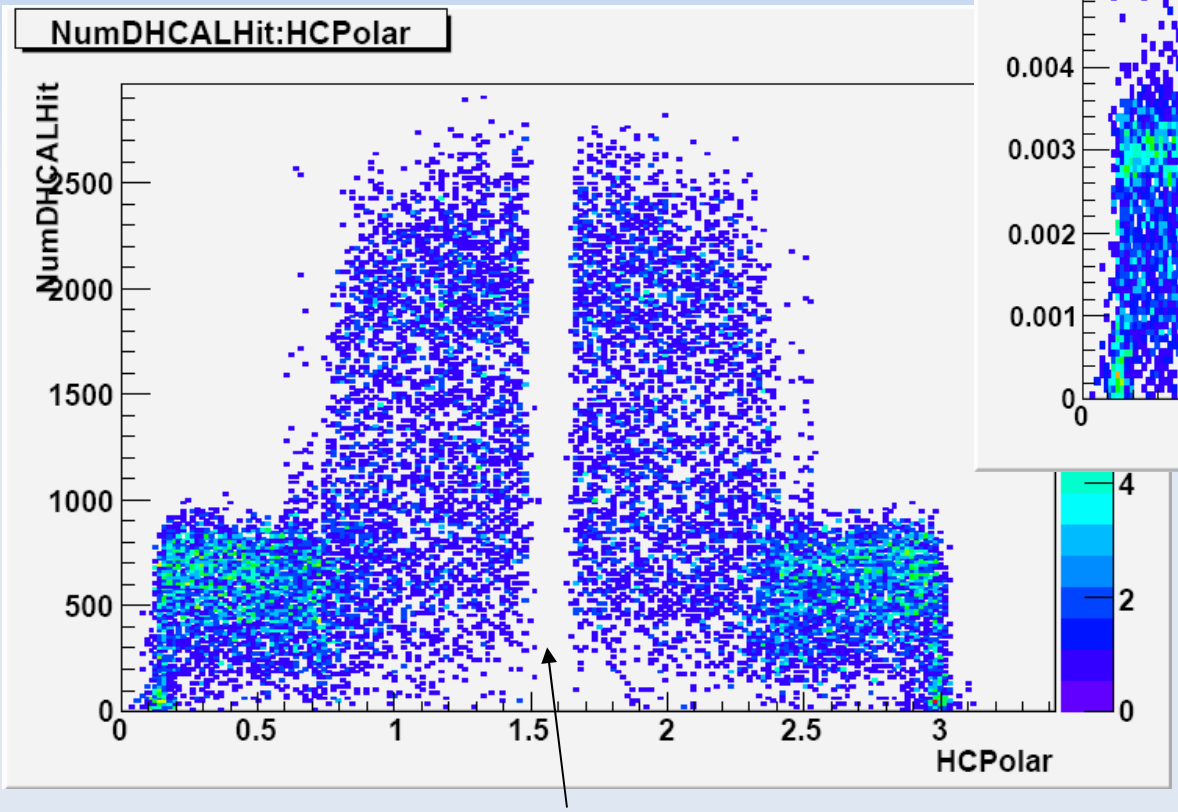


Coupe transverse

ILD sDGHCAL: première simulations

- 15k × 100 GeV π's on the grid





Pion shot at 90±5 Deg: data file not ready

Corrections:

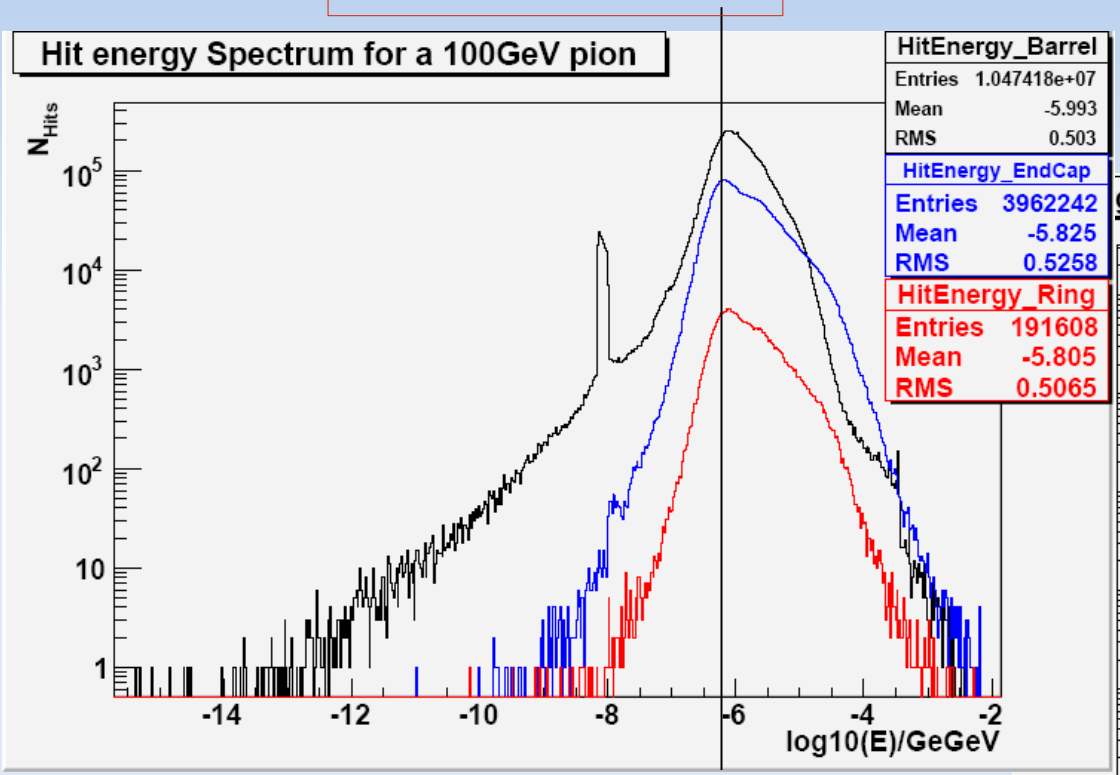
- Bug de mémoire trouvé
- Implementation distincte Baril / bouchon

Manqi Ruan
Gabriel Muşat

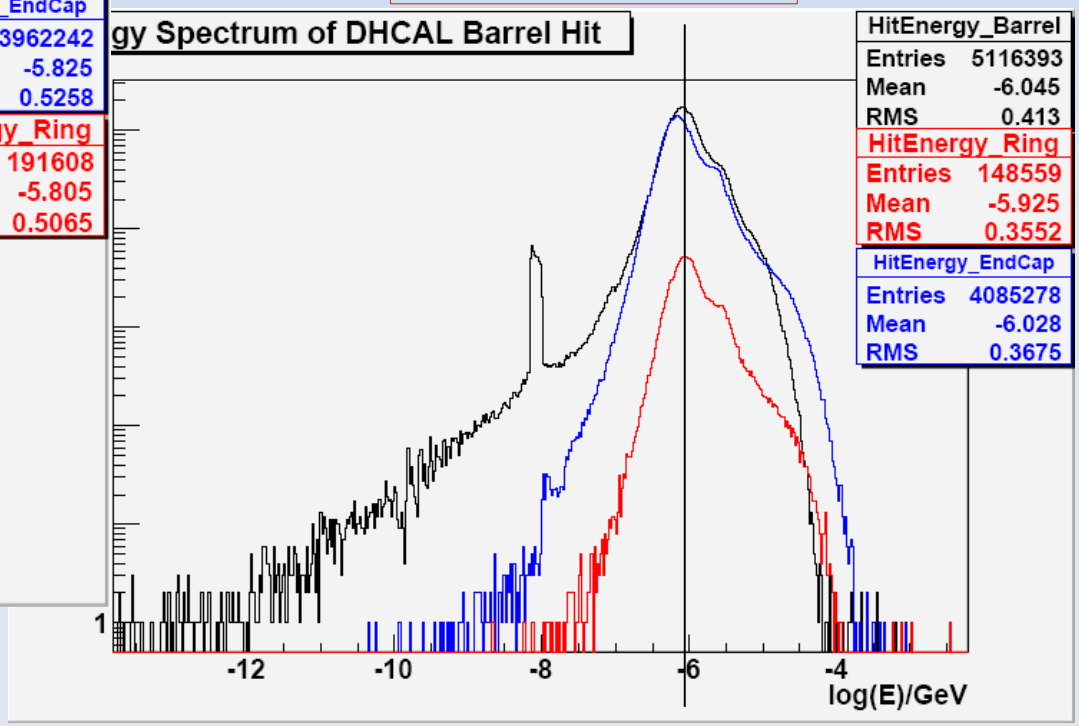
ILD sDGHCAL: premières simulations

Spectre en énergie des cellules (1×1 cm²)

100 GeV π's



50 GeV μ's



Champ électrique (manquant) ?

Validation en cours

Résumé & prospective

- Données TB
  - Premiers résultats sur l'électronique
  - Premières reconstructions de trains de type ILC
- Acquisitions de données
  - Variées
  - Évolutives
  - Gros effort encore nécessaire
    - « bien parti pour 1 m^3 »
- Implementation sDGHCAL dans ILD « en cours »