



- ECAL Silicon wafer status
- Software plans

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SOCLE 2008 @ LAPP

Disclaimer: I am newly arrived in this group - apologies for mistakes and omissions!



In2p3

The CALICE SiW ECAL concept envisages a very highly granular sampling calorimeter, with silicon pads as the active layers

Very large area required in final detector: need cost-effective (~simple) design

CALICE SiW ECAL "Physics prototype" was built with 6x6cm<sup>2</sup> wafers made up of 36 1x1cm<sup>2</sup> pads



This detector has been exposed to test beams during the last few years

Generally, it has performed well (e.g. Cristina's talk) In addition, we have learned several things about aspects of silicon wafer design



## Inter-Wafer gaps

Mean shower energy vs. shower position shows significant (~30%) effect of the dead area between adjacent wafers

Not impossible to correct for this effect, but would prefer to minimise it as much as possible



#### • "Square events" Observed in the test beam data

An effect of the "guard ring" being hit by a particle, inducing a signal on neighbouring cells.



Interesting simulation result: PandoraPFA performance seems to gain significantly when ECAL cell size decreases  $1x1 \text{ cm}^2 \rightarrow 0.5x0.5 \text{ cm}^2$  (particularly at higher energies)

# Start from LDCPrime with 5×5 mm<sup>2</sup> SiW ECAL pixel size Investigate 10×10mm<sup>2</sup>, 20×20mm<sup>2</sup> and 30×30mm<sup>2</sup>

Note: required changes in PandoraPFA clustering parameters



Performance is a strong function of pixel size
Probably rules out segmentation of >10×10mm<sup>2</sup> !!!!

M.Thomson LCWS08 For next EUDET "technological prototype" detector, we will try to address some of these features

Go from  $6x6 \text{ cm}^2 \rightarrow 9x9 \text{ cm}^2$  wafers, with smaller pixel size  $5x5 \text{ mm}^2$ 

Larger wafers inherently give less significant edge effects

Smaller pixels will improve PFA performance for energetic jets (>~200GeV)

Several studies are underway to reduce/eliminate the effect of the guard rings and/or reduce dead zone at the wafer edge

Try to segment guard ring to minimise signal propogation test @ LPC early 2009



A number of test wafers have been received from Hammamatsu, tested in the laboratory, understood

40 wafers recently ordered from Hammamatsu for EUDET technological prototype (delivery in 1<sup>st</sup> half of 2009)
20 more will soon be ordered from another company

To complete the EUDET module, need 120 additional wafers (funding may be an issue here)

### Simulations of guard rings etc.



#### Rémi Cornat

Another idea: cut a shallow trench along edge of wafer: Reduces maximum electric field

#### Simulation results:



Rémi Cornat

#### General overview of CALICE SiW software structure



#### Simulation of test-beams

Detailed simulation (In Mokka) of entire test-beam system: Calorimeters, Trigger counters, tracking detectors





F. Salvatore

Tracking software (mostly analysing the four drift chambers)

reasonably complete for 2006/07 data

Important for position and angular resolution measurement

Previously mostly a UK activity, not much work lately...



We will work in this at LLR improve tracking software & simulation measure and implement geometry/drift speeds/scattering for 2008 period GARLIC clustering algorithm

Dedicated photon finder in ECAL

Allows study of ECAL performance in real-life situation, after full event reconstruction/PFA



