

# Review of SiLC activities

***LPNHE/ IN2P3 / CNRS / U. Paris VI & VII:***

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SOCLE December 08, LAPP Annecy-le-Vieux

# Outline

R&D on Sensors

R&D on Mechanics

R&D on Electronics

Test beam activities

Simulation: tool developments and studies

Detector Integration

Letters of Intent preparation

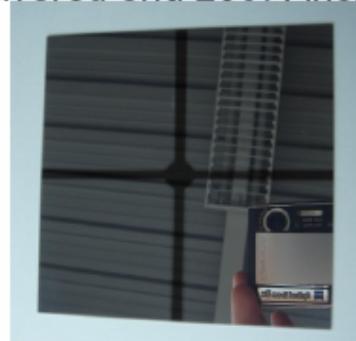
Perspectives

***Outlined in this presentation the contributions of LPNHE in these various topics***

# R&D on sensors

## **Microstrips = the short term baseline**

**Today:** HPK 6", 50  $\mu\text{m}$  pitch, 320  $\mu\text{m}$  thick, delivered end 2007. include sensors specially treated for alignment;  
Fully tested at Lab test bench and test beam



**Short term:** Look for other vendors and even more performing strip detectors: edgeless (CANBERRA S.A.)

Continuing with HPK for thinner large wafers

And novel technology: 3D planar (VTT, IRST and CNM)

## **Go to pixel technology** (longer term)

=> Presently DEPFET (IFIC-Valencia), LMB-pixels (Low Material Budget) also a 3D technology (OSU)

=> Pursue on 3D pixels and 3D vertical interconnect

*SiLC is using the experience of HEPHY Vienna and IEKP Karlsruhe gained in CMS - use of structures to study the detailed characteristics of new sensors (see next slides). The LPNHE team is developing this expertise as well and will pursue developing it in the next years acquiring/building also the needed set up and tools.*

*Concerning pixels: LPNHE intends to work on the 3D pixels as part of the global world-Wide 3D effort for pixels and for 3D vertical interconnect*

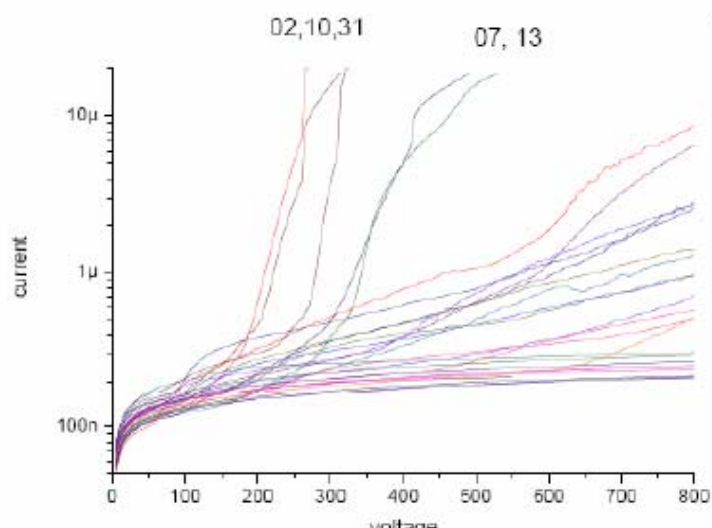
*(Note the ILC-LPNHE is part of the 3D project IN2P3-FNAL and in ANR Vitesse)*



# HPK strip sensors

*with test structures a la CMS*

*Fully tested on dedicated Lab test ber.  
At HEPHY-Vienna and IEKP Karlsruhe*

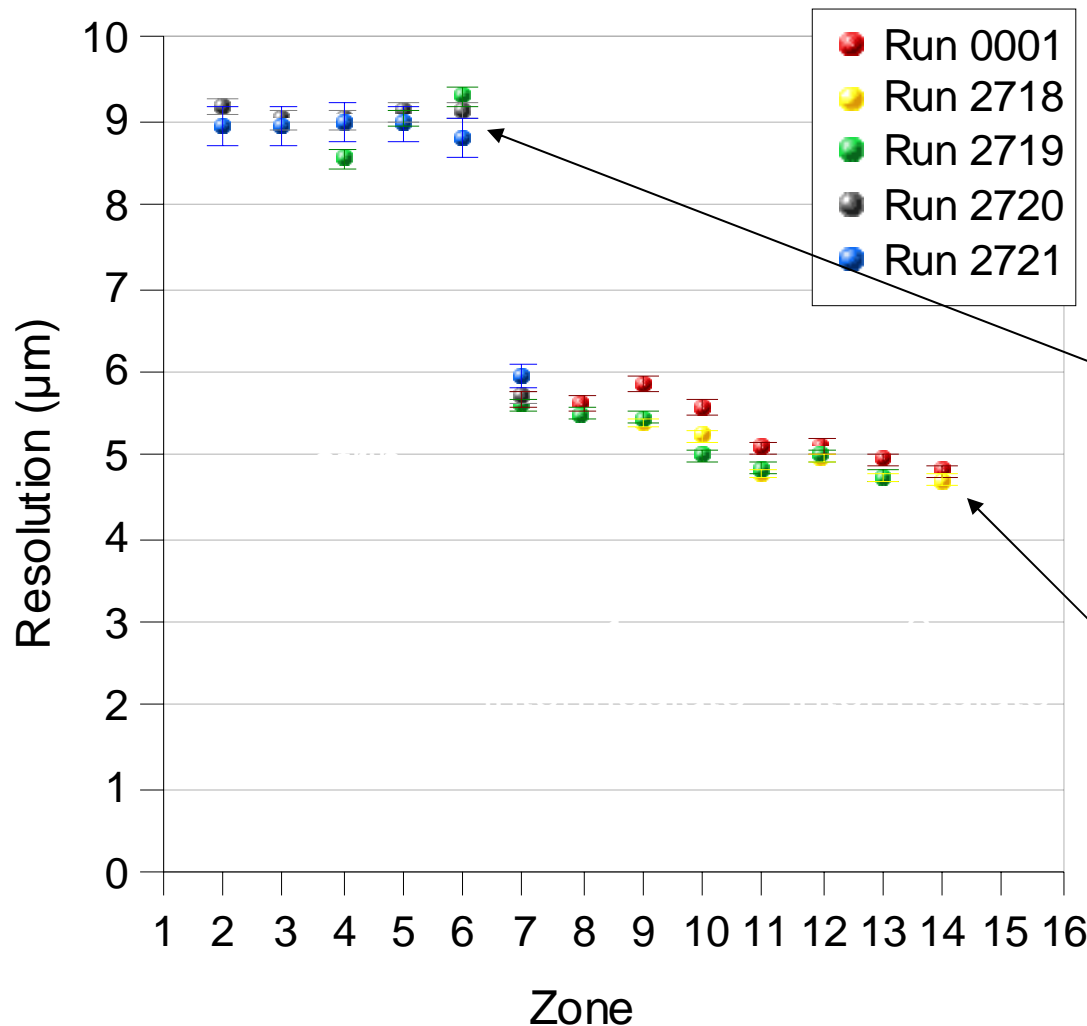


## TESTAC:

strip width [μm]	intermediate strips
5	no
10	no
12.5	no
15	no
20	no
25	no
5	single
7.5	single
10	single
12.5	single
15	single
17.5	single
5	double
7.5	double
10	double
12.5	double

*The LPNHE intends to further develop the Lab test facilities to perform detailed electrical characterization of new sensors. This is underway.*

# Spatial resolution vs. strip geometry



50 μm r/o pitch strip

**Interesting result:**  
**9 μm resolution** if no  
intermediate strip

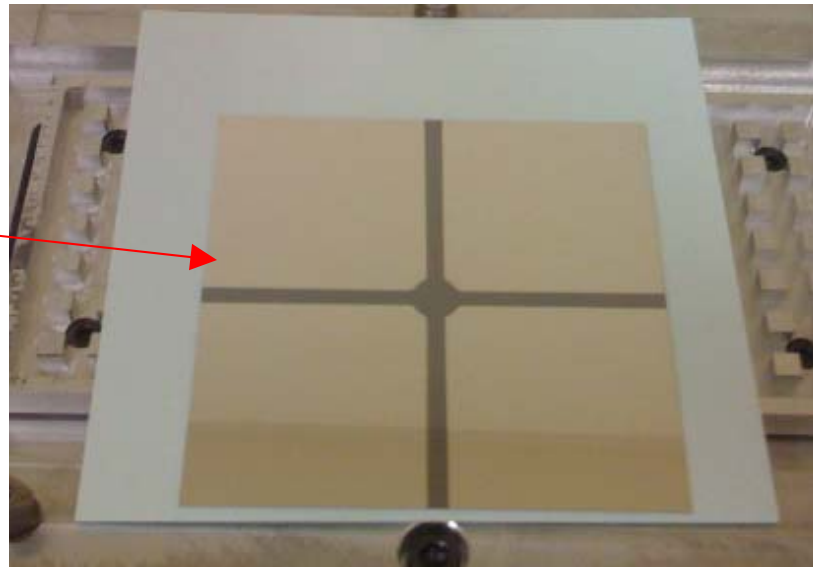
**5 or 6 μm resolution**  
if 1 or 2  
intermediate strip

*Important results on HPK test structures from sensors we bought together with HEPHY and IFCA. LPNHE will also participate to the new dedicated test beams at CERN in 2009*

# NEXT:

- New HPK sensors performance characterization with the new SiTR\_130-88 chips, first at the Lab test bench, and with the VA1' reference chips.
- Alignment system (M.Fernandez-Garcia, I.Vila and other IFCA team members) studies at a new Lab test bench using Laser IR system and the test set-up developed for the test beam at CERN (see Jacques' presentation). This Lab test set-up will be mounted at LPNHE next year.

HPK sensors treated  
for alignment



# Mechanics R&D

The LPNHE is involved in 3 main mechanics R&D aspects:

- New Silicon modules: basic element to build large area Si tracking architectures
- Developing the mechanical setup needed for test beam and lab test bench
- Integration studies: study of mechanical support structures and alignment issues

Mandatory: the development of the Lab infrastructure => great progress made this last year by our team despite real difficulties in terms of people and funding

# Mechanics infrastructure for Silicon detectors at LPNHE



SiLC testing room (upstairs)

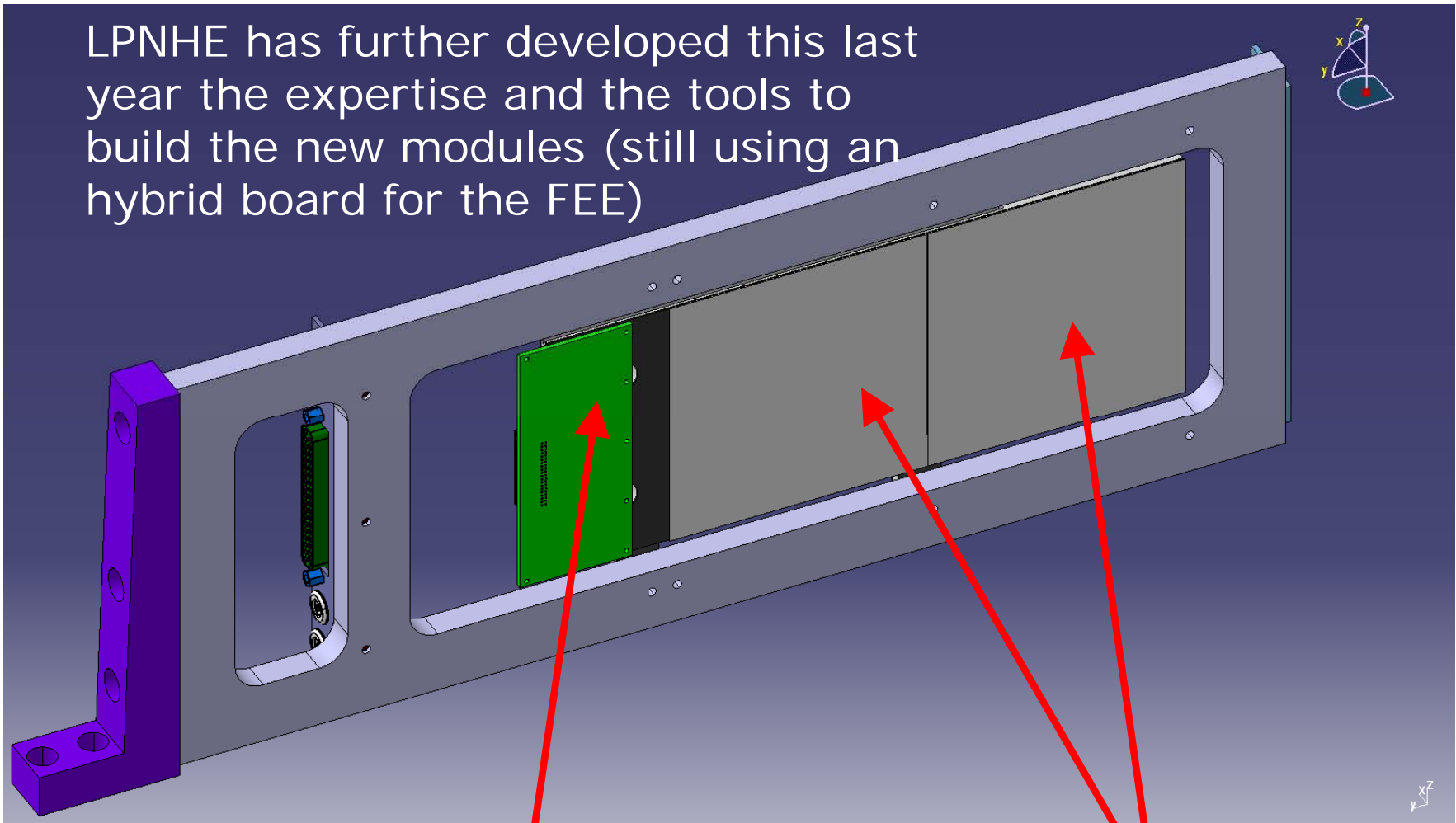
Mechanical room





## 2) Si Module: mechanical design&construction

LPNHE has further developed this last year the expertise and the tools to build the new modules (still using an hybrid board for the FEE)



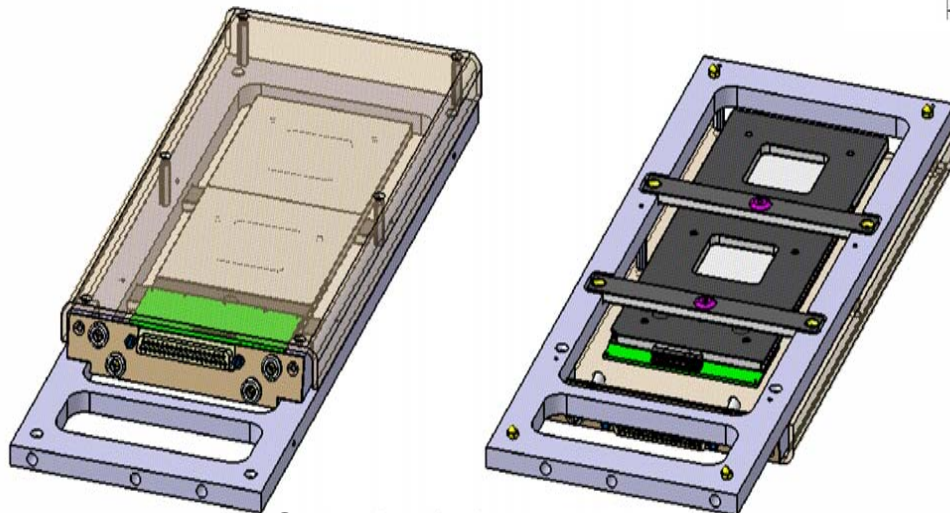
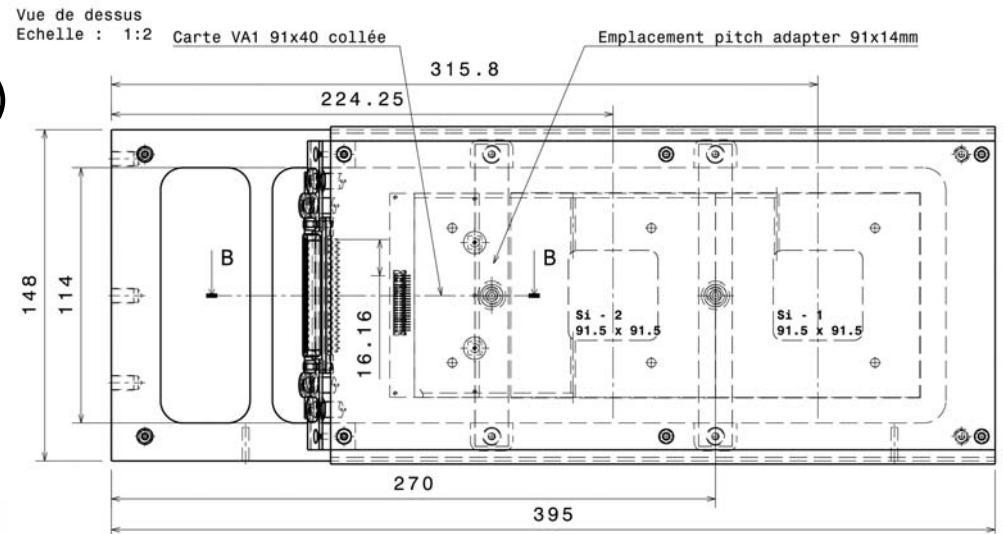
FE chip 130nm hybrid, is being soon replaced by direct connection of the FE chip onto the strips (collab with HPK)

2 HPK 6' sensors

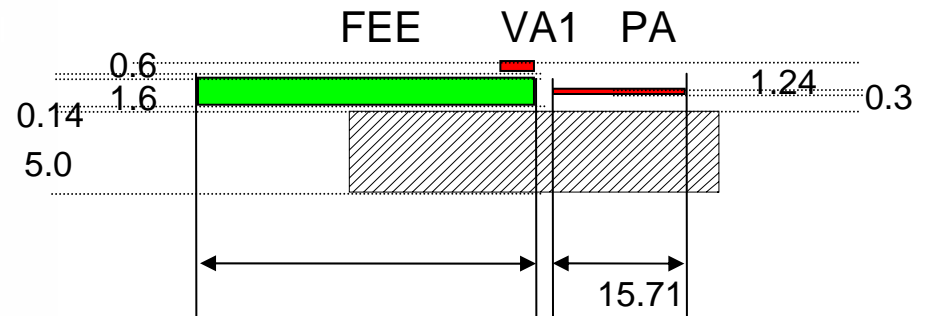
# Mechanical development

- Module conception (LPNHE team)

- Modules with two sensors
- Different FEE (chip development)
- Bonding constraints (I.McGill)
- Faraday cage integration
- Alignment study
- Easy and secure handle
- Study for global structure



Schematic view

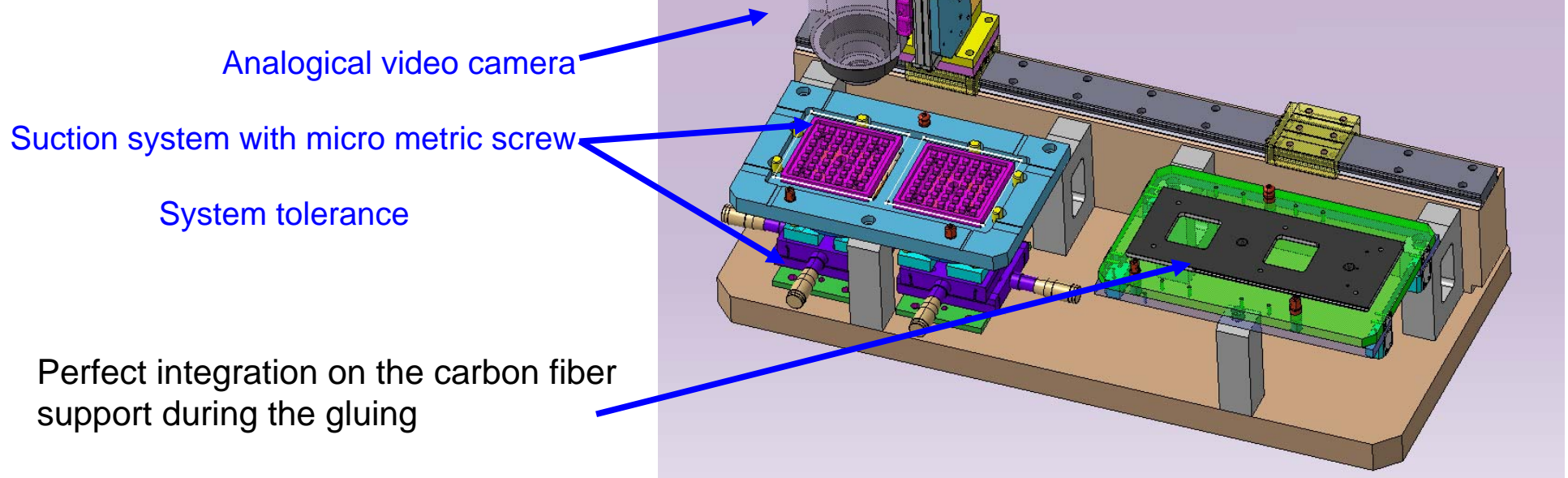


# Mechanical development

- Tools conception for “automated” manufacturing

Precise alignment of the different parts of the module::

- . silicon strips
- . pitch adapter connectivity
- . FEE



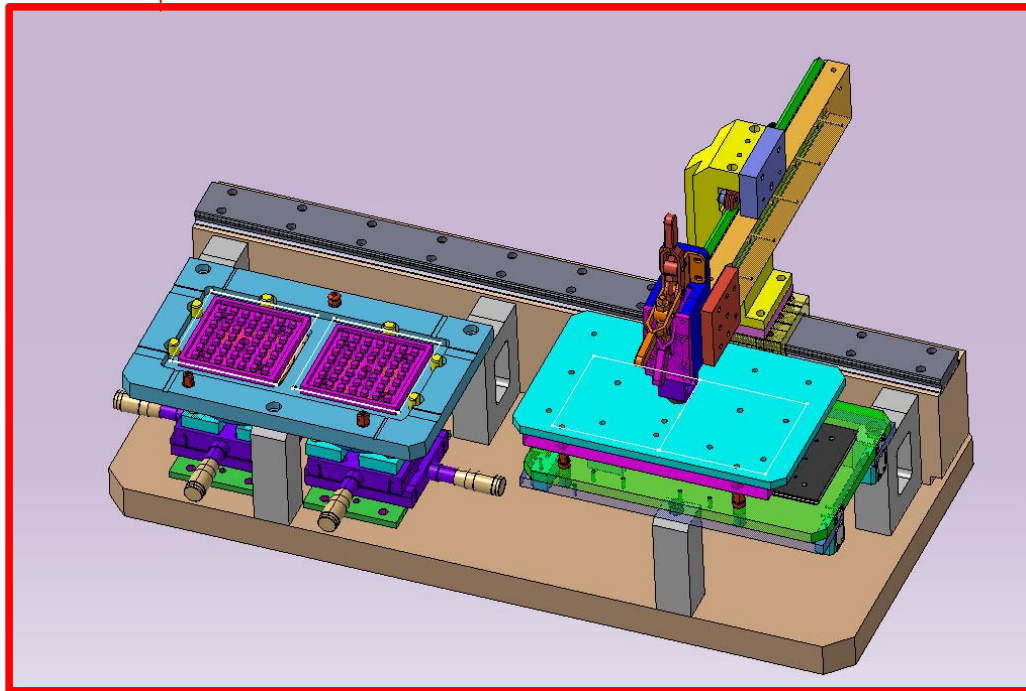
# Mechanical development

- Tools conception for “automated” manufacturing

- Keep alignment during the gluing process
- Perfect integration on the carbon fiber support during the gluing

Suction transfer tool

Gluing tool





# Mechanical development

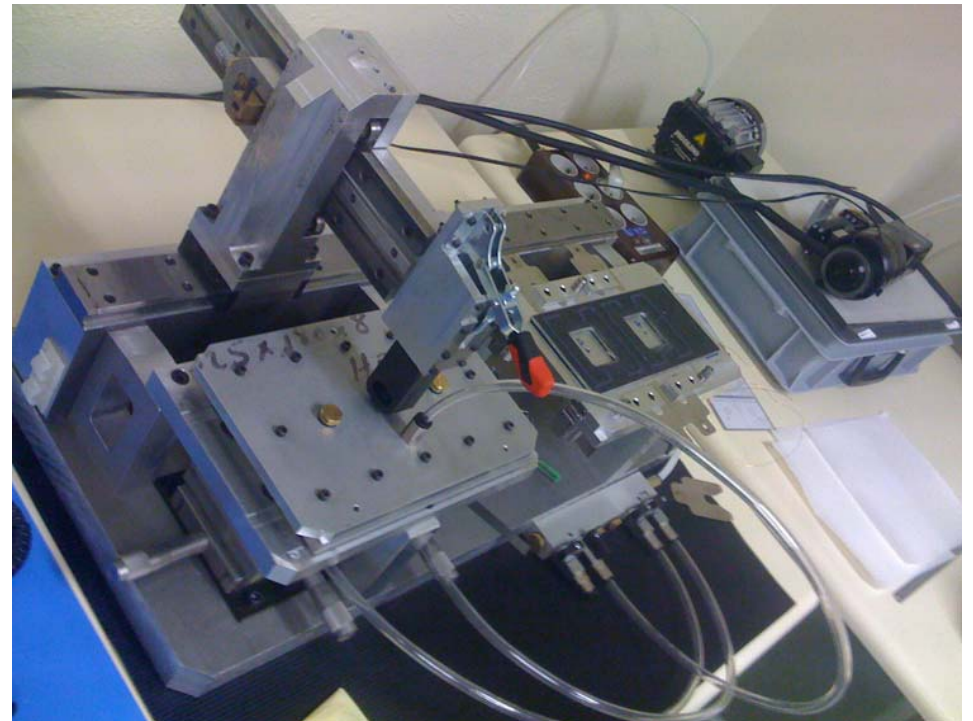
- Work environment

- Definition of the procedure and the critical point during the assembly
- Installation of the cleanroom and the first module is done



# Mechanical development

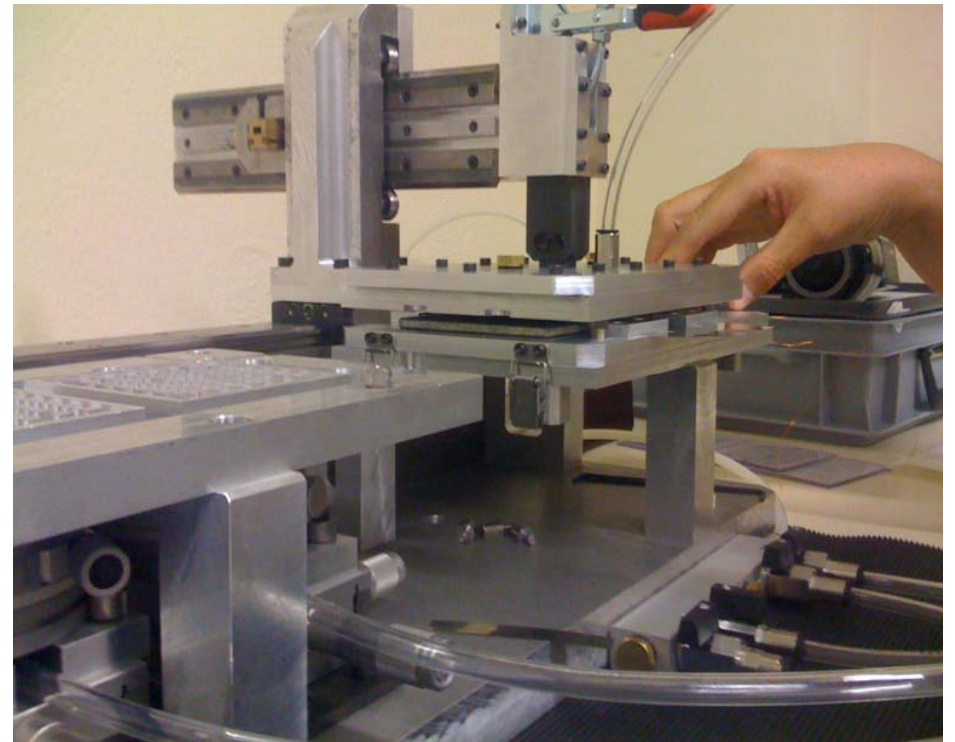
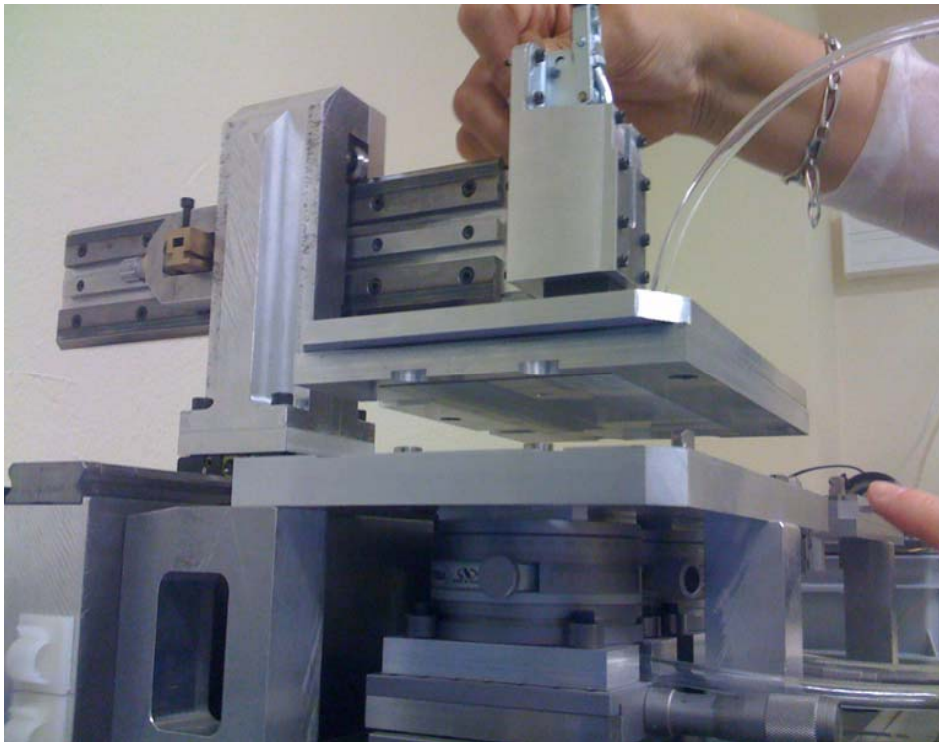
- Work environment
- Definition of the procedure and the critical point during the assembly
- Modules ready for the CERN November 2008 testbeam



# Mechanical development

- Work environment

- Definition of the procedure and the critical point during the assembly
- Modules ready for the CERN November 2008 testbeam

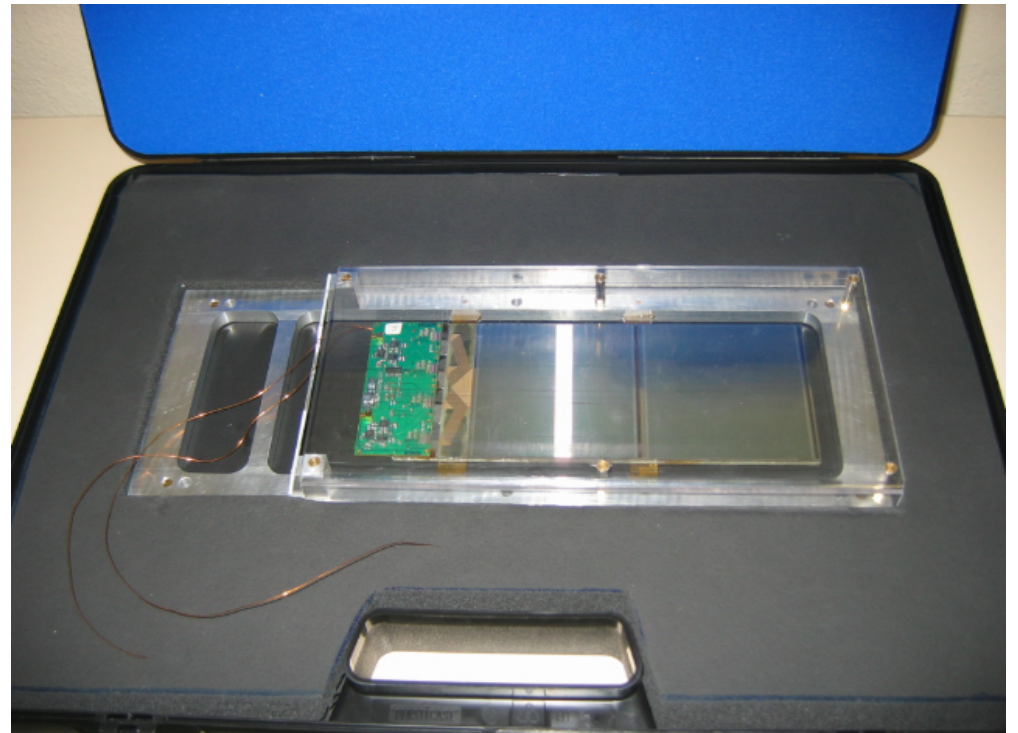
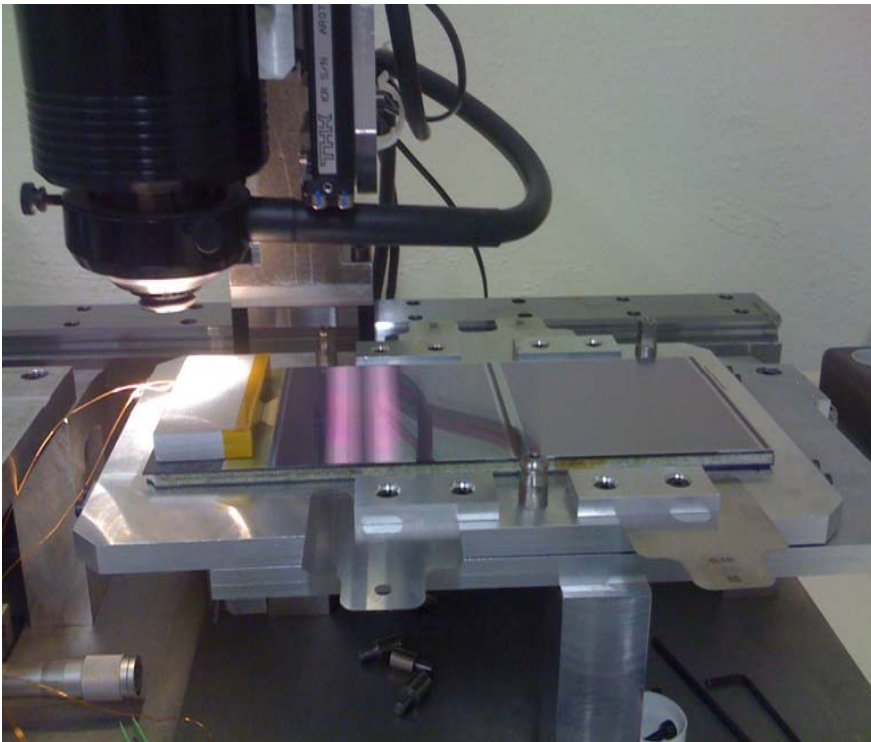




# Mechanical development

- Work environment

- Definition of the procedure and the critical point during the assembly
- Modules ready for the CERN November 2008 testbeam





## **NEXT:**

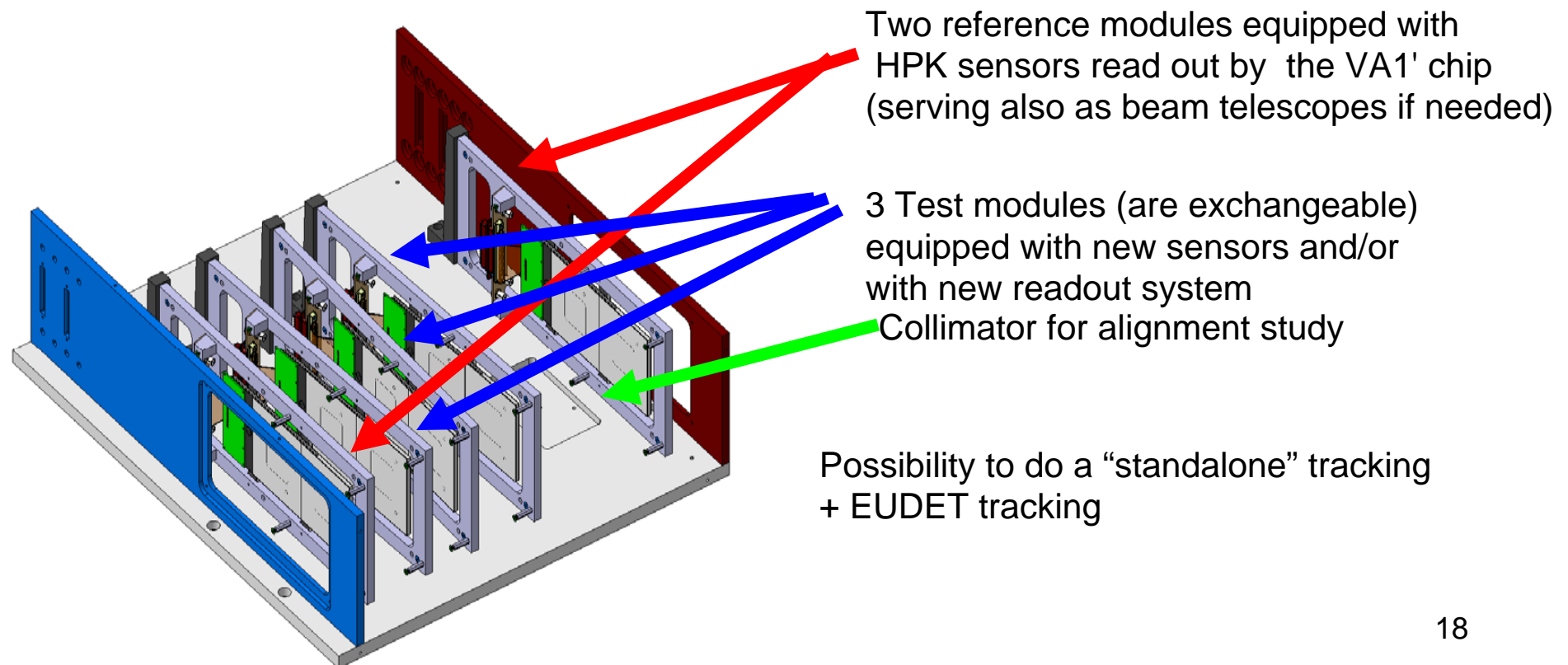
- 1) Developing an environment for modules manufacturing (G.Badet, A.Charpy, G.Daubard, J. David, C.Evrard, P.Ghislain, D.Imbault, P.Repain); also pursuing fruitful collaboration with CERN bonding Laboratory (A. Honma and I. McGill)
  - parameters of HPK sensors: dimension, pitch, transparency
  - Development of toolbox
  - Clean room installation
  - Developing expertise for working with these types of (special and delicate) detector and the needed environment for all the members of the ILC-LPNHE team.
- 2) New direct connectivity of FEE with strip detectors in collaboration with industry (presently HPK, LPNHE and a few other SiLC institutes) (see electronics section)
- 3) Developing further expertise in collaboration with other Labs in SiLC (Liverpool, IFIC...), and
- 4) Pursuing R&D towards the new elementary Si module responding to all the requirements of next generation Si trackers (synergy with LHC upgrades)

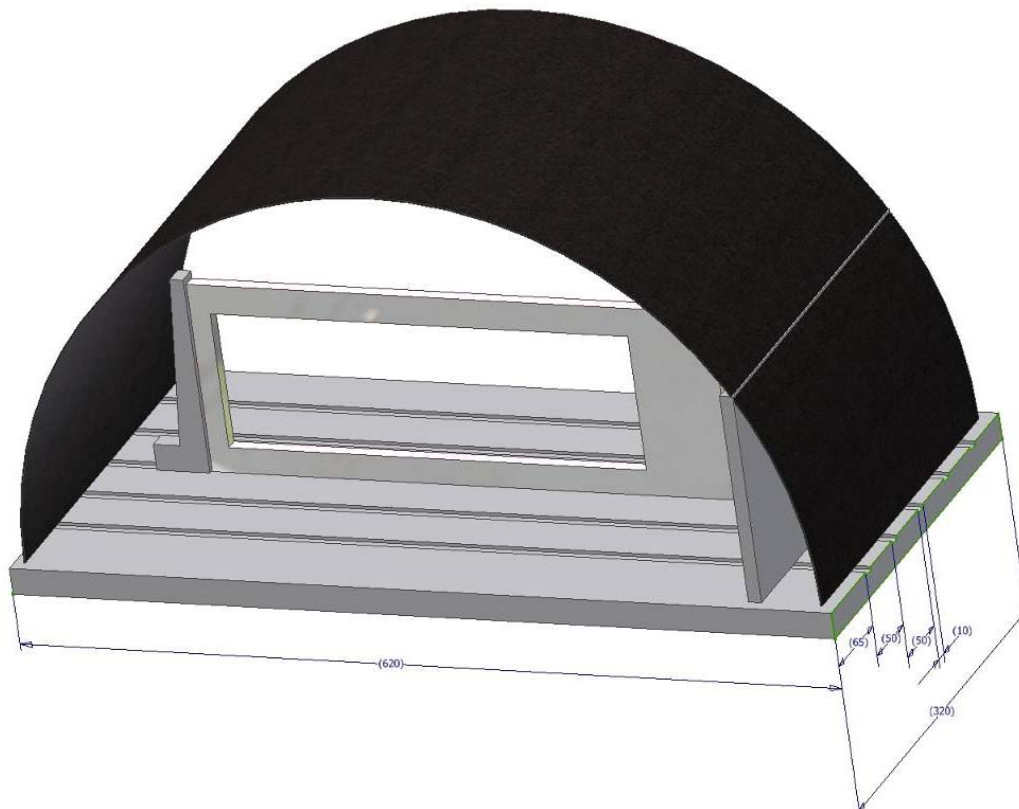
## 2) Mechanical development for test beam and lab test bench

Ex: Faraday cage new configuration

Developed with V. Saveliev and DESY; Next version will be made of composite material (developed in the framework of PiCS with Russia), see next slide

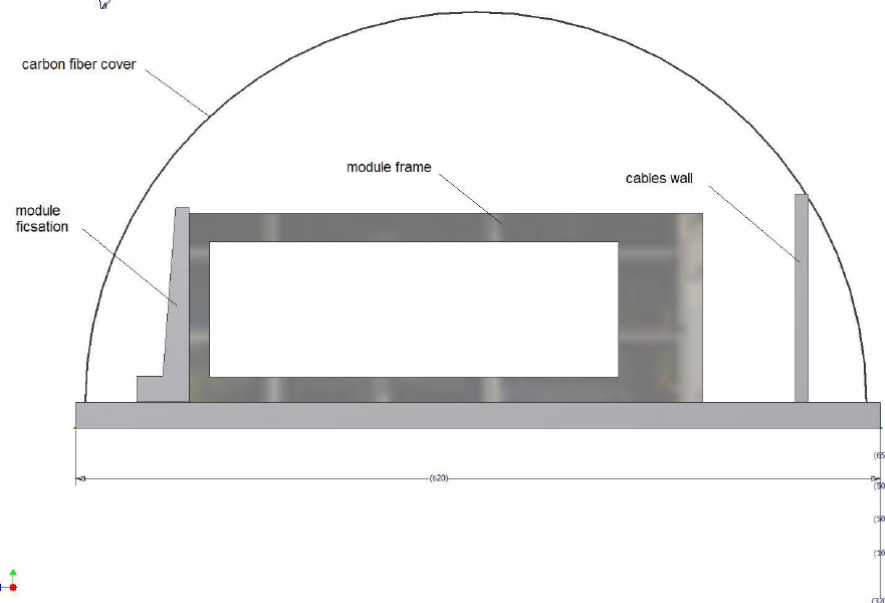
Present configuration:





system prototype of the  
module box (OSU):  
This structure has the half  
cylindrical shape as needed  
in real-life for  
cylindrical layers of Si  
detectors (ex: innermost part  
of the Si components in ILD  
design)

No cooling foreseen, because  
low power dissipation of the  
FEE.



### 3) Integration mechanical studies:

- The LPNHE team is starting to be involved in the design and studies of the integration studies for the Silicon tracking systems in the various ILC detectors (see later).
- The LPNHE mechanical team has a large expertise and is interested in contributing but lack of manpower to fully contribute.
- The LPNHE team also participates to the studies and discussion on the alignment methods and issues (crucial for the Physics)

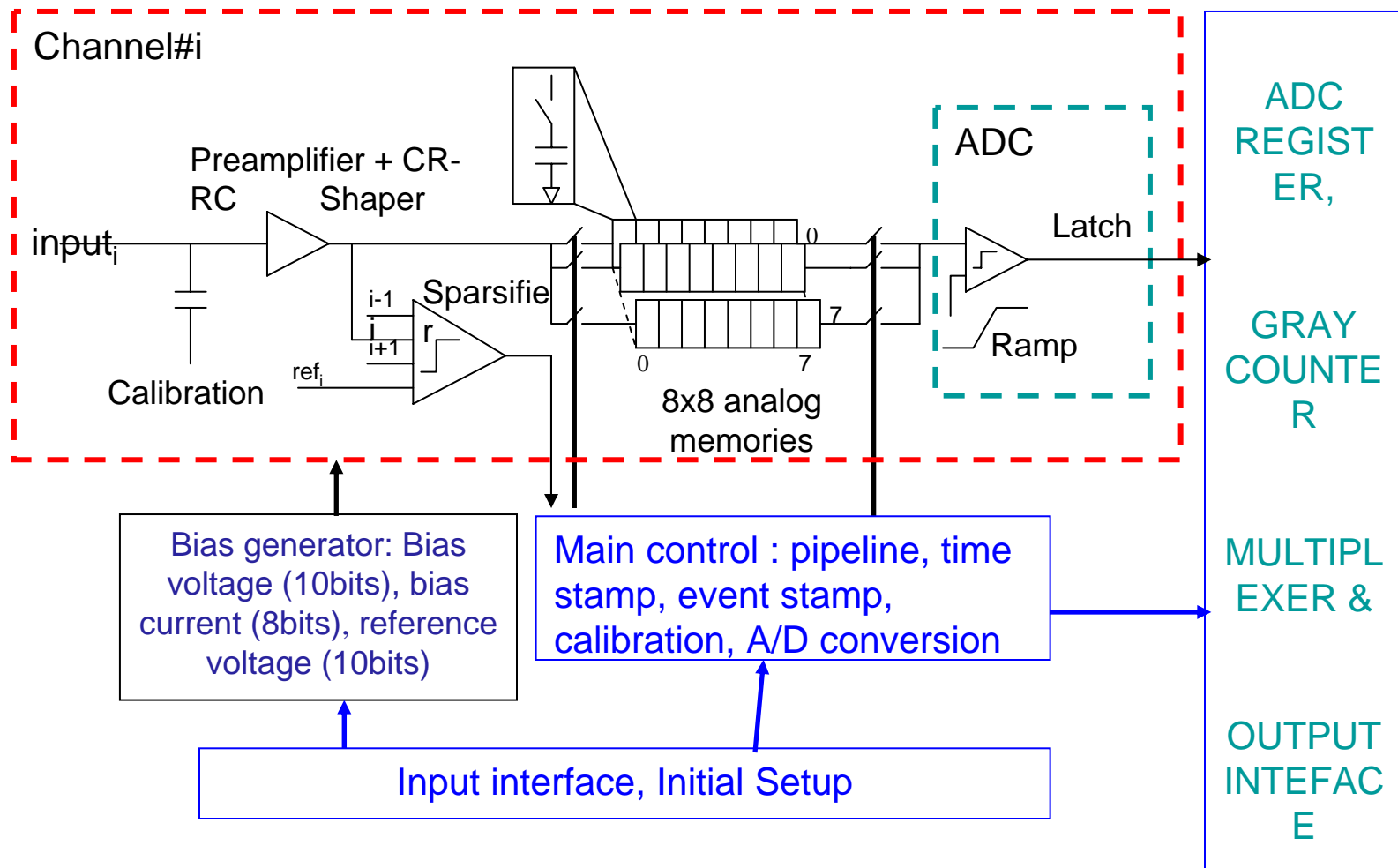
# R&D on Electronics

The ILC-LPNHE is involved in the following developments:

- FEE and readout chip in CMOS deep sub-micron electronics: new version achieved in 2008 = SiTR\_130-88 (see Hung's presentation) with U.B. and IMEC
- Direct connectivity of the FE chips onto the strip module
- Developing the next electronics stage (DAQ framework) see A.S.N. presentation at LCWS08 (DAQ session).
- Developing the complete DAQ system for the test beam set-up (see Jacques's presentation)

# NEW IMPORTANT ACHIEVEMENT:

## ***FEE complete architecture delivered in 2008 with SiTR\_130-88***



# Direct connectivity FEE & strips

- A first step is underway in collaboration between LPNHE and HPK, based on bump bonding and using the SiTR\_130-88 chip and the presently delivered HPK sensors.
- Other firms and Institutes have expressed interests in collaborating with us on this issue (under study: important not to be only dependent of HPK)
- Next step is 3D vertical interconnect: ILC-LPNHE is taking part to the global effort (ASN participation to the last Ringberg workshop in 2008).

ILC-LPNHE is part of the IN2P3-FNAL collaborative effort and of the ANR Vitesse.

Also involved in the setting up of the global worldwide effort on this topic.

# Next version improvements

- Go to basic blocks of 256 channels and build modules of 512 channels or 1024 out of them (multiplexing factor is still under investigation)
  - Thinning of the chip
  - Next version in full wafer process (gain in space)
  - Include latest results from the tests on the present chip
  - Try the 90 nm CMOS technology
- 
- For the longer term it is intended to prepare a fast version CLIC-like
  - Pursue the direct connection chip onto the strip detector (bump bonding now, and starting to investigate 3D vertical interconnect as part of the global effort)

**NOW WE ARE WORKING ON TESTING THIS CHIP!!**



# DAQ for Test beams

This last year the LPNHE has developed a full standalone framework able to be included in any combined test beam or to work in standalone.

This includes the development of the needed DAQ hardware (presently based on FPGA-USB developed by U.B.) and the associated DAQ software based on VHDL, C++ and ROOT (see next slides and Jacques's presentation).

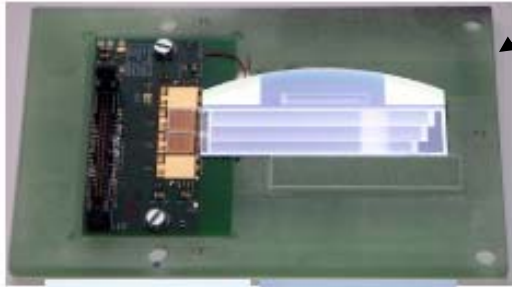
Important achievement and completion of a main deliverable for the EUDET project.

This overall system will be used for the forthcoming test beams in 2009 (see next) and has been first experienced in a short test beam period Nov 4 to 7<sup>th</sup> at the PS CERN (parasitic mode).

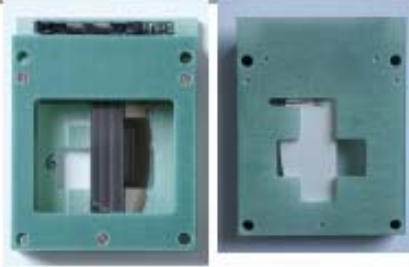
Will also be used for the dedicated Lab test bench on alignment studies in 2009.

# Test beams activities

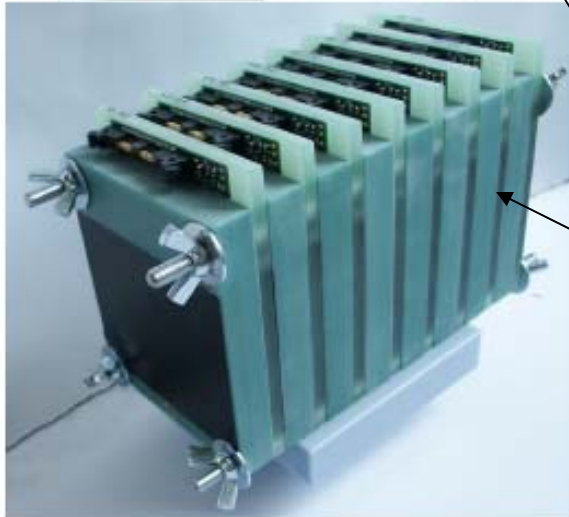
- Test beam of HPK sensor structures (June 2008) done by HEPHY Vienna and CU Prague (LPNHE will contribute next year)
- Test beam preparation for the LCTPC in DESY (since early 2008) (HEPHY, IEKP, LPNHE)
- Test beam with a standalone Si tracking system at CERN (Nov 2008) (several SiLC institutes)



HPK test structures read out with APV25 FE system.  
In 2009 will be equipped with new SiTR\_130-88  
FE readout system.



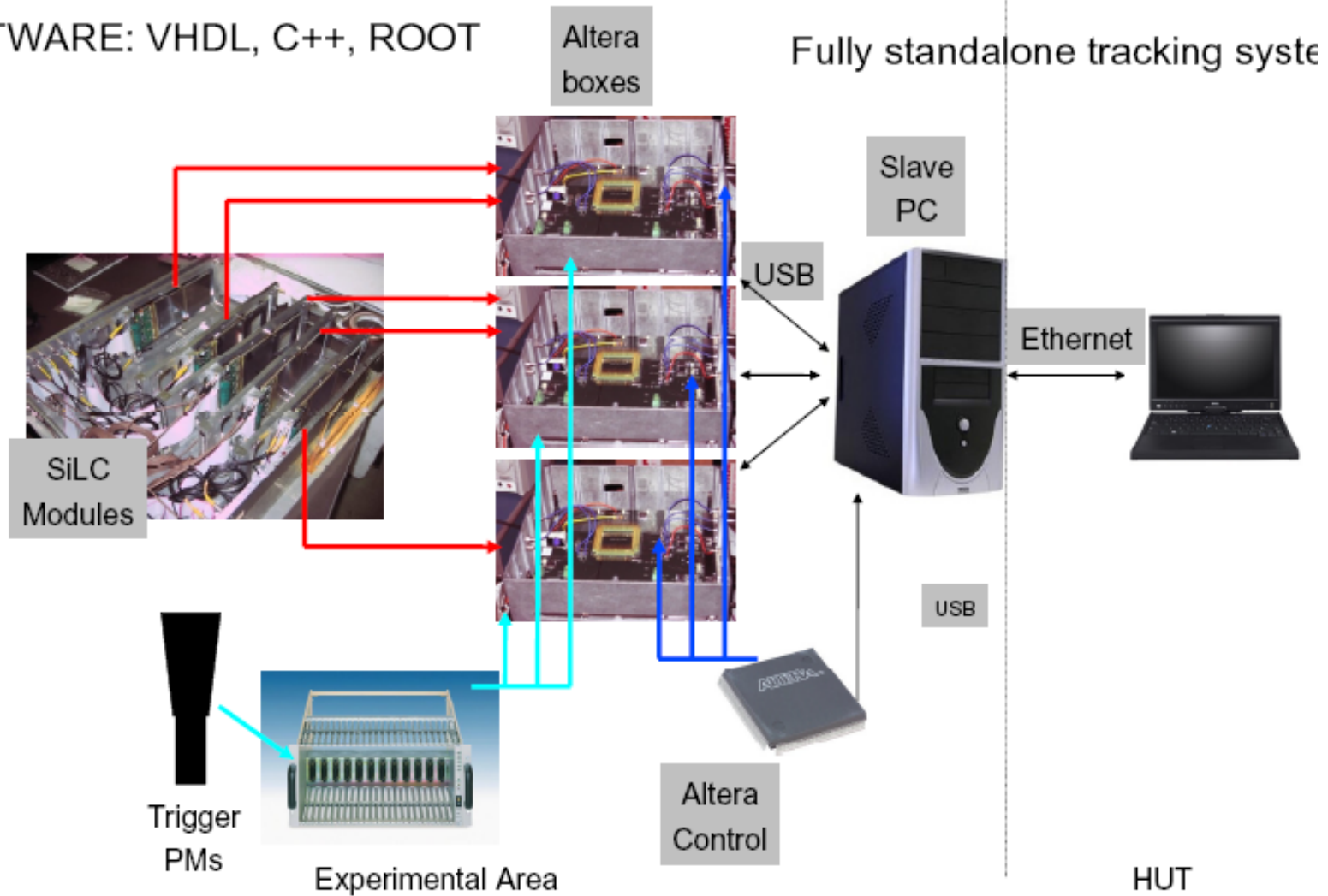
Tests of structures performed with  
HPK test structures at the SPS-CERN  
Next year another test run where  
LPNHE will take part. Instrumental for  
a detailed characterization of Silicon sensors  
and optimization of the best sensor strip  
design



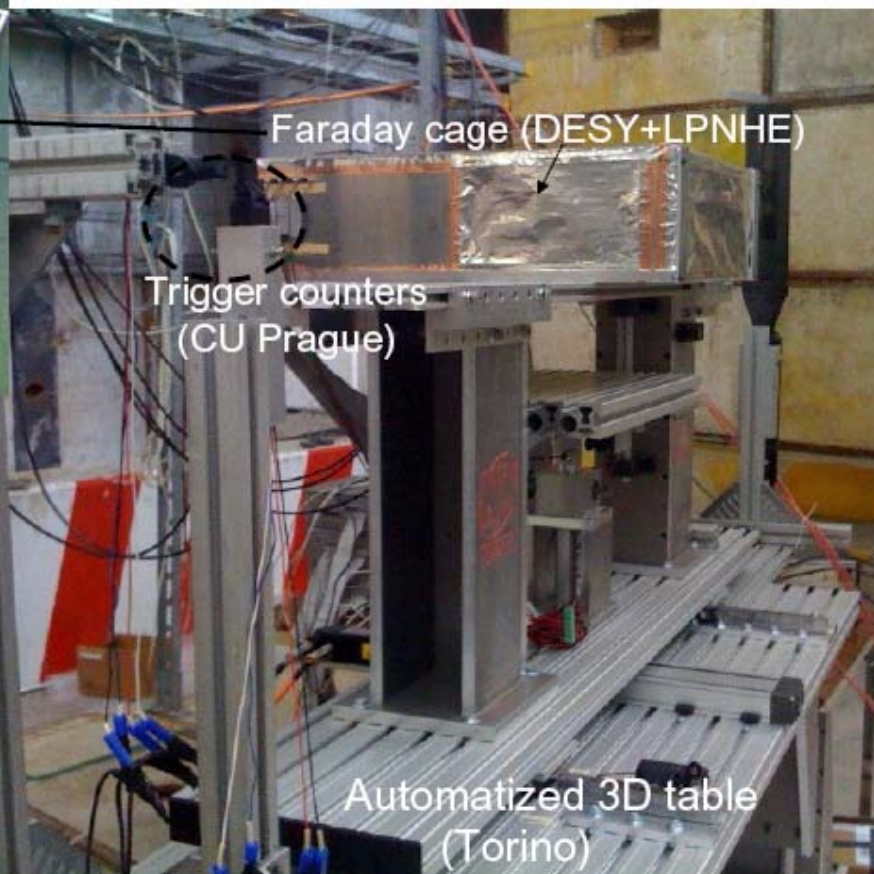
8 structures equipped with APV25 FE readout  
Installed in between the 2 parts of the EUDET  
Telescope.

Test HPK structures CERN SPS  
(HEPHY+CU Prague), June 2008

SOFTWARE: VHDL, C++, ROOT



# Test beam at CERN in November 2008: *towards a fully standalone Silicon tracking test set-up*

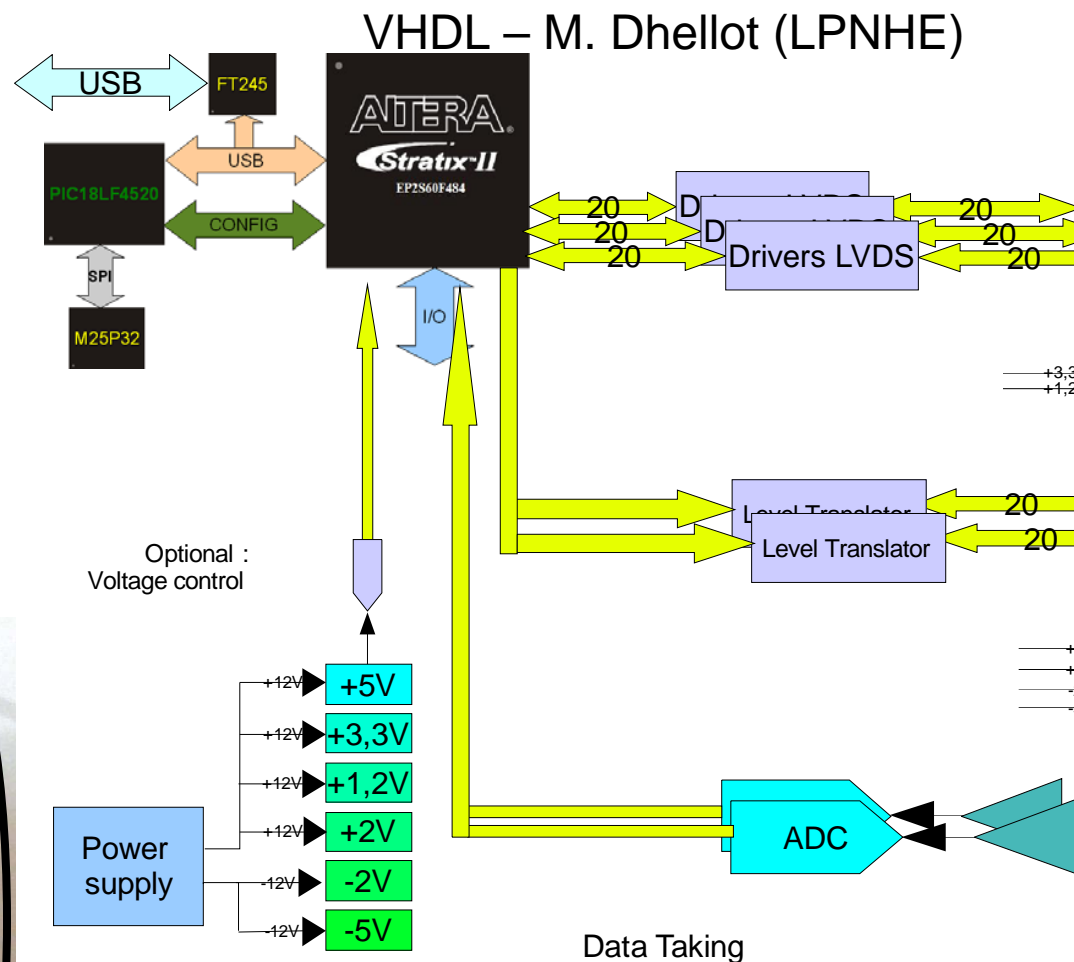
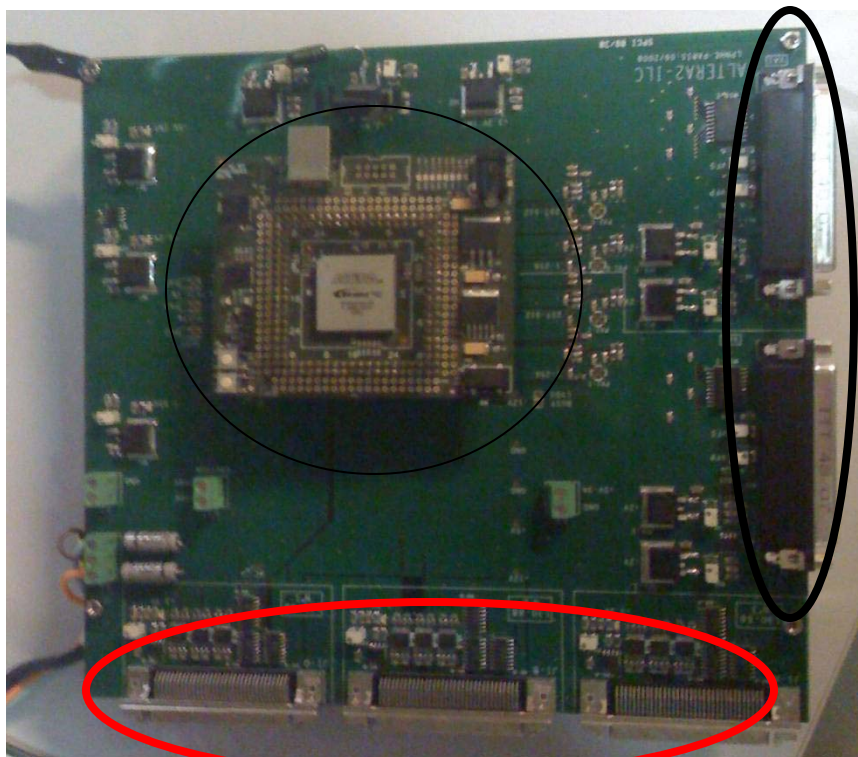




***Barcelona U. + LPNHE***

C++ code: A. Charpy (LPNHE)  
Data ana: C. Ciobanu (LPNHE),  
P. Knasnicka (Prague)  
A. Comerma (Barcelona) debugging  
and post-CERN VHDL/C++

## The FPGA board

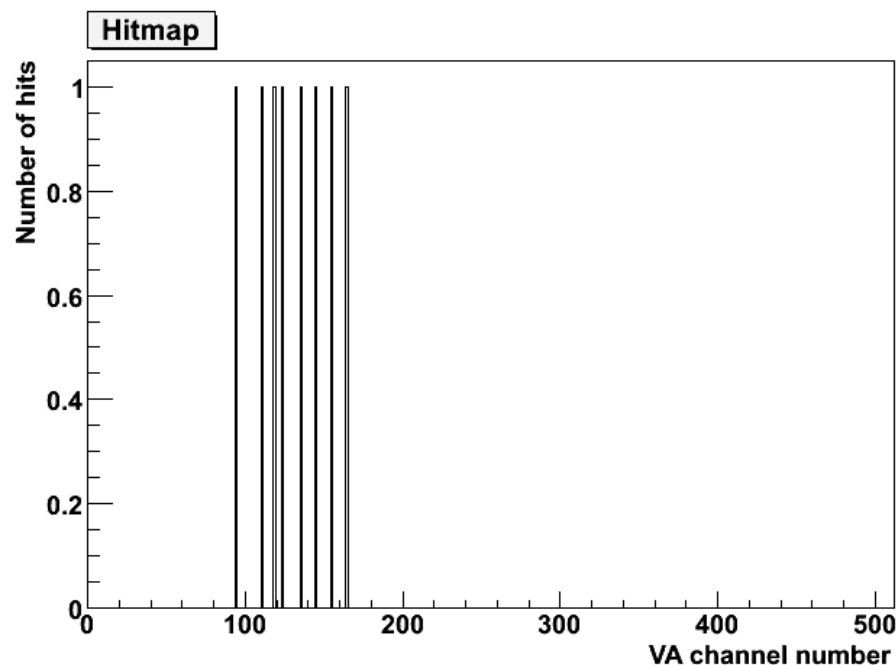
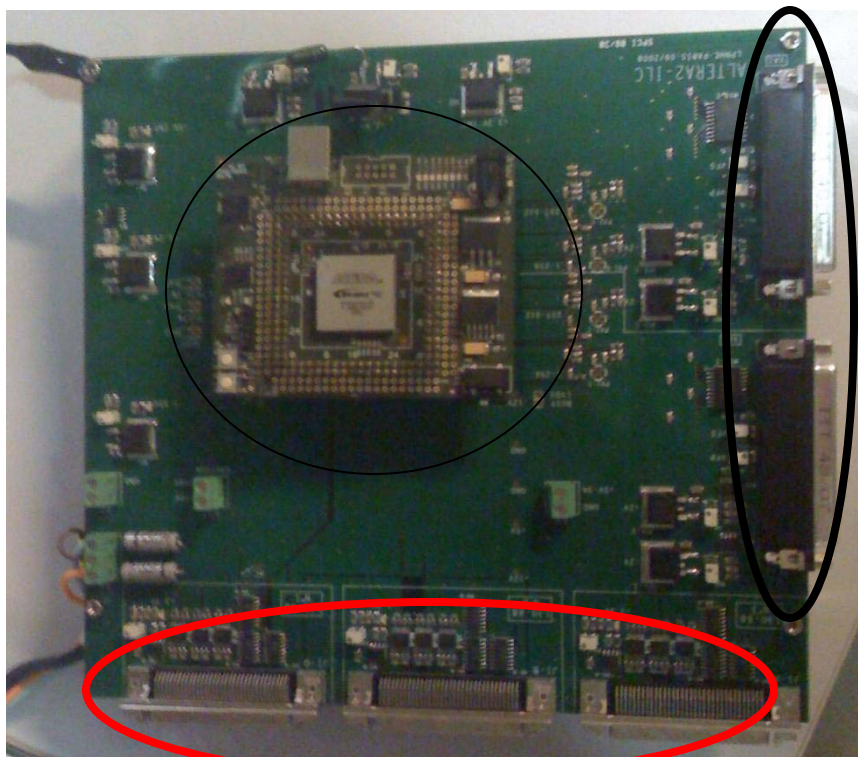


Last day at CERN succeeded in acquiring **up to** ten successive triggers (small step for the mankind).

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The FPGA board



Last day at CERN succeeded in acquiring **up to** ten successive triggers (small step for the mankind).

# NEXT: test beams in 2009

- Standalone test beam with new SiTR chips at DESY (April 2009)
- Including the new SiTR\_130-88 chip readout in the LCTPC test (summer 2009)
- Test beam at SPS CERN of Si sensor structures with EUDET telescope and of the standalone system in November 2009
- Test beam at FNAL in 2009 under discussion with FNAL upon request of FNAL and other American SiD teams (M. Demarteau+ASN)

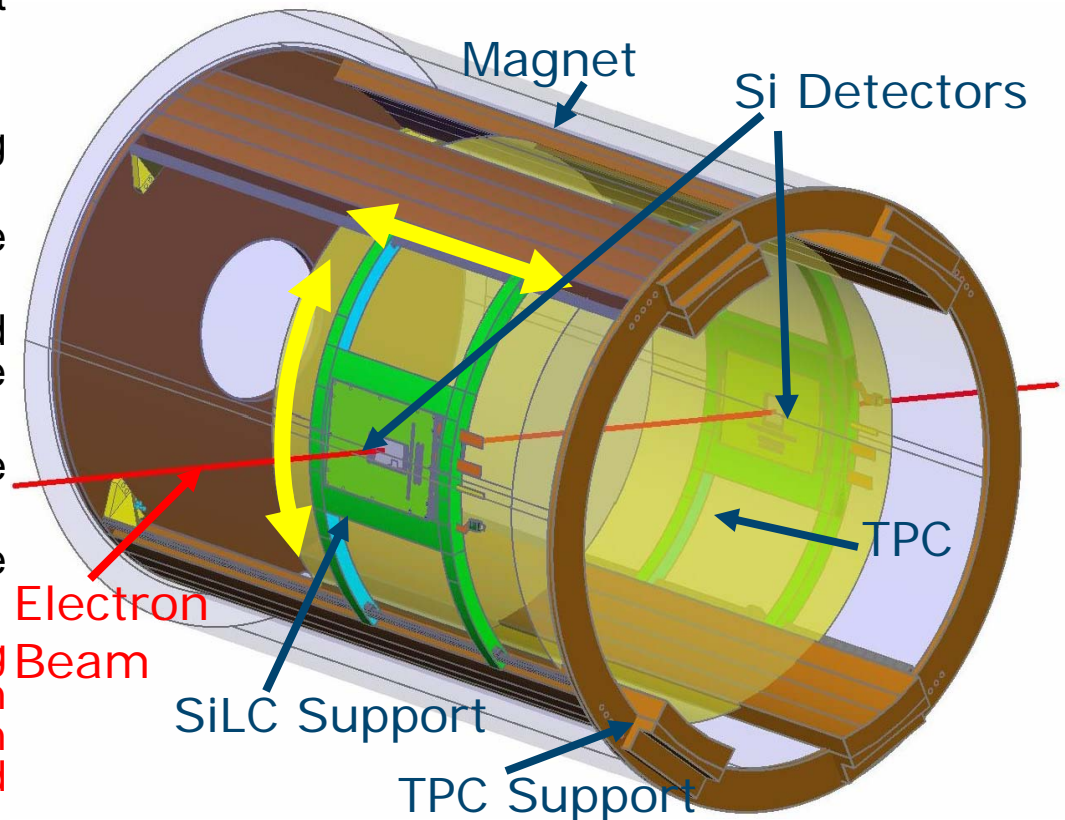


# LP-TPC: Silicon Envelope

(HEPHY, IEKP Karlsruhe, LPNHE)

- **four silicon modules** will be installed (feb 2009)
  - two in front and two behind the TPC, with respect to the e-beam
    - two independent support structures are needed
  - on each side:
    - one horizontal module consisting of two daisy-chained sensors
    - and one vertical module consisting of one sensor
- **movable support system** is needed because it must be possible to scan the TPC
  - the TPC and the magnet will move relative to the beam
  - the sensors have to stay inside the beam line

The LPNHE will contribute in including the new FE chip read out between spring and summer next year, in replacement of present APV25 read out.



# Simulation studies

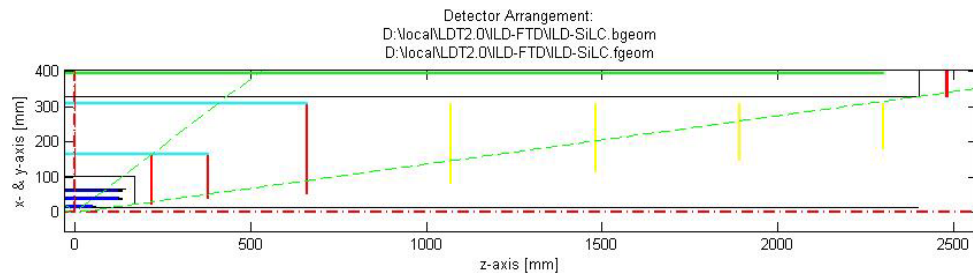
- LicToy: imported at LPNHE from HEPHY Vienna (useful for preliminary optimization studies)
- MOKKA: main GEANT-based full simulation for ILD; in collaboration with V. Saveliev via PICS project.
  - ALL 4 Si components for ILD have been included in 2008 and are part of the reference design optimization study for ILD- LOI (ASN & V. Saveliev).

Maintenance of geometry DB (V. Saveliev+ A. Charpy) Evolving with detector optimization and integration.

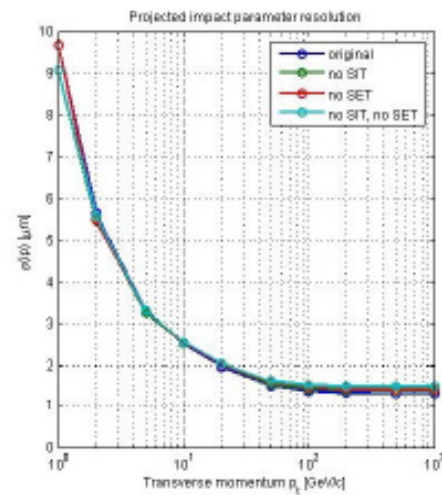
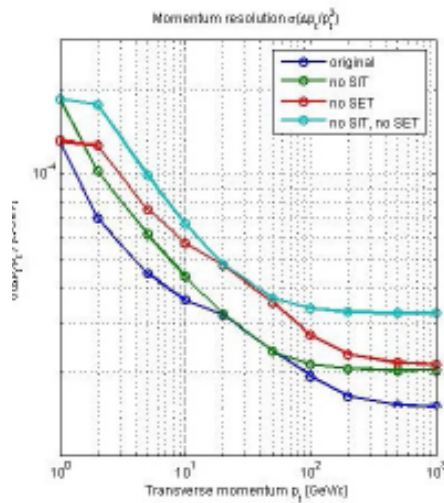
- ILCROOT: expertise from ALICE ROOT (A. Charpy). Used to develop two tracking strategies: TPC + Si components and all Silicon Tracking.

Collaboration with FNAL (base of ILCROOT) and Italian developers (see Alexandre's presentation).

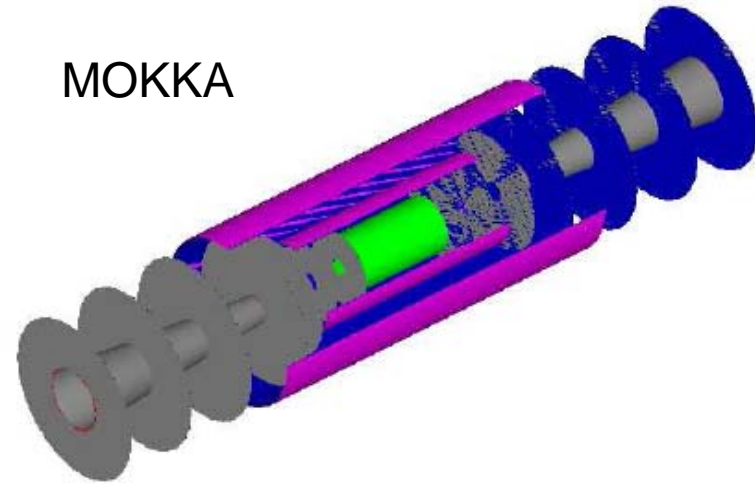
Aim: to compare both tracking concepts, underway.



## LICTOY for fast detector studies

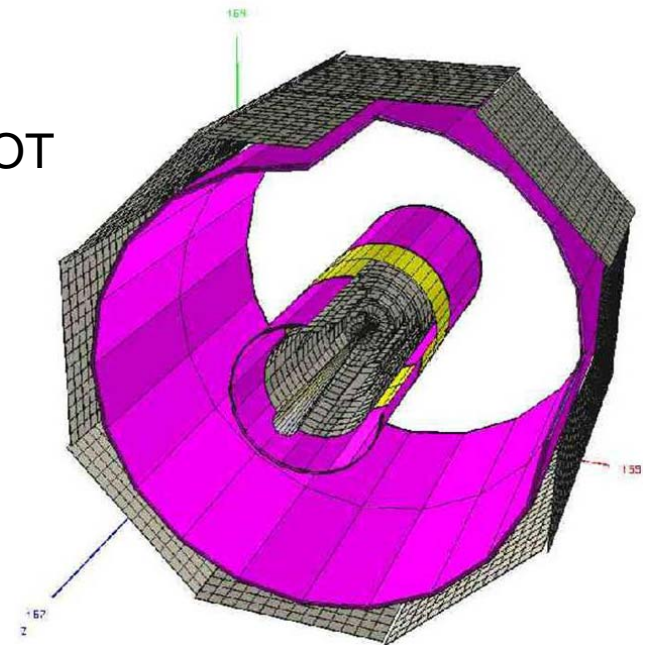


## MOKKA

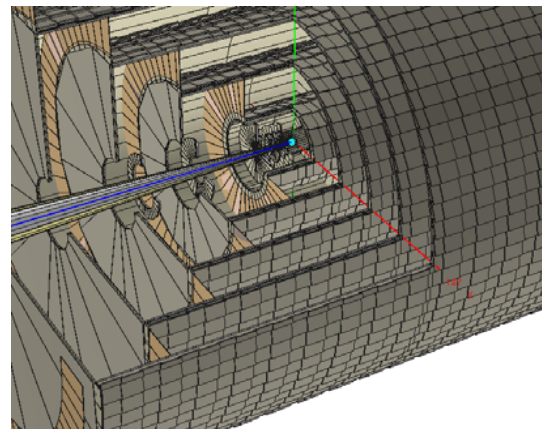


Detector model for the Silicon Intermediate Tracker and the Forward Tracker Disks of LDC in the MOKKA simulation framework (the green colour component is the VDX).

## ILCROOT



Some examples of the available simulation tools:



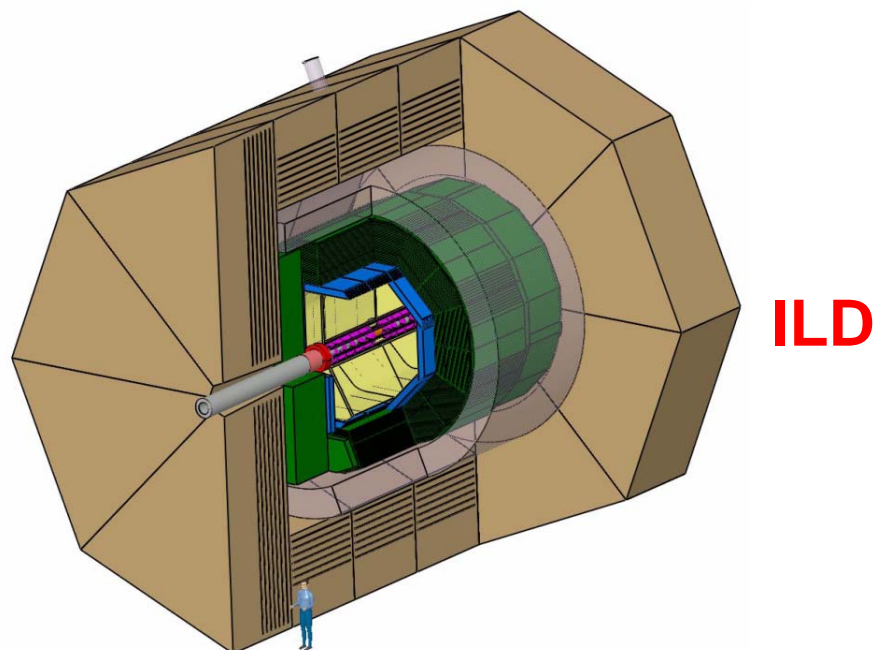
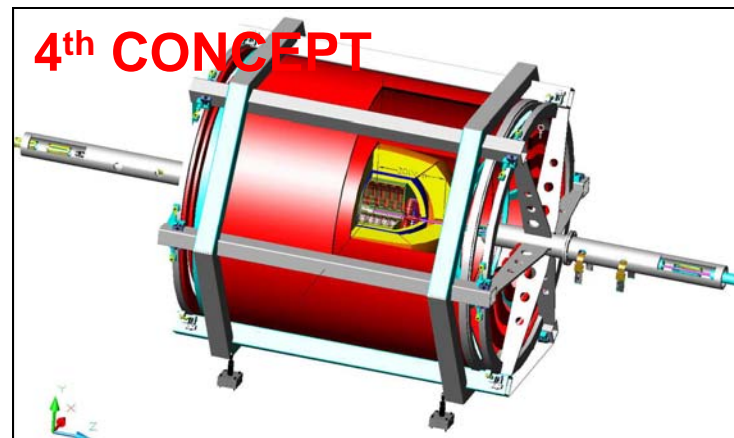
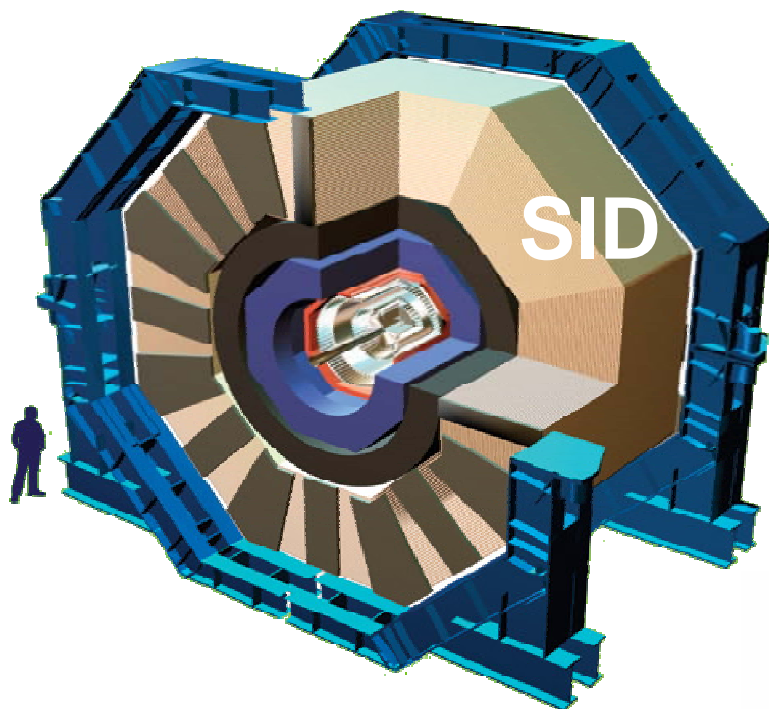
# Integration studies and issues

- The SiLC collaboration is a generic R&D collaboration that applies to all 3 detectors presently considered for ILC and submitting LOI's.
- Indeed the 3 ILC detectors: ILD, SiD and 4<sup>th</sup> concept are soliciting SiLC assistance for the Silicon tracking.
- The LPNHE is instrumental in developing and optimizing the Silicon tracking system for these 3 detectors.
  - Major involvement in ILD
  - Natural involvement in SiD with main collaborative contacts with FNAL SiD team (B. Cooper & collaborators for the overall mechanical design)
  - Starting collaborative studies for Silicon integration in the 4th concept design (solicited by this detector from the beginning of 2008).

LPNHE has a leading role on these studies.



# Si Tracking for all 3 ILC detector LOI's



# Integration cont'd

LPNHE has set-up a collaborative effort with Torino U. and OSU for detector integration studies in conjunction with simulation studies and tools development

**Main focus: ILD Silicon component integration** (see example for SET component in next slide)

- Contribution to the inner Silicon tracking is foreseen in collaboration with all the other components in this region and MDI.

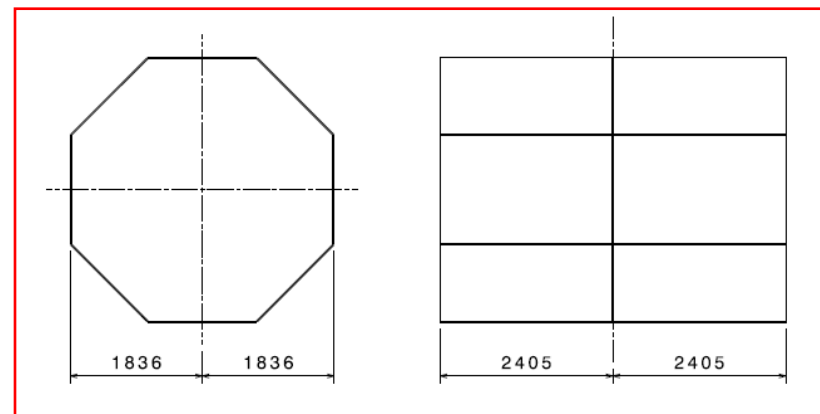
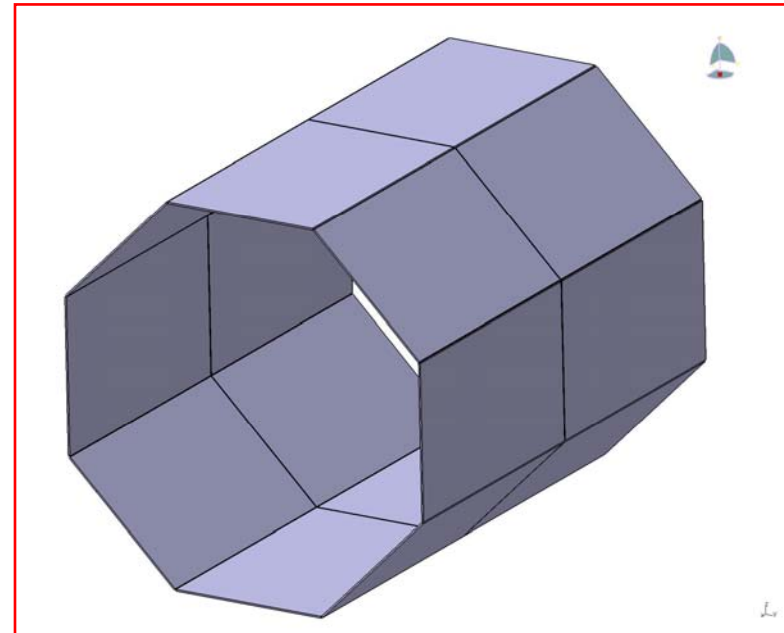
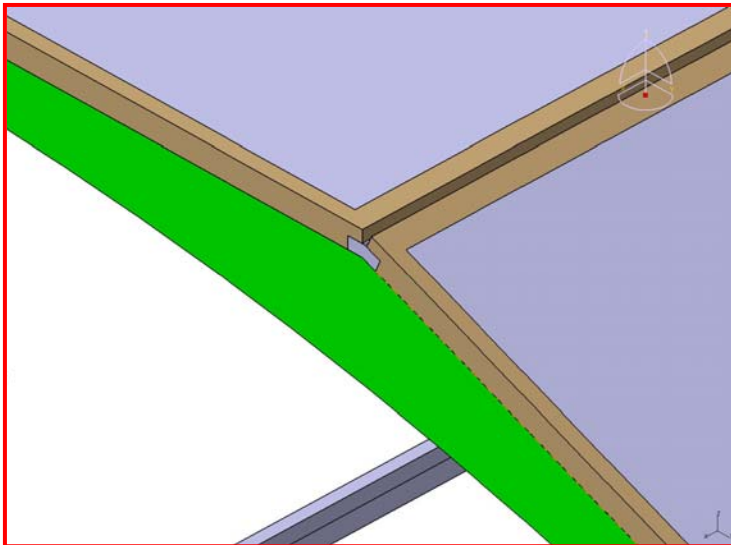
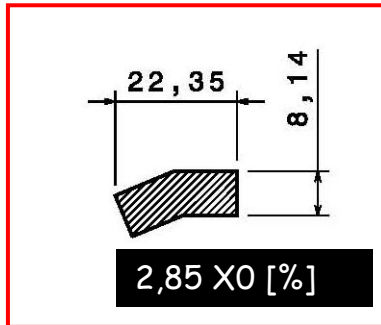
A preliminary integration set-up of the SIT+FTD will be provided for the ILD-LoI by LPNHE based on previous preliminary studies (last LCWS08 ILD meeting)

- LPNHE main interest is on building the ETD (end cap) component

# Ex: SET mechanical structure

Collaboration between Torino, Obninsk  
and LPNHE, design by P. Mereu (T.U.)

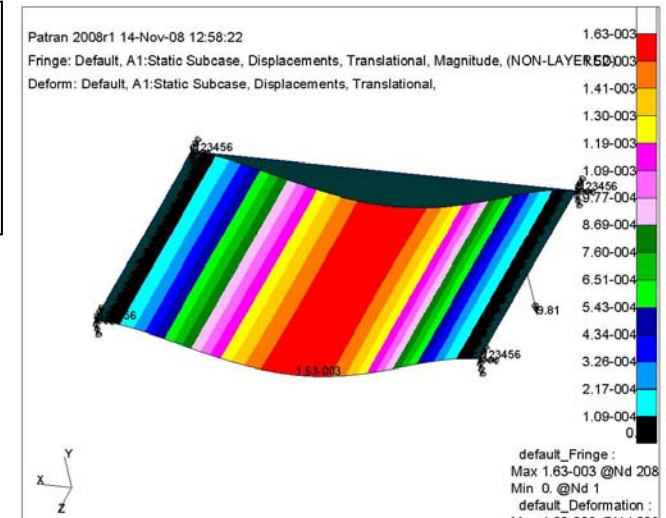
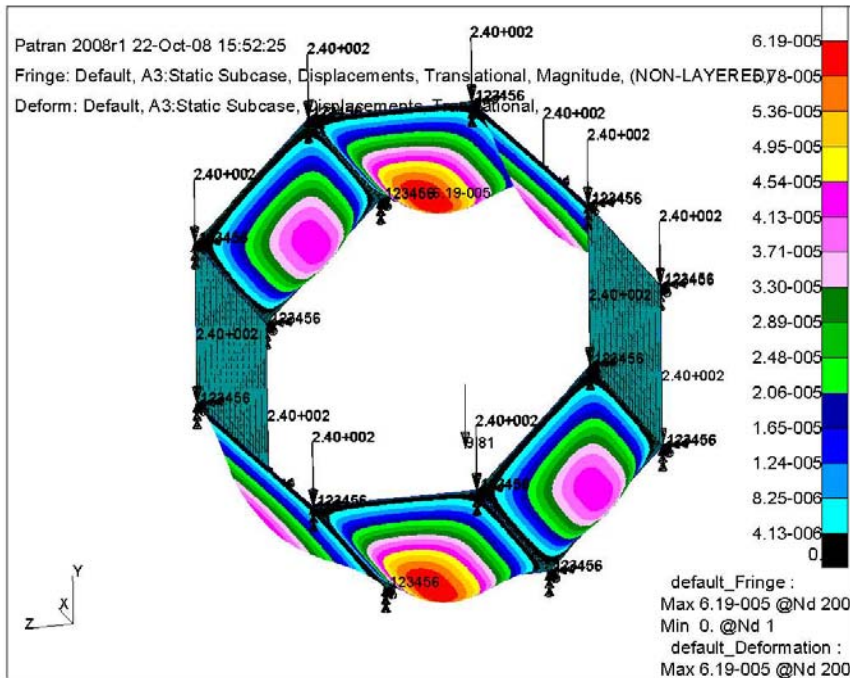
Each panel is constrained at 4 sides;  
-> 3 support rings on TPC



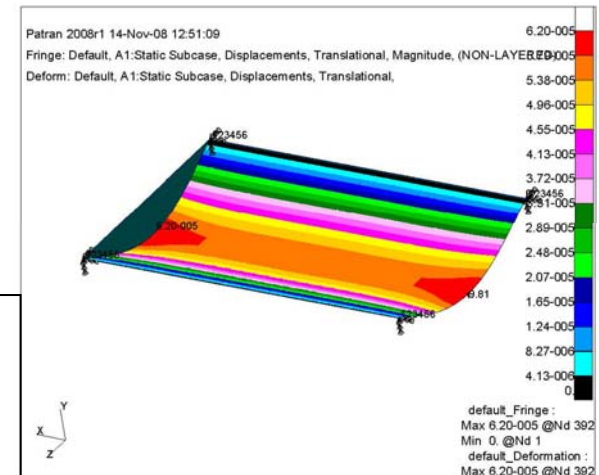
# Ex: SET mechanical structure

constrained on short sides;

- 8,9 kg dead load;
- 3 kg payload.
- MAX deflection: 1,6 mm



STATIC DEFLECTION OF ONE PANEL



constrained on long sides;

- 8,9 kg dead load;
- 3 kg payload.
- MAX deflection: 62 micron



# Further integration studies

Pursuing discussion on detector integration for SiD:

- Several preliminary discussions between Aurore and the SiD tracking mechanical FNAL experts (B. Cooper et al).
- Study of alternative design to:
  - => the central barrel (more layers & two-sided layers)
  - => the end caps (XUV instead of projective layers).

Comparison between these two all silicon tracking designs is undertaken with simulation studies ILCROOT based. Expected results for March 2009.

# Contribution to LOL's

- All these R&D activities are bringing key information to write the Lol's due in March 2009.
- Simulation studies and developing the mechanical concepts to build these tracking components on mechanical key questions.
- LPNHE (ASN) in charge of writing the Si tracking part for the ILD-Lol
- LPNHE contributes also to both SiD and 4<sup>th</sup> concept in different ways.

# Perspectives and concluding remarks

- Over the last year the SiLC collaboration has made significant progress:
  - Sensor development
  - Mechanical development
  - Electronics development
  - Simulation
  - Integration
  - Test beams
- More work and resources needed to keep or improve this rate of progress
- Short term: contributions to Lol's
- Longer term: expanding our efforts to stay in tune with the evolution of the technology and concurrent developments in the field
  - eg CLIC studies