CPPM seminar – Feb. 22th 2016

From Vertex Detectors to Inner Trackers with CMOS Pixel Sensors

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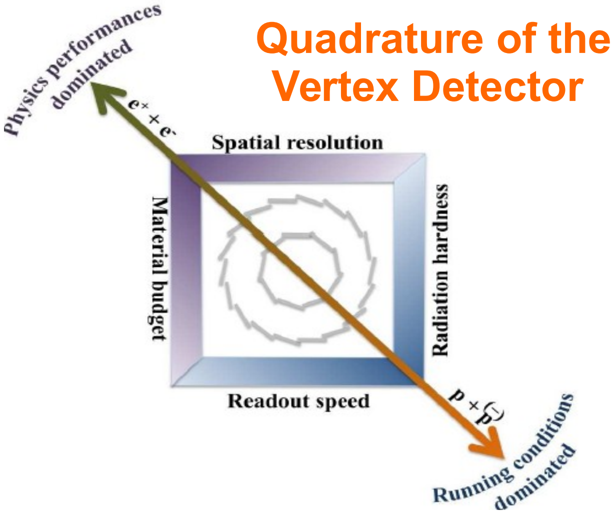
PICSEL GROUP

Outline

- Introduction to CMOS Pixel Sensors (CPS)
- CPS adapted to an inner tracker: ALICE-ITS Upgrade
- Next R&D challenges
- Summary

Introduction to CPS

CPS: Development motivation



- CPS triggered by the need of very granular and low material budget sensors

- CPS applications exhibit milder running conditions than at pp/LHC
  - Relaxed readout (r.o.) speed & rad. tolerance

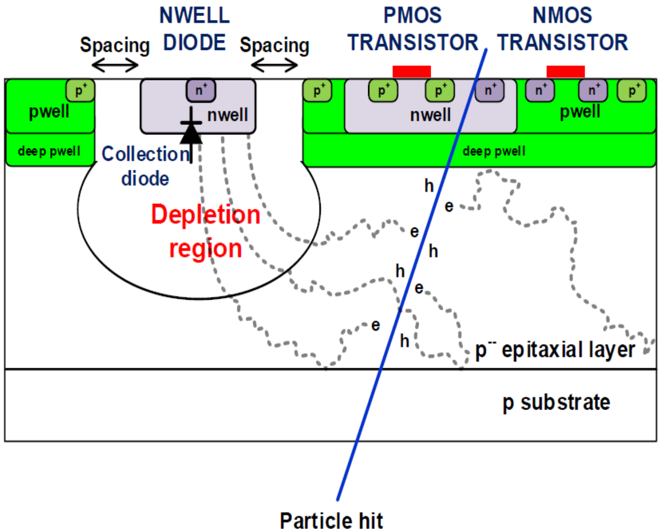
- Application domain widens continuously (existing/foreseen/potential)
  - **Heavy-ion collisions**
    - STAR-PXL, ALICE-ITS, CBM-MVD, NA61…
  - **e^+e^- collisions**
    - BES-III, ILC, Belle II (BEAST II)
  - **Non-collider experiments**
    - FIRST, NA63, Mu2e, PANDA, …
  - **High-precision beam-telescopes (**adapted to medium/low energy e^+ beams**)**
    - Few µm resolution @ DUT achievable with EUDET-BT (DESY), BTF-BT (Frascati)

CPS: Main features

The basic working principle

- Secondary charges generated in epi-layer by ionization
  - Signal proportional to epi-thickness
- Charges transport driven by 3 potentials
  - P-well/coll. node/P++ (usually GND/few volts/GND)
- Epi-layer not fully depleted: $d_{dep} \sim 0.3 \sqrt{\rho_{sub} \times U_{bias}}$

  $\Rightarrow$ transport is mix of thermal diffusion & drift



Prominent features

- Signal processing integrated on sensor substrate $\Rightarrow$ downstream electronics & syst. integration
- High granularity $\Rightarrow$ excellent spatial resolution (O(μm))
- Signal generated in thin (10-40μm) epi-layer $\Rightarrow$ usual thinning up to 50 μm total thickness
- Standard fabrication process $\Rightarrow$ low cost & easy prototyping, many vendors, …

CPS technology potential

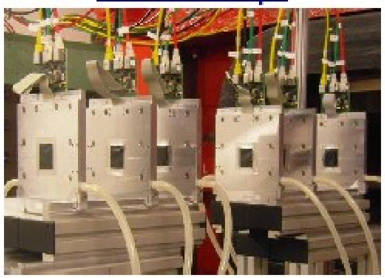
- Mainly driven by commercial applications $\Rightarrow$ Not fully optimized for particle detection
- R&D largely consists in exploiting as much as possible the potential of the accessible industrial processes

CPS @ PICSEL - IPHC: A long term R&D

- ***Ultimate objective: ILC, with staged performances***
  - *CPS applied to other experiments with intermediate requirements*

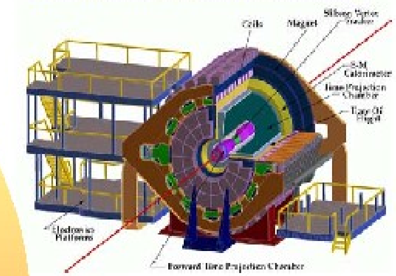
running

EUDET 2006/2010
Beam Telescope



STAR 2013
Solenoidal Tracker at RHIC

running

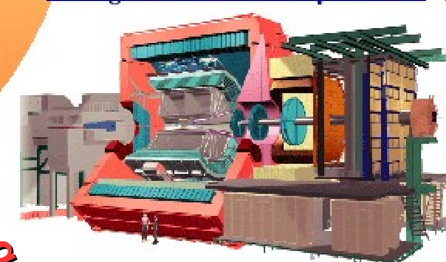


EUDET (R&D for ILC, EU project)
STAR (Heavy Ion physics)
CBM (Heavy Ion physics)
ILC (Particle physics)
HadronPhysics2 (generic R&D, EU project)
AIDA (generic R&D, EU project)
FIRST (Hadron therapy)
ALICE/LHC (Heavy Ion physics)
EIC (Hadron physics)
CLIC (Particle physics)
BESIII (Particle physics)
...

ILC >2020
International Linear Collider

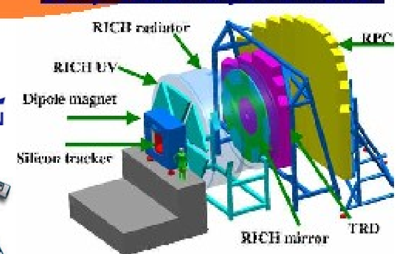
ALICE 2018
A Large Ion Collider Experiment

On-going R&D



CBM >2018
Compressed Baryonic Matter

On-going R&D



On-going R&D

SOLEIL SYNCHROTRON

HR-CMOS for X-rays (2018)

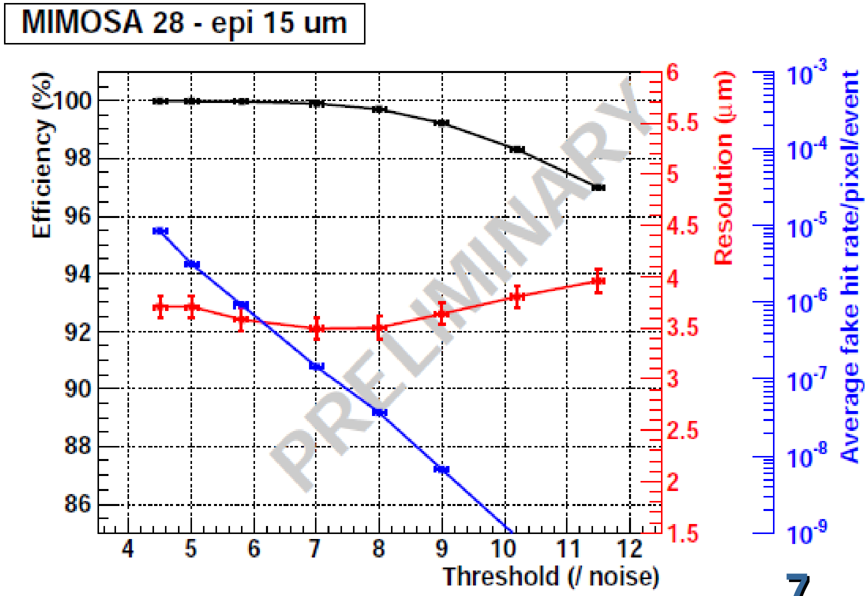
CPS State-of-the-Art in operation: STAR-PXL sensor

ULTIMATE main characteristics

- CMOS sensor (0.35 μm AMS twin-well) high-ρ epi-layer 15μm
- Sensor thinned to 50 μm (total thickness $\Rightarrow$ 0.05% X_0)
- || column (rolling shutter) r.o. with in-pixel CDS & amplification
- End-of-column discriminator (1-bit) followed by $\varnothing$-suppression
- 960 x 928 (columns x rows) pixels of 20.7 μm pitch
  $\Rightarrow$ 19.9 x 19.2 mm^2 sensitive area
- $t_{r.o.} \lesssim$ 200 μs (~5x10^3 frames/s) $\Rightarrow$ suited for > 10^6 part./cm^2/s
- 2 outputs @ 160 MHz
- Operation @ T ~30 °C & W $\lesssim$ 150 mW/cm^2

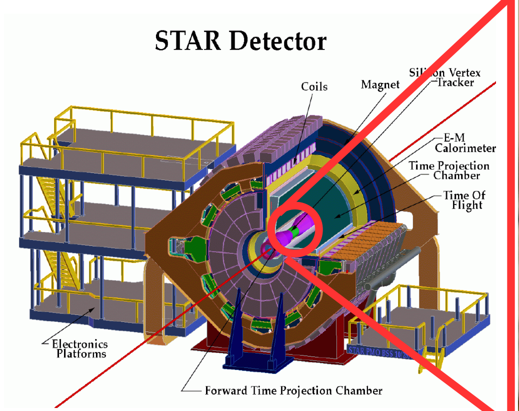
ULTIMATE Performances

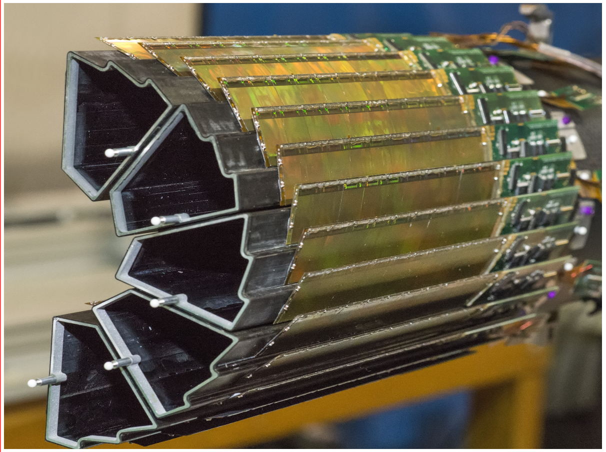
- Noise $\lesssim$ 15 e$^-$ ENC @ 30-35 °C
- $\varepsilon_{det} \gtrsim$ 99.9%, $\sigma_{sp} \gtrsim$ 3.5μm, Fake rate $\lesssim 10^{-5}$
- Rad. hardness validated @ 30 °C
  (150 kRad $\oplus$ 3×10^{12} n_{eq}/cm^2)



CPS State-of-the-Art in operation: STAR-PXL detector

STAR-PXL @ RHIC: 1st CPS @ a collider experiment !

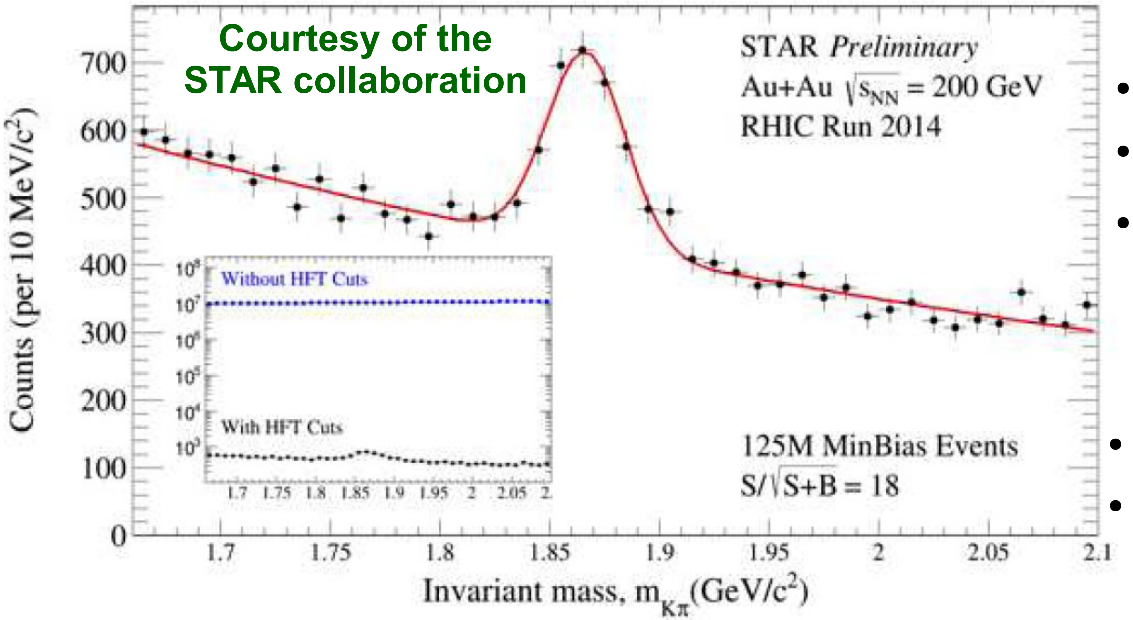




STAR-PXL HALF-BARREL

- 2 layers @ r = 2.8,8 cm
- 20 ladders (10 sensors) (0.37% X_0)

  ⇒ 180M pixels
- Air flow cooling: T < 35°C



Several Physics-runs

- **1st /2nd run in 2014 & 2015**
- **Preparation for 3rd run (Jan. 2016)**
- **$\sigma_{ip}(p_T)$ matching requirements**

~40 μm @ 600 MeV/c for $\pi^{\pm}/K^{\pm}$

Observation of D^0 production

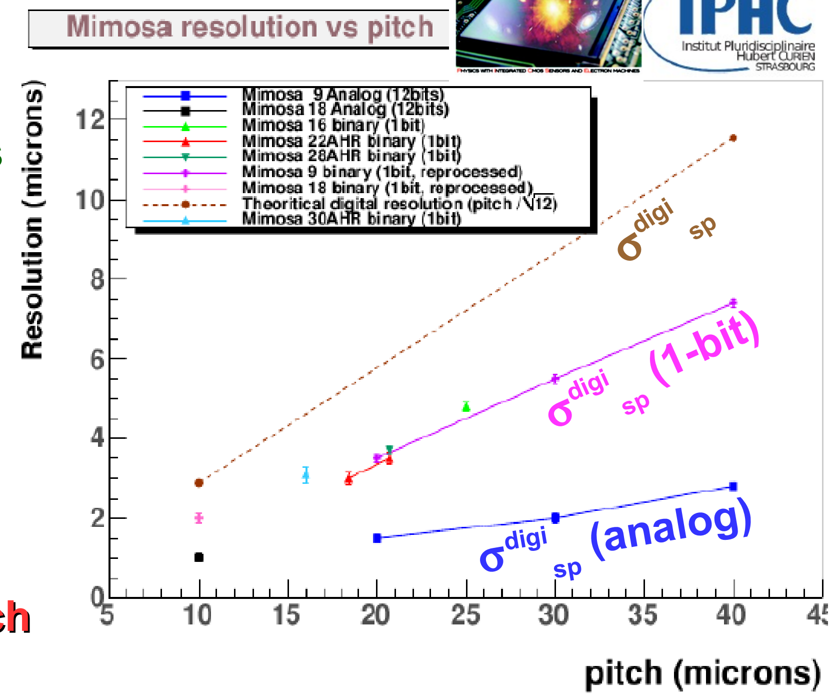
- **STAR:** peak significance = 18
- **ALICE:** peak significance = 5

CPS performances: Spatial Resolution (σ_{sp})

- **Several parameters govern σ_{sp}**
  - **Pixel pitch**
  - **Epi-layer:** thickness & ρ
  - **Sensing node:** geometry & electrical properties
  - **Signal-encoding resolution:** Nb of bits
  - **σ_{sp} function of:**

    pitch ⊕ SNR ⊕ charge-sharing ⊕ ADCu ⊕ ...

- **Pixel-pitch impact (analogue output)**
  - Pitch = 10 (40) µm ⇒ σ_{sp} ~ 1 µm ($\lesssim$ 3 µm)
  - **Nearly linear improvement in σ_{sp} vs pixel pitch**

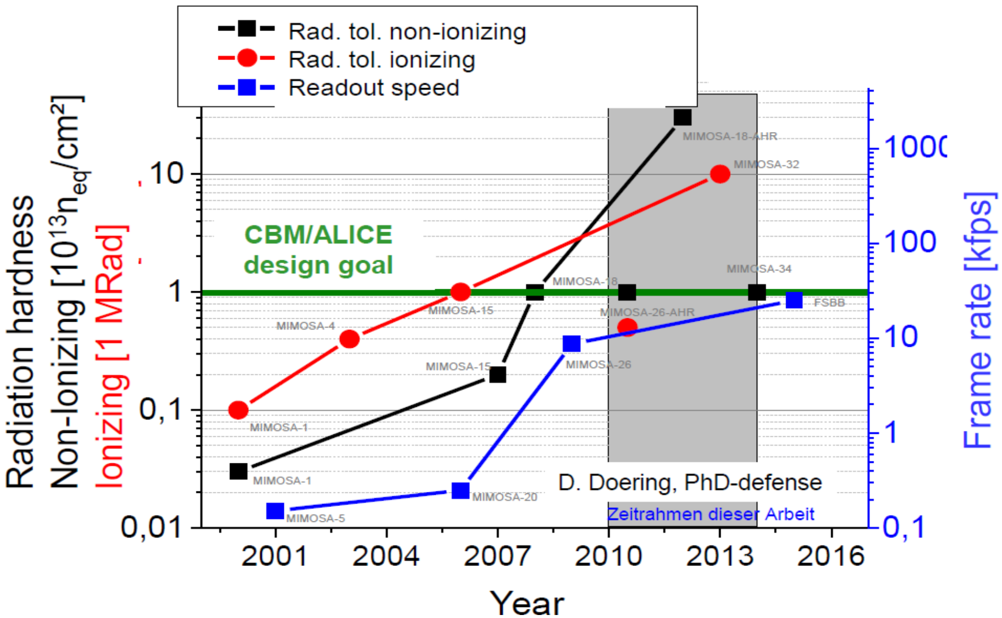


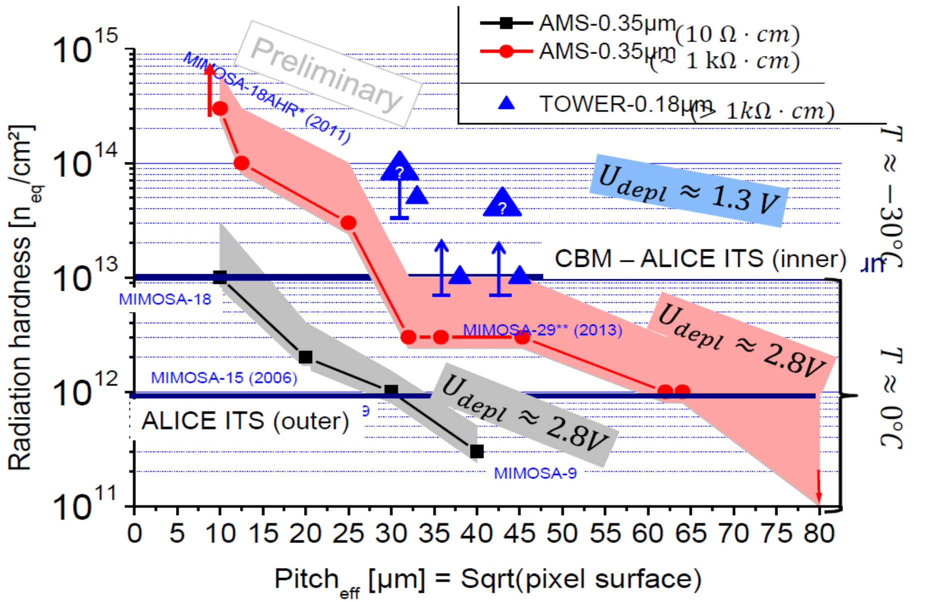
- **Signal-encoding impact (digital output)**
  - σ^{digi}_{sp} = pitch/(12)$^{1/2}$

    ⇒ e.g. σ^{digi}_{sp} ~ 5.7 µm for 20 µm pitch
  - **Significant improvement in σ_{sp} by increasing signal encoding resolution**

Nb of bits	12	3-4	1
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$

CPS performances: r.o. speed & rad. hardness





Sensors: IPHC Strasbourg
M. Deveaux, D. Doering, B. Linnik, S. Strohauer, CBM/IKF Frankfurt

PICSEL GROUP

ADvanced MOnolithic Sensors for FAIR

- **15 years of experience of PICSEL group in developing CPS**
- **Strong collaboration with ADMOS group at Frankfurt**

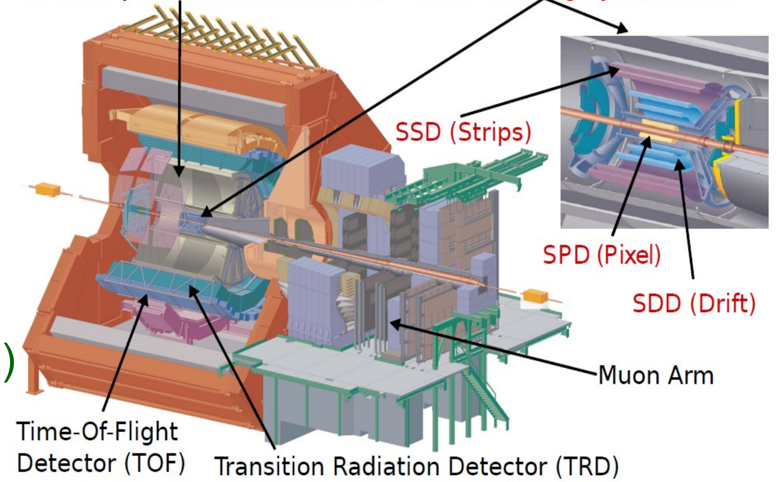
- **r.o. speed evolution**
  - Two orders of magnitude improvement in 15 years of research

- **Radiation tolerance**
  - Significant improvement with time
  - Sensor validation up to 10 MRad ⊗ $10^{14} n_{eq}/cm^2$
  - Adequacy to ALICE-ITS and CBM applications

Development of CPS adapted to Vertex & Tracker detector

Next challenge: ALICE-ITS upgrade

- **ALICE goals**
  - Study quark gluon plasma in heavy-ion collisions
  - High precision measurements @ low-p_T

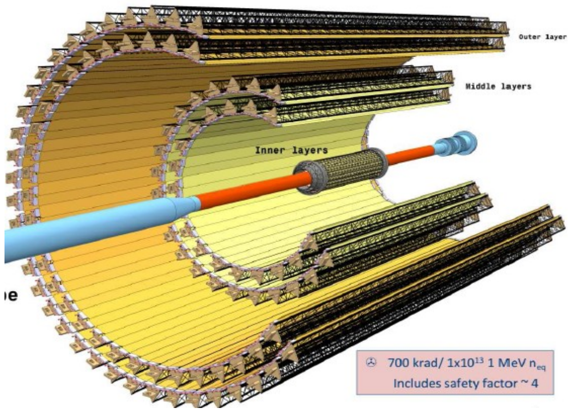


- **Upgraded ITS entirely based on CPS**
  - **Present detector:** 2xHPD/2xDrift-Si/2xSi-strips
  - **Future detector:** 7-layers with CPS (25-30k chips)

    ⇒ 1^{st} large tracker (~ 10 m^2) using CPS
  - ITS-TDR approved on March 2014 (Pub. In J.Phys. G41 (2014) 087002)

- **New ALICE-ITS requirements**

	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	$3\cdot10^{12}$ n_{eq}/cm^2	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim 30\ \mu s$	**2.7 MRad**	$1.7\cdot10^{13}$ n_{eq}/cm^2	30°C	$<$ 300 mW/cm^2	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim 30\ \mu s$	100 kRad	$1\cdot10^{12}$ n_{eq}/cm^2	30°C	$<$ **100 mW/cm^2**	$\sim$ **10 m^2**

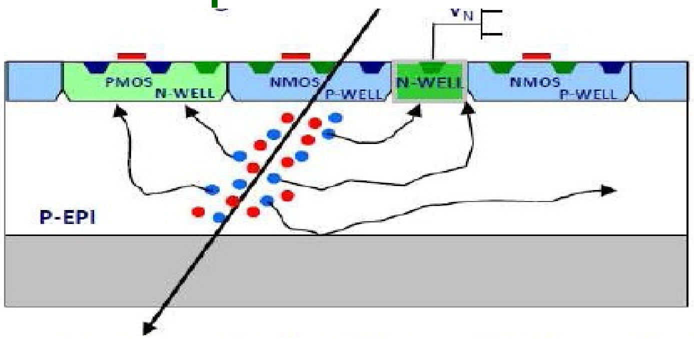


  - **Different requirements on inner & outer layers calls for different chips designs!**

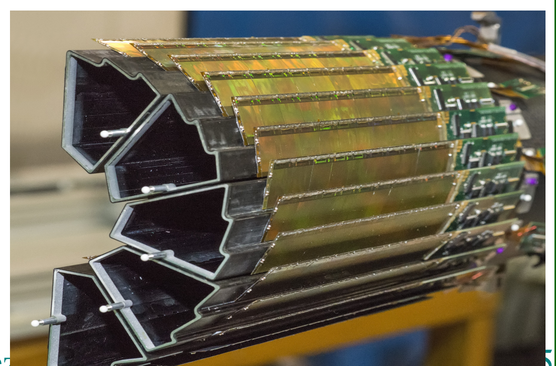
⇒ **0.35 µm CMOS process (STAR-PXL) marginally suited to this r.o. speed & rad. hardness**

CMOS Process Transition: STAR-PXL → ALICE-ITS

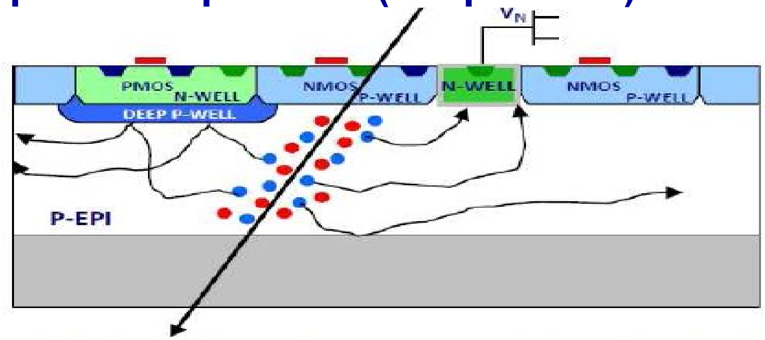
Twin well process: 0.6-0.35 um



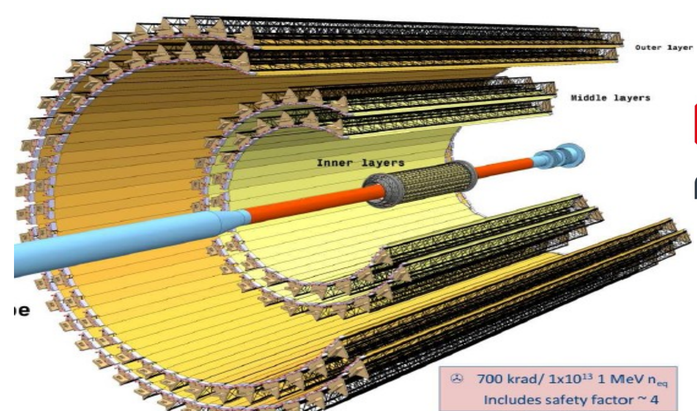
- Use of PMOS in pixel array not allowed
  ⇒ parasitic q-collection of additional N-well
- Limits choice of readout architecture strategy
- Already demonstrated excellent performances
  - **STAR-PXL:** Mi-28 (AMS 0.35 μm process)
    ⇒ $\varepsilon_{det} > 99.5\%$, $\sigma_{sp} < 4\mu m$
  - 1st CPS detector @ collider experiment



Quadrupole well process (deep P-well): 0.18 um



- N-well of PMOS transistors shielded by deep P-well
  ⇒ both types of transistors can be used
- Widens choice of readout architecture strategies
  - **New ALICE-ITS:** 2 sensors R&D in || using TowerJazz CIS 0.18 um process (quadru. well)
    - **Synchronous Readout R&D:** proven architecture ⇒ safety
    - **Asynchronous Readout R&D:** challenging



ALICE

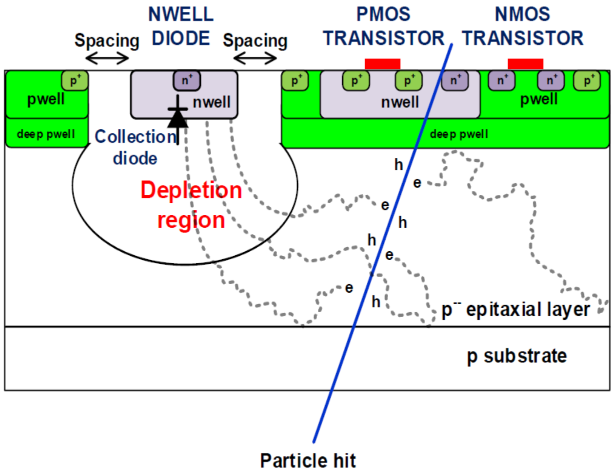
ALICE-ITS: Boundaries of the CPS Development

- **New fabrication process (TowerJazz CIS 0.18 µm)**
  - Expected to be ration tolerant enough
  - Expected to allow for fast enough readout
  - Larger reticule: ~ 25 x 32 mm^2

STAR-PXL	ALICE-ITS	added-value
0.35 μm	0.18 μm	speed, TID, power
4 ML	6 ML	speed. power
twin-well	quadruple-well	speed, power
EPI 14/20 μm	EPI 18/40 μm	SNR
EPI $\gtrsim$ 0.4 k$\Omega \cdot cm$	EPI $\sim$ 1 - 8 k$\Omega \cdot cm$	SNR, NITD

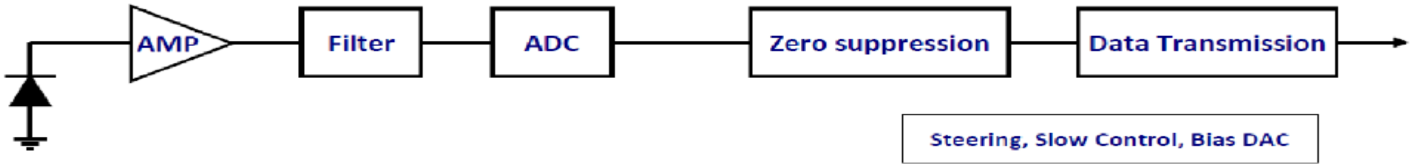
- **Drawback of smaller feature size**
  - 1.8 V operative voltage (instead of 3.3 V)

    ⇒ reduced dynamics in signal processing circuit and epi-layer depletion voltage
  - Increase risk of Random Telegraph Signal (RTS) noise



- **Requirements of the larger surface to cover**
  - Good fabrication yield ⇒ sensor design robustness
  - Mitigate noisy pixels
  - Sensor operation stable along 1.5 m ladder (voltage drop)
  - Material budget
    - Minimize power consumption
    - Minimal connexions to the outside ⇒ sensor periphery (slow-control, steering, ...)

ALICE-ITS: Readout chain components



- **Typical readout components**
  - **AMP:** in-pixel low noise pre-amplifier
  - **Filter:** in-pixel filter
  - **ADC** (1-bit ≡ discriminator): may be implemented at end-of-column or pixel level
  - **Zero suppression** (SUZE): only hit pixel info is retained and transferred
    - Implemented at sensor periphery (usual) or inside pixel array
  - **Data transmission:** O(Gbps) link implemented at sensor periphery

- **r.o. alternatives**
  - Rolling shutter (synchronous): || column r.o. reading N-lines at the time (usually N = 1-2)
  - data-driven (asynchronous): only hit pixels are output upon request (priority encoding)

- **Rolling shutter:** best approach for twin-well process
  - Trade-off between performance, design complexity, pixel dimensions, power, …
    e.g.: Mimosa-26 (EUDET-BT), Mimosa-28 (STAR-PXL)

ALICE-ITS: Two Architectures for the pixel chip

MISTRAL-O

Pixel pitch: 36x64 μm^2

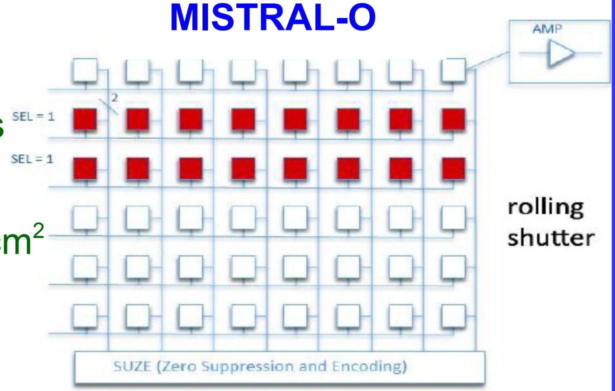
Time resolution: ~ 20 μs

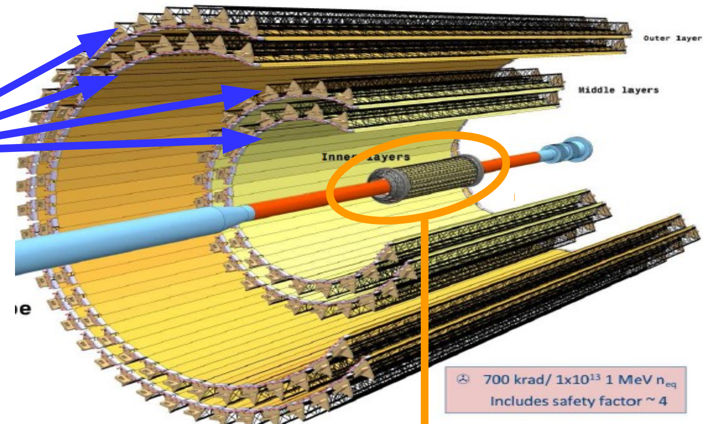
W: 80 mW/cm^2

Max hit rate: ~0.8 MHz/cm^2

Dimension: 15 x30 mm^2

Dead area: 1.5x30 mm^2





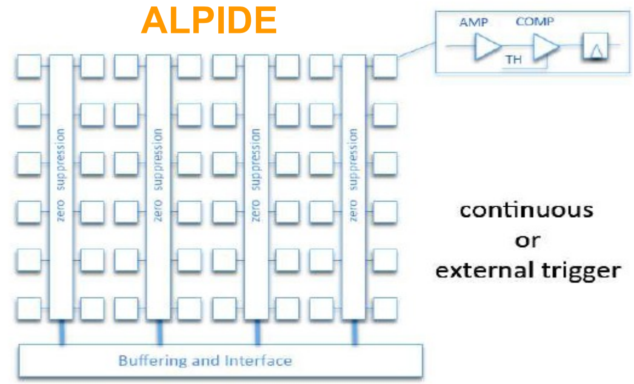
Goal: early available and reliable solution

- **Conservative design based on STAR-PXL**
- Big pixel ⇒ low power & high speed
- Moderate rad. hardness & σ_{sp} ~10 μs ⇒ OK

Goal: high performance, accept risks

- **Aggressive design**
- In-pixel discrimination
- Data-driven r.o. (priority encoder)

ALPIDE



Pixel pitch: 28x28 μm^2

Time resolution: $\lesssim$ 5 μs

W: 39 mW/cm^2

Max hit rate: ~ 3MHz/cm^2

Dimension: 15 x30 mm^2

Dead area: 1.1x30 mm^2

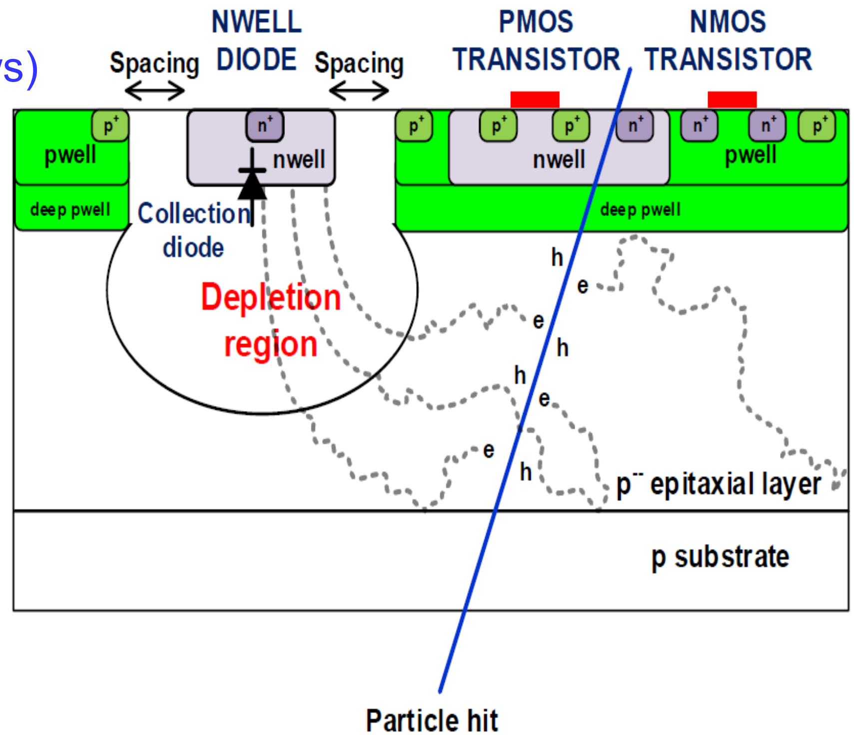
- **Both chips have same physical & electrical interfaces**
- **Base-line solution: ALPIDE for all ITS layers**

Exploring the new technology

Technology Exploration & Sensor Performances

- **Goal:** understand the detection performances in terms of external parameters
  ⇒ Optimization for ALICE-ITS (and evaluate adequacy for other applications)

- **External parameters**
  - Diode and spacing (footprint) size/geometry
  - **Pixel size/geometry:** square vs elongated
    - Elongated pixels in row direction (less rows)
      ⇒ Lower $t_{r.o.}$ of rolling shutter
  - **Diode layout of elongated pixels**
    - Staggering ⇒ lower diode inter-distance
  - **Epi-layer:** thickness and resistivity (profile)

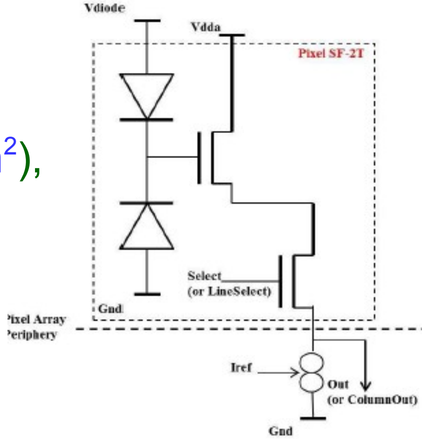


- **Performances in terms of**
  - Noise
  - CCE, SNR @ seed pixel
  - Hit pixel multiplicity ⇒ data transmission
  - ε_{det}, σ_{sp} & Fake-rate
  - Rad. Tolerance

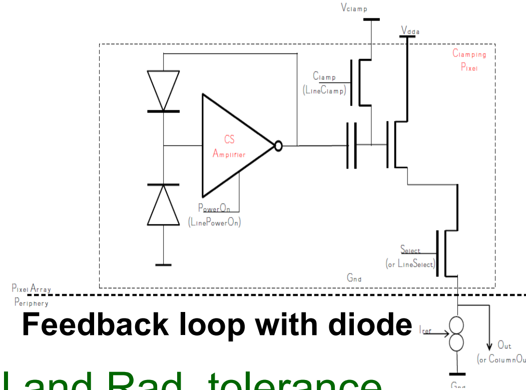
Exploratory chips: MIMOSA-32ter & MIMOSA-34

- **TowerJazz 0.18um technology validation & performances optimization**
- **MIMOSA-32ter**
  - **Analog-output:** source follower or feedback-loop (t_{int}~34 or 12 μs)
  - Sub-matrices of 16x64 pixels with different sizes (20x20,33,40,80 μm^2), diodes geometries (octagonal vs square) and some with deep P-well
  - **Epi-layer:** 18 μm HR (ρ = 1 kΩ cm)
- **MIMOSA-34**
  - **Analog-output:** source follower (t_{int} ~ 32μs)
  - 30 sub-matrices with 16x64 staggered pixels
    - **Dimensions:** 22 or 33 x(27, 30, 33, 44, 66) μm^2
    - **Diode/footprint:** 1+1, 2, 5, 5+5, 8, 11, 15 μm^2 / 11,15 μm^2
  - **Epi-layer:** 18, 20, 30 μm HR (ρ = 1 – 6 kΩ cm)
- **Test purposes**
  - **Validate new technology:** epi-layer characteristics, deep P-well and Rad. tolerance
  - **Study:** sensing node charge collection, elongated pixels performances

source follower



Diode & pre-ampli

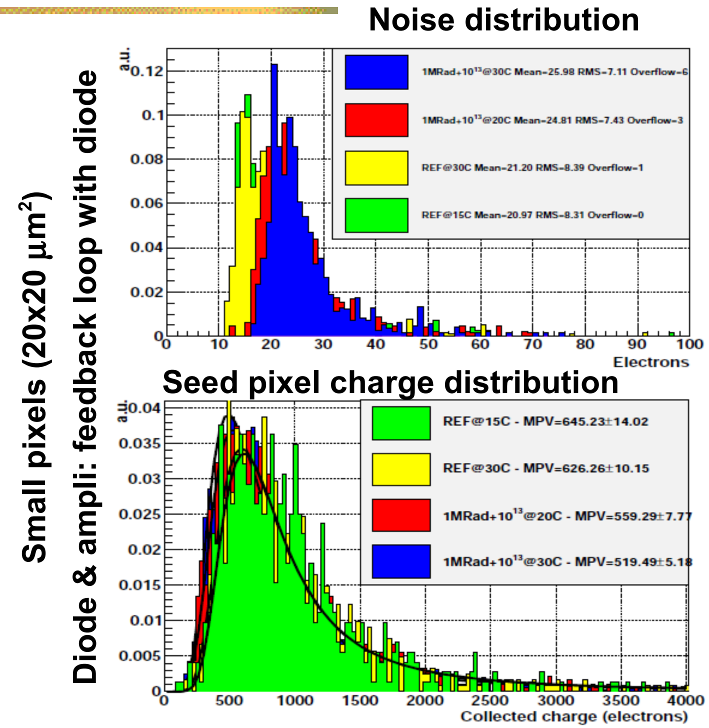


Feedback loop with diode

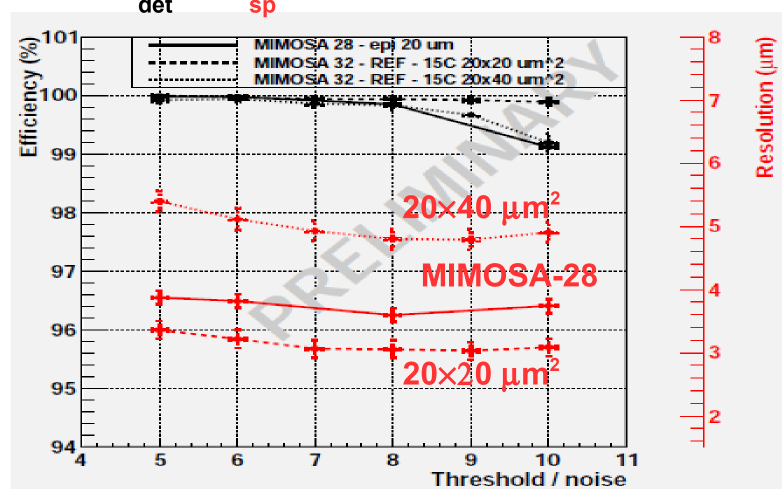
MIMOSA-32ter: performances

- **CERN-SPS BT Set-up**
  - **Beam:** 60-120 GeV/c π^+
  - $T_{cooling}$ = 15, 20 & 30°C
- **Main results**
  - 20x20 μm^2 pixel (performances vs rad. dose @ 30°C)
    - Small noise increase: 21 → 26 e^- ENC
    - SNR_{seed} reduction: 26-28 → 19 (30%)
    - ε_{det} > 99% for 1MRad ⊕ $10^{13} n_{eq}/cm^2$
    - σ_{sp} ~ 3.2 μm
  - 20x40 μm^2 pixel (@ 20°C)
    - ε_{det} > 99% for 1MRad ⊕ $10^{13} n_{eq}/cm^2$
    - σ_{sp} ~ 5.0 μm
- **Technology validation**
  - HR epi-layer ✓
  - deep P-well (no parasitic charge coll.) ✓
  - Radiation tolerance ✓

- 15°C, No rad.
- 30°C, No rad.
- 20°C, 1MRad⊕10^{12} $_{neq}$/cm^2
- 30°C, 1MRad⊕10^{13} $_{neq}$/cm^2



ε_{det} & σ_{sp} vs threshold

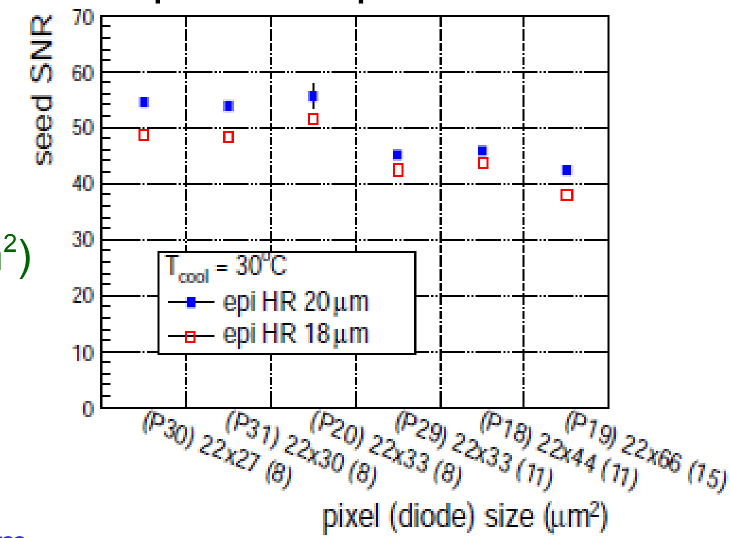


MIMOSA-34: performances vs diode & pixels sizes

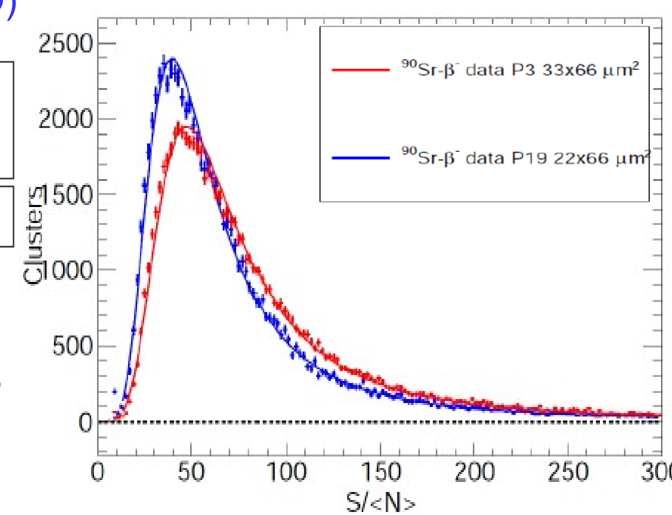
- **DESY BT Set-up (August 2013):**
  - 2BT: 8xSi-strips & 6xMIMOSA-26 (120 µm thick)
  - ~4.4 GeV/c e^- beam
- **MIMOSA-34:** Various pixels & diode dimensions
  - Pixel (22x27,30,33,44,66) & diode (8,11,15) sizes (μm^2)
  - Excellent SNR_{seed} for various considered pixels

    ⇒ e.g. MPV > 40 for 22x66 μm^2 pixel ⇒ ε_{det} ~100%
  - **33x66 μm^2 pixel:** Not tested in BT but with β-source
    - Excellent MPV (> 50) ⇒ expects ε_{det} ~100% & σ_{sp} ~ 10µm
    - Pixel size adapted for ALICE-ITS outer layers (MISTRAL-O)

Seed pixel SNR vs pixel variations



Seed pixel SNR vs pixel size



Process ▷	0.35 μm	0.18 μm				
Pixel Dim. [μm^2]	20.7×20.7	20×20	22×33	20×40	22×66	33×66
σ_{sp}^{bin} [μm]	3.7 ± 0.1	3.2 ± 0.1	~ 5	5.4 ± 0.1	~ 7	$\sim 10\ \mu m$?

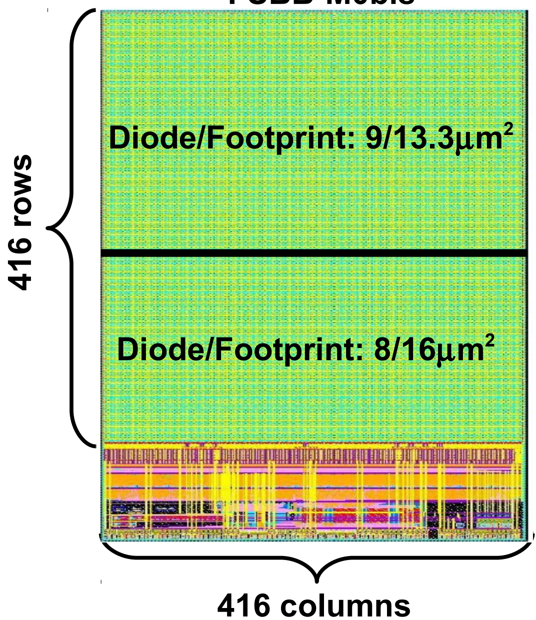
- **Variations showed acceptable degradation of performances for nominal TID + NIEL @ ALICE-ITS**
- **Next-step: optimization with pre-ampli scheme**

Going MISTRAL-O

Main features of the Sensors Studied on Beam

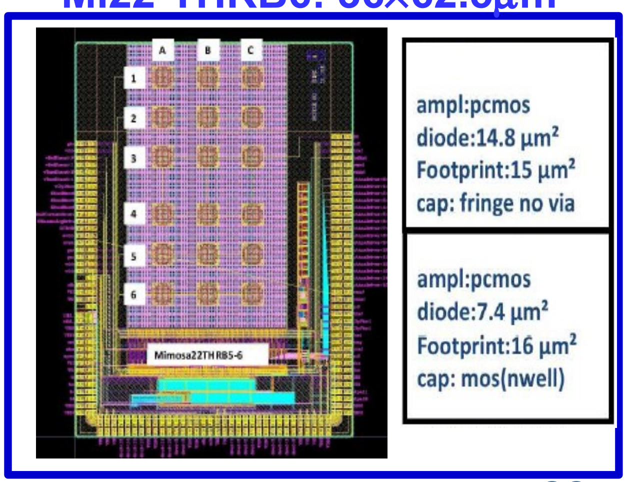
- **Full Scale Building Block (FSBB) sensor**
  - Complete (fast) chain of double-row r.o. and 2D sparcification (SUZE): $t_{r.o.}$ = 40 µs
  - Sensitive area (~1 cm^2) ≈ area of final building bock
  - Similar Nb of pixels (~170k) than complete final chip (160k)
  - Epi-layer: high-ρ 18 µm thick
  - **BUT:** pixels are small (22x32.5 µm^2 staggered layout) & sparsification circuitry is oversized (power!)

FSBB-M0bis



- **Large-pixel prototype (MIMOSA-22THRb)**
  - Two slightly different large pixels
    - 36x62.5 µm^2 and 39x50.8 µm^2 (staggered layout)
  - Pads over pixel array (3ML used for in-pixel circuitry)
  - Double-row r.o. with no-sparsification ($t_{r.o.}$ ~ 5 µs)
  - Epi-layer: high-ρ 18 µm thick
  - **BUT:** only ≲ 10 mm^2, 4k pixels & no sparsification

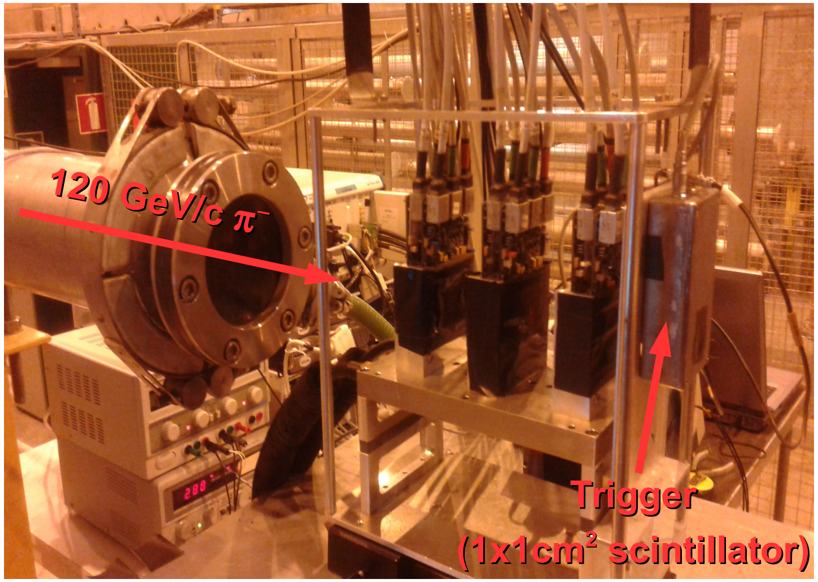
Mi22-THRB6: 36×62.5µm^2



Main goals of MIMOSA-22THRb & FSBB-M0 Prototyping

Parametres investigated	MIMOSA-22THRb7/6	FSBB-M0bis
Sensing node geometry	X	X
Epitaxial layer parametres	x	X
In-pixel signal processing	X	x
on 3 ML (Pre-Amp, clamping)	X	–
Pads over pixels	X	–
Large pixel detection efficiency	X	–
at 30°C (incl. after OB radiation load)	X	–
Large pixel single point resolution	X	–
Complete signal sensing & processing chain	–	X
Fake rate (160,ooo pixels)	x	X
Impact of voltage drop	–	X
Cluster encoding data size	X	x

FSBB BT @ CERN-SPS in Oct. 2015



- **Experimental set-up**
  - 3 pairs of FSBB planes on T4/H6 (120 GeV/c π^-)
  - Particle flux: trigger rate ~4, 25 & 100 kHz/cm^2
  - **All measurements performed at $T_{coolant}$ = 30 °C**

- **Measurements vs discriminator threshold**
  - Detection efficiency vs fake rate (noisy pixel)
  - Spatial resolution associated with binary encoding of 22x32.5 μm^2 pixels
  - Radiation tolerance @ $T_{coolant}$ = 30 °C: up to 1.6 MRad $\oplus$ 1.0×10^{13} n_{eq}/cm^2
  - Studies of the impact of operation parameters on sensor performances
    - e.g. input voltage (VDD), pixel current, ...
  - Study of the impact of noisy pixel masking on efficiency and spatial resolution

- **Main Goal:** validation of r.o. architecture and pixel masking in full size chip

Main FSBB-M0 detection performances (1/3)

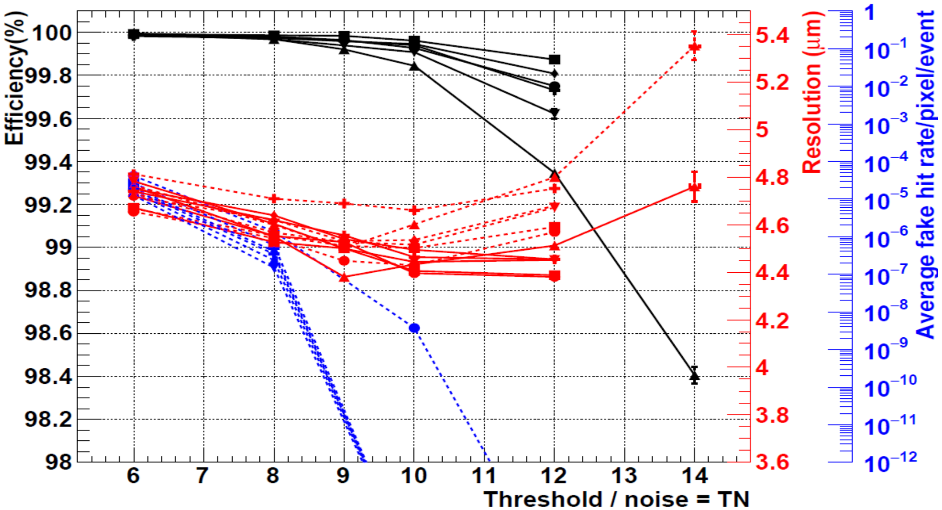
All the 6 sensor performances on the same plot

- Efficiency
- U residue
- V residue
- Fake rate @ 10^{-3} masking

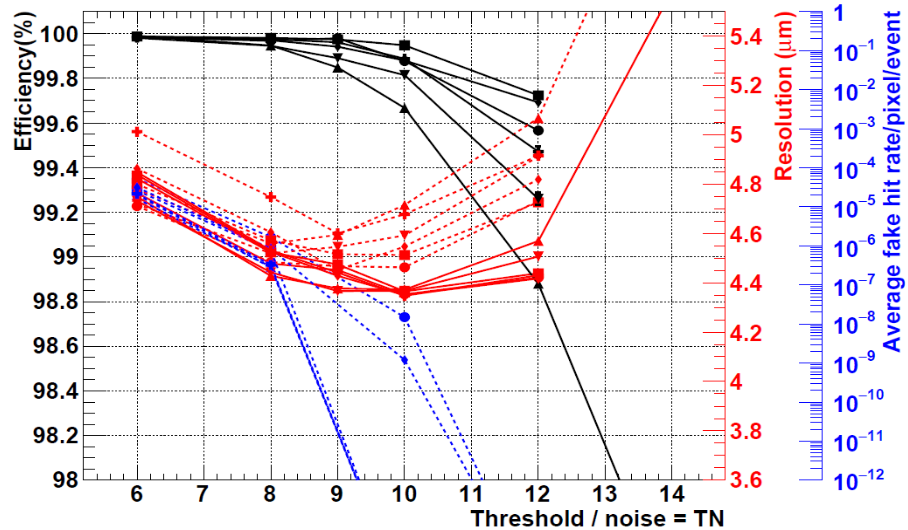
Excellent and uniform performances among sensors (thr < 10xNoise)

- detection efficiency: > 99%
- spatial resolution: < 5µm
- Fake rate: < 10^{-6} with moderate (10^{-3}) hot pixels masking

Diode/Footprint: 8/16 µm²



Diode/Footprint: 9/13.3 µm²



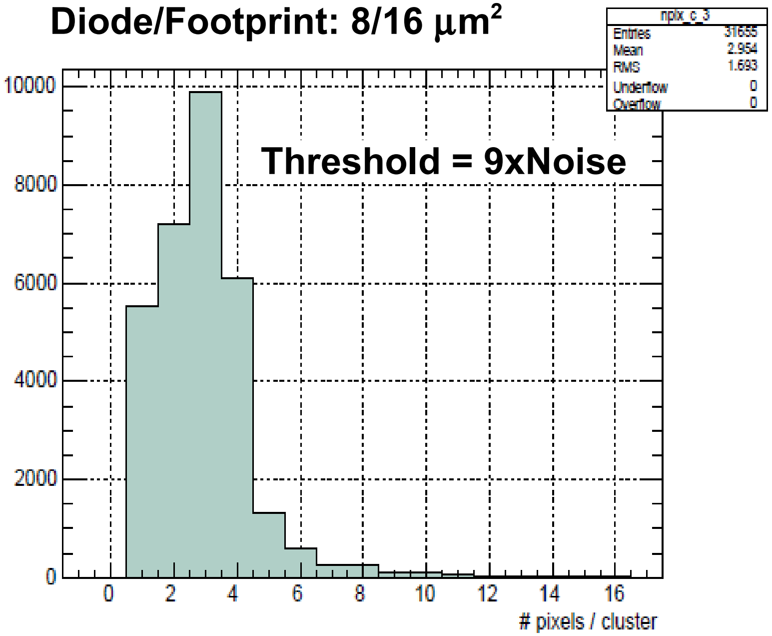
Detection performances stability

- Same results obtained @ DESY (4.5 GeV/c e^-) and CERN-SPS (120 GeV/c π^-)
- Same results for different particles rates: 1 – 25 hits/frame
- Robust performances in terms of operation parameters

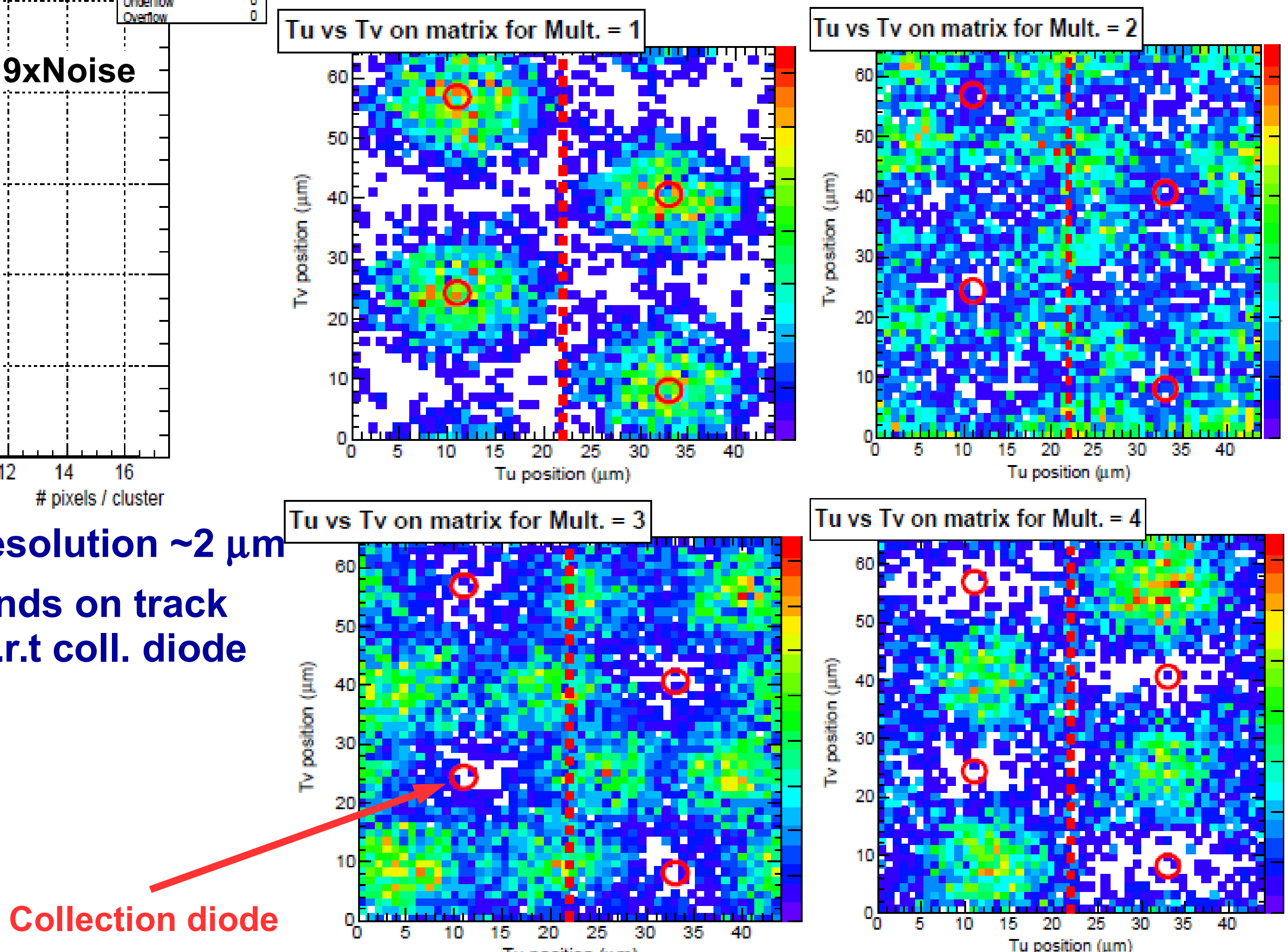
Main FSBB-M0 detection performances (2/3)

- **Spatial resolution vs cluster pixel size**

Diode/Footprint: 8/16 µm²



Track position @ DUT w.r.t closest set of collection diodes as a function of cluster pixel multiplicity

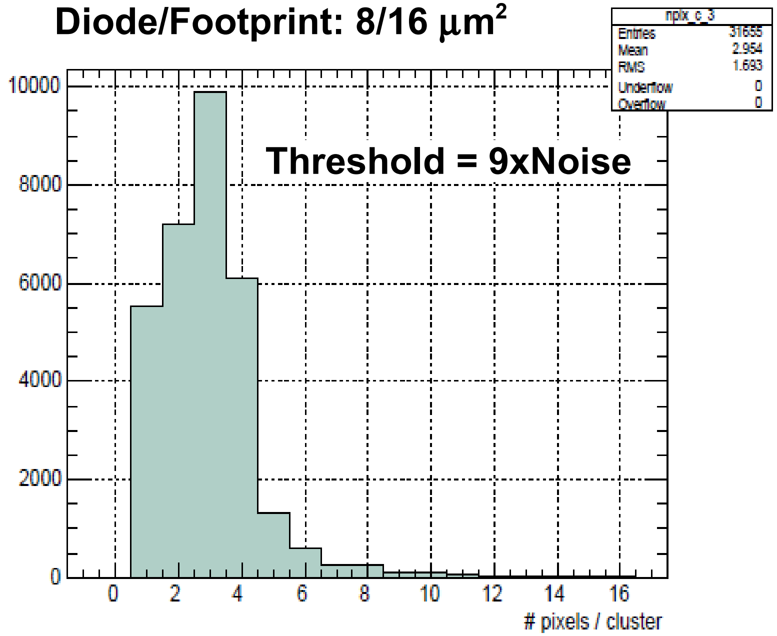


- **Telescope pointing resolution ~2 µm**
- **Charge sharing depends on track impinging position w.r.t coll. diode**

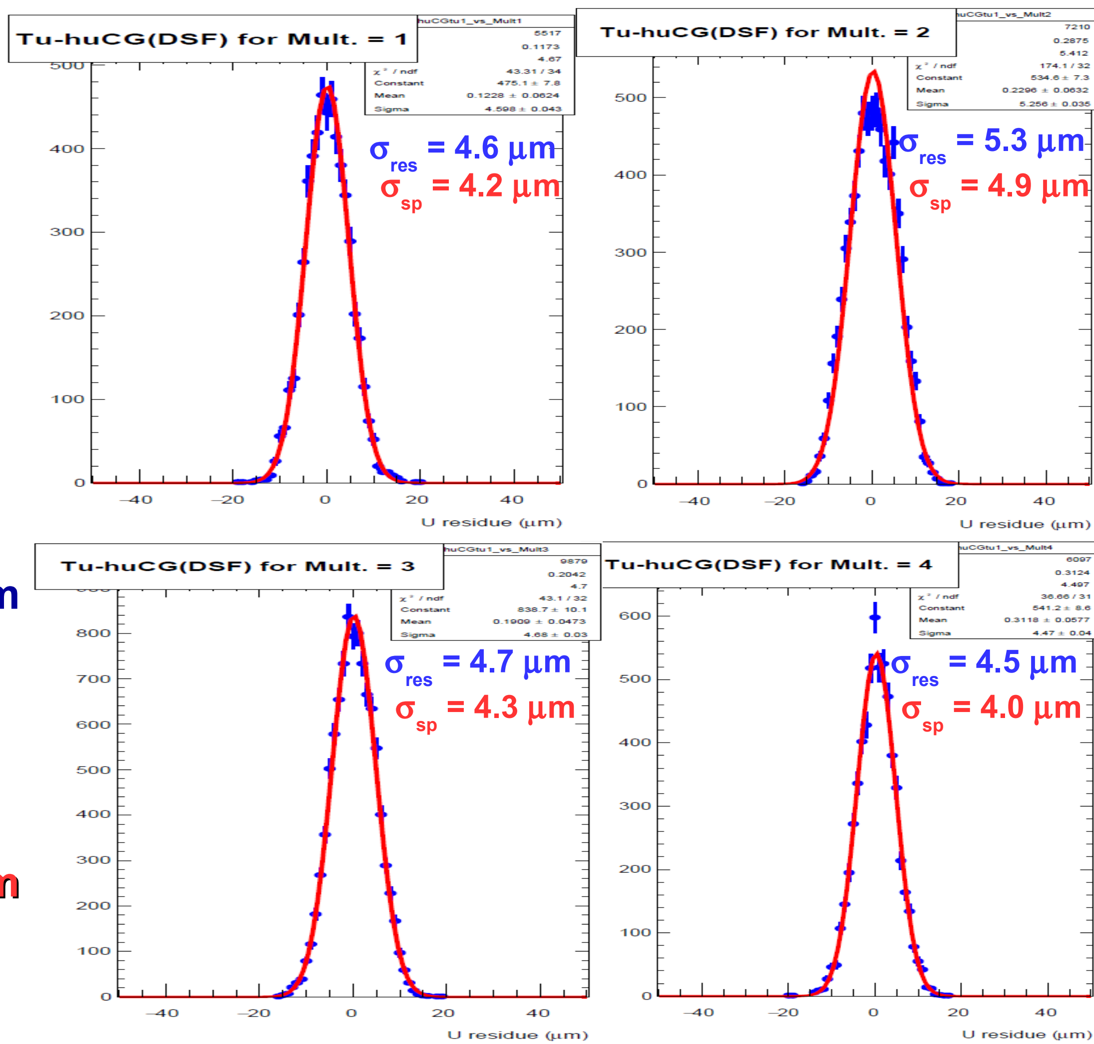
Main FSBB-M0 detection performances (2/3)

Spatial resolution vs cluster pixel size

Diode/Footprint: 8/16 µm²



Residue distribution in the raw parallel direction as a function of cluster pixel multiplicity

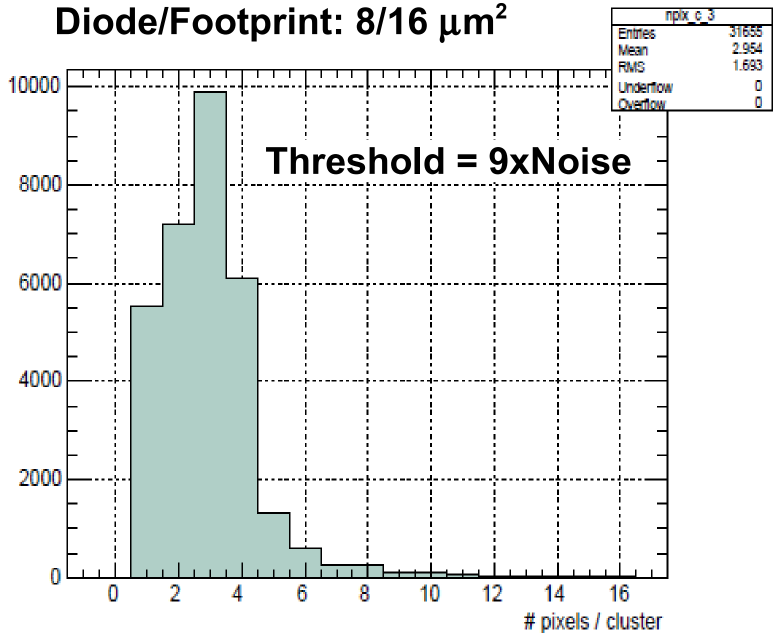


- Telescope pointing resolution ~2 µm
- Charge sharing depends on track impinging position w.r.t coll. diode
- **Spatial resolution is mostly dependent on # pixels/cluster**
- σ_{sp}(Mult=1) ~ 4.2 µm < σ^{digi}_{sp} ~ 7.8 µm

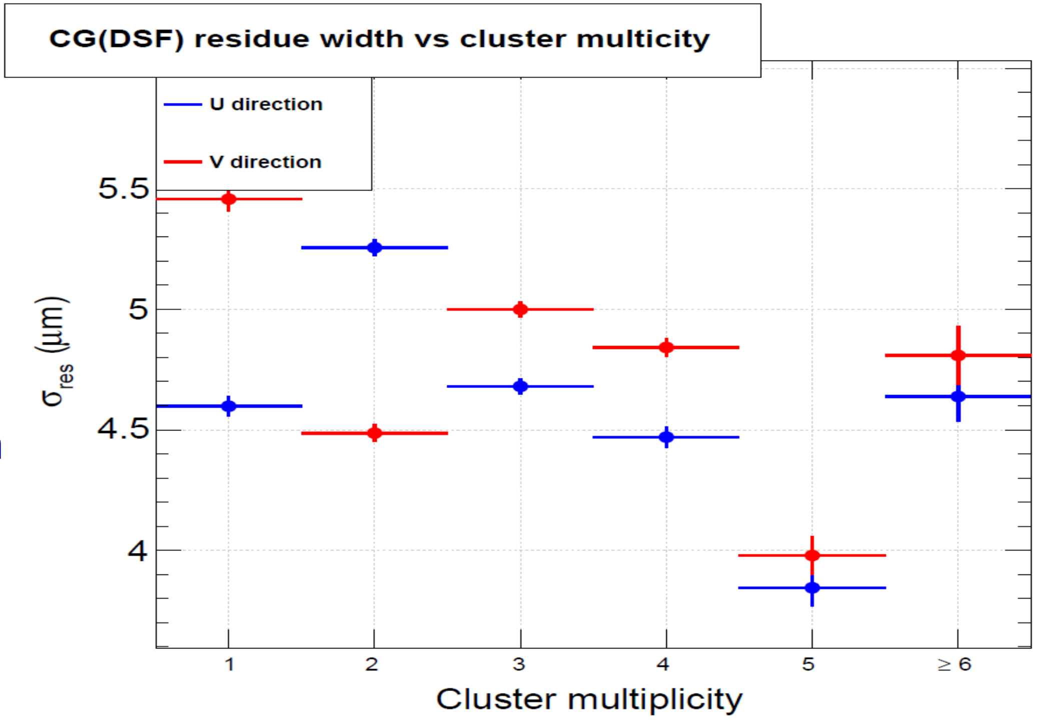
Main FSBB-M0 detection performances (2/3)

- **Spatial resolution vs cluster pixel size**

Diode/Footprint: 8/16 μm^2



Residue RMS in the raw/column parallel direction as a function of cluster pixel multiplicity



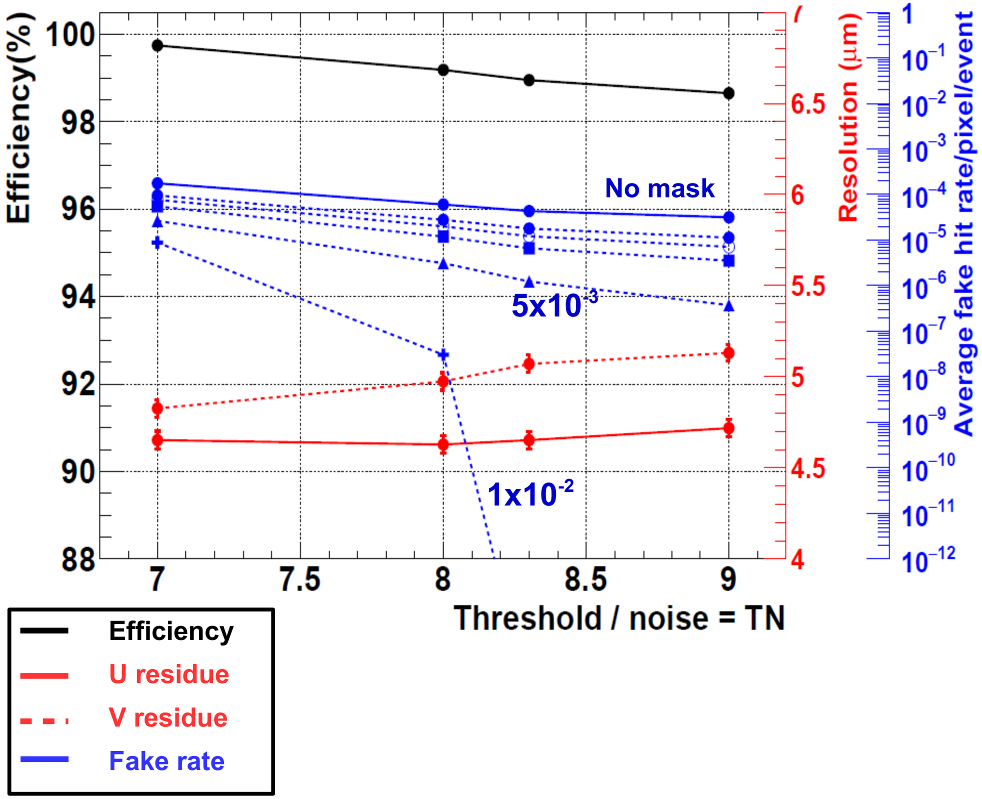
- **Telescope pointing resolution ~2 µm**
- **Charge sharing depends on track impinging position w.r.t coll. diode**
- **Spatial resolution is mostly dependent on # pixels/cluster**
- **σ_{sp}(Mult=1) ~ 4.2 µm < σ^{digi}_{sp} ~ 7.8 µm**
- **Staggering mitigates σ_{sp} difference in raw/column directions**

Main FSBB-M0 detection performances (3/3)

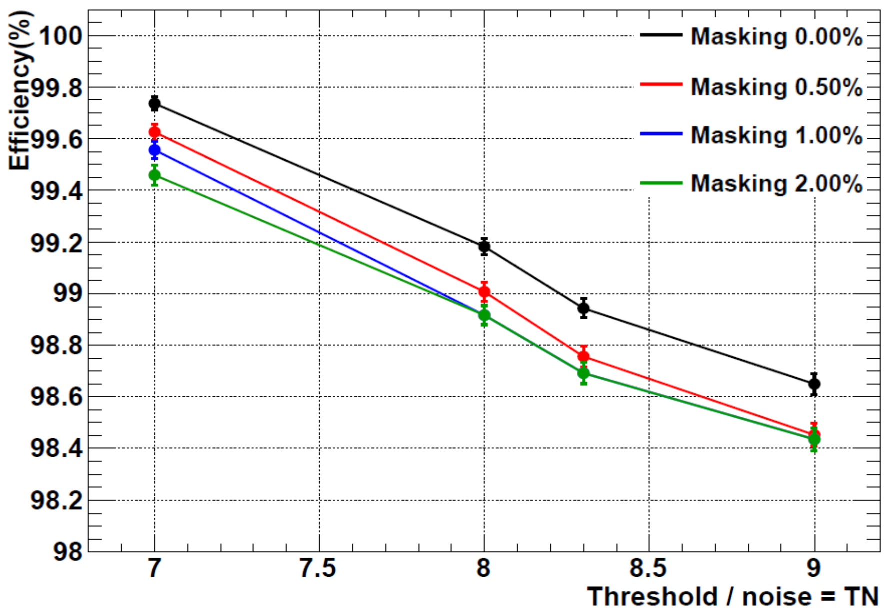
- **Study of rad. tolerance @ T $\gtrsim$ 30 °C:** loads relevant to ALICE-ITS inner layers
  - **Load:** 1.6 MRad ⊕ $10^{13} n_{eq}/cm^2$

Diode/Footprint: 9/13.3 μm^2

ε_{det}, σ_{sp} & fake-rate vs Discr. Threshold



ε_{det} vs Discr. Threshold vs pixel masking

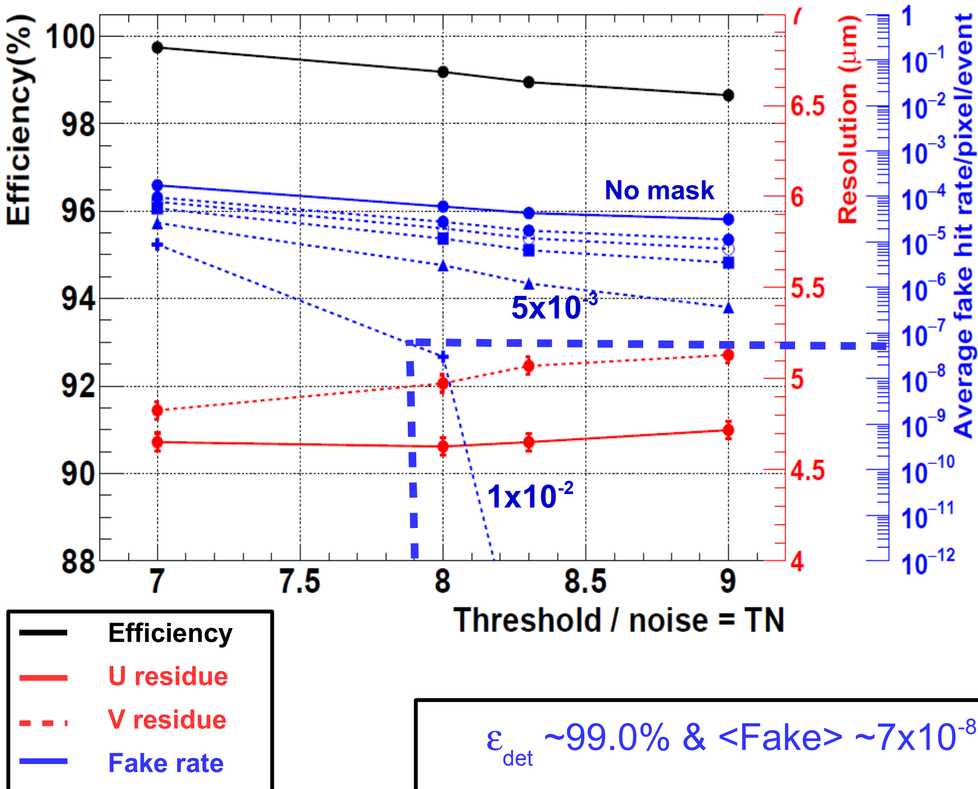


Main FSBB-M0 detection performances (3/3)

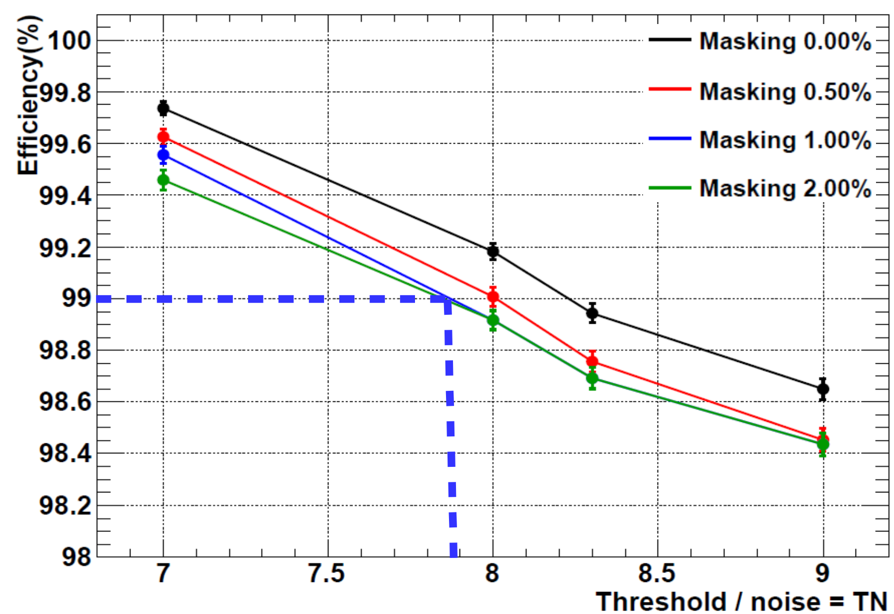
- **Study of rad. tolerance @ T ≳ 30 °C:** loads relevant to ALICE-ITS inner layers
  - **Load:** 1.6 MRad ⊕ $10^{13} n_{eq}/cm^2$

Diode/Footprint: 9/13.3 μm²

ε_{det}, σ_{sp} & fake-rate vs Discr. Threshold



ε_{det} vs Discr. Threshold vs pixel masking



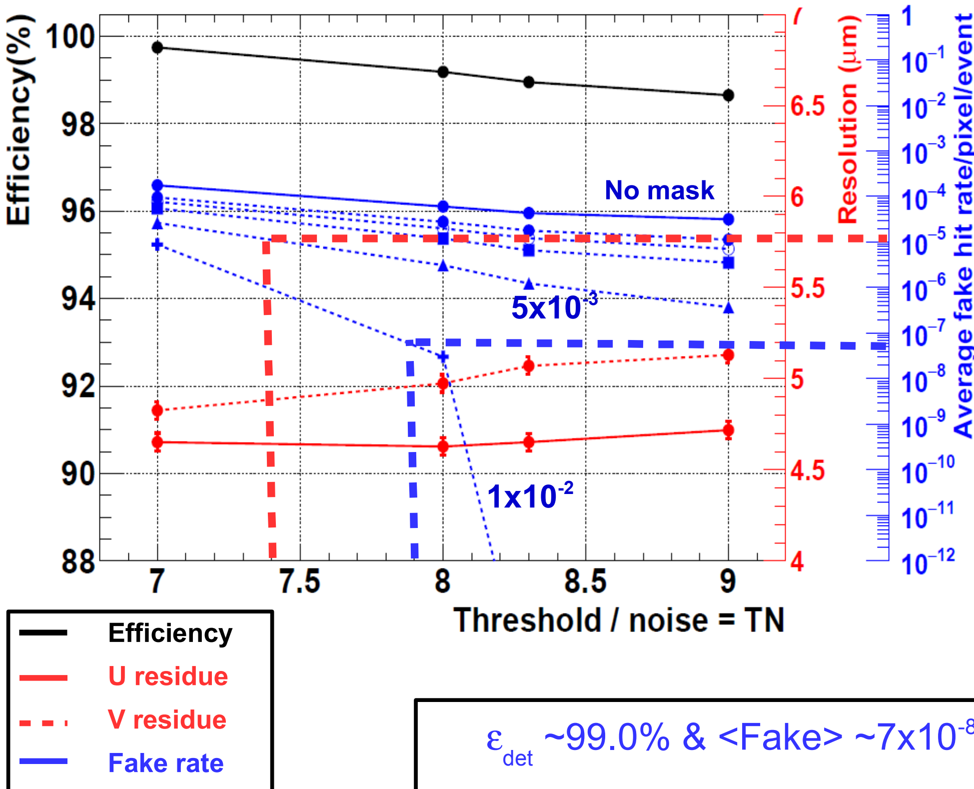
ε_{det} ~99.0% & <Fake> ~7×10^{-8} (1.0% masking) @ Thr = $7.9\times\sigma_{TN}$

Main FSBB-M0 detection performances (3/3)

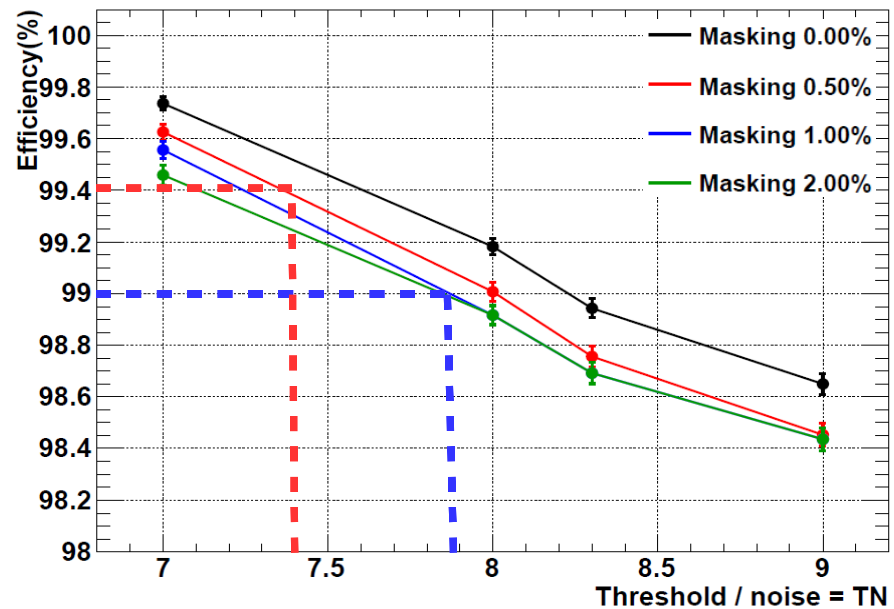
- **Study of rad. tolerance @ T ≳ 30 °C:** loads relevant to ALICE-ITS inner layers
  - **Load:** 1.6 MRad ⊕ $10^{13} n_{eq}/cm^2$

Diode/Footprint: 9/13.3 μm^2

ε_{det}, σ_{sp} & fake-rate vs Discr. Threshold



ε_{det} vs Discr. Threshold vs pixel masking

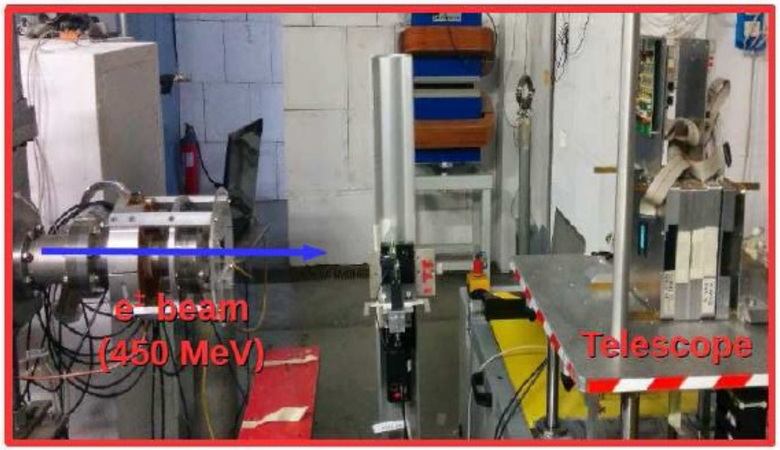


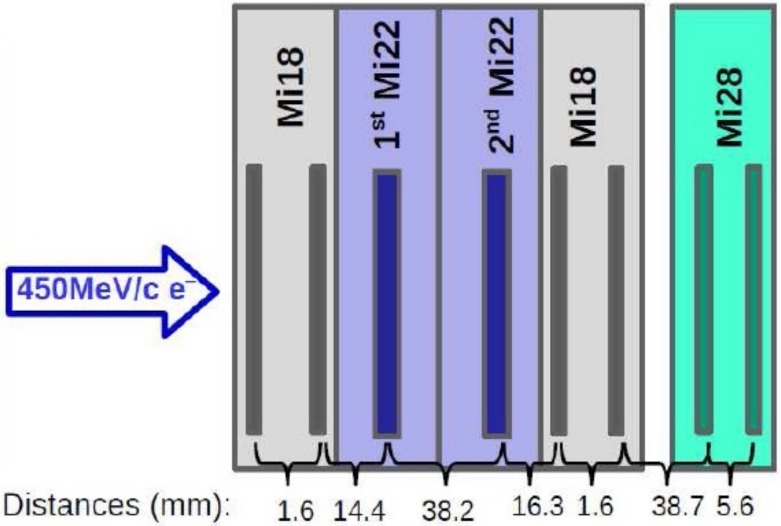
ε_{det} ~99.0% & <Fake> ~7×10^{-8} (1.0% masking) @ Thr = $7.9\times\sigma_{TN}$

ε_{det} ~99.4% & <Fake> ~1×10^{-5} (0.5% masking) @ Thr = $7.4\times\sigma_{TN}$

MIMOSA-22THRb BT @ Frascati in May 2015

- **Experimental set-up**
  - **Beam:** 450 MeV/c e^-
  - **Telescope:** 2xMi28 (digital output) and 4xMi18 (analog-output) sensors thinned to 50 μm
  - **Trigger:** beam injection signal ⇒ synchronisation due to small spill length (few ns)





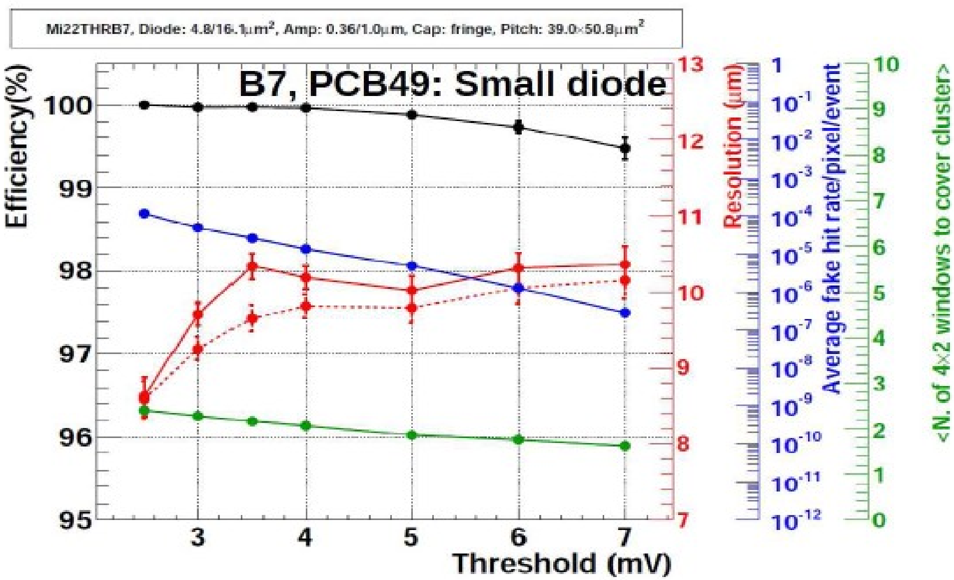
Mi18: σ_{sp} = 1-2 μm

Mi28: σ_{sp} ~ 3.5 μm

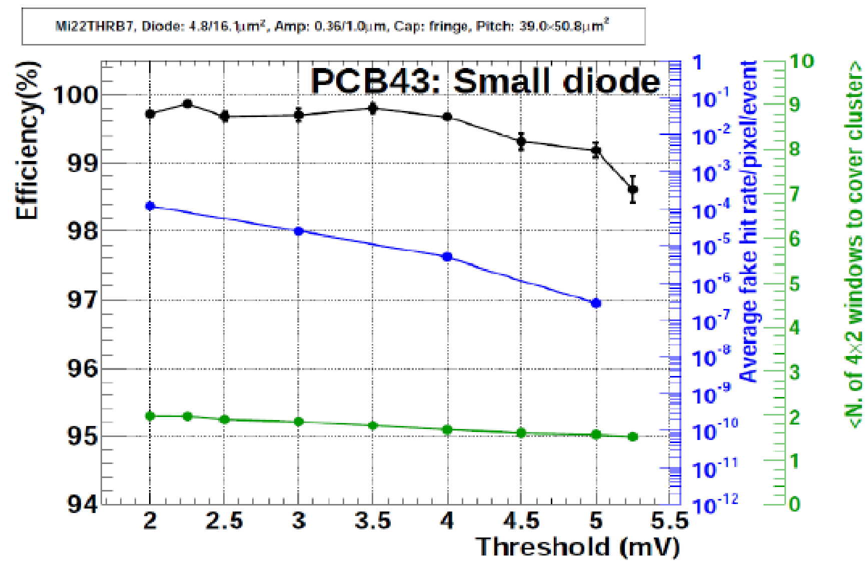
- **Measurements vs discriminator threshold**
  - Detection efficiency vs fake rate (noisy pixel)
  - Spatial resolution associated with binary encoding of 36x65.2 μm^2 & 39x50.8 μm^2 pixels
  - Radiation tolerance @ $T_{coolant}$ = 30 °C: up to 150 kRad ⊕ 1.5×10^{12} n_{eq}/cm^2
- **Main Goal:** validation of large pixel performances

Main MIMOSA-22THRb detection performances (1/2)

Pixel type	Pixel dim.	Diode/Footprint	Pre-Amp T.	Clamping capa.	Integ. time
MIMOSA-22THRb7	39 μm x 50.8 μm	5/16 μm^2	N-MOS	MOS (N-well)	5 μs



No Irradiation



150 kRad ⊕ 1.5×10^{12} n_{eq}/cm^2

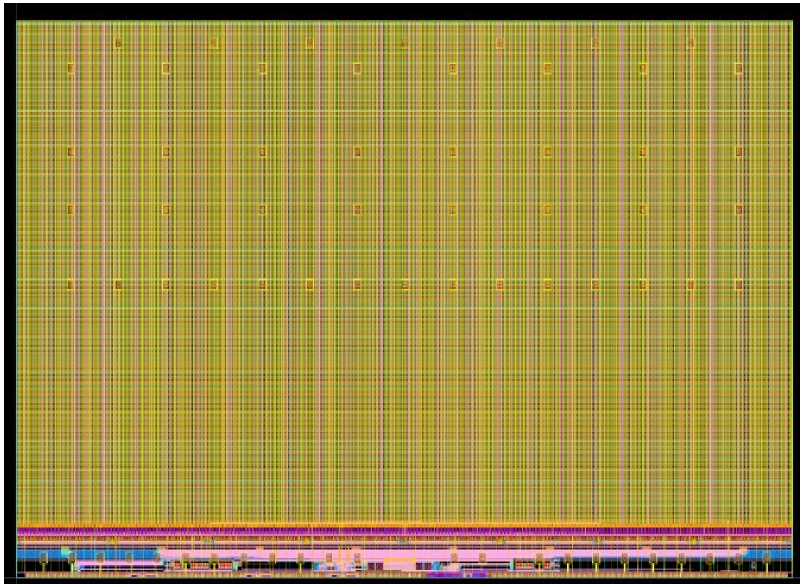
- Efficiency
- U residue
- V residue
- Fake rate
- <# Suze Windows>

- **Excellent detection performances**
  - ε_{det} > 99% & σ_{sp} ~ 10 µm (as expected)
  - Good performances for radiation load relevant for outer ALICE-ITS

- **Validation of large pixel design for the outer layers of the ALICE-ITS!**

Final Sensor: MISTRAL-O

- **Combination of 4 FSBB-M0 with MIMOSA-22THRb7 pixels**
- **Main characteristics**
  - Chip dimensions: 15 x 30 mm^2
  - Sensitive area: 13.5 x 29.95 mm^2
    - 1.5 mm wide side band (insensitive) (evolving towards 1 mm)
  - 832 columns of 208 (160k) pixels
  - Pixel dimensions: 36 x 65 μm^2
  - In-pixel Pre-Amp & clamping (fringe capa)
  - End-of-column signal discriminator
  - Discriminator's output 2D sparsification (SUZE)
  - Fully programmable control circuitry
  - Pads over pixel array

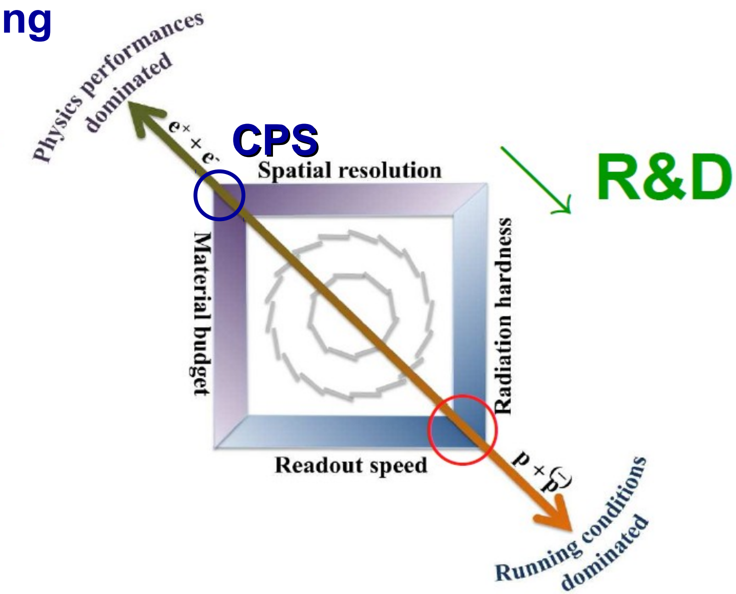


- **Typical performances (**based on FSBB-M0 & MIMOSA-22THRb tests**)**
  - $t_{r.o.}$ ~ 20 μs; σ_{sp} ~ 10 μm; Power consumption $\lesssim$ 80 mW/cm^2
  - Rad. Hardness > 150 kRad $\oplus$ 1.5×10^{12} n_{eq}/cm^2 @ T $\gtrsim$ 30 °C

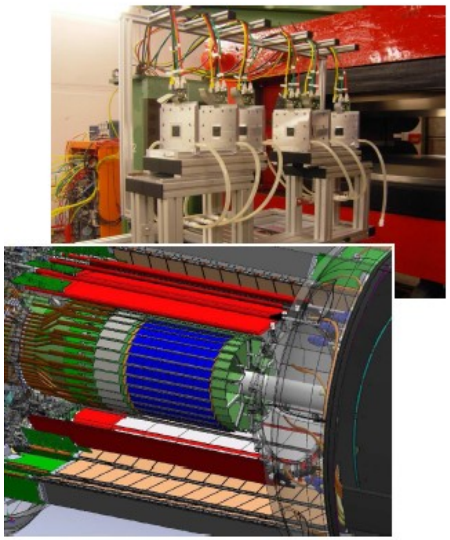
Forthcoming Challenges

Forthcoming Challenges: R&D @ IPHC

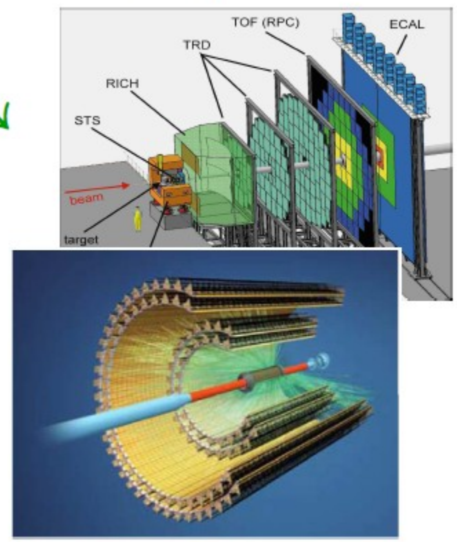
How to improve speed and rad. tolerance while preserving σ_{sp} (3-5 μm) and material budget (< 0.1% X_0)?



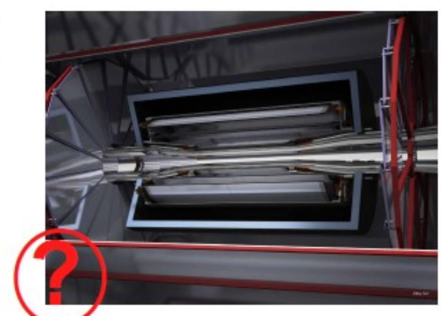
O(10^2) μs



O(10) μs



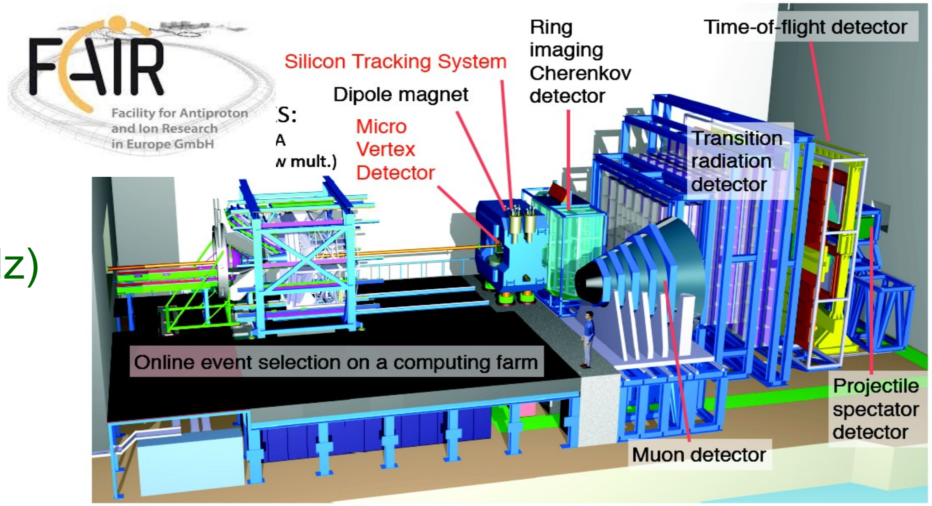
O(1) μs



EUDET/STAR	⟼	ALICE/CBM	⟼	?X?/ILC
2010/14	⟼	2015/2019	⟼	$\gtrsim$ 2020

Micro Vertex Detector (MDV) of CBM @ SIS100

- **Goals**
  - Study of super-dense nuclear matter with relativistic ion-collisions
  - Open charm from 30 GeV p-Au (10 MHz)
  - Low-p tracker: 1-12 GeV Au-Au (30-100 kHz)
- **Beam on target ≳ 2021**
- **MVD**
  - 4 planes of pixels sensors
  - Sensor requirements

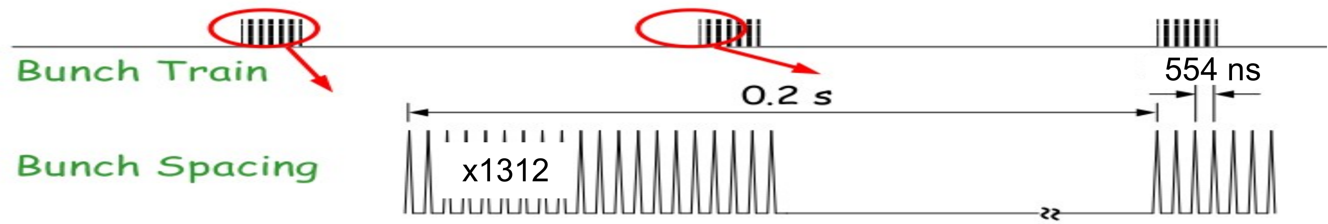


Sensor properties	MISTRAL - O	MIMOSIS-100 (preliminary)
Active surface	13.5 x 29.95 mm²	~ 10 x 30 mm²
Pixels	832 colls x 208 pixels	~ 1500 colls x 300 pixels
Pixel pitch	36 x 65 μm²	22x33 μm ²
Integration time	20.8 μs	30 μs
Data rate	320 Mbps	> 6x 320 Mbps
Rad tol. (non-io)	$>10^{12}$ n_{eq}/cm^2	$>3 \times 10^{13}$ n_{eq}/cm^2
Rad tol (io)	> 100 kRad	> 3 MRad
Operation Temperature	+30°C	-20°C in vacuum

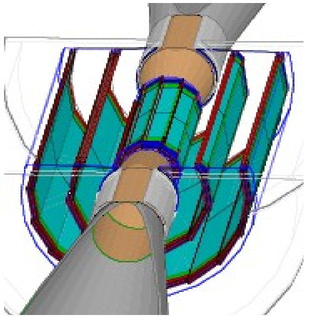
- **In reach with lightly modified APIDE (FSBB?)**

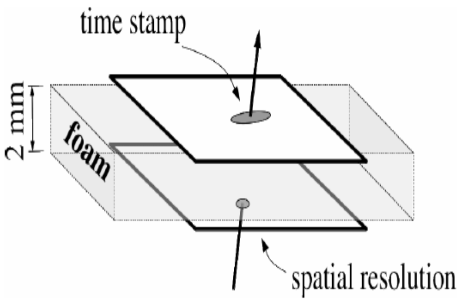
Towards ILC vertex detector

- **ILC collision scheme**



- **Vertex detector (VXD) layout:** 3 layers of double-sided CPS
  - **Mini-vectors:** associate hits in double-sided layers (track seeding in VXD)
  - Different optimization approaches for the different layers
    - **Innermost layers:** low surface & larger occupancy
      - Workout σ_{time} (reduce pile-up) & σ_{sp} (impact parameter)
    - **Outer layers:** larger surface & lower occupancy
      - Can deal with degraded σ_{time} & σ_{sp}
      - Minimize power consumption $\Rightarrow$ material budget



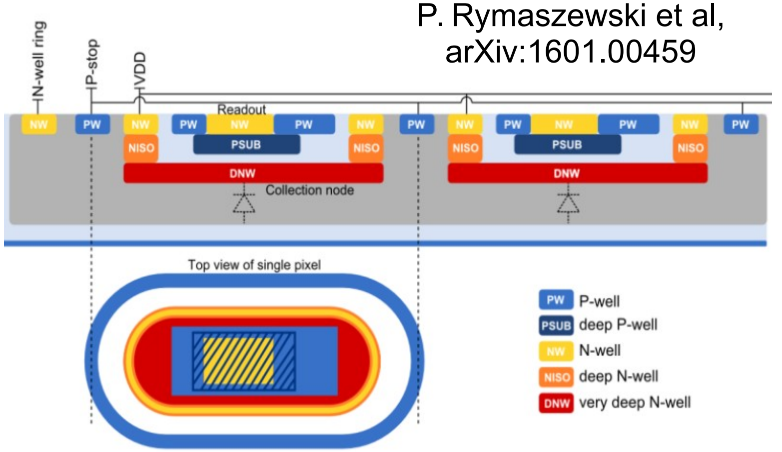


- **R&D ideas (**So far a concept, design being started**)**
  - **Innermost layer:** two digital output sensors with σ_{time} ~ 1 µs (~2 bunches pile-up) in one side and $\sigma_{sp} \lesssim$ 3 µm on the other $\Rightarrow$ Combine asynchr. (σ_{time}) and synchr. (σ_{sp}) readouts
  - **Outer layers:** larger pixels with higher signal-charge-encoding resolution (3-4 bits)

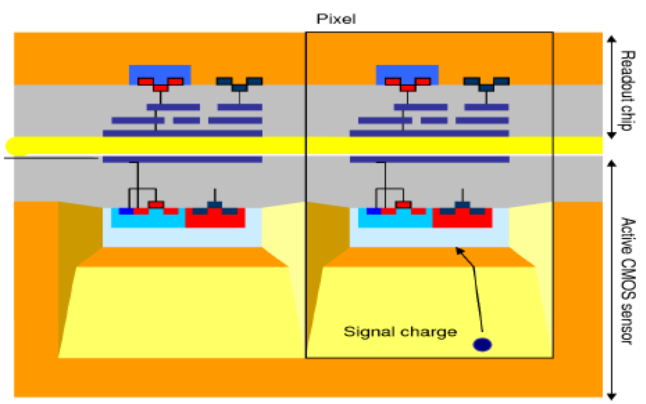
Technology Perspectives for Performance Improvements

- **HV/HR-CMOS sensors:** $d_{dep} \sim 0.3 \sqrt{\rho_{sub} \times U_{bias}}$
  - Extend sensitive volume & improved q-collection
    $\Rightarrow$ Faster signal & stronger rad. tolerance
  - Not bound to CMOS processes using epi-layers
    - Easier access to VDSM (< 100 nm) process
    - Higher in-pixel μ-circuitry density
  - Unanswered questions
    - Minimal pixel dimensions (σ_{sp}) ?
    - Uniformity over large sensitive area & production yield?

P. Rymaszewski et al, arXiv:1601.00459



- **2-tiers chips**
  - Signal sensing (front-end) & processing (r.o.) parts distributed over two interconnected tiers (AC coupling)
  - Smart sensor $\Rightarrow$ 1 r.o. pixel addressing N pixel-front-ends
    $\Rightarrow$ Reduce density of interconnections
  - Can combine 2 diff. CMOS processes: front-end/r.o.
  - **Benefits:** small pixels $\Rightarrow$ resolution, speed, data-compression and robustness
  - **Challenges:** interconnection technology (reliability & cost)



Ivan Peric: CPIX14, Bonn, 2014

Summary

Summary

- **Substantial experience has been collected with running STAR-PXL proving added value of CPS to physics**
  - Demonstrated that CPS can provide spatial resolution and material budget required for numerous applications

- **CPS are suited for vertex detectors (<< 1 m^2) and have attractive features for tracking devices (>> 1 m^2)**

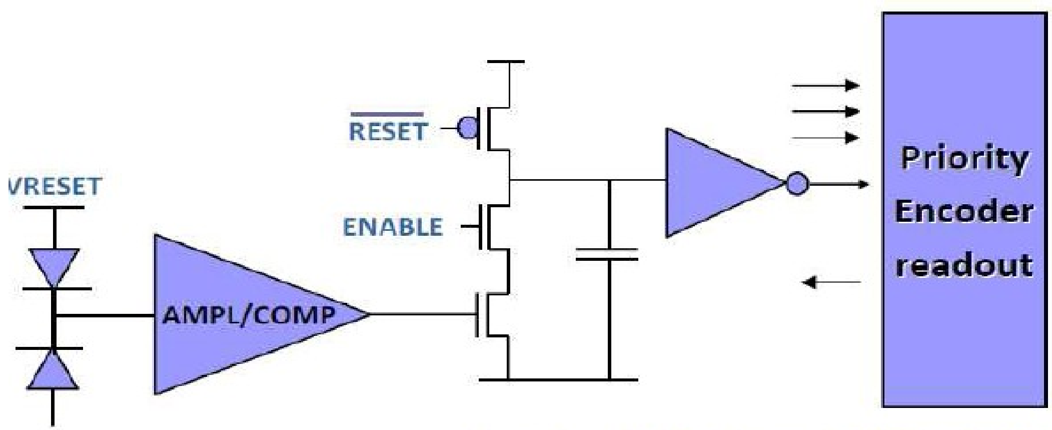
- **Forthcoming Challenges**
  - **CPS for inner trackers:** ALICE-ITS ⇒ large area (10 m^2) to cover with 20-30k sensors
  - **Improve rad. tolerance:** CBM experiment @ FAIR/GSI ⇒ $\gtrsim$ 10MRad ⊕ $\gtrsim 10^{14}\ n_{eq}/cm^2$
  - **Improve readout speed:** ILC vertex detector ⇒ $\lesssim$ 1 µs

- **Perspectives for technological advances**
  - **HV/HR-CMOS sensors:** improvement on charge collection
    ⇒ faster signal and stronger rad. tolerance
  - **2-tier sensors:** combine of 2 CMOS processes for sensing & r.o. parts
    ⇒ more in-pixel intelligence

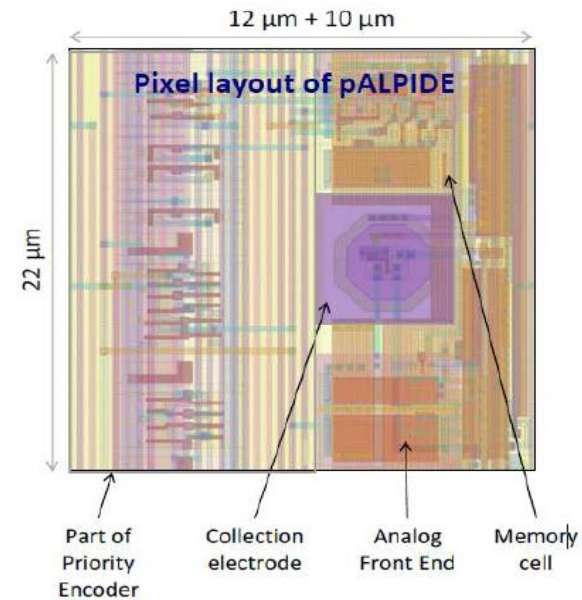
Backup

ALPIDE (ALice PIxel DEtector): readout architecture

- **Concept similar to hybrid pixel readout architecture**
  - TowerJazz CIS quadrupole well process: both N & P MOS can be used
- **Continuously power active in each pixel**
  - Low power consumption analogue front-end (< 50nW/pixel) based on single stage amplifier with shaping
    - High gain ~100
    - Shaping time few μs
  - In-pixel discriminator
  - Binary output stored into multi-event buffer awaiting for external readout
- **Only zero-suppressed data transferred to periphery ⇒ priority encoder readout**



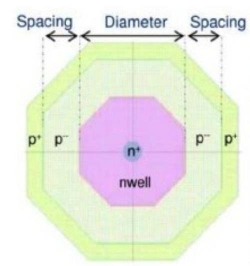
Courtesy of W. Snoeys / TWEPP-2013

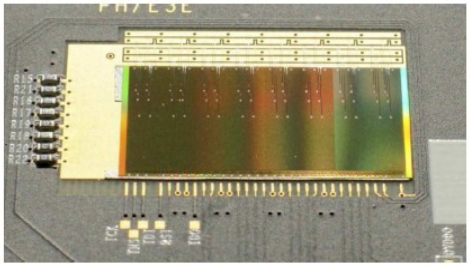


ALPIDE: performances assessment

APIDE-1 beam test @ DESY (5-7 pions)

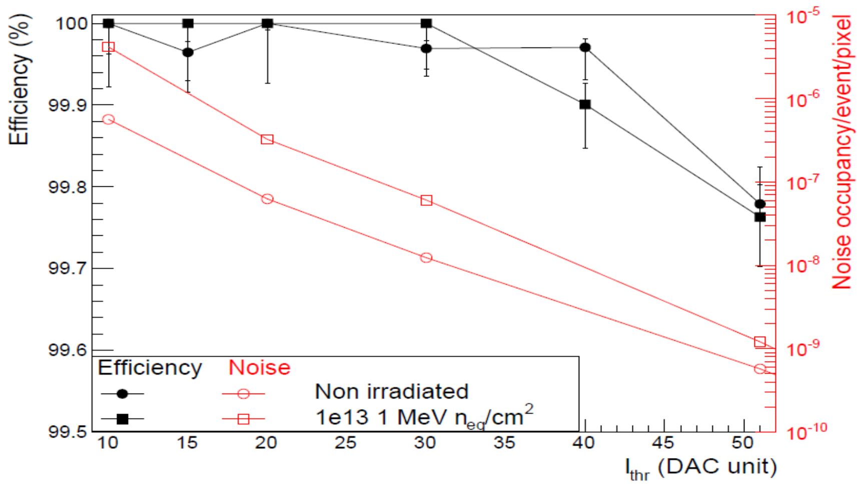
- Final sensor dimensions: 15x30 mm^2
- ~0.5M pixels of 28x28 μm^2
- 4 different sensing node geometries
- Possibility of reverse biasing the substrate
  $\Rightarrow$ default is -3 V (better epi-layer depletion)
- Possibility to mask pixels (fake-rate mitigation)
  $\Rightarrow$ default is O(10^{-3}) pixels

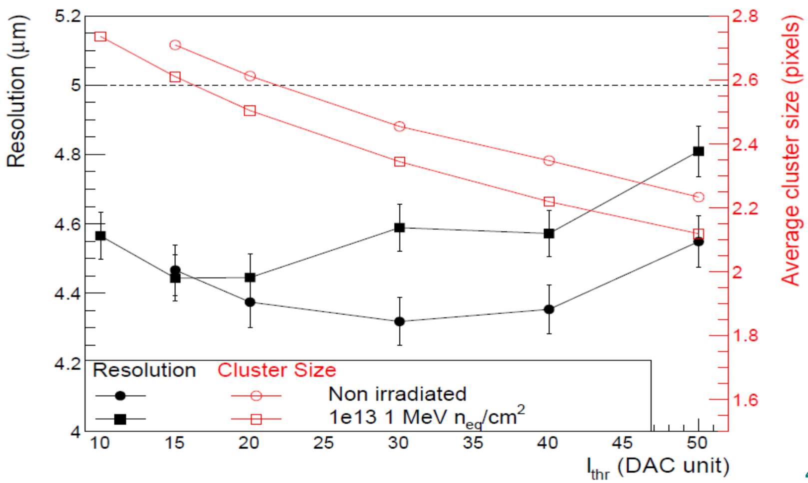




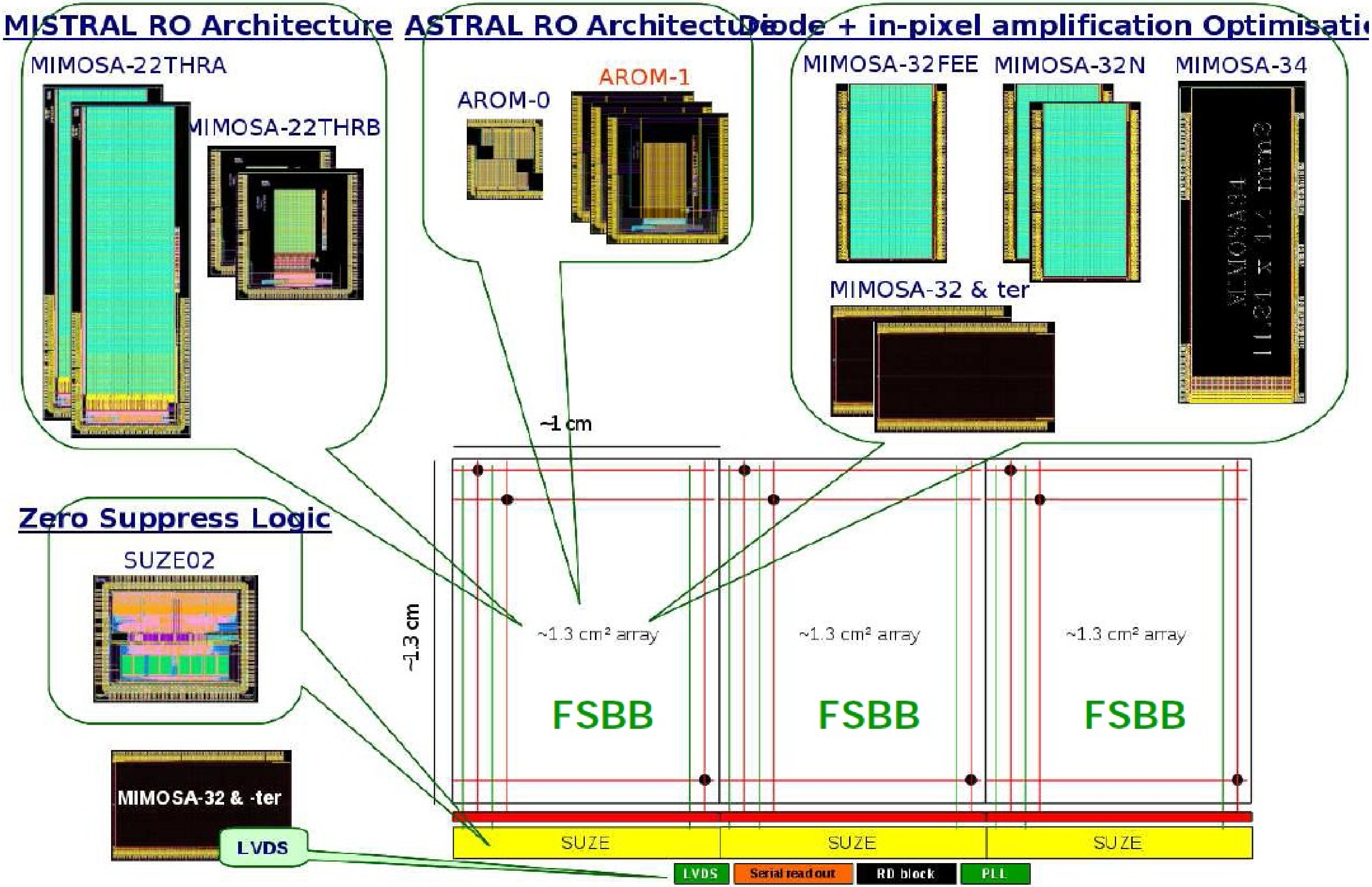
Performances

- ε_{det} > 99%, σ_{sp} < 5μm, fake-rate < 10^{-5}
- Slight deterioration after irradiation



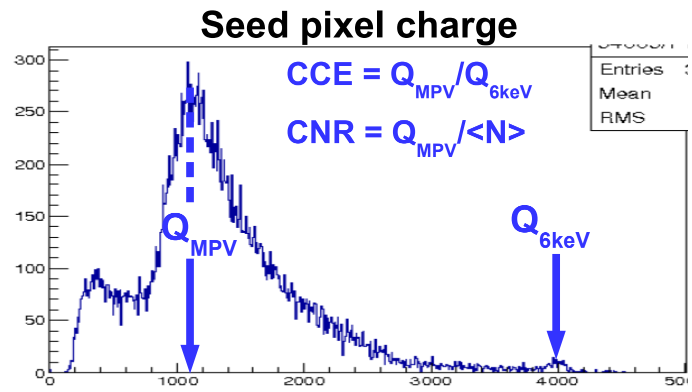


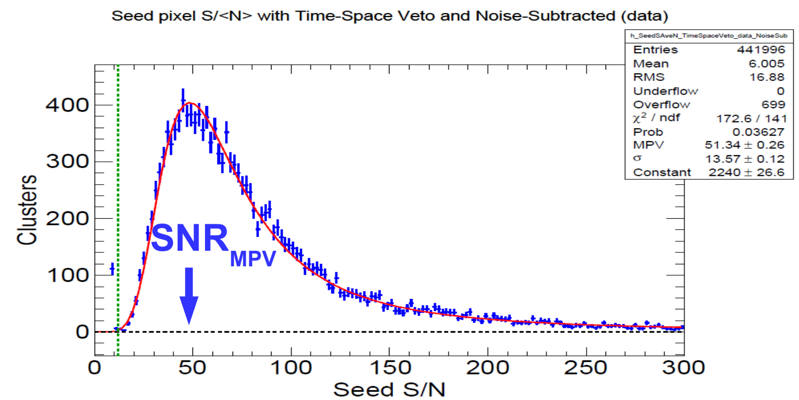
Exploring full sensor chain: Prototypes fabricated

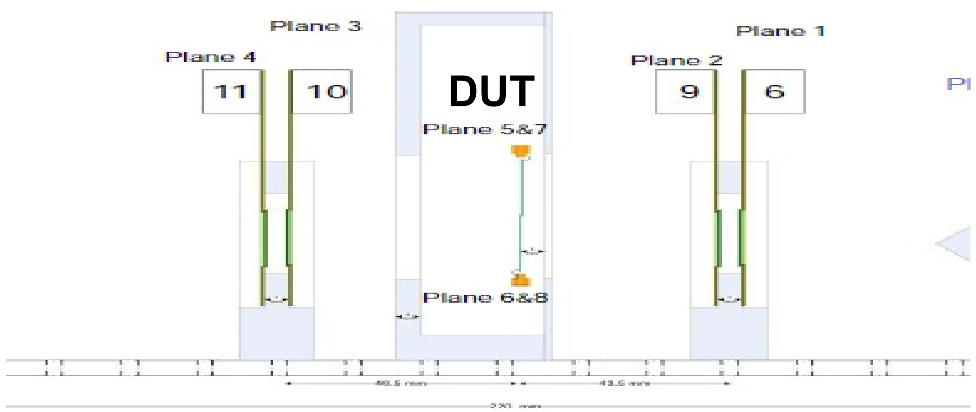


The Testing Probes

- **Laboratory tests**
  - Noise characterization and fake rate
  - ^{55}Fe X-ray source
    - ~6keV line
    - Gain, CCE and CNR
  - ^{90}Sr β^- source (Q = 2.28 MeV)
    - SNR, ε_{det} and cluster multiplicity
- **Test-beam (TB) facilities**
  - SPS: ~100 GeV/c $\pi^\pm$
  - DESY: ~5 GeV/c e^-
  - Frascati: ~500 MeV/c e^-
  - SNR, ε_{det}, cluster multiplicity and σ_{sp}

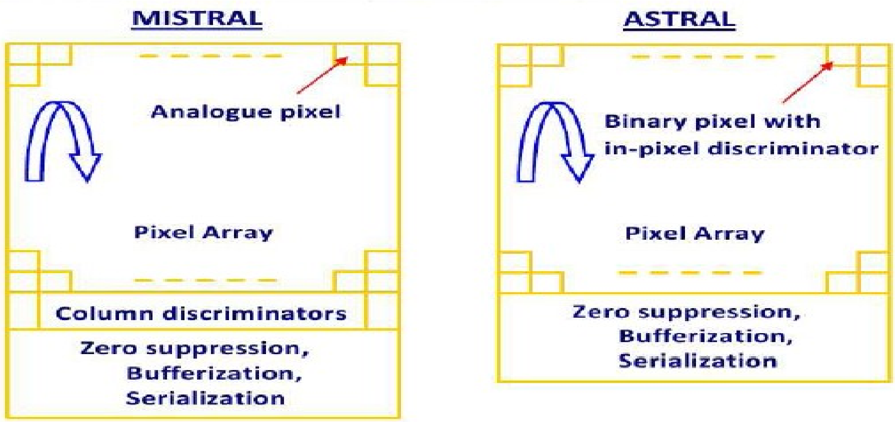




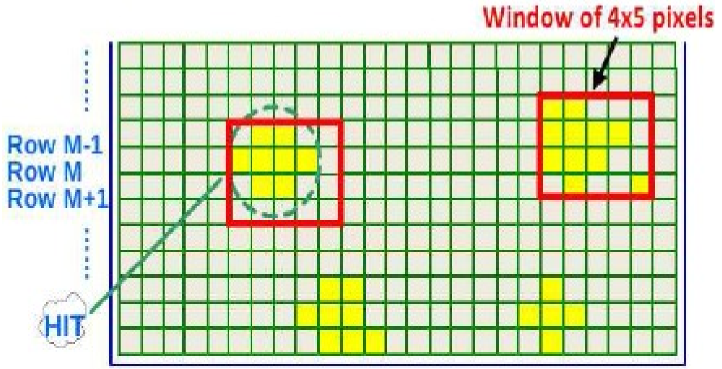


MISTRAL-O: Synchronous readout

- **Design addresses 3 issues**
  - Increasing S/N at pixel-level
    - Sensing node optimization
  - ADC @
    - end-of-column ⇒ **MISTRAL**
    - pixel ⇒ **ASTRAL**



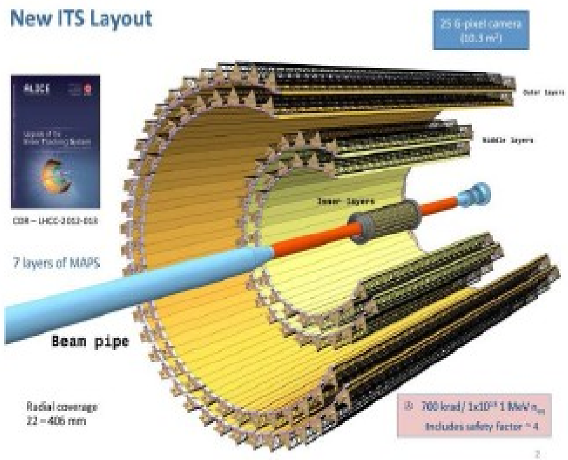
  - SUZE at chip periphery
    - 2D sparsification algorithm with 4x5 pixels window (evolution from 1D sparsification on ULTIMATE chip)



- **Power vs Speed**
  - **Power:** only the selected rows (N=1,2,3 …) to be readout
  - **Speed:** N rows of pixels are readout in ||
    - Integration-time (t_{int}) = frame readout time ⇒

$$t_{int} = \frac{(Row\ readout\ time) \times (No.\ of\ Rows)}{N}$$

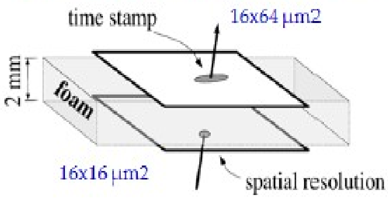
R&D of CMOS pixel sensors



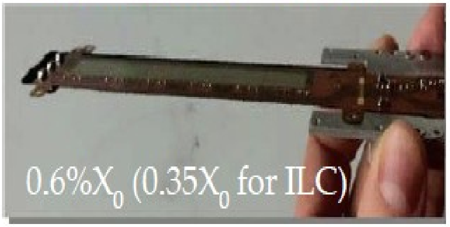
ALICE-ITS =NEW DRIVING APPLICATION OF CPS
based on a better suited (180 nm) CMOS process
(TDR approved by LHCC in March '14)

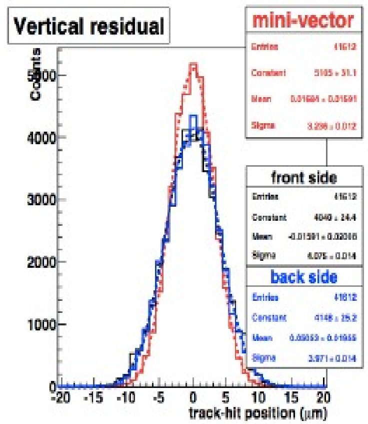
- 1st real scale sensor prototype adapted to 10 m² fabricated
  → 1st test results validate achitecture in 180 nm technology
  → 2-4 times faster read-out w.r.t. 0.35 μm technology, with up to 60 % power reduction

CPS MAPS: Spatial Resolution and Time Stamping



Ultrathin ladder - PLUME

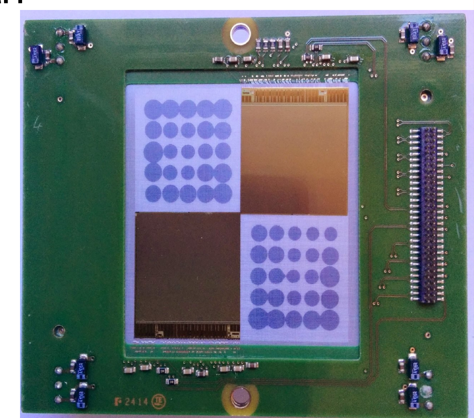




AIDA Telescope

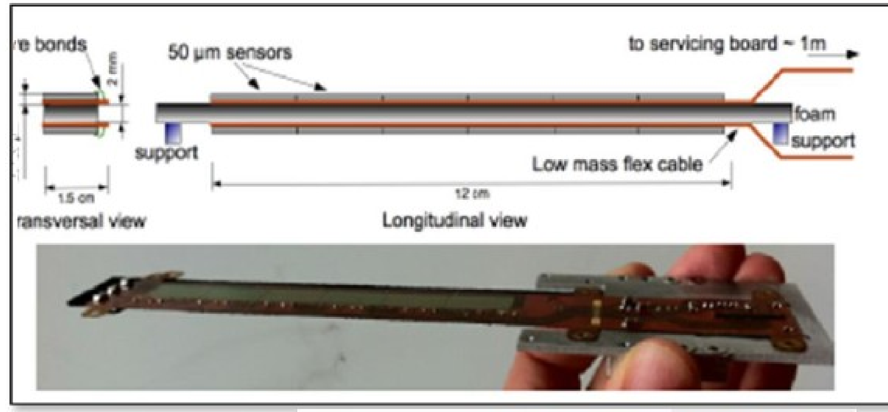
- Big surface and thin reference planes with high spatial resolution
- Sensing area = 4x3.8cm2
- Additional plane with high temporal resolution

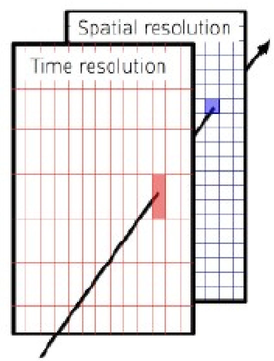
  ⇒ time stamping

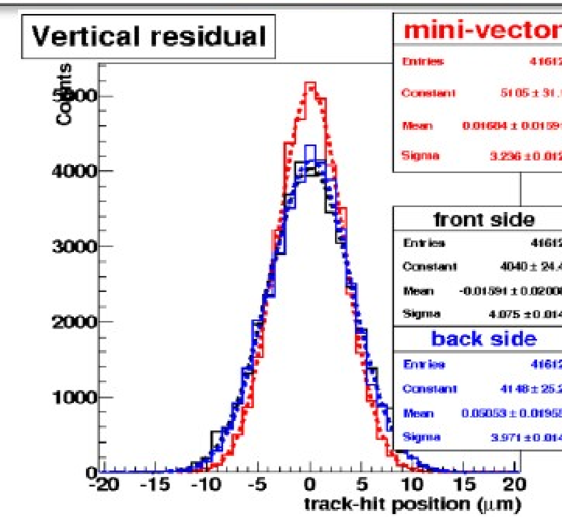


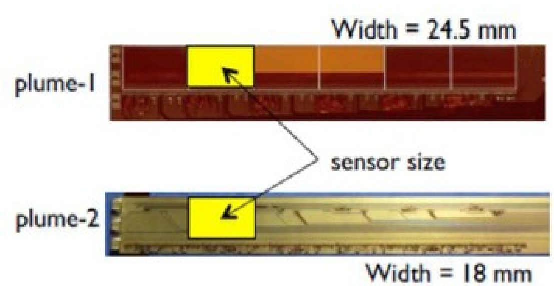
Sensor integration in Ultra Light Devices

- Double sided ladders expected benefits
  - Alignment & tracking (pointing)
  - Beam background rejection ?
  - Material budget, 1 mechanical support
  - Redundancy (efficiency)
  - Each layer optimized
    - ➢ read-out speed vs resolution
- PLUME coll. (Bristol, DESY, IPHC)
- Plume 01 prototype (<2012)
  - Fabricated
    - ➢ 2 x 6 Mimosa 26 chips
    - ➢ 2 mm low density SiC foam
    - ➢ Validated in test beam (2011)
    - ➢ Operated with air cooling
    - ➢ 0.6 % X_0
- Plume 02 prototype
  - Under construction (spring 2015)
  - Reduced mat. Budget
    - ➢ Reduced width (24.5 mm ⇨18mm)
    - ➢ Lighter (alu) flex cable, mechanical support
    - ➢ 0.6 % X_0 ⇨ ~ 0.35 % X_0 (cross-section)

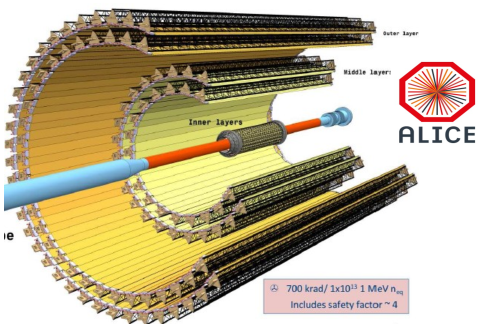








Next Forthcoming device: CBM Micro-Vertex Detector (MVD)

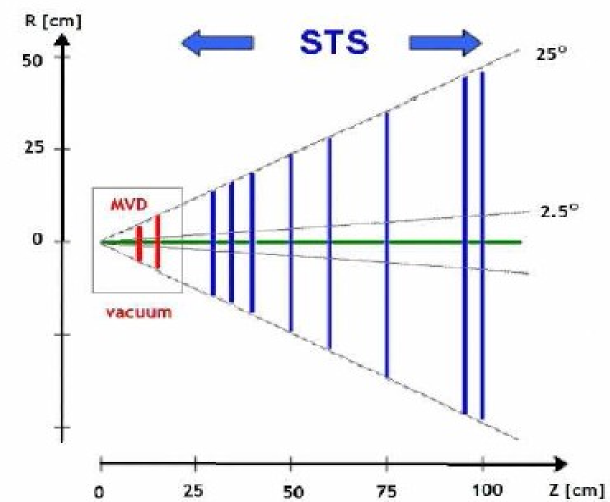


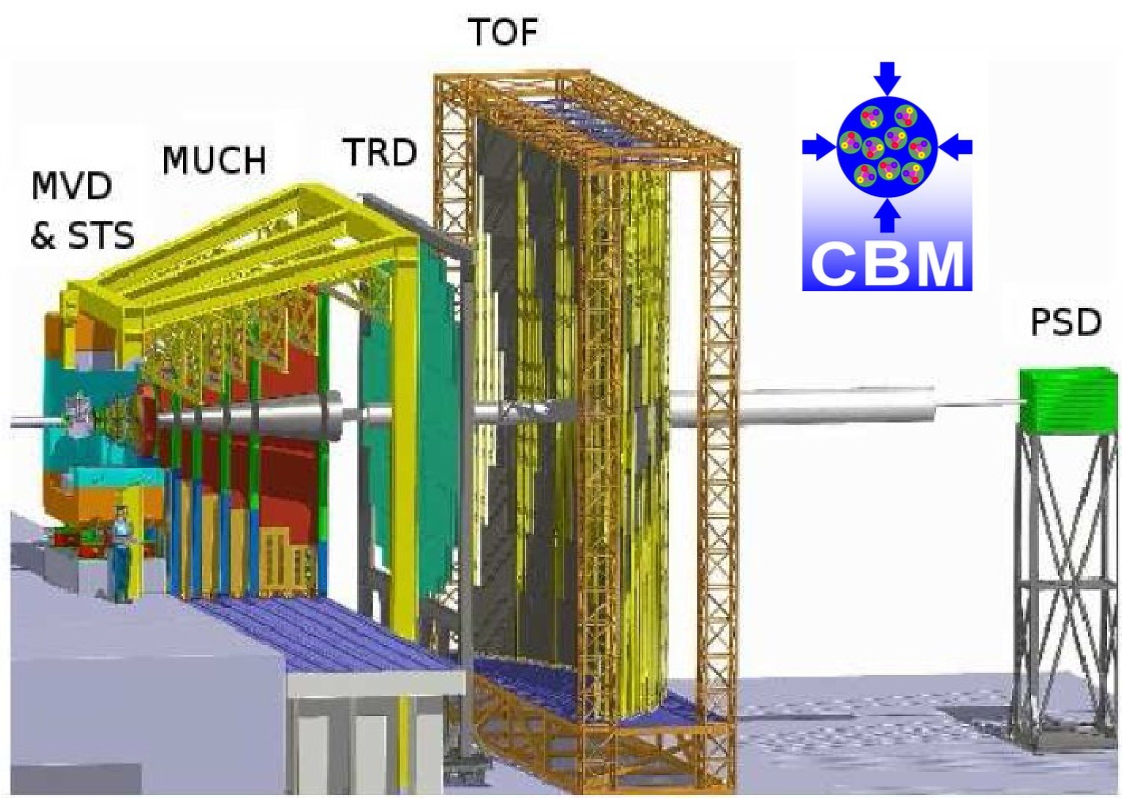
ALICE-ITS 2018/19

CBM-MVD at FAIR/GSI

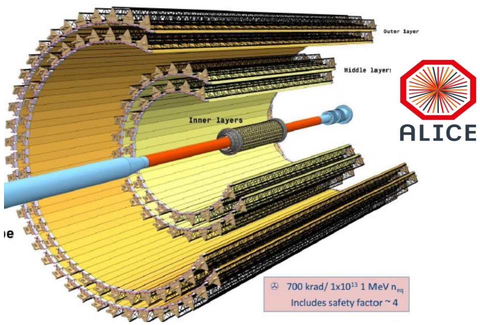
3 double-sided stations in vacuum at T < 0°C

- $\sigma_{sp} \lesssim 5\ \mu m$
- $\sim 0.5\ \%\ X_0$ / station
- Radiation load: $\gtrsim 10^{14}\ n_{eq}/cm^2$

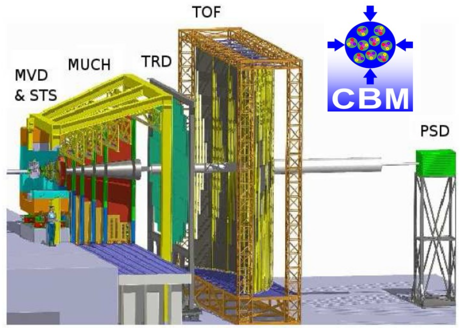




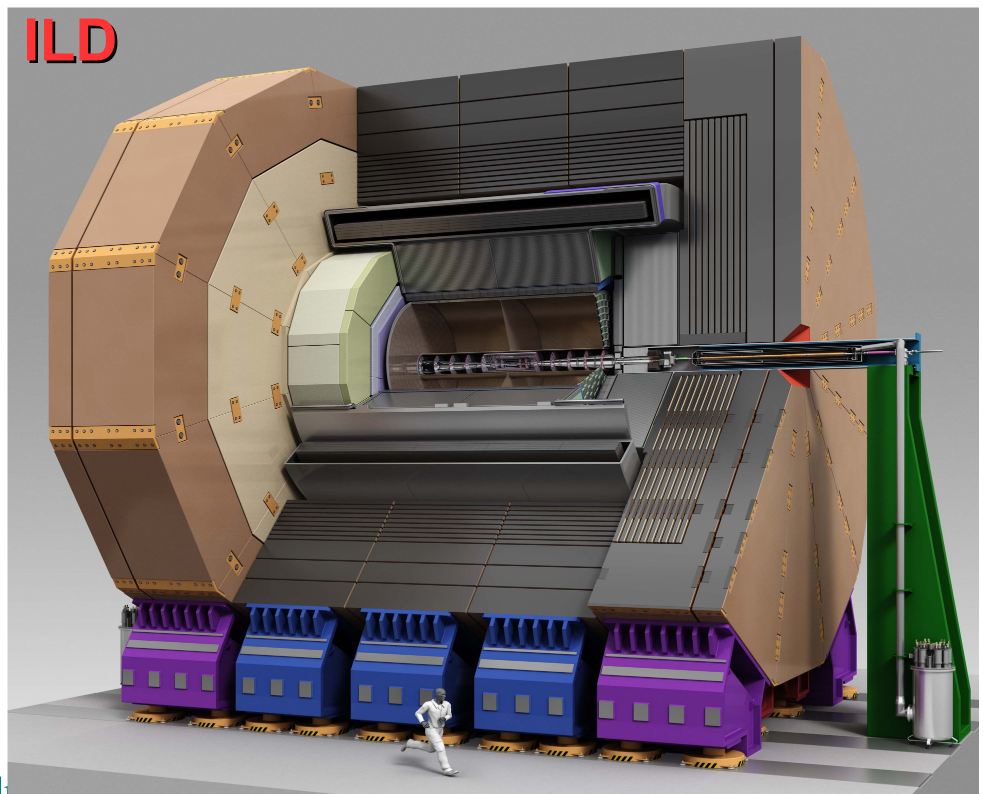
Device under Study: ILC Vertex Detector



ALICE-ITS 2018/19



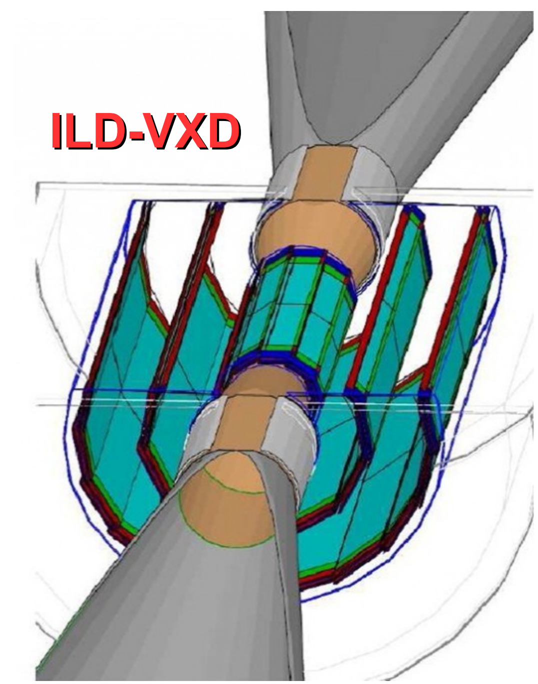
CBM-MVD > 2020



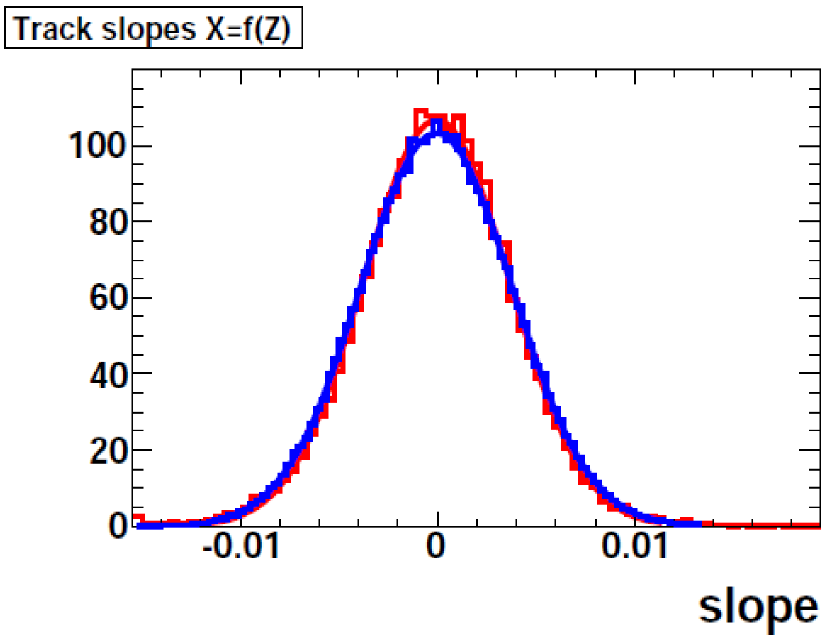
ILD-VXD at ILC

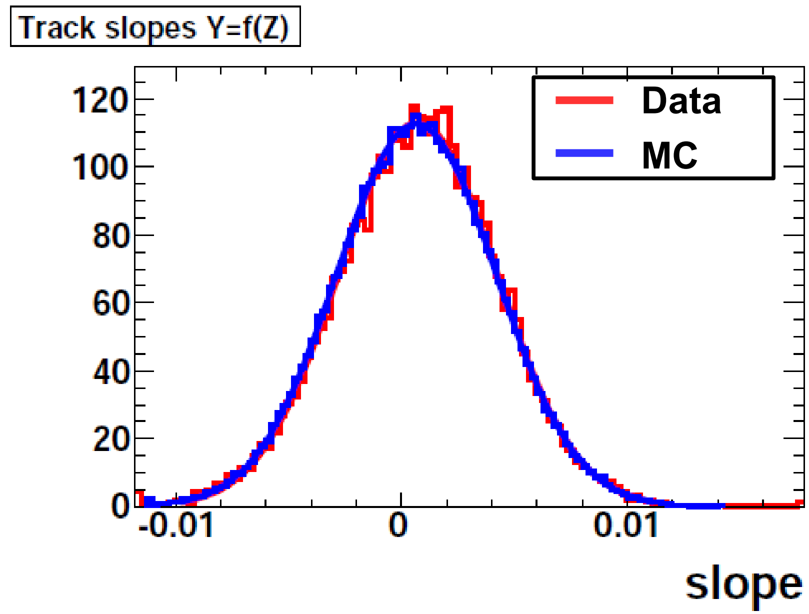
3 double-sided layers

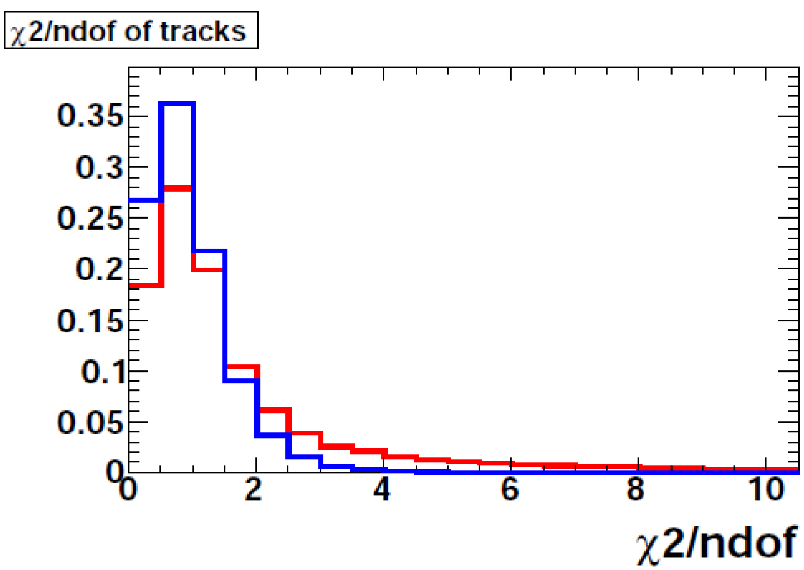
- $\sigma_{sp} \lesssim 3\ \mu m$
- ~ 0.3 % X_0 / layer
- Radiation load: O(100) kRad + $O(10^{11})\ n_{eq}/cm^2$ (1yr)



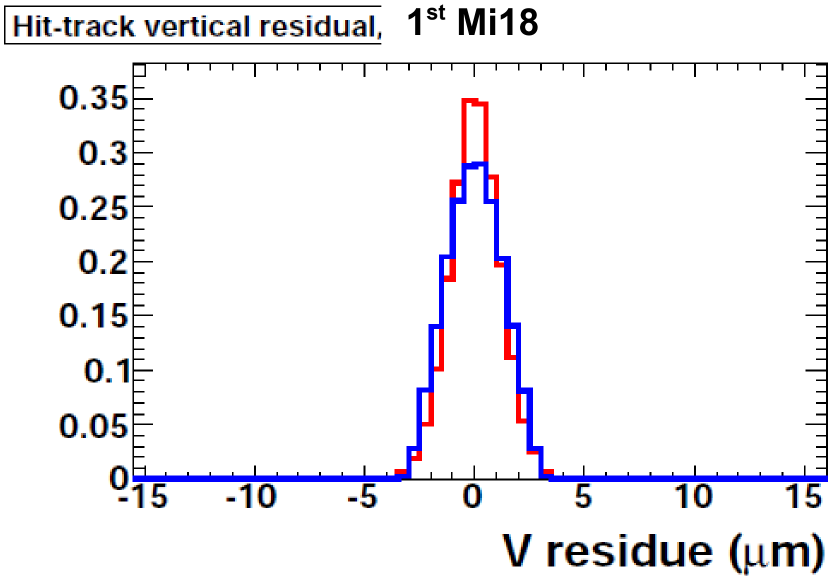
BTF Telescope Simulation: Performances (I)

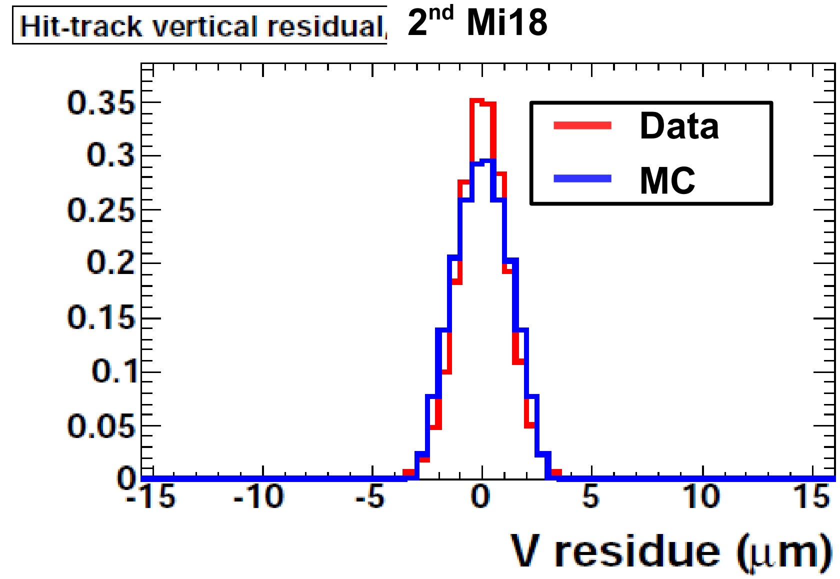


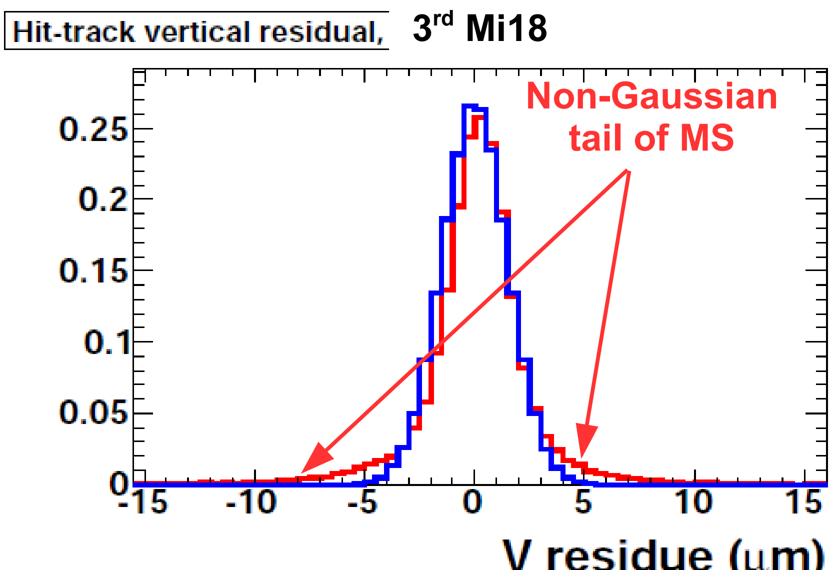


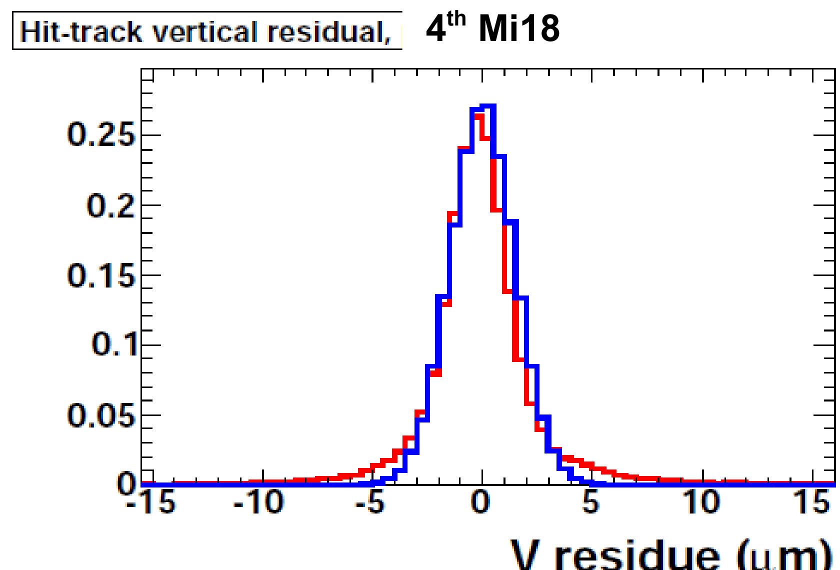


BTF Telescope Simulation: Performances (II)



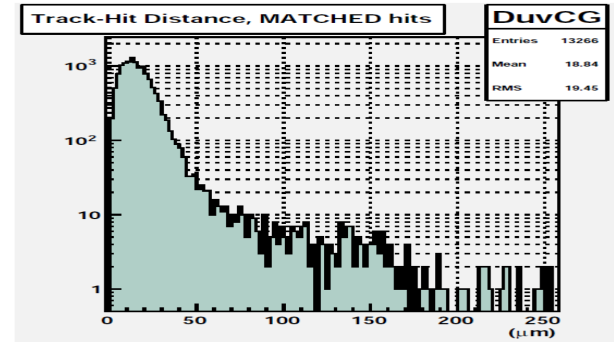






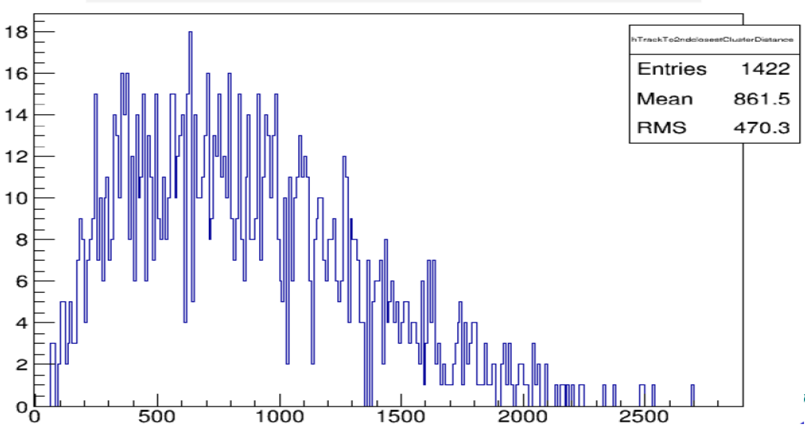
BTF Analysis strategy & Efficiency correction

- **Analysis strategy**
  - Reconstruct tracks and extrapolate @ DUT
  - Associate DUT hits to track within track-hit distance cut
  - Evaluate DUT ε_{det} and σ_{sp}

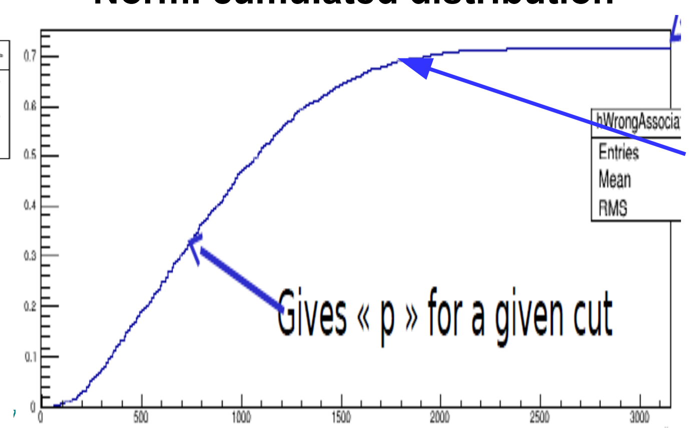


- **Efficiency Correction: $\varepsilon_{det}^{corr} = (\varepsilon_{det}^{raw} - p)/(1 - p)$**
  - Due to MS non-Gaussian tails some track-hit distance seems quite large (few 100μm)
    - Enlarging the track-hit distance has 2 consequences on non-efficient events
      - Increases probability to get a fake hit in this area
      - Increases probability to associate a real hit from other track
  - Method
    - Use efficient events to get the distribution of the 2nd closest hit to the track
    - Use normalized cumulated distribution to estimate **p**

Track – hit distance of the 2nd closest hit

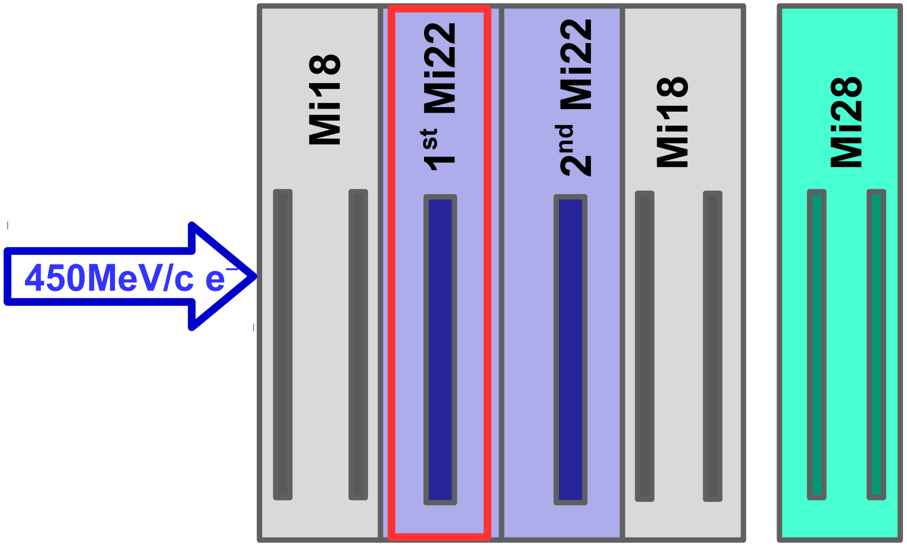


Norm. cumulated distribution



Doesn't saturate to 1 because some events have only one hit

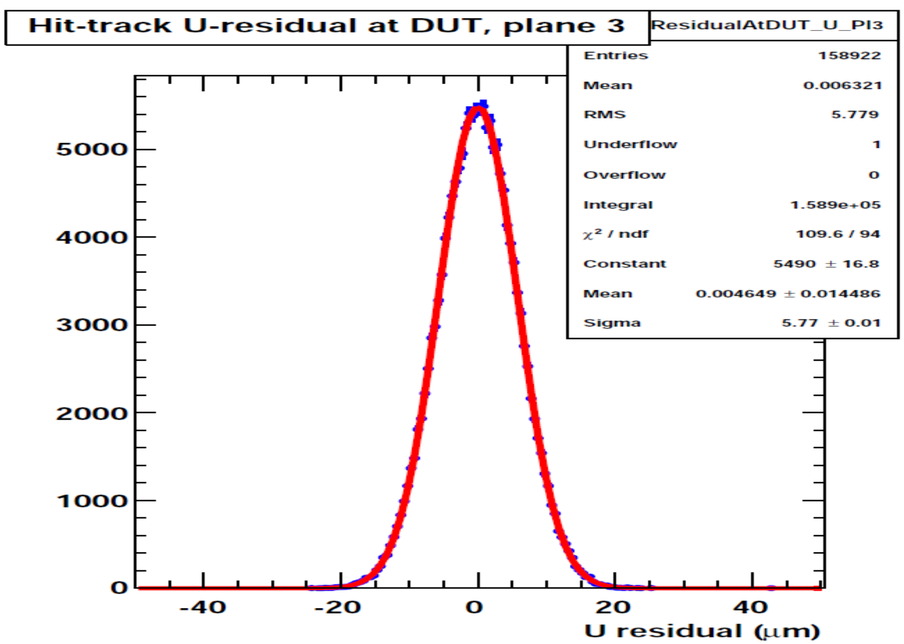
BTF Telescope Simulation: σ_{Tel} @ 1st DUT position

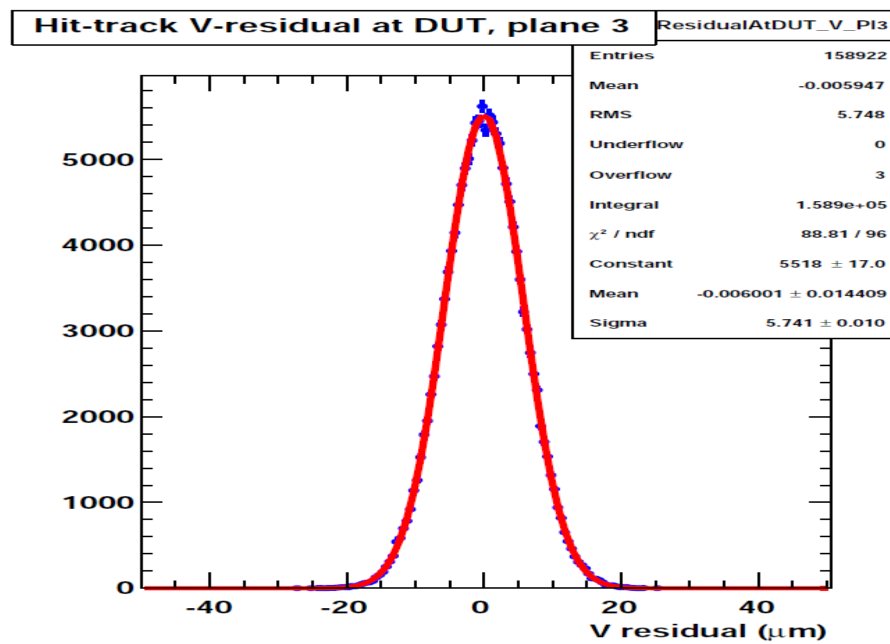


Telescope resolution @ 1st DUT position
(both DUTs supposed thinned to 50µm)

$$\sigma_{Tel} = (5.77 \pm 0.01_{stat} \pm 0.20_{syst})\ \mu m$$

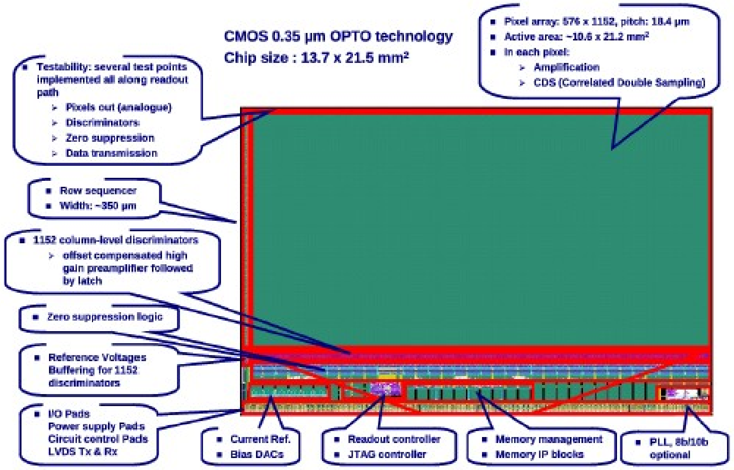
Telescope resolution confirmed with Geant3 based simulation

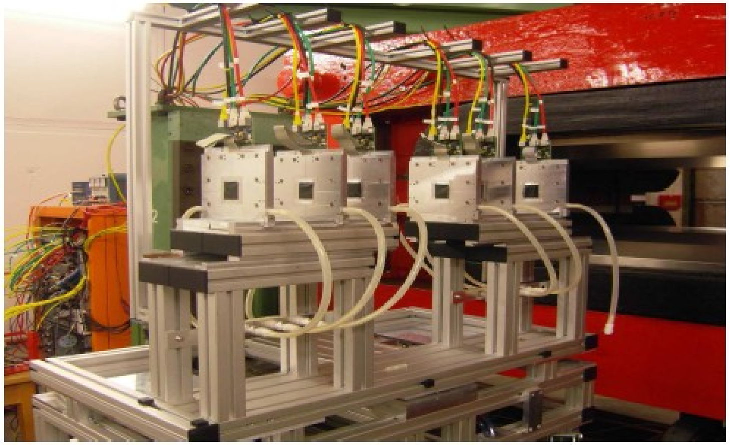




CMOS Pixel Sensors: Established Architecture

- **Main characteristics of MIMOSA-26 sensor equipping EUDET BT :**
  - 0.35 μm process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)
  - column // architecture with in-pixel amplification (cDS) and end-of-column discrimination, followed by $\emptyset$
  - binary charge encoding
  - active area: 1152 columns of 576 pixels (21.2×10.6 mm^2)
  - pitch: 18.4 μm $\longmapsto$ $\sim$ 0.7 million pixels
    - $\triangleright$ charge sharing $\Rrightarrow$ $\sigma_{sp} \sim$ 3.-3.5 μm
  - $t_{r.o.} \lesssim$ 100 μs ($\sim 10^4$ frames/s)
    - $\hookrightarrow$ suited to $> 10^6$ part./cm^2/s
  - JTAG programmable
  - rolling shutter architecture
    - $\Rrightarrow$ full sensitive area dissipation $\cong$ 1 row
    - $\triangleright$ $\sim$ 250 mW/cm^2 power consumption (fct of N_{col})
  - thinned to 50 μm (yield $\sim$ 90 %)





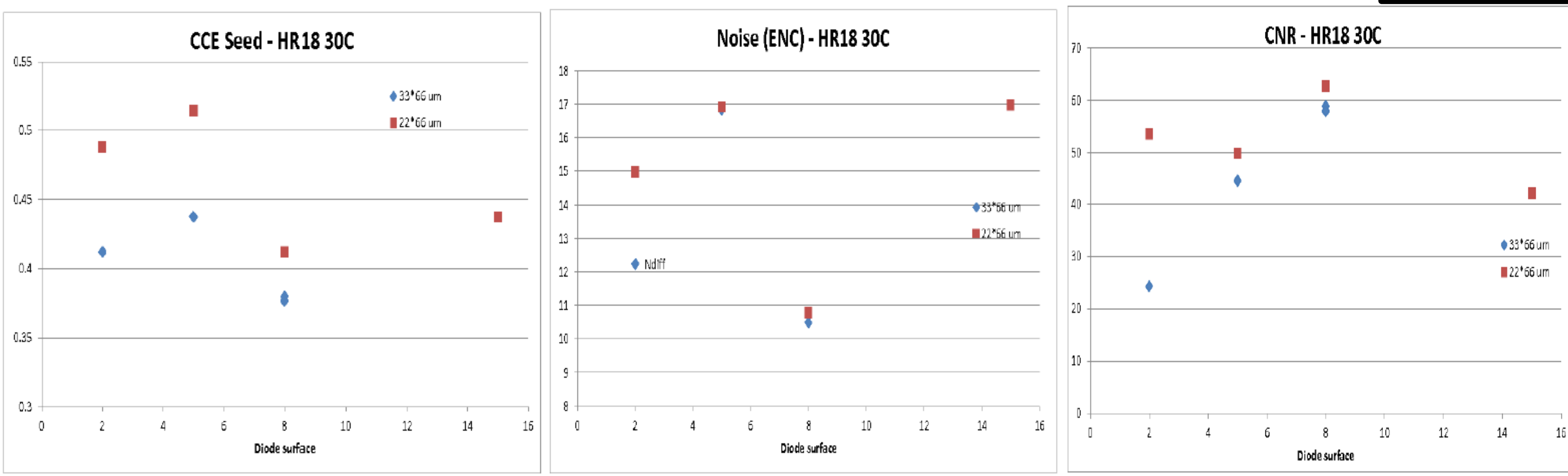
- **Various applications :** VD demonstrators, NA63, NA61, FIRST, oncotherapy, dosimetry, ...

9

^{55}Fe source: CCE/Noise/CNR vs diode for large pixels

- CCE, TN and CNR vs sensing node for large pixels with HR18 epi-layer

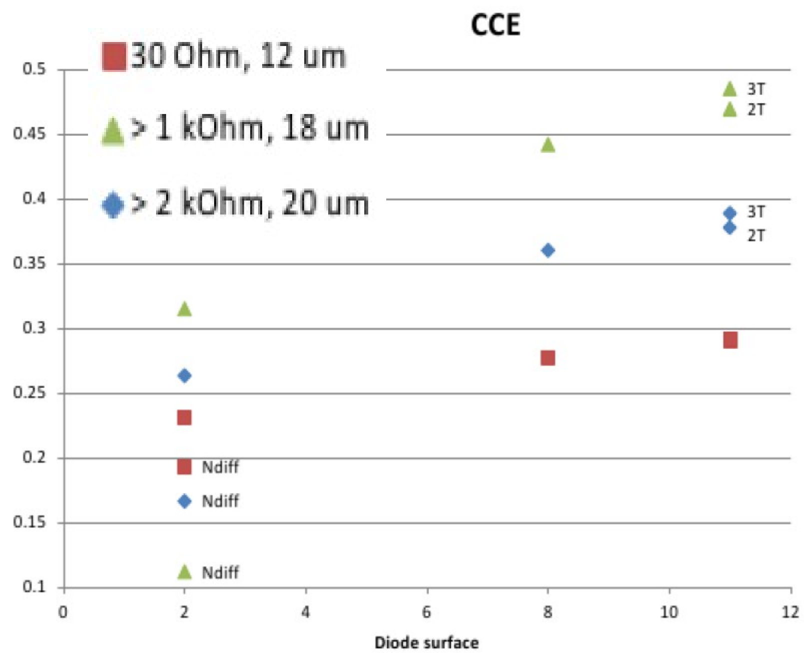
33*66 um
22*66 um

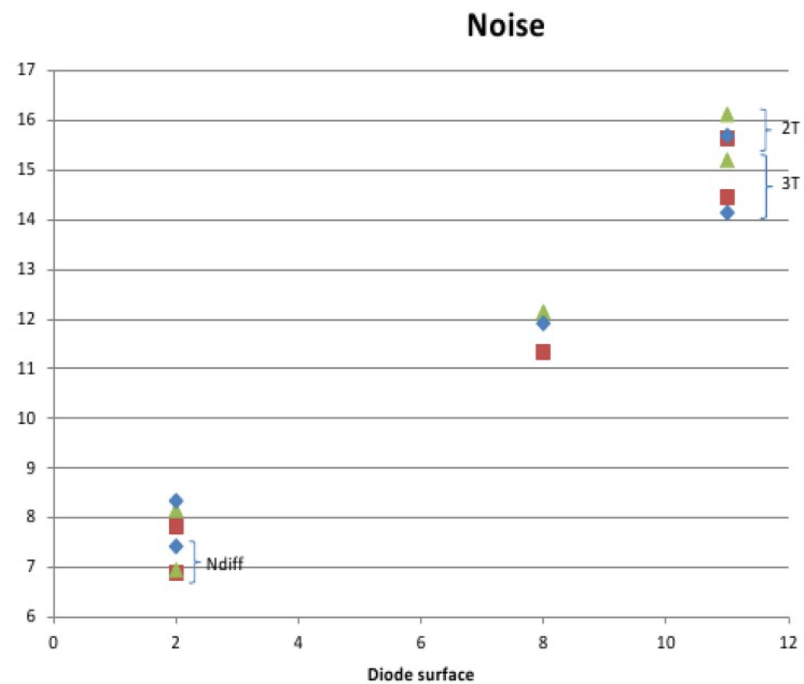


- Good to excellent CCE, even for small sensing diodes or for 33x66 μm^2 pixels
- TN ~ 17/11 e^- ENC for single 10.9/8 μm^2 sensing diodes
- TN ~ 17/15 e^- ENC for pairs of 5/2 μm^2 sensing diodes
- High CNR: up to ~60 for 8 μm^2 sensing diodes
- Pixel detection performances fully satisfactory ⇒ confirmation from beam test (see next slide)

^{55}Fe source: CCE & Noise vs diode for small pixels

- CCE and TN for 22x33 μm^2 pixels for different diode dimensions (footprint 10.9 μm^2)



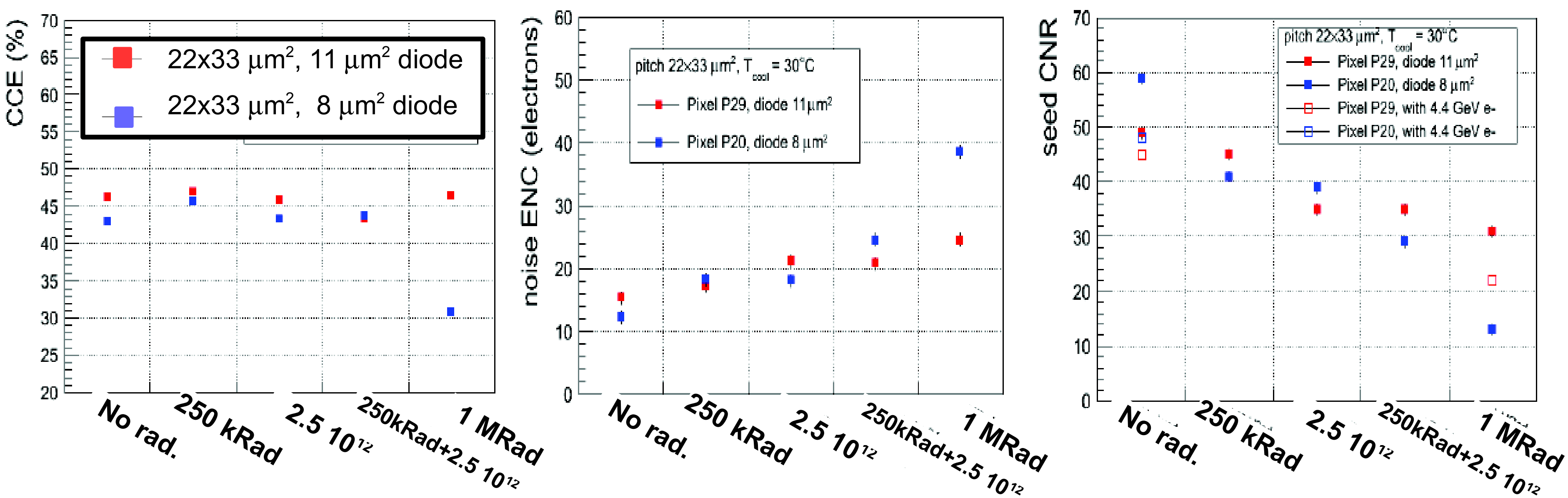


- CCE is highest for HR18 epi-layer
- Weak dependence of CCE with diode dimensions ⇒ around 30% for 2μm^2
- Nearly linear variation of TN with diode dimensions

  ⇒ 8 → 16 e$^-$ ENC for diode 2 → 10.9 μm^2
- Small sending diode with > 10 μm^2 footprint attractive in terms of CCE

^{55}Fe source: radiation tolerance for 22x33 μm^2 pixels

- **MIMOSA-34:**
  - 22x33 μm^2 pixels with diode of 8 and 10.9 μm^2: TN and CCE/CNR @ T = 30° C from ^{55}Fe source for different irradiations
  - Comparison when possible of CNR and SNR from 4.4 GeV e$^-$ TB (DESY)
  - **Comments:**
    - Small diode more sensitive to TID
    - TID impacts both CCE and TN
    - CNR of 10.9 μm^2 diode pixel exceeds 20 (MPV) after 250 kRad + 2.5x10^{12}n$_{eq}$/cm^2

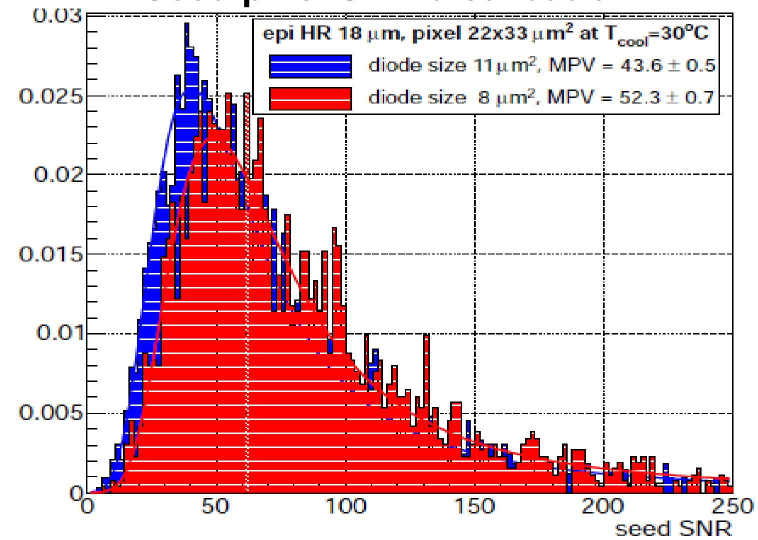


MIMOSA-34: sensing node impact for small pixels

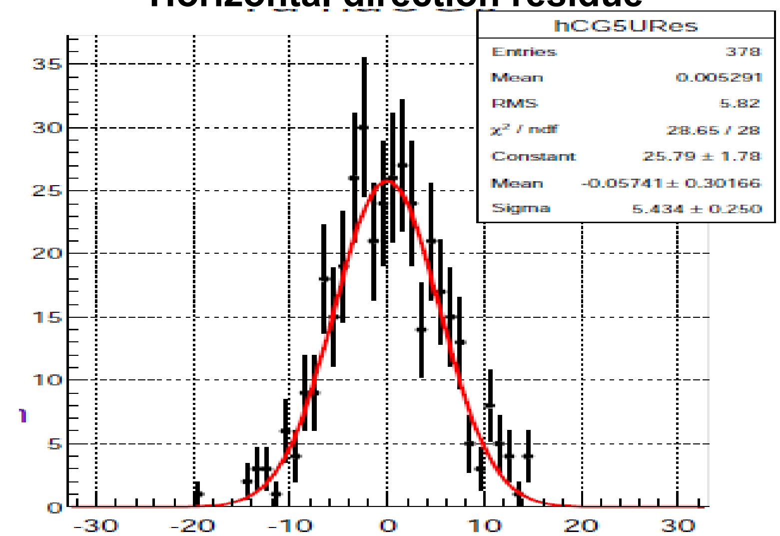
- **DESY BT Set-up (August 2013):**
  - 2BT: 8xSi-strips & 6xMIMOSA-26 (120 μm thick)
  - ~4.4 GeV/c e^- beam

- **MIMOSA-34:** 22x33 μm^2 pixels @ T = 30°C
  - **Sensing node impact (HR18)**
  - Sub-arrays: P-29 10.9/10.9 μm^2 diode/footprint
    P-20 8.0/10.9 μm^2 diode/footprint
  - 8μm^2 diode features ~20% higher SNR (MPV)
    ⇒ slightly higher ε_{det} (both > 99%)
  - Q_{clus} ~ 1350/1500 e^- for 8/10.9μm^2 diode
    ⇒ marginal charge loss
  - Binary residue: 5-5.5 μm ⇒ σ_{sp} < 5 μm

Seed pixel SNR distribution

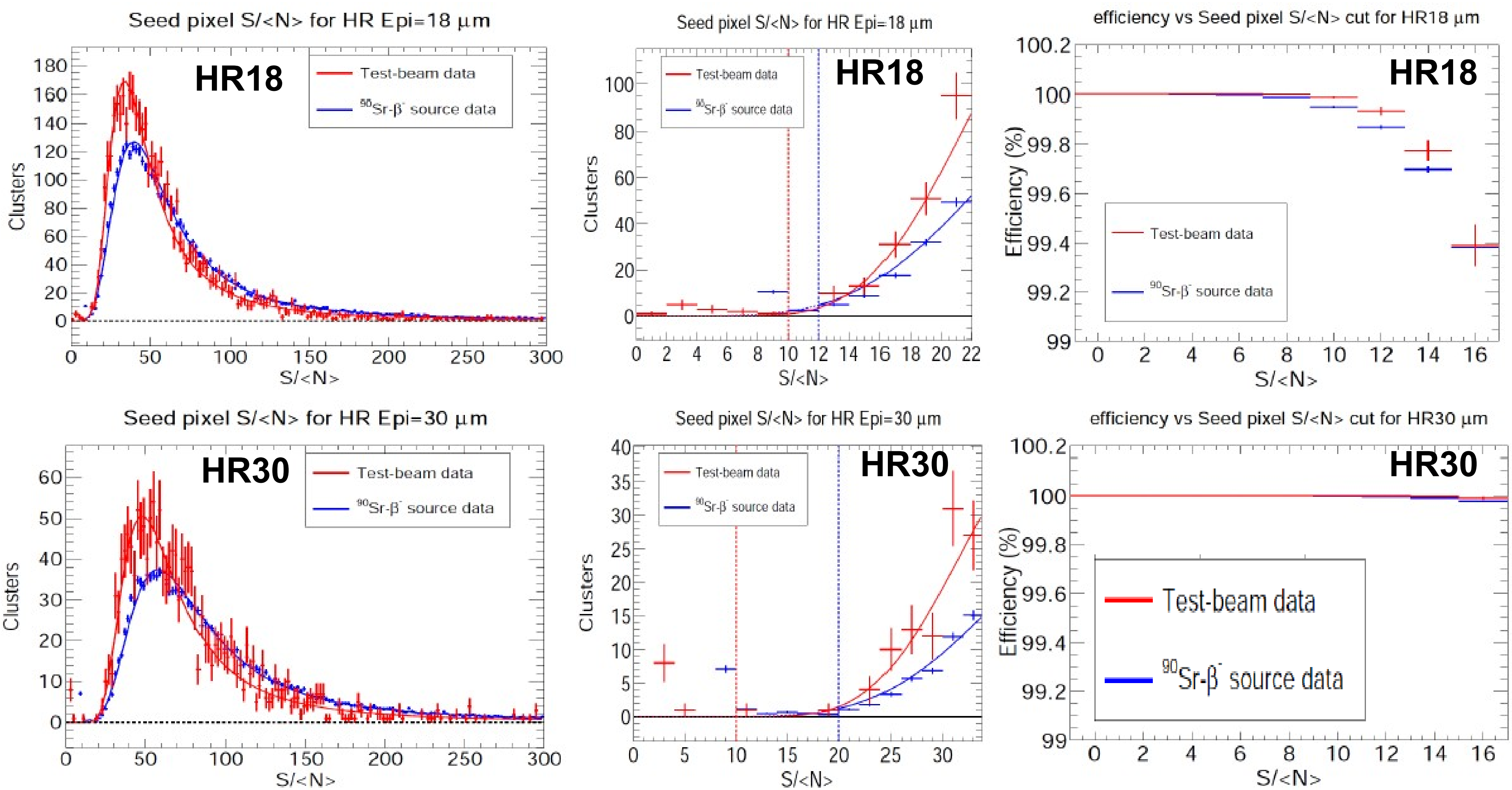


Horizontal direction residue



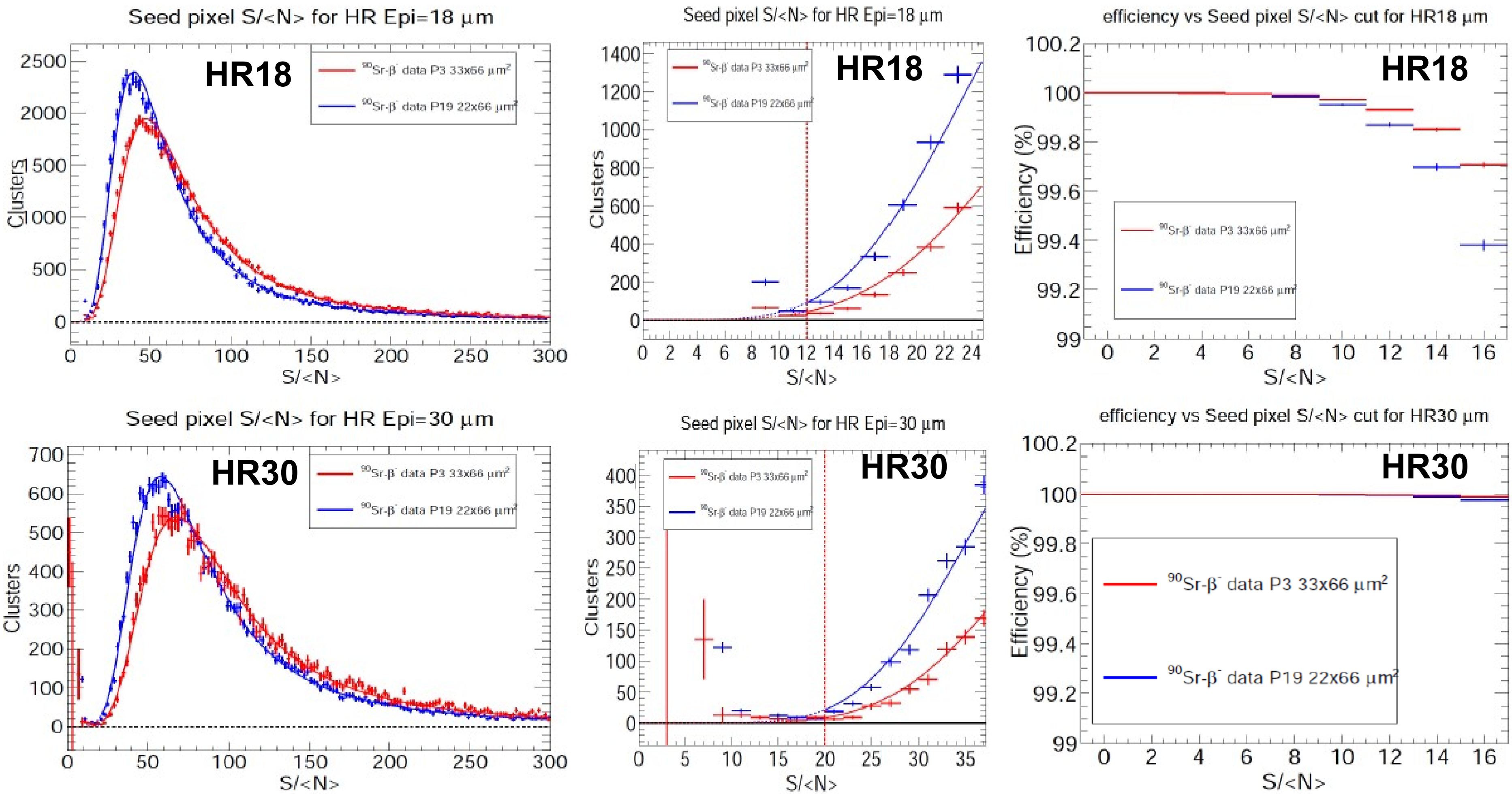
β^- (^{90}Sr) source vs 4.4 GeV e^- (DESY)

- **MIMOSA-34:**
  - β^- (^{90}Sr) vs 4.4 GeV e^- for 22x66 μm^2 pixels: SNR & ε_{det} for HR18/HR30
  - **Conclusion:** lab test with β^- (^{90}Sr) source allow estimating ε_{det}



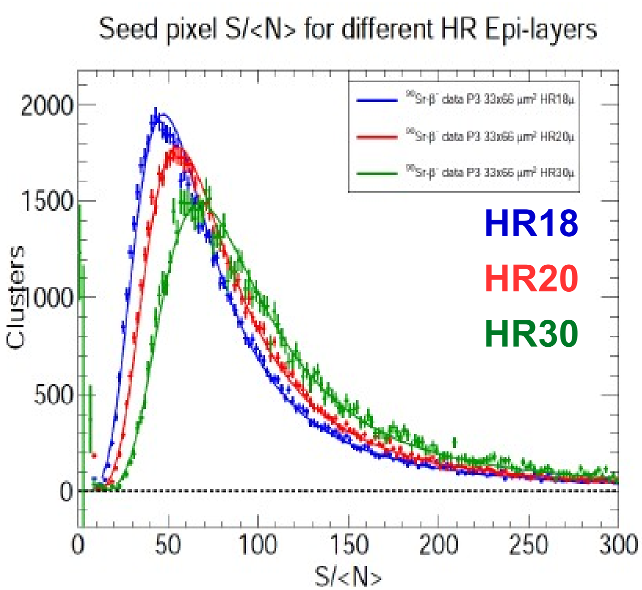
From 22x66 to 33x66 μm^2 pixels

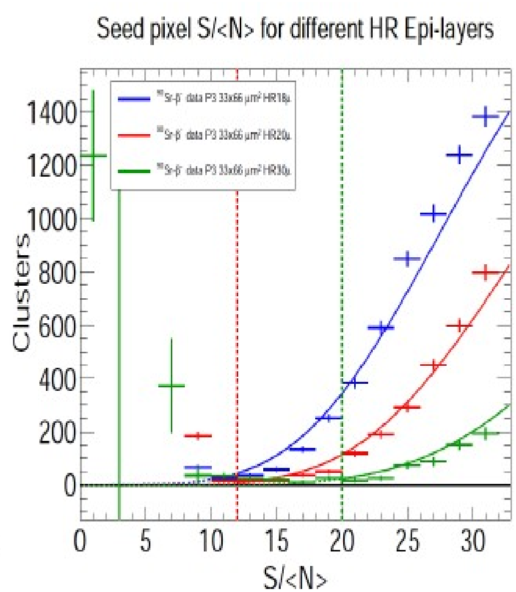
- **MIMOSA-34:**
  - 22x66 vs 33x66 μm^2 pixels: SNR & ε_{det} with β^- (^{90}Sr) for HR18/HR30
  - **Comment:** 33x66 μm^2 (8/15 μm^2 diode/footprint) pixels exhibit high SNR ⇒ high ε_{det}

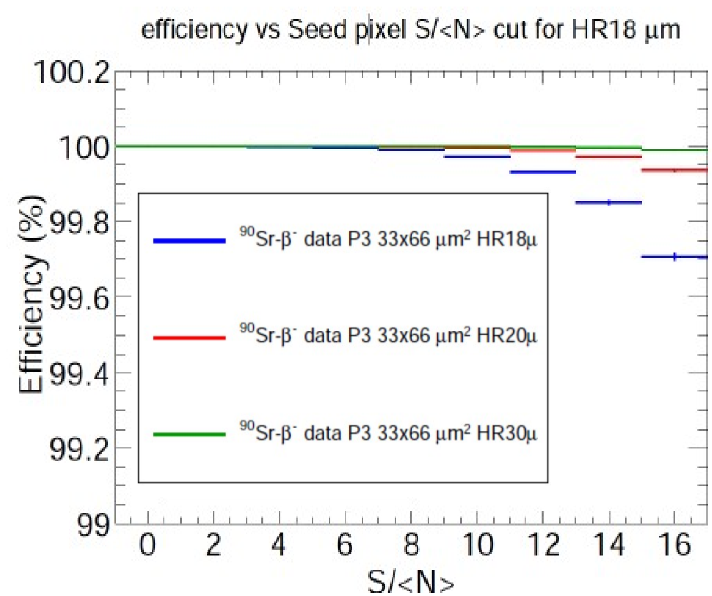


33x66 μm² pixels vs epitaxial-layer

- **MIMOSA-34:**
  - 33x66 μm² pixels (8/15 μm² diode/footprint): SNR & ε_{det} with β^- (^{90}Sr) for HR 18,20,30
  - **Comments:**
    - Single 8/15 μm² diode/footprint provides high SNR despite large pixel (low sensing node density)
    - HR30 epi-layers gives high SNR (MPV ~ 70) from β^- (^{90}Sr) $\Rightarrow$ pretty high ε_{det} for high SNR cut (e.g. 10)
    - Expected spatial resolution for 33x66 μm² pixels: $\sigma_{sp} \approx 10\mu m$

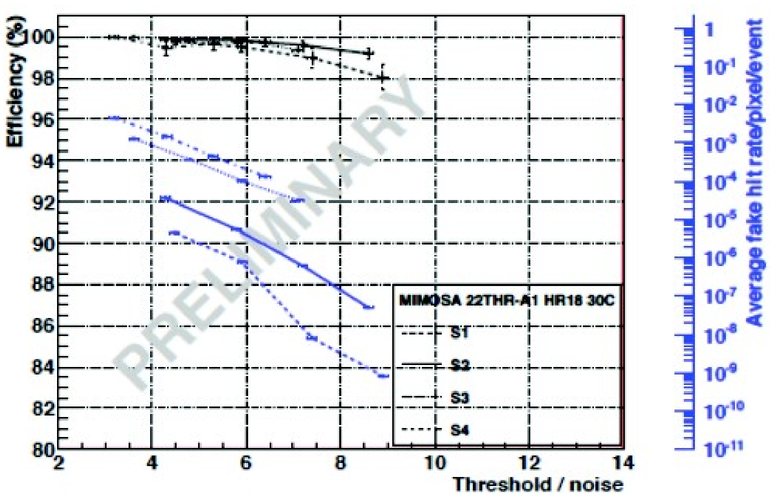


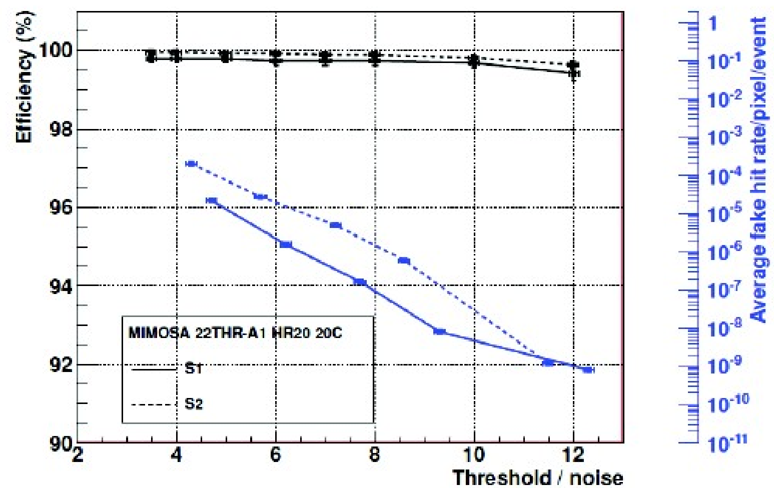




Det. Efficiency & Fake rate

- Measured from 128 columns ended with discriminators: MIMOSA-22THRa1

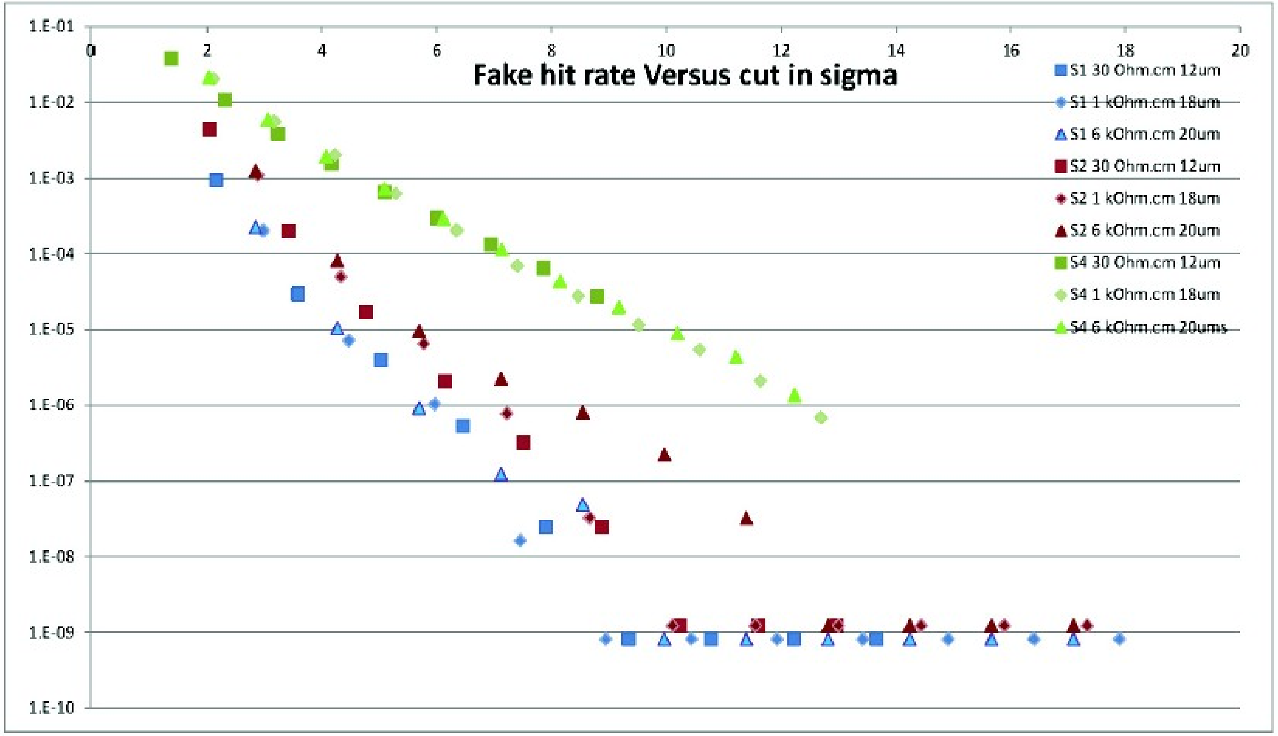




- For threshold within 5 to >10 times the <noise>
  - Efficiency > 99.5 %
  - Fake hit rate $\lesssim$ O(10^{-5})

- S1 = T gate: 2x0.36 μm^2
- S2 = T gate: 1x0.36 μm^2
- S3 = T gate: 1x0.18 μm^2 (small diode)
- S4 = T gate: 1x0.18 μm^2

MISTRAL-like: fake rate



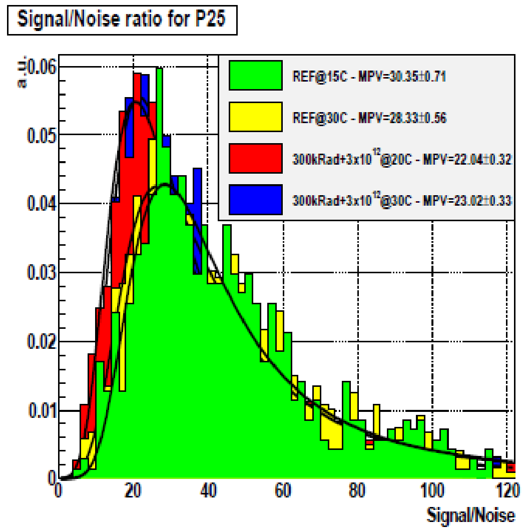
Input transistor gate

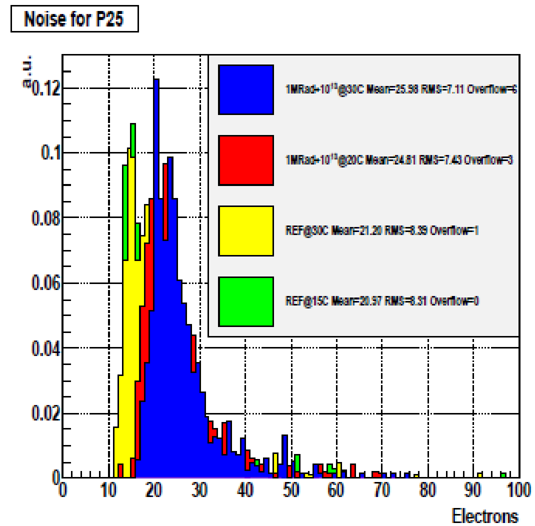
- S1 = 2x0.36 μm^2
- S2 = 1x0.36 μm^2
- S3 = 1x0.18 μm^2 (small diode)
- S4 = 1x0.18 μm^2

Enlarged input transistor gate:

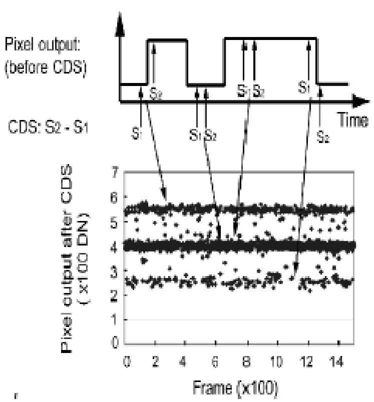
➡ Effective mitigation of fake rate due to noisy pixels

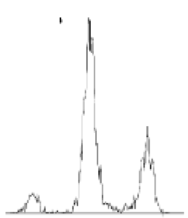
- **Steps validated in 2012 :**
  - ✳ Several in-pixel amplifier variants lead to satisfactory SNR & det. eff. ($20\times20\ \mu m^2$) incl. after 1 MRad & $10^{13} n_{eq}/cm^2$ at 30°C
  - ✳ Results pres. at VCI-2013 (J. Baudot)

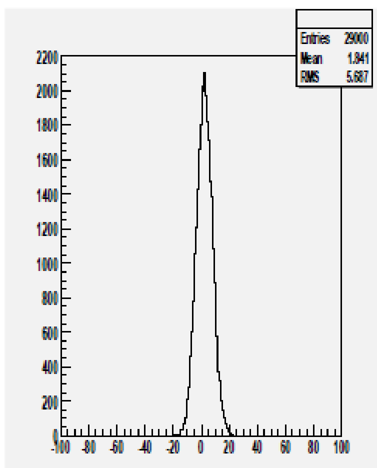


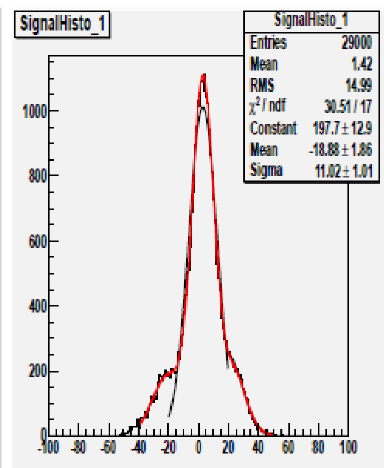


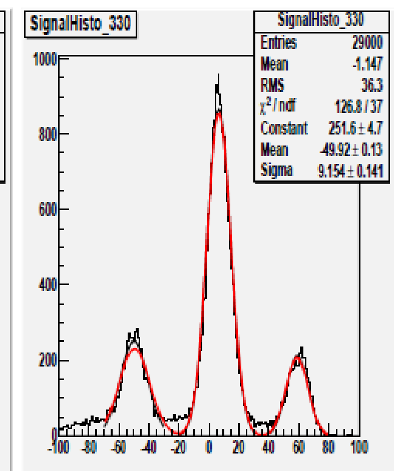
- **Call for improvement :**
  - ✳ **Pixel circuitry noise :**
    tail due few noisy pixels
    ↪ **attributed to RTS noise**
    ⇒ required optimising T geometries







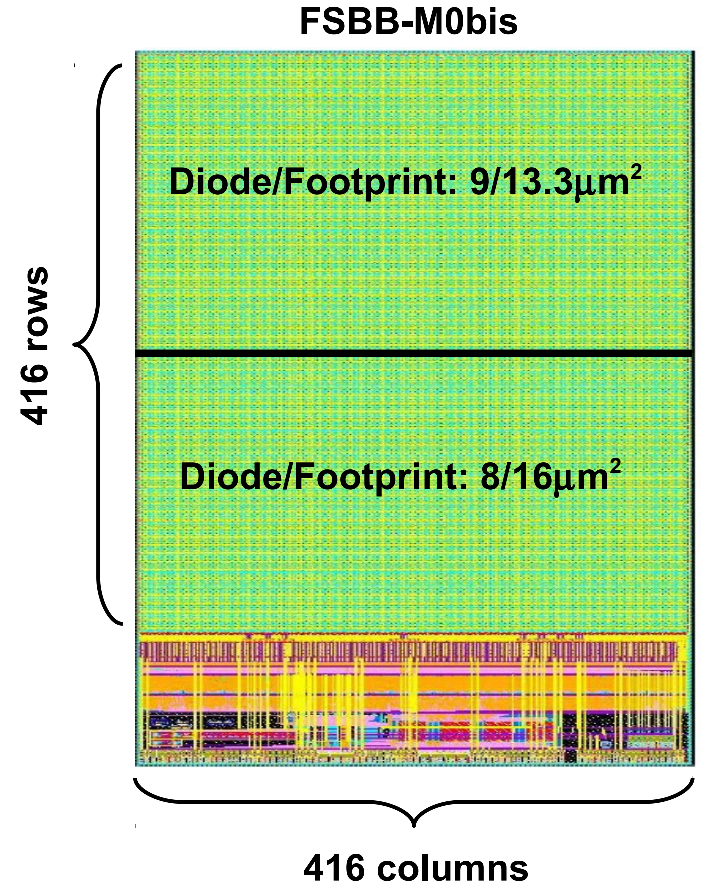




FSBB-M0bis main features

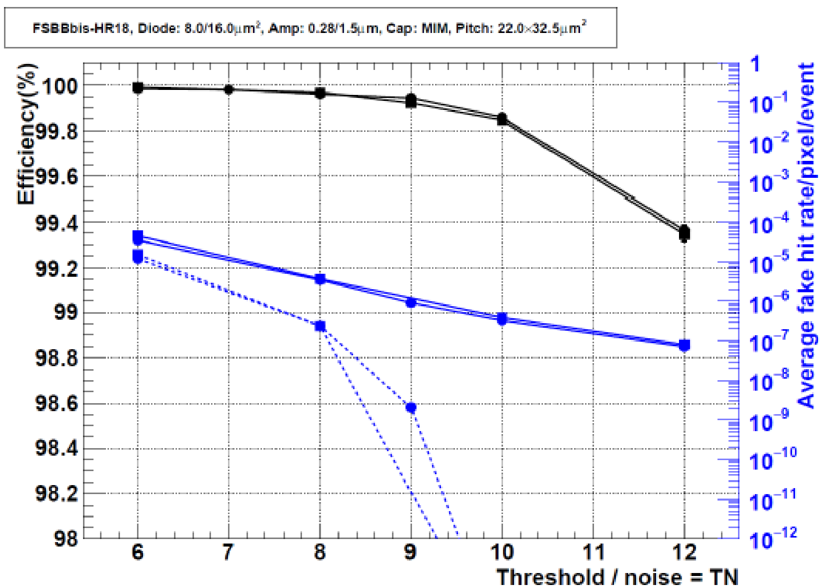
- TJsc-0.18 CIS process, HR (~1–2kΩcm) 18/25/30μm epitaxy, thinned to 50μm
- Staggered pixel: 22x32.5 μm^2 including pre-amplification and clamping with 6 metal layers (ML)
- 416x416 = 173k of col. x row of pixels ended by discriminator (8-cols with analogue output)
- Double-row readout at 160MHz clock frequency ⇒ 40μs integration time
- On-chip 3-stage sparsification: SUZE-02 (different from MISTRAL-0, SUZE-03)
- 4 Memories of 512x32 bits
- 2 output nodes at 320Mbits/s (used only one for TB)
- Integrated JTAG and regulators
- Sensitive area is 13.7 x 9.0 mm ~ 1.2cm^2

- **Improvements w.r.t FSBB-M0 ⇒ shortcomings solved**
  - Mitigation of cross coupling effects
    ⇒ now capable of operating full matrix
  - Bit transmission: bit inversion at discriminator output
- **Two sensing node variations in same chip**
  - (NMOS T_{input} Pre-Amp W/L = 1.5/0.28μm)
  - Diode/Footprint: 8/16 μm^2
  - Diode/Footprint: 9/13.3 μm^2

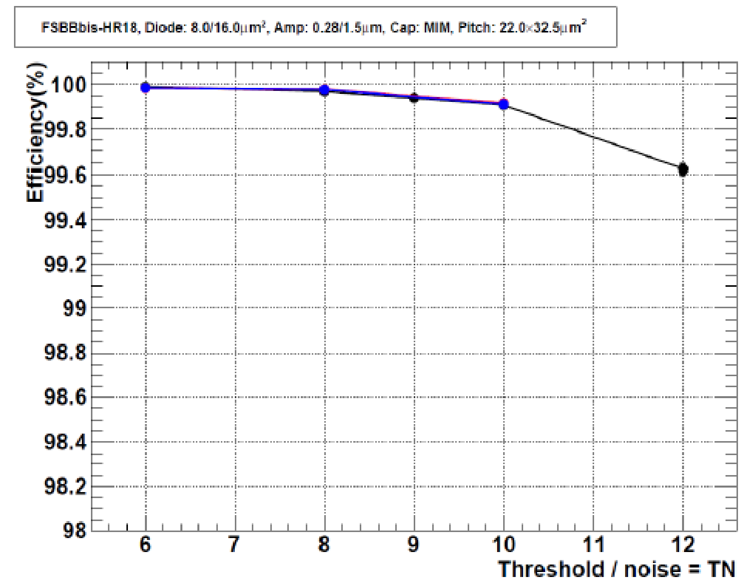


Main FSBB-M0 Detection Performances (2/3)

- **Study of detection efficiency stability :**
  - Difference between SPS (120 GeV pions) & DESY (4.5 GeV electrons)
  - Effect of occupancy : from $\sim$ 1 hit/frame to $\sim$ 25 hits/frame



SPS vs DESY



$\sim$ 1 to 20-30 hits/frame

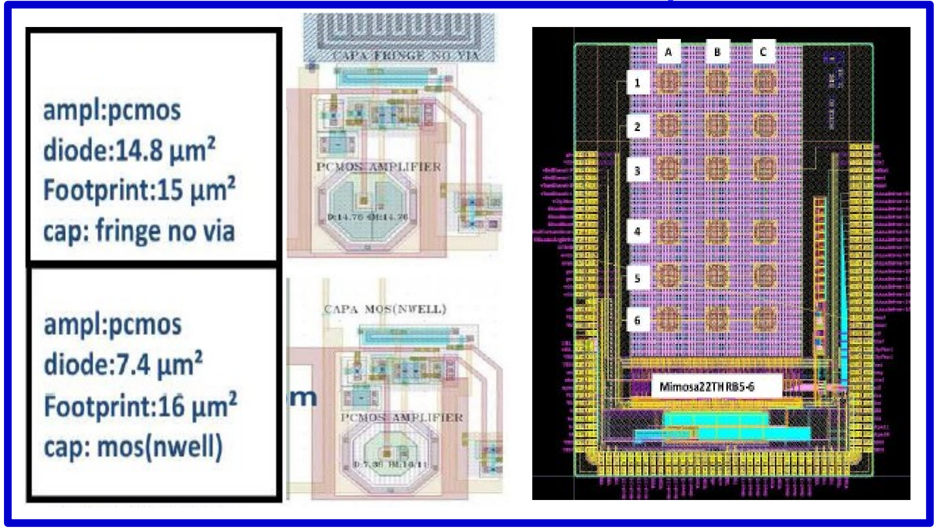
$\Rightarrow$ **No variation observed**

9

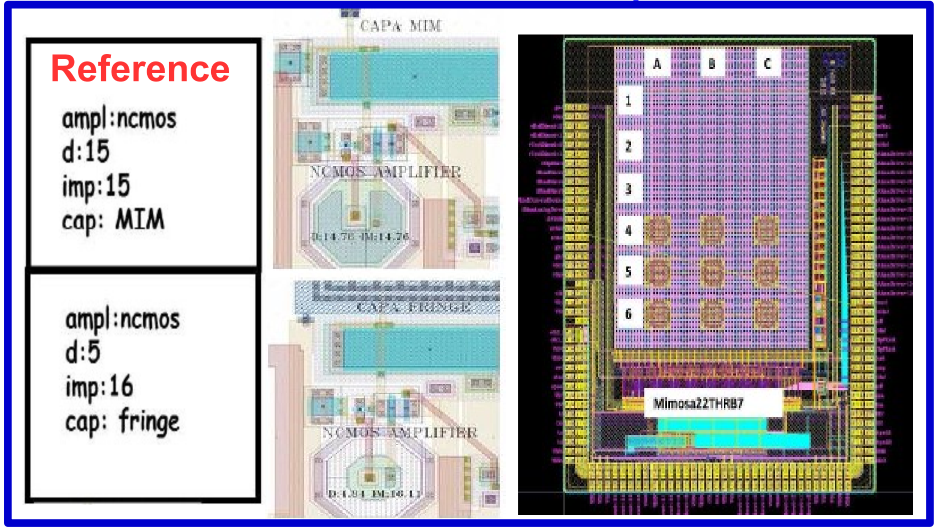
MIMOSA-22THRb6/7: characteristics

- **Design features**
  - 64x64 pixel array (staggered): 56 columns ended with discri. and 8 with analog output
  - Readout ≈ 5µs (100MHz clock)
  - Epitaxial layer: HR18

Mi22-THRB6: 36×62.5µm^2



Mi22-THRB7: 39×50.8µm^2



- **Purpose of the chip**
  - Validate pads over pixels
  - Validate in-pixel circuitry concentrated on ≈ 3ML ⇒ modified clamping capacitor
  - Validate large pixel performances w.r.t. TDR requirements on layers 3 – 6

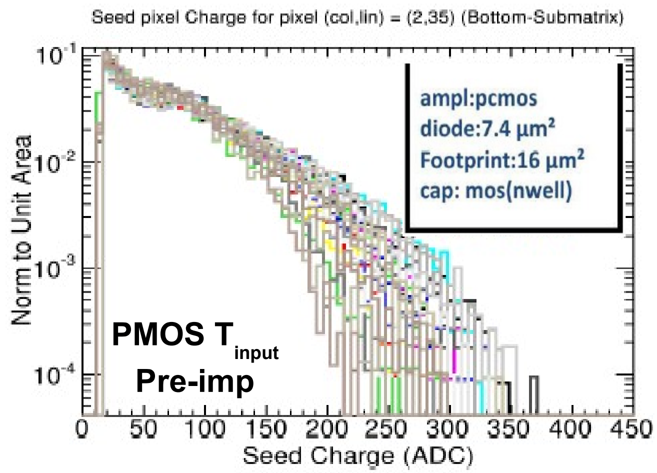
    ⇒ **MISTRAL-O**

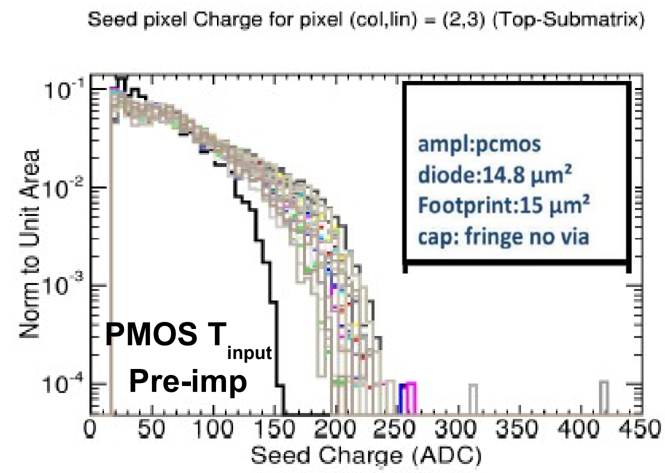
Reminder of lab results: Individual pixel response to ^{55}Fe X-rays

- **Mi22THRb7 has a gain quite uniform**
- **Mi22THRb6 shows gain dispersion among pixels** ⇒ were not sure about the effect on ε_{det}

- MIMOSA-22THRb6

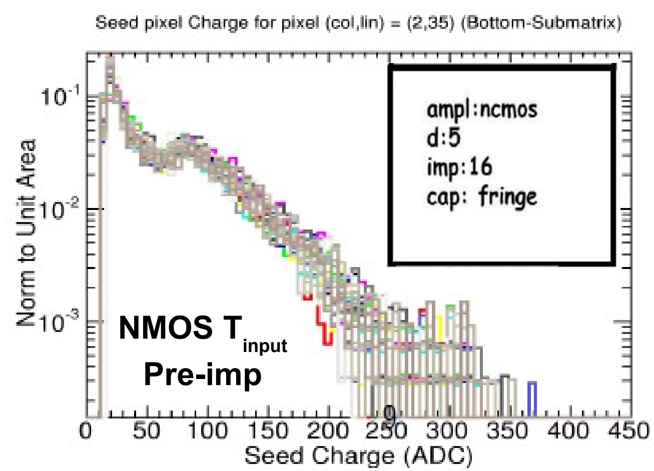
  analog outputs

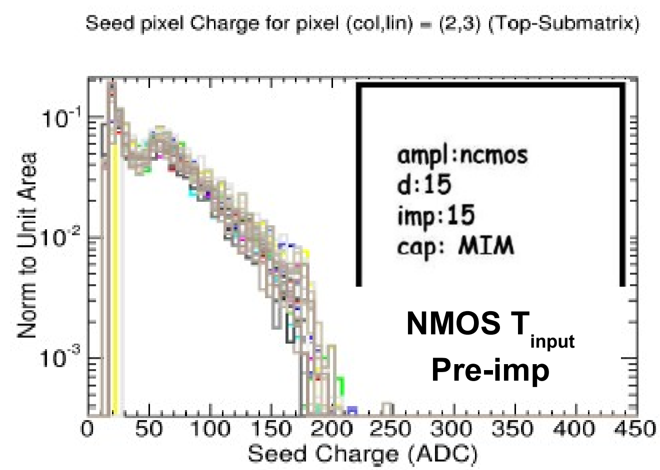




- MIMOSA-22THRb7

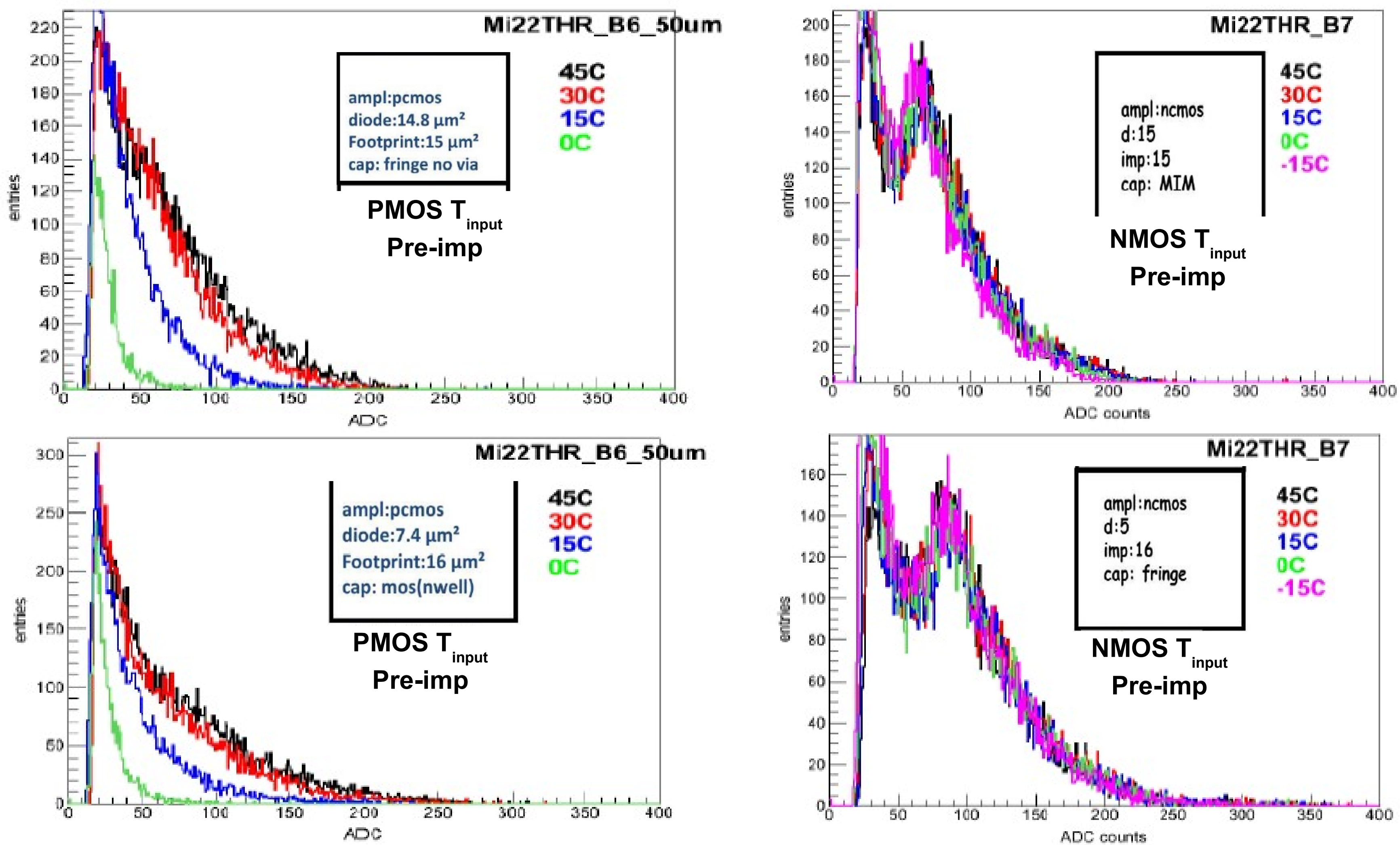
  analog outputs



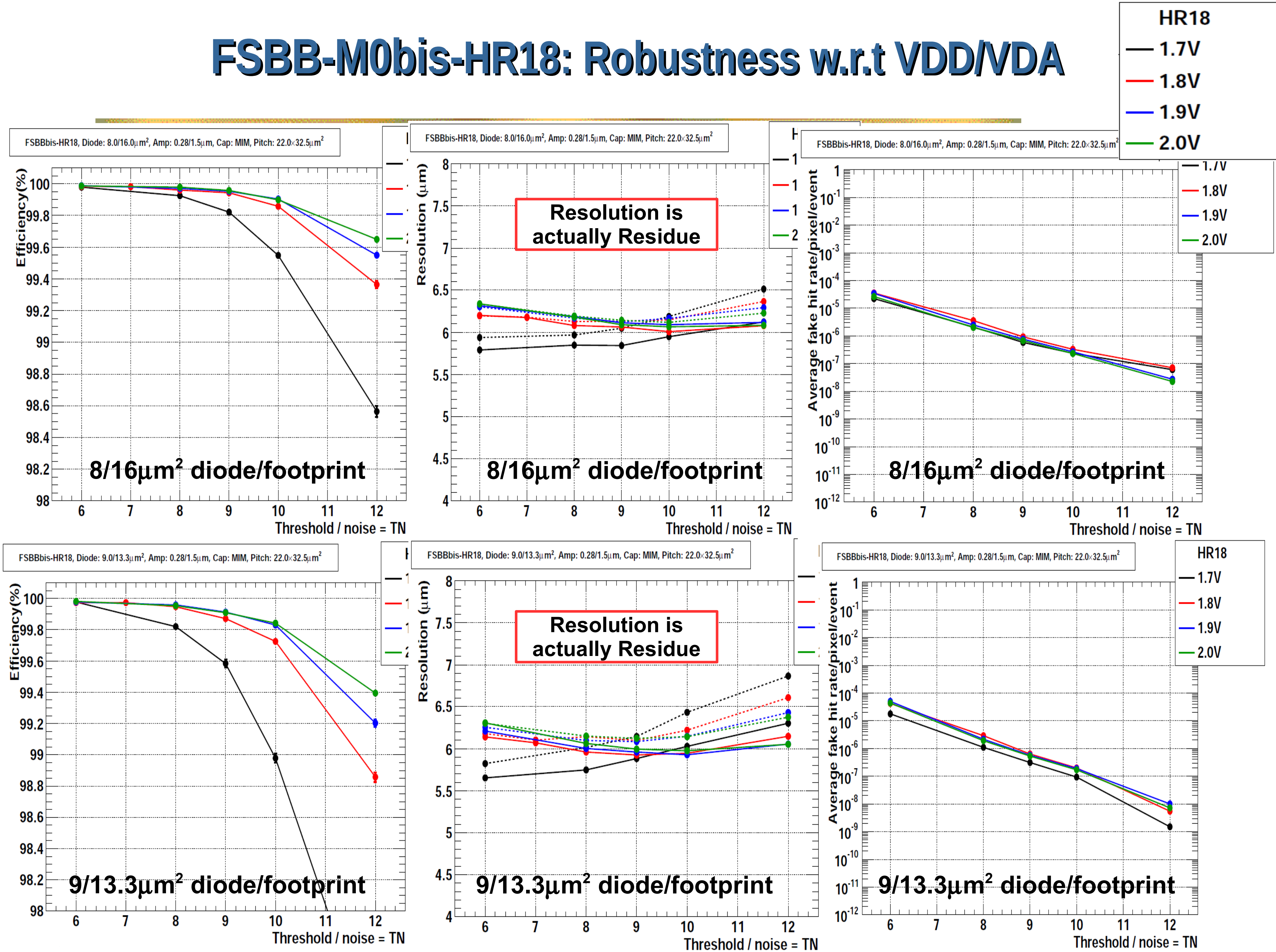


Reminder of lab results: Temp. dependence of pixels to ^{55}Fe X-rays

- **Mi22THRb7 has quite stable response vs T**
- **Mi22THRb6 shows a significant dependence with T: ↗T ⇒ ↗gain**



FSBB-M0bis-HR18: Robustness w.r.t VDD/VDA



Hot pixel masking effect on ε_{det} & σ_{sp}: Motivation

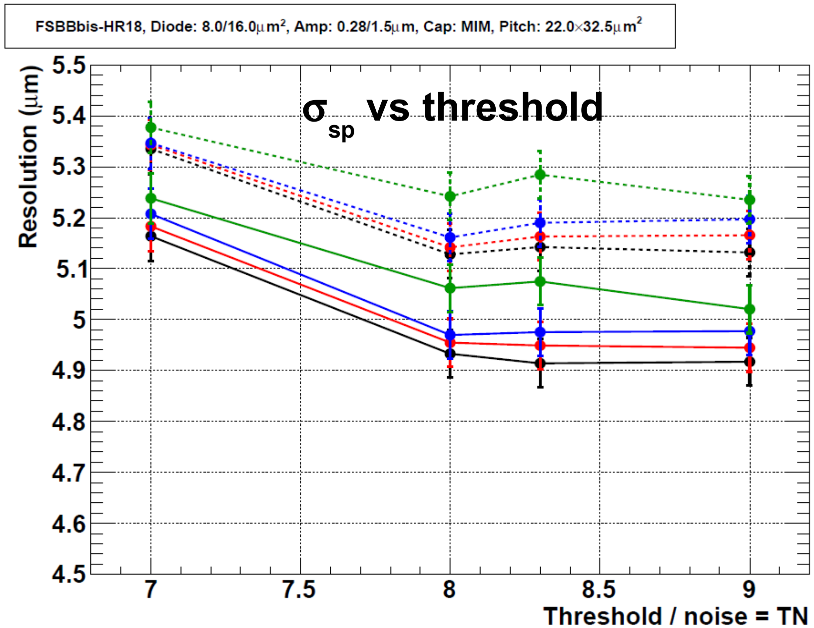
- **Reducing I_{pix}**
  - Increases ε_{det} ⇒ dramatical effect for highly irradiated sensors ☺
  - Increases fake rate ⇒ factor of 10 increase for highly irradiated sensors ☹
  - Masking procedure can be a good strategy for highly irradiated sensors
    ⇒ can reduce fake rate by ~1 – 2 orders of magnitude depending masking fraction

- **It is then important to study the effect of masking on ε_{det} & σ_{sp}**
  - Masking will cut away some single pixel clusters
  - ε_{det} relative reduction should be prop. to (masking fraction) x (fraction mult. = 1 clusters)
    - Should be a marginal effect due to sizeable pixel cluster multiplicity of FSBB
    - $\Delta\varepsilon_{det}$ vs (fraction mult. = 1 clusters) should be linearly related
  - σ_{sp} should get marginally degraded due to loss of hit position information of masked pixels

- **Tested the above hypothesis on different sensors and varied configurations**
  - Non-irradiated sensors @ nominal configuration
  - Highly irradiated sensor (1.6MRad + $10^{13} n_{eq}$(MeV)/cm^2) for I_{pix} = 30 & 50 (nominal) μA

Hot pixel masking effect on ε_{det} & σ_{sp}: Results (I)

Masking 0.00%
Masking 0.50%
Masking 1.00%
Masking 2.00%



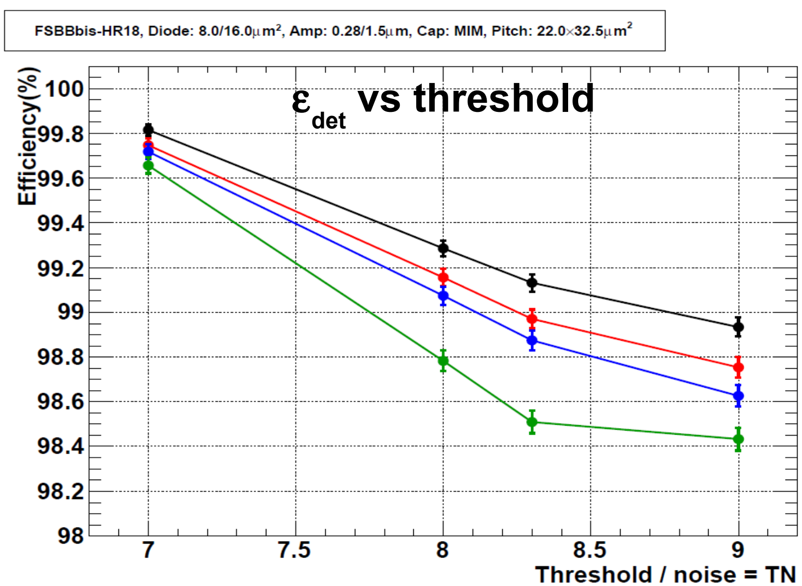
Example:

Irradiated sensor 1.6MRad + $10^{13} n_{eq}/cm^2$

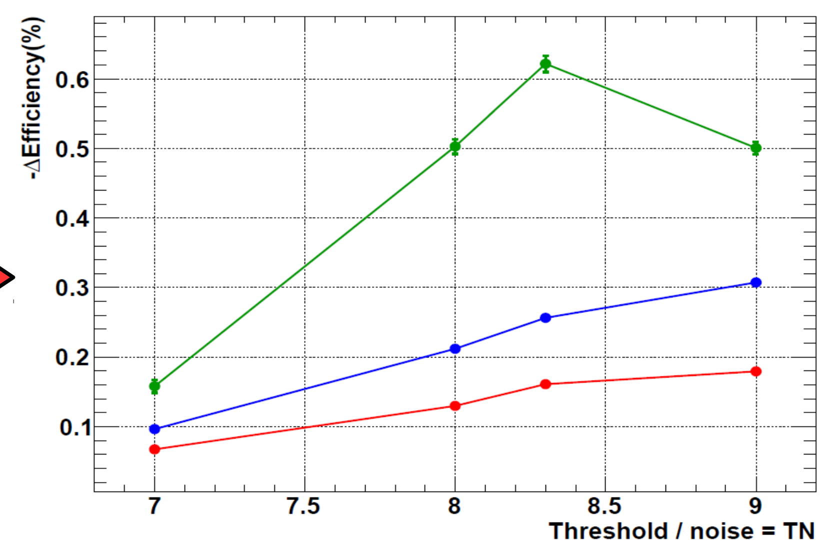
Diode/Footprint: 8/16μm^2

- Marginal increase of σ_{sp}
- Small reduction of ε_{det}

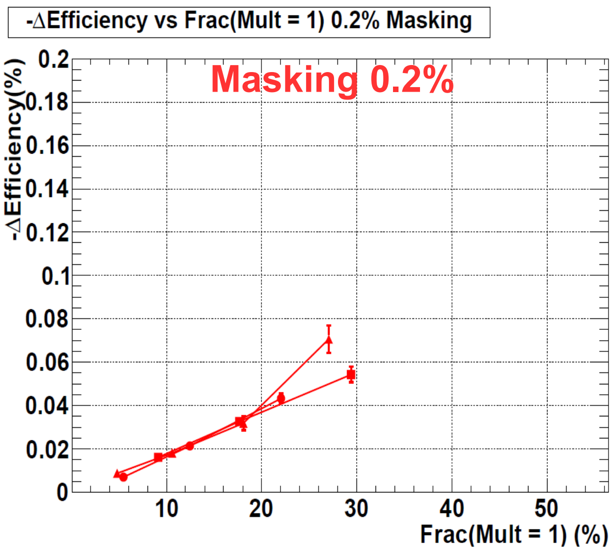
$\Rightarrow$ quite smaller than masking fraction

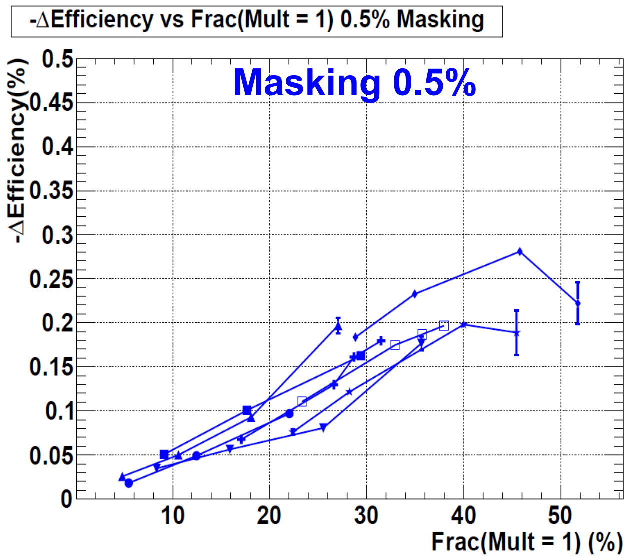


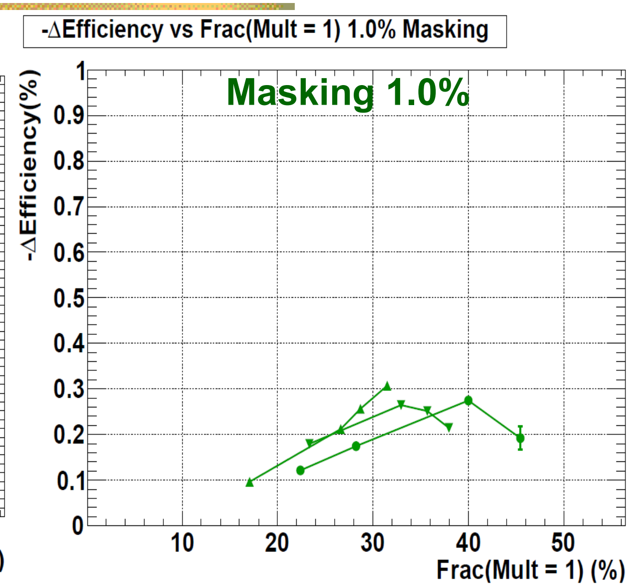
$-\Delta\varepsilon_{det}$ (w.r.t 0% masking) vs threshold

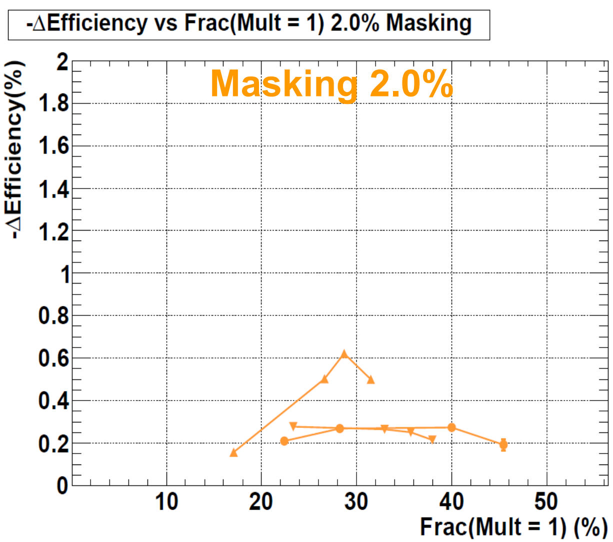


Hot pixel masking effect on ε_{det} & σ_{sp}: Results (II)







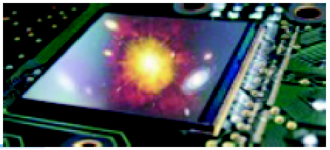


$-\Delta\varepsilon_{det}$ vs fraction mult = 1 clusters (Frac(Mult = 1))

- Different markers in a plot correspond to the different sensors and configurations studied
- $-\Delta\varepsilon_{det}$ values quite smaller than masking fraction in full Frac(Mult=1) (threshold)
- Nearly linear correlation between $-\Delta\varepsilon_{det}$ & Frac(Mult=1)

$\Rightarrow$ Useful to predict efficiency reduction for a given masking fraction and threshold

Motivation for depleted CPS



- High energy physics trend
  - Tolerate high non-ionizing part. Fluences 10^{15} n_{eq}/cm^2 (tracker / ~~vertex~~)
  - Integration time ≪ µs
- X-rays detection
  - Require thickness (Beer-Lambert attenuation law)
  - Require equivalent collection properties all over epi-layer

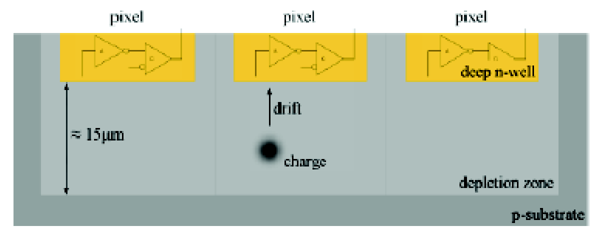
- Fully depleting the sensitive layer is a key
  - However situation different / sensors for hybrid-systems (CERN-RD50)
    - ➡ Same substrate embed sensitive and first amplification layer

- Open questions
  - Which structure to enforce depletion?
    - Depth & uniformity on chip area
  - impact on in-pixel treatment µ-circuits?
    - Noise, transistor behavior

Way 1: High Voltage

- Experiments
  - ATLAS, μ2e, CLIC
  - Groups in Bonn, CERN, Genève, Heidelberg, Karlsruhe, Marseille…
  - new collab. ➣ CERN-RD53
- Concept
  - Low resistivity (10-20 Ω.cm)
    ➡ High Voltage applied few 10s V
  - HV-compliant CMOS technologies

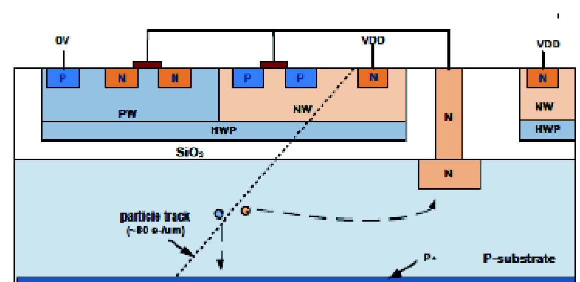
- HV-CMOS
  - Deleted depth demonstrated
    5 to 15 μm with 60-70V
  - Fast amplification ~ 1 μs
  - Only 30% signal loss after 10^{15} n_{eq}/cm^2



S.Feigl et al., PoS (TIPP2014) 280

! Prototypes area 10 mm²

- HV-SOI
  - Depleted depth demonstrated
    40-50 μm with 150-200 V
  - Hint of tolerance beyond 10^{14} n_{eq}/cm^2



T.Hemperek et al., arXiv:1412.3973

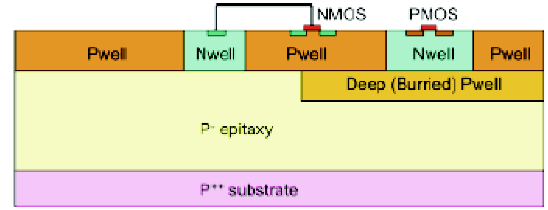
Way 2: High Resistivity

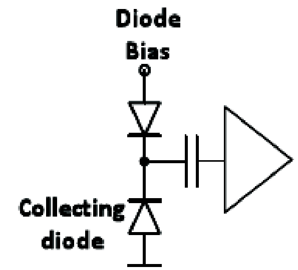
- Experiments
  - ALICE, CBM
  - soft X-rays detection
  - Groups in Bonn, CERN, RAL, Strasbourg
- Concept
  - High Resistivity thin epi-layer
    ➡ moderate voltage ≲ 10 V

➡ See next slides for IPHC developments

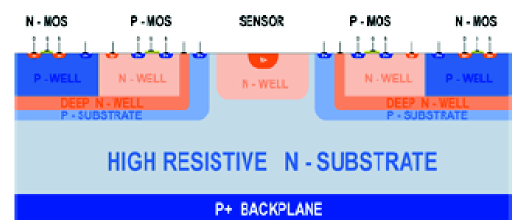
Depleted-CPS prototypes

- 2 Technologies explored
- Tower Jazz 0.18 µm ➛ Pegasus-1/2
  - Various sensitive layers
    - epi with >1 kΩ.cm, 18, 30, 40 µm thick
    - Czochralski substrate-thick
  - Main architecture tested
    - Analogue readout with 10 µs integration time
    - Collection node AC-coupled to amplificator
  - Small matrix: 32 columns x 56 rows
  - Pixel size 25x25 µm^2





- EPC-ESPROSS 0.15 µm ➛ MIMOSA-33
  - high resistivity 50 µm thinned + passivated substrate
  - Main architecture tested
    - Analogue read-out with 11 µs integration time
    - Back-side biasing through IP structure
  - Small matrix: 8 columns x 44 rows
  - Pixel size 25x25 µm^2



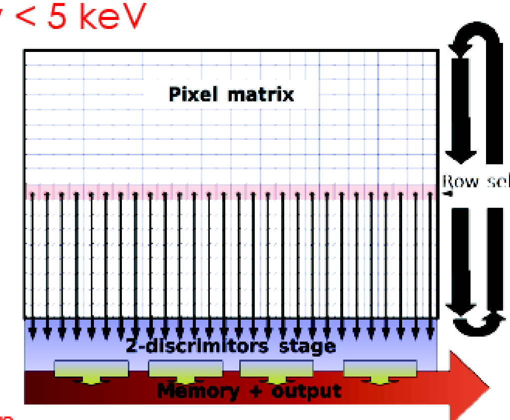
M. Havranek et al., JINST 10 (2015) 02, P02013

Ready for back-side illumination !

Ongoing prototypes design

- Submission to Tower-Jazz 0.18 μm technology (June 2015)

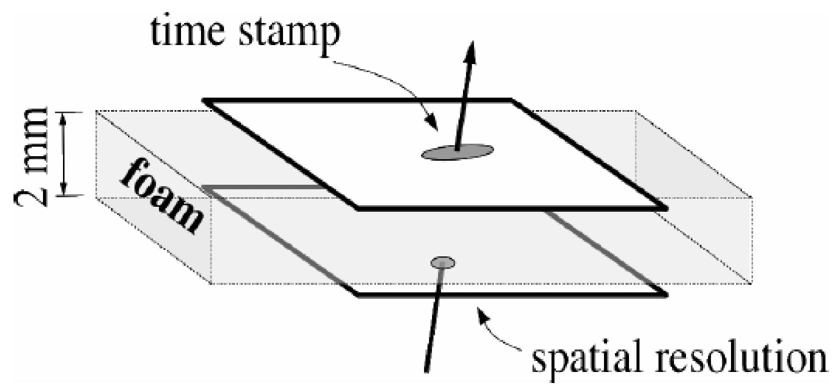
- MIMOSA - 22 SX
  - Forerunner of sensors dedicated to X-rays with energy < 5 keV
    - Pixel pitch ≲ 25x25 μm² and ≈10⁴ photons/pixel/sec
  - Developed with the detector group of SOLEIL
  - "Not so small" matrix: 5.6x 4.4 mm²
  - combine :
    - AC coupled collection diode from PEGASUS
    - read-out architecture developed for ALICE
  - Binary output:
    - From 2 discriminators/column → energy window selection
    - Photons detected individually → counting & spatial resolution



- Small analogue prototype
  - Faster amplification → target 10^6 photons/pixel/sec
  - Mitigation of noise

ILD - VXD Concept Addressed

- **Two types of CMOS Pixel Sensors :**
  - **Inner layers :** Priority to read-out speed & spatial resolution
  - **Outer layers :** Priority to power consumption and good resolution



- **Inner layers : $\sim$ 300 cm^2**
  - L1 : small pixels with end-of-column binary charge encoding $\mapsto \lesssim 3\ \mu m$
    - $20\times14\ \mu m^2$ with 2-row read-out : $\lesssim 40\ \mu s$
    - $17\times17\ \mu m^2$ with 1-row read-out : $60\ \mu s$
      - $\hookrightarrow$ 2-row read-out : $30\ \mu s$ (tbc)
  - L2 : elongated pixels with in-pixel binary charge encoding $\mapsto \sim 5\ \mu m$
    - $22\times33\ \mu m^2$ with 2-row read-out : $\sim 8\ \mu s$
    - $22\times33\ \mu m^2$ with 4-row (tbc) read-out : $\sim 4\ \mu s$
- **Outer layers : $\sim$ 3000 cm^2**
  - L3-6 : large pixels with end-of-col 3-4 bit ADCs
    - $35\times35\ \mu m^2$ pixels : $\lesssim 4\ \mu m$ & $120\ \mu s$
    - $25\times50\ \mu m^2$ pixels : $\lesssim 4\ \mu m$ & $80\ \mu s$

Processes Suited to the R&D

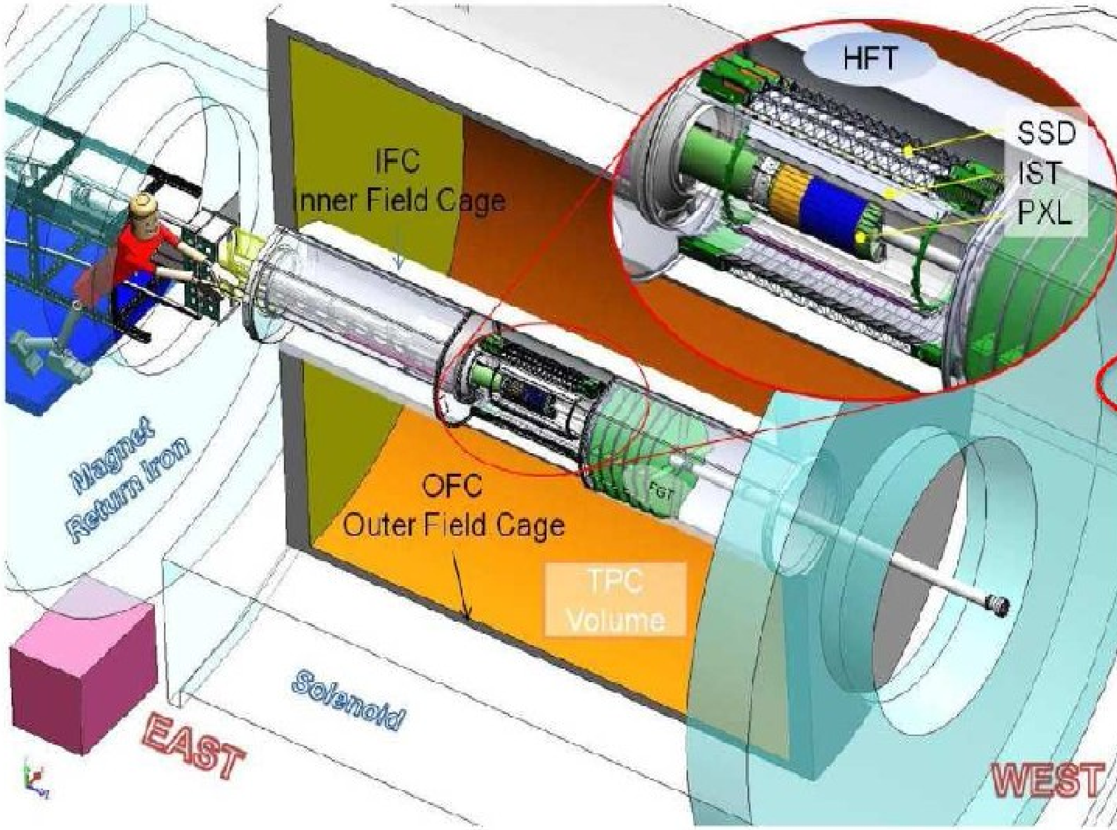
- SPECIFIC ASPECTS OF TOWER 0.18 μm CIS PROCESS : **established contact**
  - access to various starting materials (incl. in MPW)
  - designing details well known by the designers and testing crews
- COMPARISON TO L-FOUNDRY (INFO. TBC) : **used by HL-LHC R&D groups**

Process	Feature Size	Supply Voltage	Number of ML	Type	Comments
Tower-SC	180 nm	1.8 V (3.3 V)	6	4-well	
L-Foundry	150 nm	1.8 V (3.3 V)	8	4-well	110 nm : 1.2 V

Process	MPW runs			MLM runs	
	min. area	cost	duration	area	cost
Tower-SC	5x5 mm^2	37,500 USD	$\gtrsim$ 4.5 months	none	
L-Foundry	???	???	???	11x11 mm^2	60-80 kE

Process	Starting Material				Comments
	thickness	resistivity	source	availability	
Tower-SC	18-40μm or more	$\sim$ 1 - 10 k$\Omega \cdot cm$	internal & external	MPW, ER	
L-Foundry	??	High-Res	internal only ?	MLM, ER	

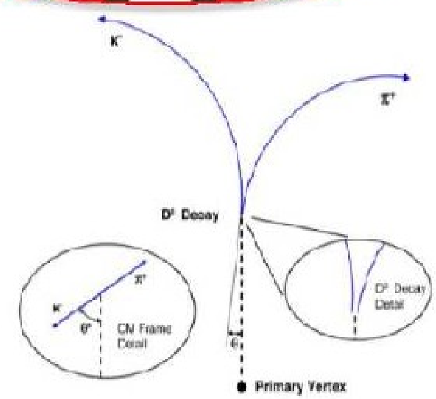
PXL in STAR Inner Detector Upgrades



TPC – Time Projection Chamber (main tracking detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.8, 8 cm



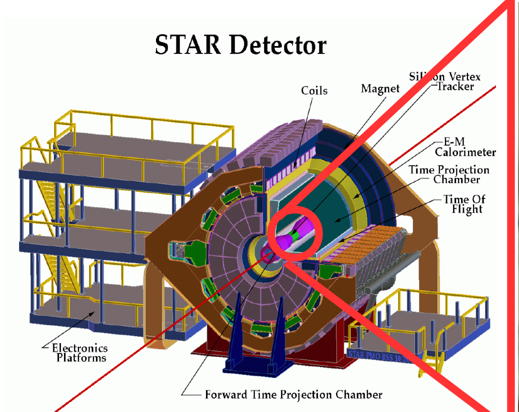
Direct topological reconstruction of Charm – displaced verticies

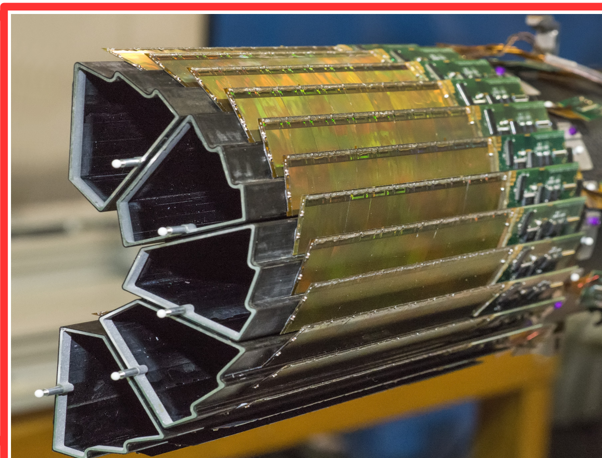
We track inward from the TPC with graded resolution:

L. Greiner (CPIX-14)

CPS State-of-the-Art in operation: STAR-PXL detector

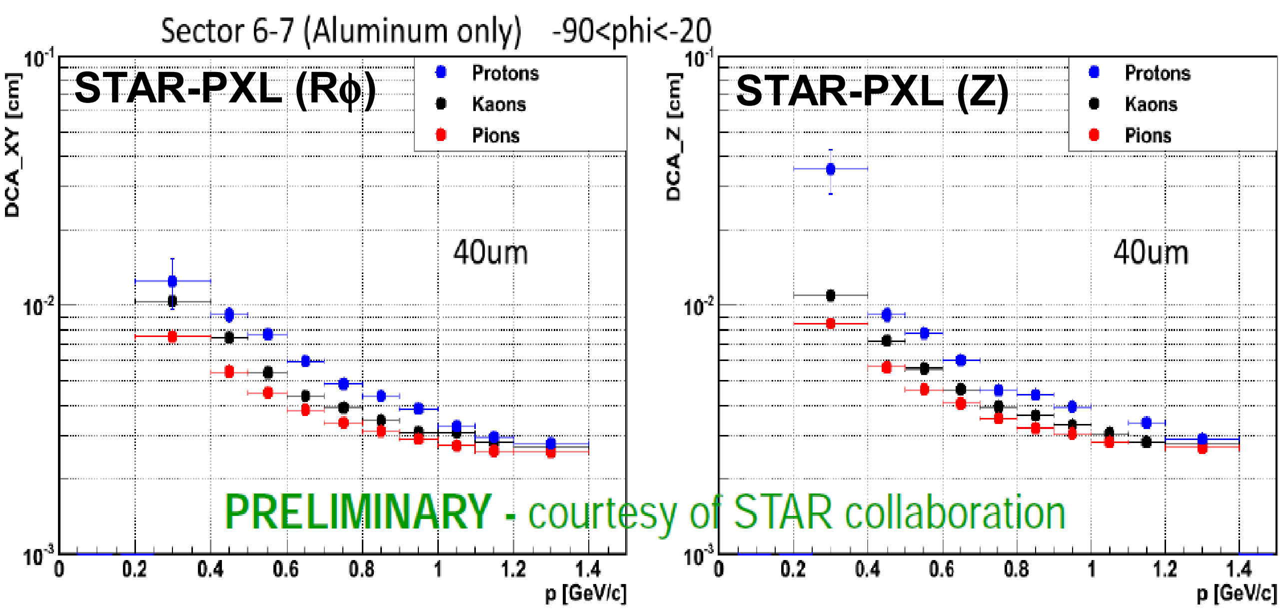
STAR-PXL @ RHIC: 1st CPS @ collider experiment !





STAR-PXL HALF-BARREL

- 2 layers @ r = 2.8,8 cm
- 20 ladders (10 sensors) (0.37% X_0)
  - 200 sensors ⇒ 180x10^6 pixels
- Air flow cooling: T < 35°C

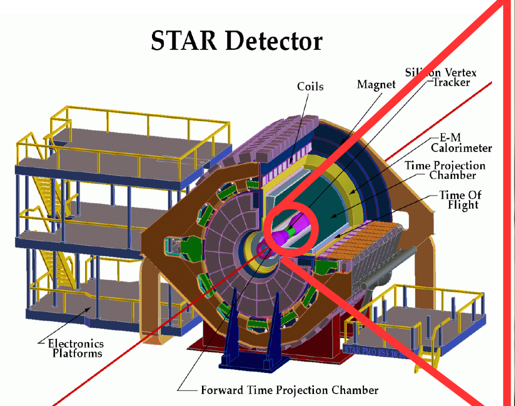


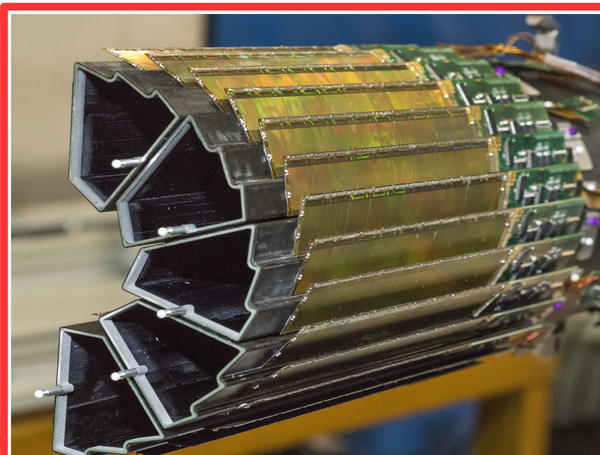
Several Physics-runs

- **1st run Mar-Jun 2014**
- **2nd run Jan-Jun 2015**
- **Measured $\sigma_{ip}(p_T)$ matching requirements (~40 μm @ 600 MeV/c for $\pi^{\pm}/K^{\pm}$)**
- **Getting prepared for 3rd run (Jan. 2016)**

CPS State-of-the-Art in operation: STAR-PXL detector

STAR-PXL @ RHIC: 1st CPS @ a collider experiment !

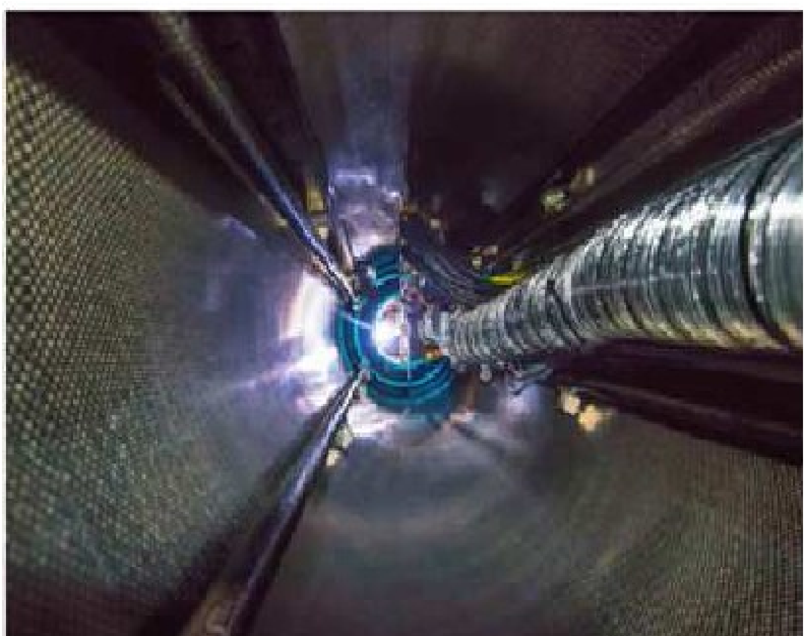




STAR-PXL HALF-BARREL

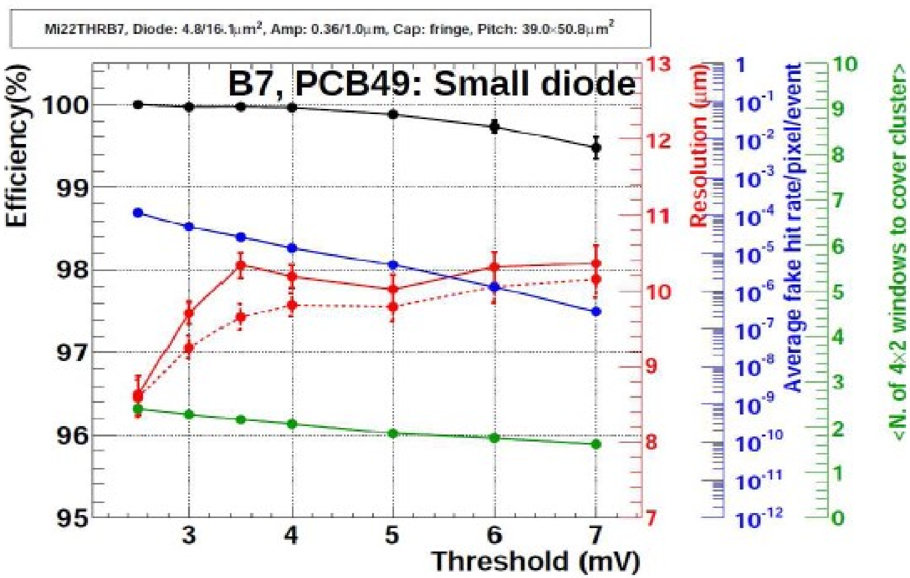
- 2 layers @ r = 2.8,8 cm
- 20 ladders (10 sensors) (0.37% X_0)

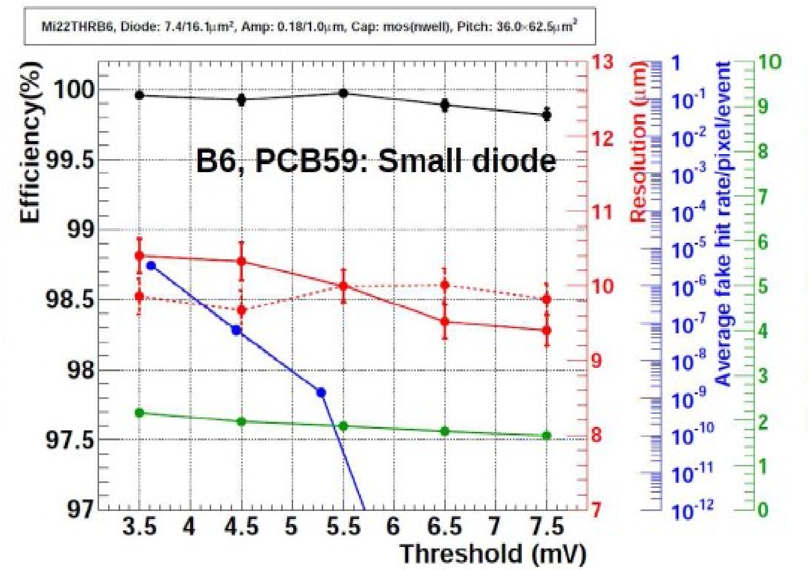
  ⇒ 180M pixels
- Air flow cooling: T < 35°C

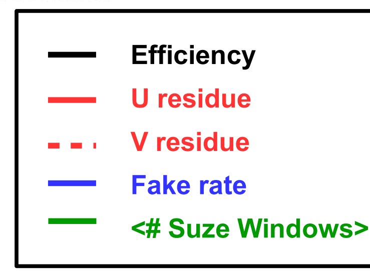


Main MIMOSA-22THRb detection performances (1/2)

Pixel type	Pixel dim.	Diode/Footprint	Pre-Amp T.	Clamping capa.	Integ. time
MIMOSA-22THRb7	39 μm x 50.8 μm	5/16 μm^2	N-MOS	MOS (N-well)	5 μs
MIMOSA-22THRb6	36 μm x 62.5 μm	7/16 μm^2	P-MOS	fringe (metal layers)	5 μs



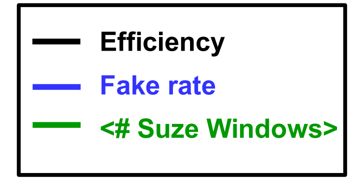




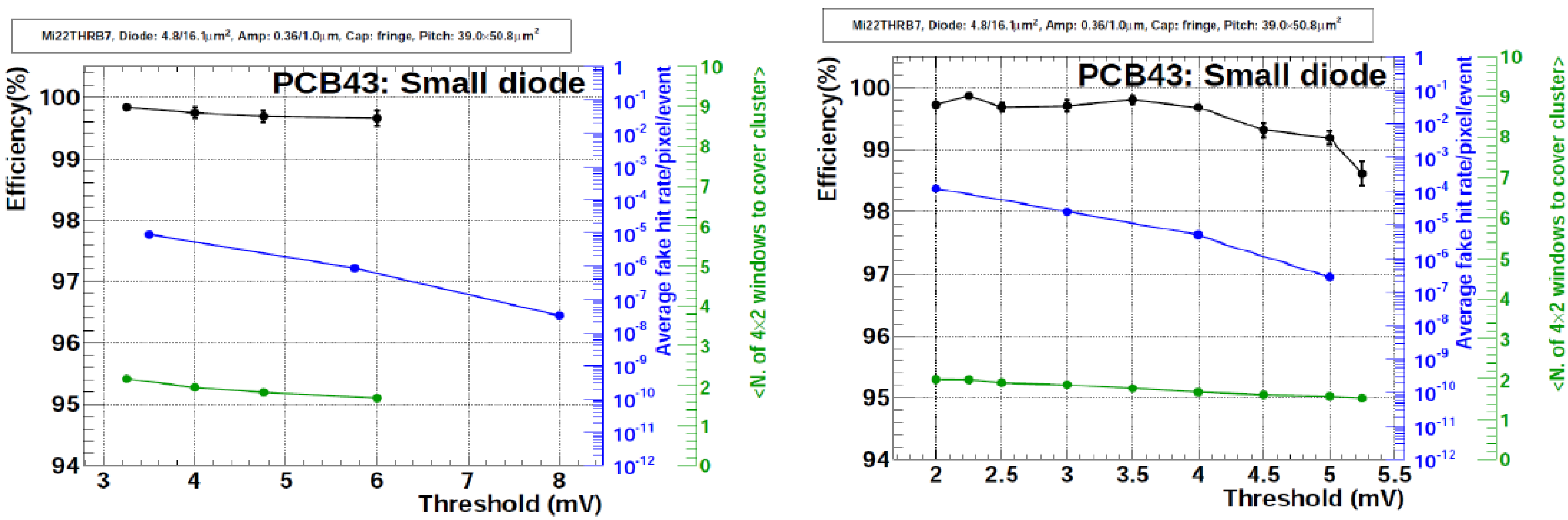
- **Excellent detection performances for both chip variations**
  - ε_{det} > 99% & σ_{sp} ~ 10 µm (as expected)
- **P-MOS vs N-MOS Pre-Amply input transistor**
  - **P-MOS:** less RTS noise, higher gain and sensing node voltage
  - **N-MOS:** better pixel response uniformity, less T-dependency and maturity (STAR-PXL)

Main MIMOSA-22THRb detection performances (2/2)

- **Study of rad. tolerance @ T $\gtrsim$ 30 °C:** loads relevant to ALICE-ITS outer layers
  - **Load:** up to 150 kRad ⊕ $1.5\times10^{12} n_{eq}/cm^2$



MIMOSA-22THRb7 (N-MOS Pre-Amp input transistor)



50 kRad ⊕ 5×10^{11} n_{eq}/cm^2 — 150 kRad ⊕ 1.5×10^{12} n_{eq}/cm^2

- **Good detection performances after irradiation**
- **Validation of large pixel design for the outer layers of the ALICE-ITS!**