ATLAS R&D ON ACTIVE CMOS SENSOR (HVCMOS)

FCPPL 2016 — Strasbourg, FRANCE

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1 April 2016

On behalf of the Silicon detector FCPPL and ATLAS project

CPPM / Atlas Chinese Cluster Collaboration

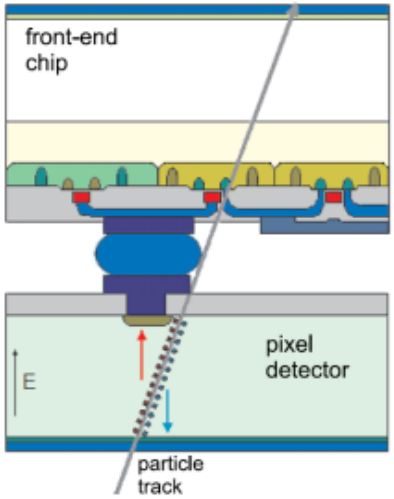
- CPPM / ACC collaboration for design and test of Front-End pixel electronics for ATLAS phase II upgrade.

- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG and Pr. Marlon BARBERO & Dr. Alexander ROZANOV, derived from ATLAS CPPM / ACC project (Pr. Shan JIN / Dr. Emmanuel MONNIER).

- Co-PhD Jian Liu (SDU – Pr. Meng WANG / CPPM Pr. Marlon BARBERO & Dr. Alexander ROZANOV).

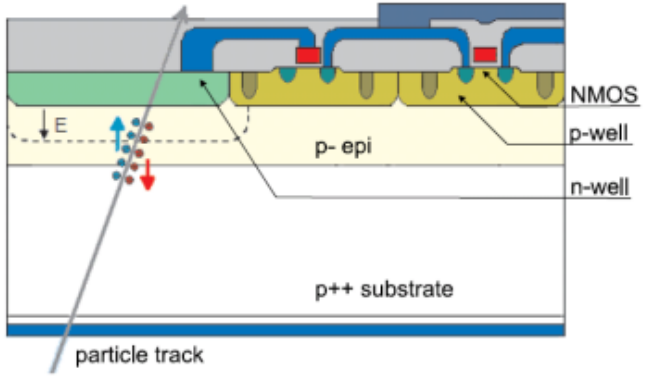
- The last development topics involve:
  - The tests and simulation in LFOUNDRY HV CMOS technology. Jian Liu (SDU /CPPM).

Hybrid Pixel Detectors



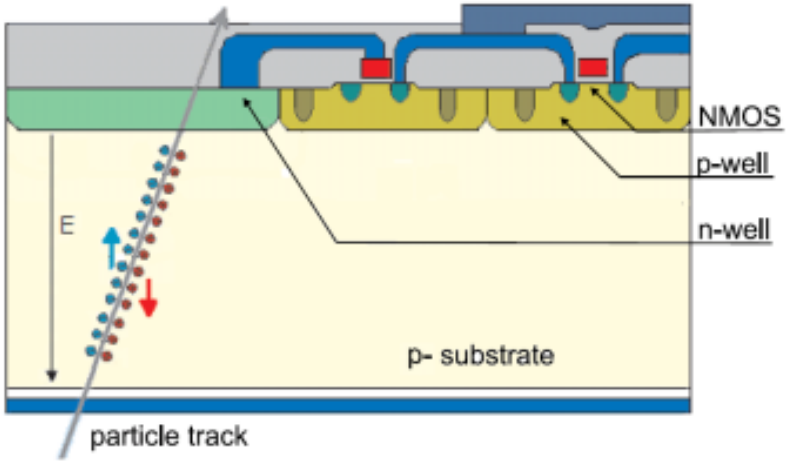
Various Sensor Planar : Si, 3D, diamond ..
Mixed signal on ROC (FE-I3 ; FE-I4 ; etc)

Monolithic Pixels



MAPS using CMOS with Q-collection in Epi layer (largely by diffusion)

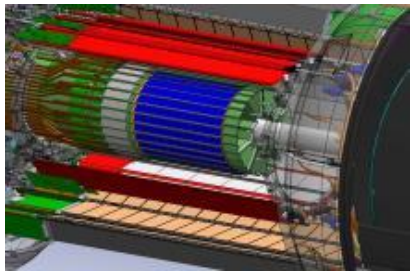
Depleted Monolithic Pixels



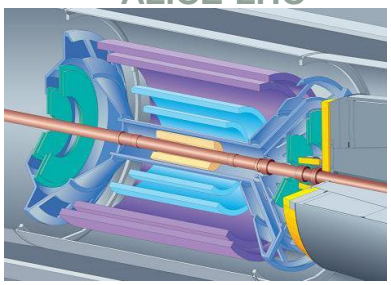
Depleted MAPS using HR substrate or/and HV process to create depletion region $d \approx \sqrt{\rho . V}$

CMOS Sensors for HEP

STAR

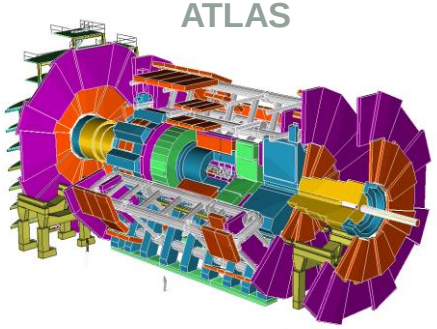


ALICE-LHC



ILC

ATLAS



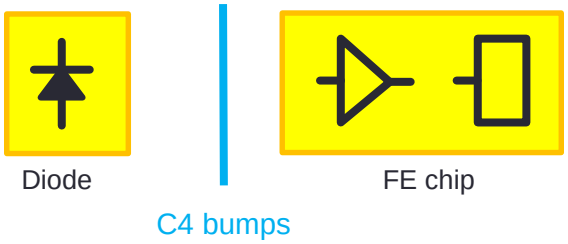
Requirements for inner pixel layers

	STAR	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	**25**	**25**
Particle Rate [kHz/mm^2]	100	10	250	1000	10000
Fluence [n_{eq}/cm^2]	> 10^{12}	> 10^{13}	10^{12}	**2×10^{15}**	**2×10^{16} - 2×10^{15}**
Ion. Dose [Mrad]	> 0.3	0.7	0.4	**80**	**>500 - 100**

Monolithic CMOS ?

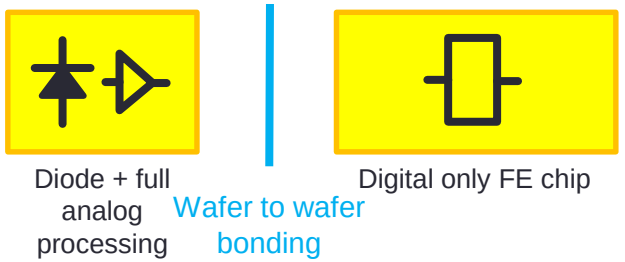
Possible scenarios for Active CMOS Sensors

- Passive CMOS Sensor + R/O chip
  - HR- or HV-CMOS sensor
  - Dedicated **FE chip**
  - Low cost **C4 bumping** and flip-chip

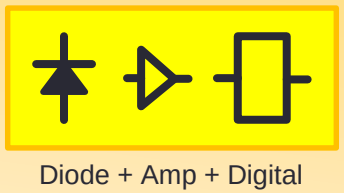


- Hybrid Pixels with “smart” diodes:
  - HR- or **HV-CMOS** as a sensor (8”)
  - Standard FE chip
  - CCPD (HVCMOS) on FE-I4

- CMOS Active Sensor + Digital R/O chip
  - HR- or HV-CMOS sensor + CSA (+Discriminator)
  - Dedicated **“digital only” FE chip**

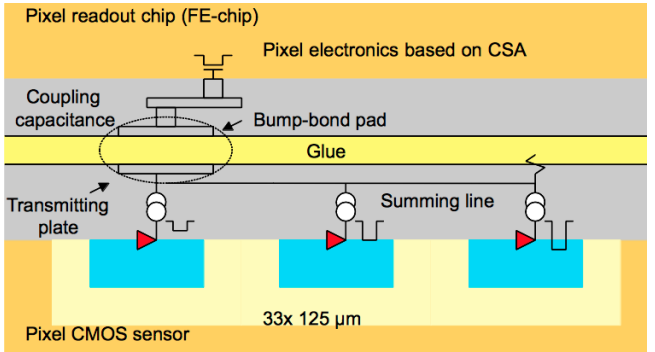


- Depleted Monolithic Active Pixel Sensor
  HR- material (charge collection by drift) ➔ Fully depleted MAPS (DMAPS)



Why Active CMOS Sensor for HEP ?

- Commercial process in large 8 or 12 inch wafers and potentially much cheaper than customer HEP sensors.
- Potentially much cheaper bonding processes available.
  (capacitive coupling gluing, oxide/Cu-Cu bonding, etc)
- Smaller pitch due to the separation between CMOS sensor/analog tier and digital tier: sub-pixels in CMOS tier.
- Thin sensor (15-100 µm) reduce clusters at large η.
  (improve cluster size, two tracks resolution, sensor radiation hardness).
- For initial prototypes, FE-I4 digital tier is available,
  for final on FE-RD53 will be suitable.
- Low occupancy layers (outer pixel, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas.

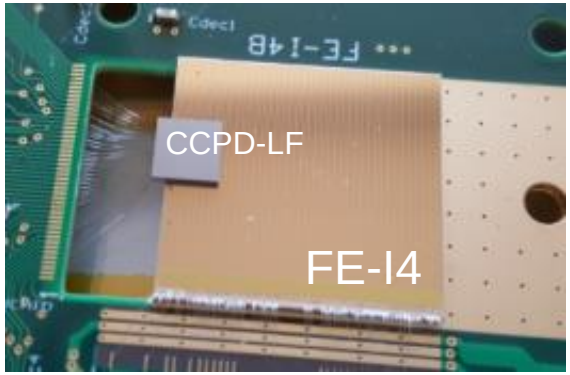


HVCMOS Demonstrator Working Group

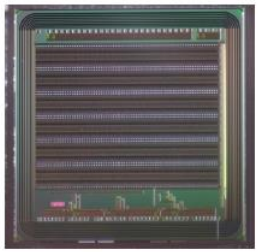
- R&D started by Heidelberg-Berkley-Bonn-CERN-Geneva-Marseille since 2012.
- From June 2014 in the framework of ITK Pixel Module under chair of Norbert Wermes (Bonn) with many institutes : Karlsruhe-Berkley-Bonn-CERN-Geneva-Marseille-Gottingen-Prague-IRFU-Glasgow-Oxford-Liverpool-INFN-Genova-Milan-SLAC-UCSC-…….
- Addressed the development of Demonstrator Pixel module at end of 2015.
- Goal of preparing CMOS pixel option in the ITK Pixel TDR at end of 2017.
- Two main technologies are explored for creating depletion region: HV (10-20 ohms.cm substrate and 30-90 V applied) or HR (0.1-3.0 KOhms. cm substrate) or both

CCPD-LF 150 nm prototype in 2015

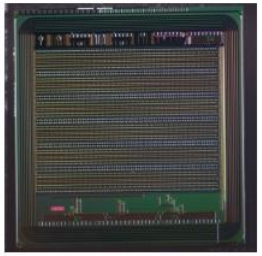
- Large fill factor for radiation hardness and charge collection
- Full CMOS , isolation via deep p-well (PSUB), wafer 2k Ohms.cm
- 24x114 pixels of 33x125 um
- 3 CCPD pixels connected to one FE-I4 pixel
- 5 thinned wafers and backside implant processing

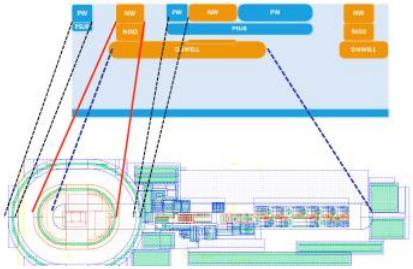


- CCPD_LF ver. A
  - CMOS inside collection electrode
  - Test structures: NMOS and PMOS transistors
- CCPD_LF ver. B
  - Smaller collection electrode
  - Test structure: diodes

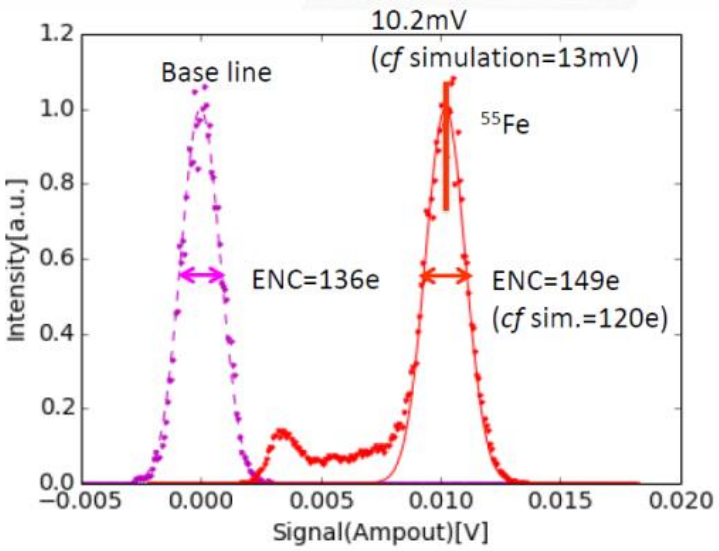


Design: Bonn, CPPM, Heidelberg



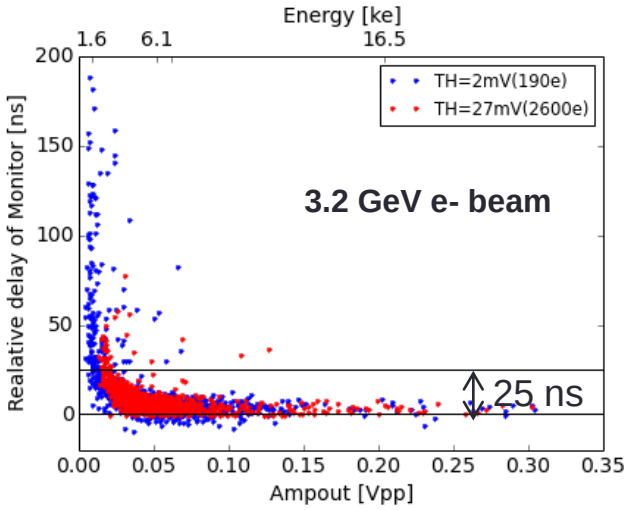


CCPD_LF : 1st results

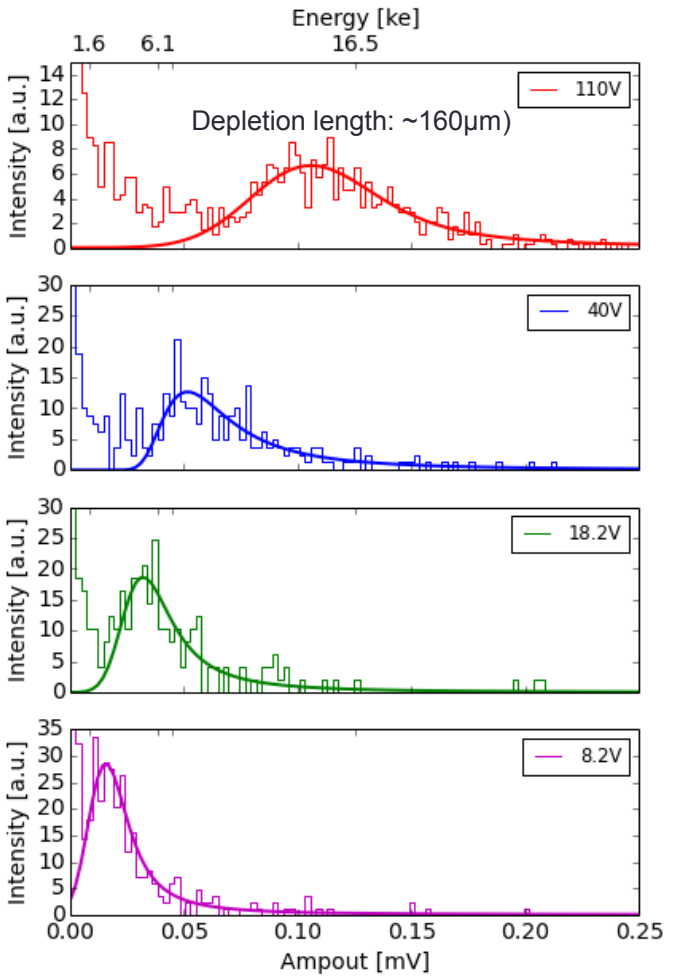


Spectrum of 55Fe (Bias=-101.8V)

Time Walk



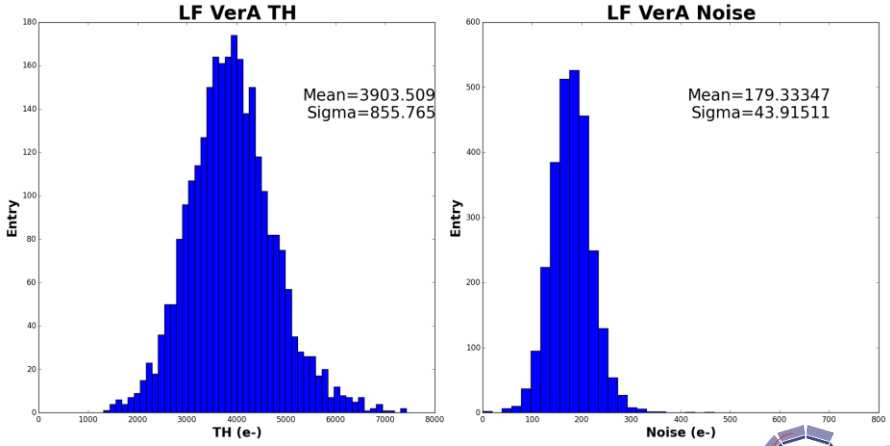
3.2 GeV spectrum



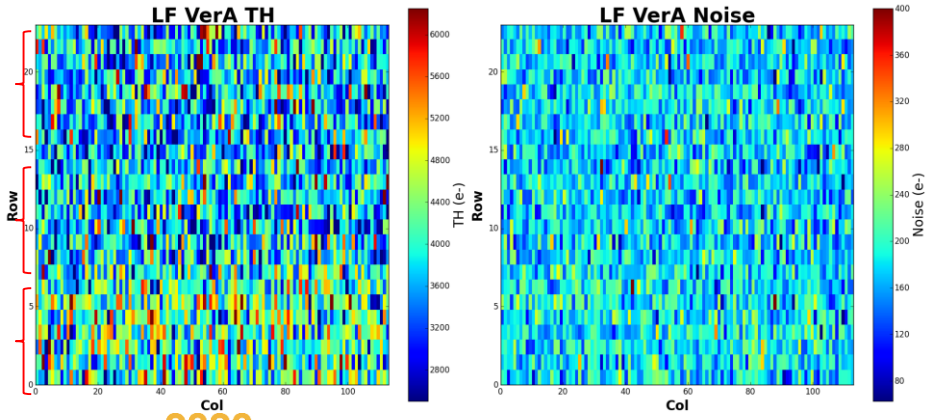
T. Hirono et al.

CCPD-LF irradiated to 100Mrads protons beam

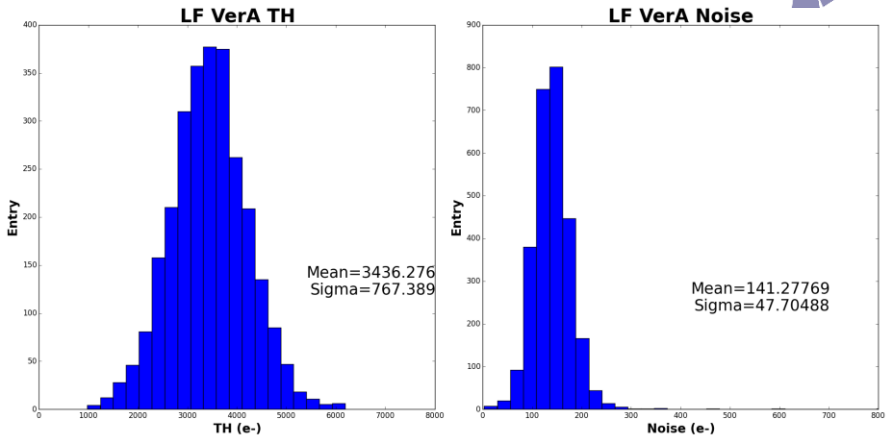
5 MRads



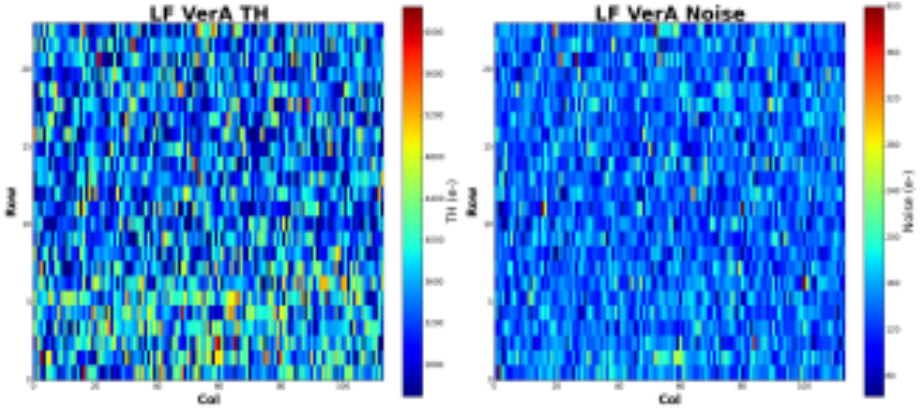
5 MRads



100 MRads



100 MRads

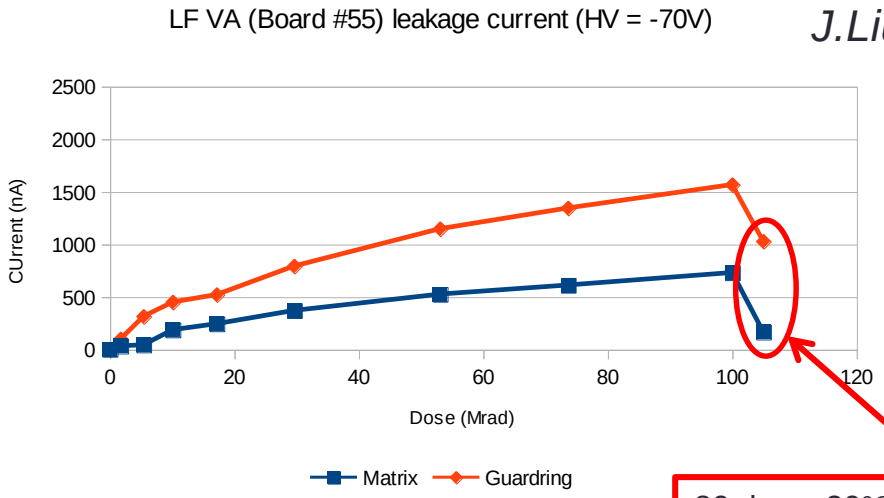


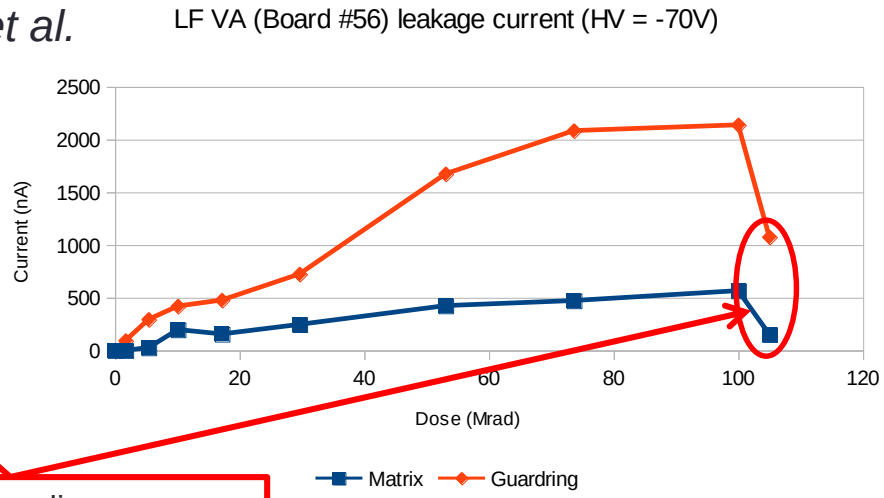
J.Liu et al.

The pixels electrical parameters not really affected by the protons irradiation (10-20% variations)

CCPD-LF irradiated to 100Mrads protons

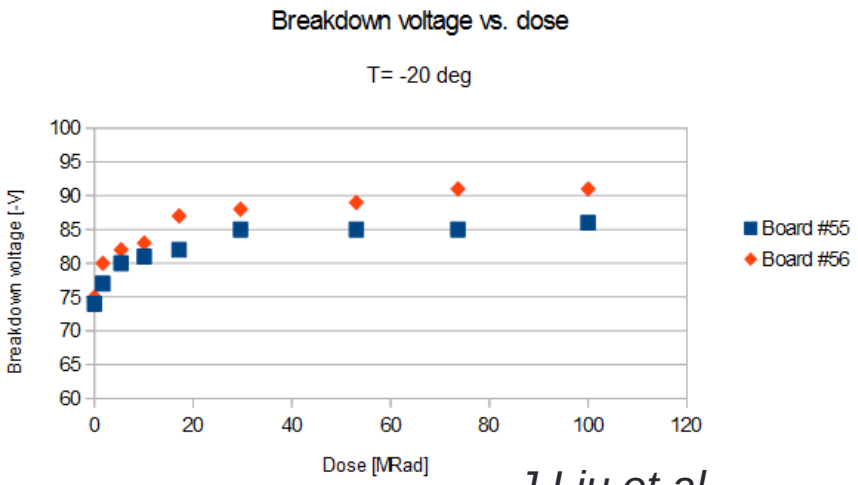
J.Liu et al.





80 days -20°C annealing.

Leakage current reduced approximately by factor of 50, after annealing period.



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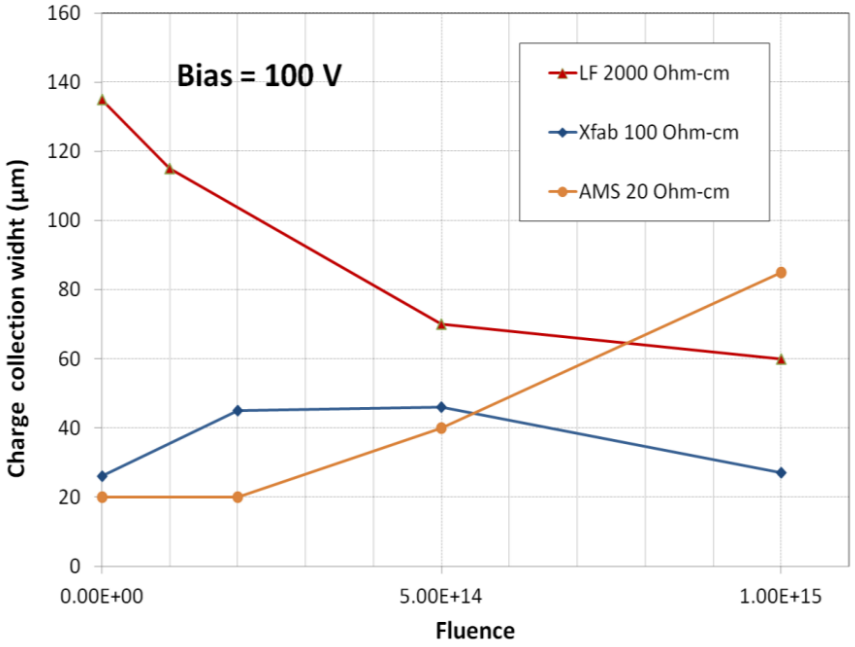
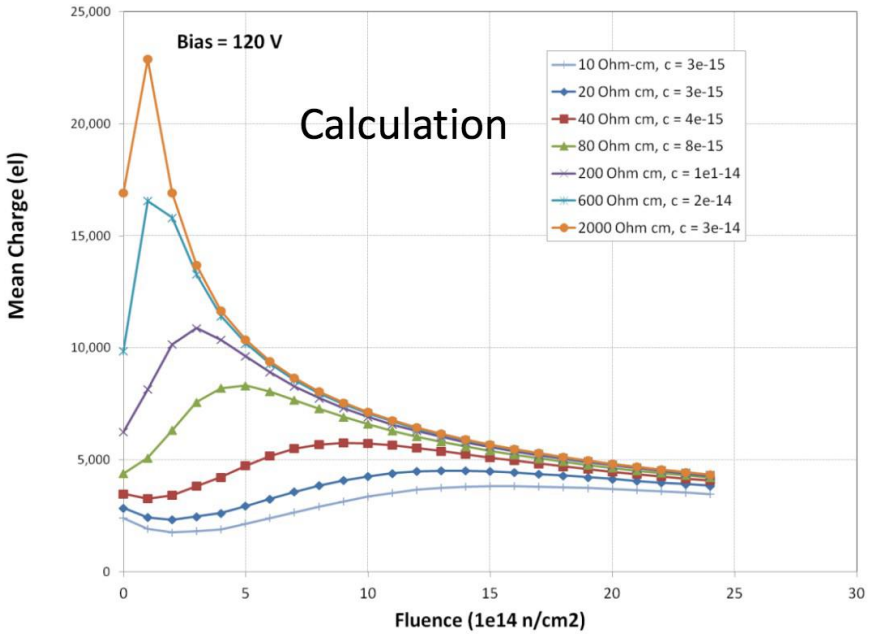
Unusually, the Break Down voltage increases with the dose level.

Resistivity variation under neutron fluence



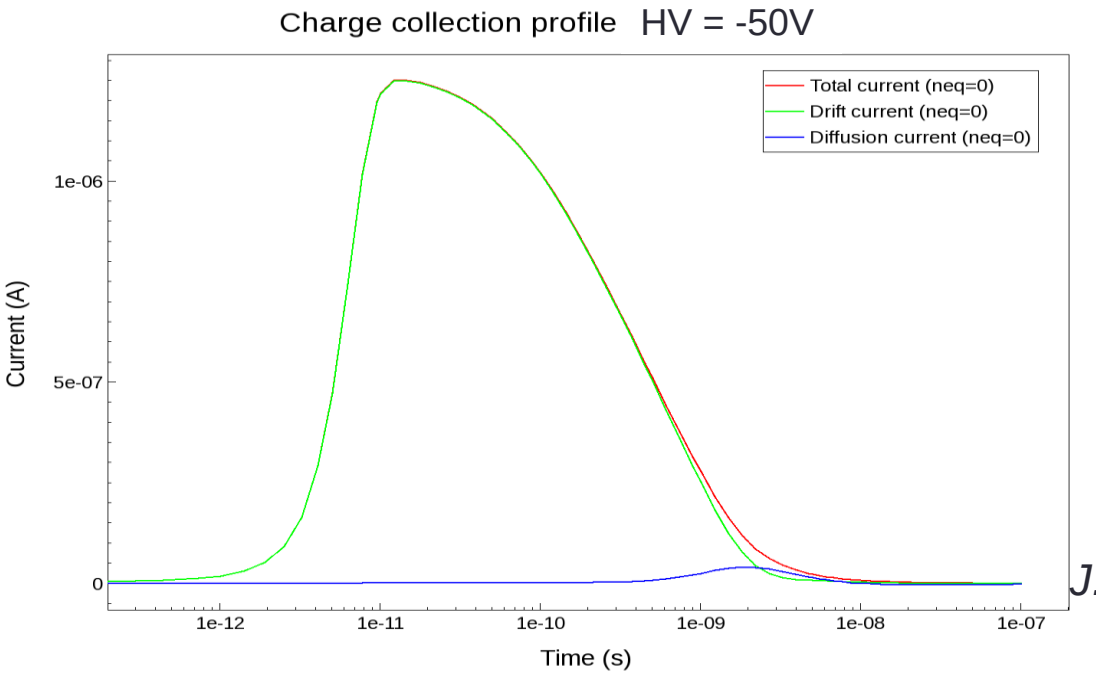
I. Mandić et al.

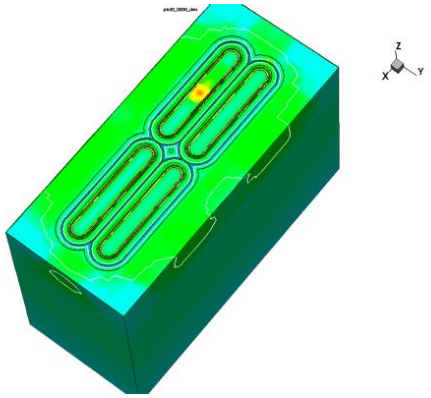


D. Muenstermann et al.

The doping (Neff) variation (acceptor removal phenomenon) was predicted by calculation and measured for LFoundry and other technologies (losing diffusion)

CCPD-LF : transient simulation & charge profile





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Fluence (neq.cm^{-2})	Drift(e-) @ -50V	Diffusion(e-) @ -50V
0	4812	850
1e^{14}	4507	491
1e^{15}	2536	188
1e^{16}	1081	0

43% diffusion charges are lost at approximately 5 Mrads by TCAD charge collection transient simulation

Specification of CMOS Pixel (CPIX) Demonstrator

- Design Task Force (chair Maurice Garcia) Nov 2014
- Pixel module of 1-2 cm^2
- Radiation tolerance more than 50 MRads TID and 10^{15} $neq.cm^{-2}$ NIEL
- Readout by the FE-I4 chip
- When possible also standalone readout
- Power less than 20 µA/pixel
- In-time efficiency more 95% after irradiation
- Bondable either by bumps or glue to FE-I4 with capacitive coupling
- Pin-out compatibility of demonstrators in different technologies for test by many groups

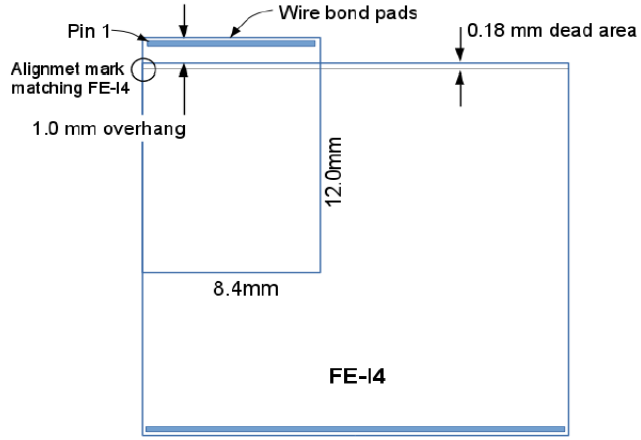


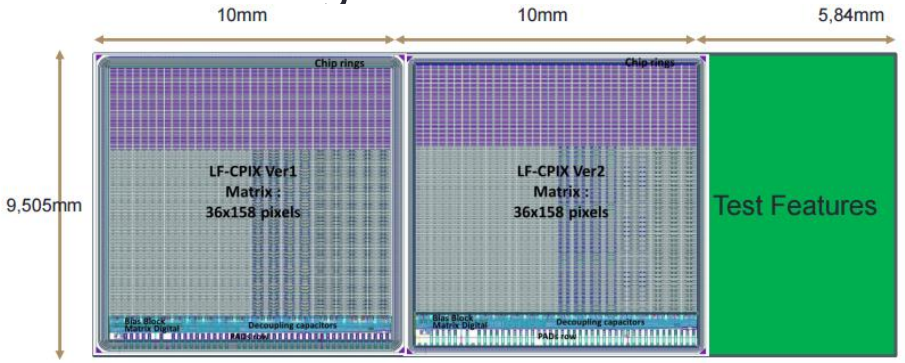
Fig. 1: Alignment of demonstrator to FE-I4 chip

CPIX : Technology Overview

- AMS 350 nm
- AMS 180 nm
- **LFoundry 150 nm**
- Global Foundry 130 nm
- ESPROS 150 nm
- Toshiba 130 nm
- TowerJazz 180 nm
- STM 160 nm
- IBM 130nm
- XFAB 180 nm

LF-CPIX chip V1 and V2

- The first large ~1cm² demonstrator LF CPIX is being submitted:

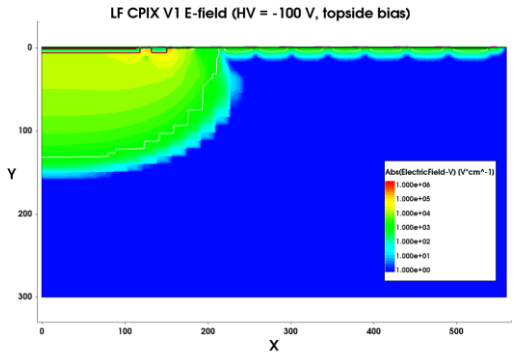


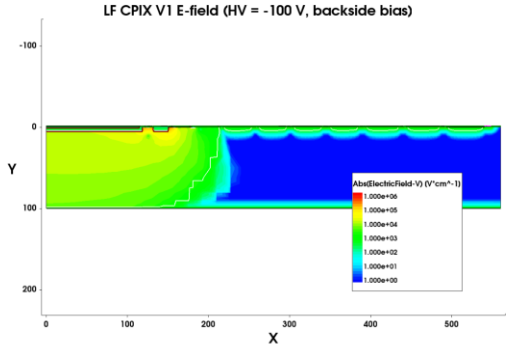
  - Consists of three pixel flavors: passive, digital and analog pixel. Some improvements have been brought to them with respect to the characterizations of the LF CCPD prototypes.
  - New guard-ring strategy in LF CPIX Ver2 to increase the breakdown voltage and reduce the inactive region (edgeless fill factor)

- Improved electronics performance and better charge collection efficiency are expected.
- Further TCAD simulations were carried out for the LF CPIX particularly the capacitance, breakdown and the charge collection taking into account the bulk and surface damages.

Depletion and e-field of LF CPIX V1 and V2 by simulation

V1





Big un-depleted area between depleted edge and cutting edge → guard-ring reducing is possible → reduced dead region.

V2

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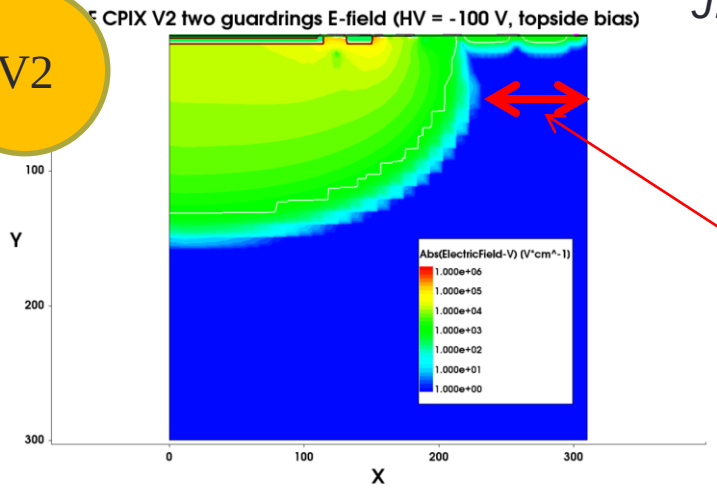
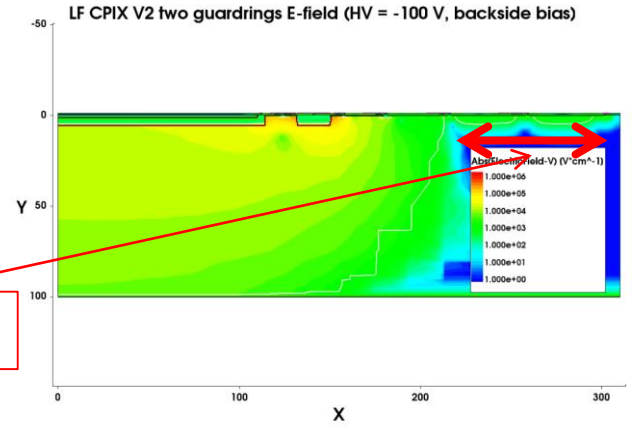




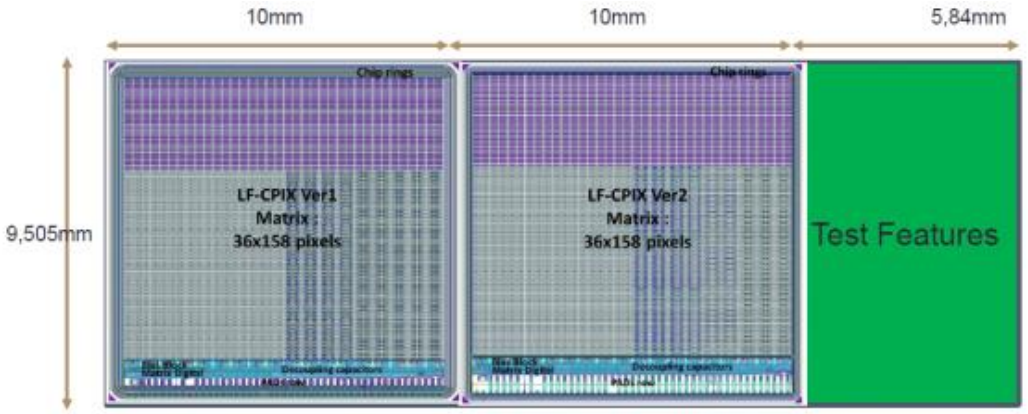
~100 µm

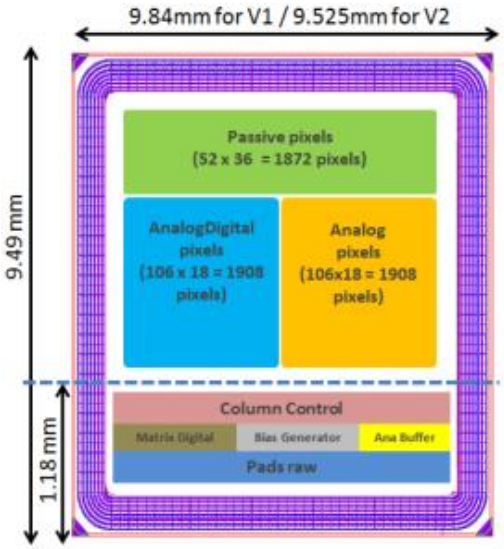
Better than V1 but the depleted region can not reach the chip edge even with removed 5 outer guard-rings. Too much dangerous to deal with leakage current and High Electrical Field on the edge.

LF-CPIX Demonstrator + Fully Monolithic

LF-CPIX :

- 150nm CMOS (Avezzano, Italy)
- 2kΩcm p-type bulk
- Deep N-Well/P-Well available
- HV process
- CPPM + IRFU/CEA + Bonn





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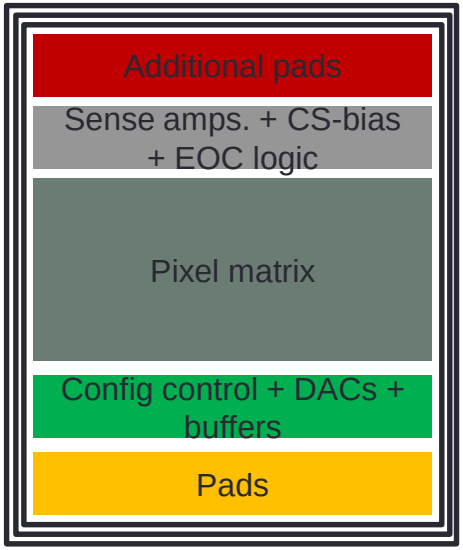

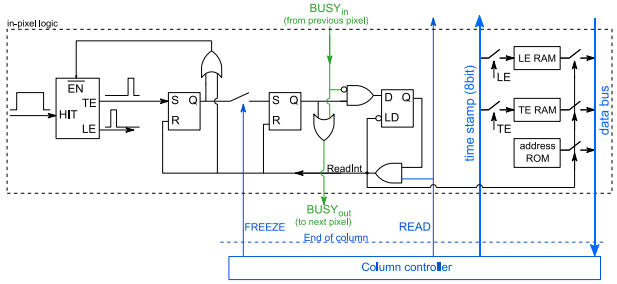

submission 05/2016

Full 1cm² monolithic (à la FE-I3 readout)

Conclusions and future plans

- HVCMOS pixel prototypes produced in 10 different technologies. We have the choice…
- Most advanced CCPD test beam results in previous prototypes made in AMS 180 nm technologies gave 99.7% efficiency before radiations.
  The CCPD_LF chip is still alive after radiations up to 1Grads, and show very good results and behavior at 100Mrads. Very promising LFoundry technology.
- Timing collection to be improved (lower thresholds, higher signals with HR, time slewing corrections) for the CPIX demonstrator, and some minors bugs to correct.
- TCAD simulation, a very good help addressed to the HVCMOS project. Thanks for the Jian Lu (CPPM/SDU) contribution and work through his Co-PhD (simulation, setup development, prototype characterization, test beam...)
- CPIX Demonstrator program started with the goal to produce 2-3 demonstrator types for the TDR in fall of 2016.
- The IHEP, SDU and CPPM have a very strong collaboration since many years, on ATLAS developments. We are willing to expand the partnership between Chinese institutes and CPPM on further HVCMOS .