

Achievements and Perspectives of CMOS Pixel Sensors for **HIGH-PRECISION** Vertexing & Tracking Devices

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<http://www.iphc.cnrs.fr/-PICSEL-.html>

9th FCPPL Workshop / Strasbourg / April 1st, 2016

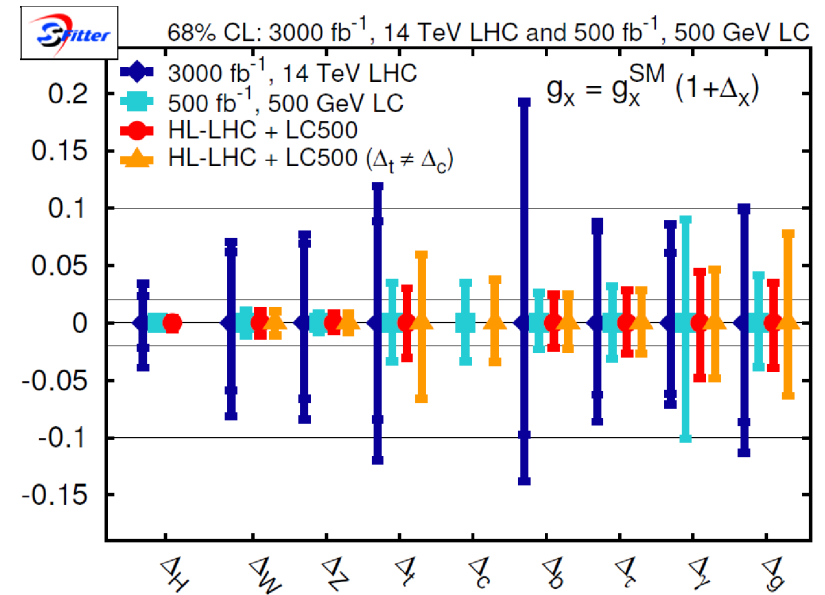
Contents

- *Primordial motivations & main features of CMOS sensors*
- *1st architecture developed - state of the art*
 - MIMOSA-26 (EUDET chip applications) $\rightarrow$ MIMOSA-28 (STAR-PXL)
- *Extension towards more demanding experiments*
 - ALICE-ITS & -MFT ○ CBM-MVD ○ ILC
- *Perspectives for ILC-CEPC & forthcoming challenges*
 - read-out speed ○ architectures
- *Conclusion*

Original Motivation for the R&D: Vertexing at the ILC

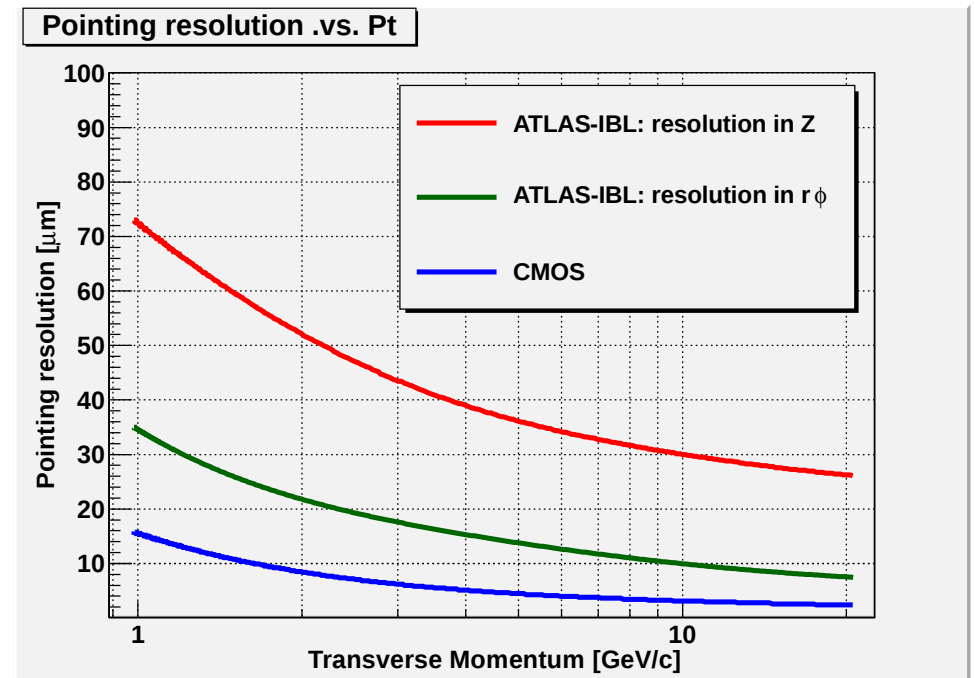
● CMOS PIXEL SENSORS (CPS) pioneered for the vertex detector requirements :

- * unprecedented granularity & material budget (very low power)
- * much less demanding running conditions than at LHC
 - ⇒ alleviated read-out speed & radiation tolerance requests
- * ILC duty cycle $\sim 1/200$
 - ⇒ power saving by power pulsing sub-systems



● Vertexing goal:

- * achieve high efficiency & purity flavour tagging
 - ↗ charm & tau, jet-flavour !!!
- $\sigma_{R\phi, Z} \leq 5 \oplus 10/p \cdot \sin^{3/2}\theta \text{ } \mu\text{m}$
 - ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot \sin^{3/2}\theta$
- ▷ Comparison: $\sigma_{R\phi, Z}(\text{ILD})$ with VXD
 - made of ATLAS-IBL or ILD-VXD pixels



The Central Conflict of Vertexing

- A COMPLEX SET OF STRONGLY CORRELATED ISSUES :

- ✧ **Charged particle sensor technology :**

- highly granular, thin, low power, swift pixel sensors

- ✧ **Micro-electronics :**

- highly integrated, low power, SEE safe, r.o. μ circuits

- ✧ **Electronics :**

- high data transfer bandwidth (no trigger), some SEE tol.
- low mass power delivery, allowing for power cycling

- ✧ **Mechanics :**

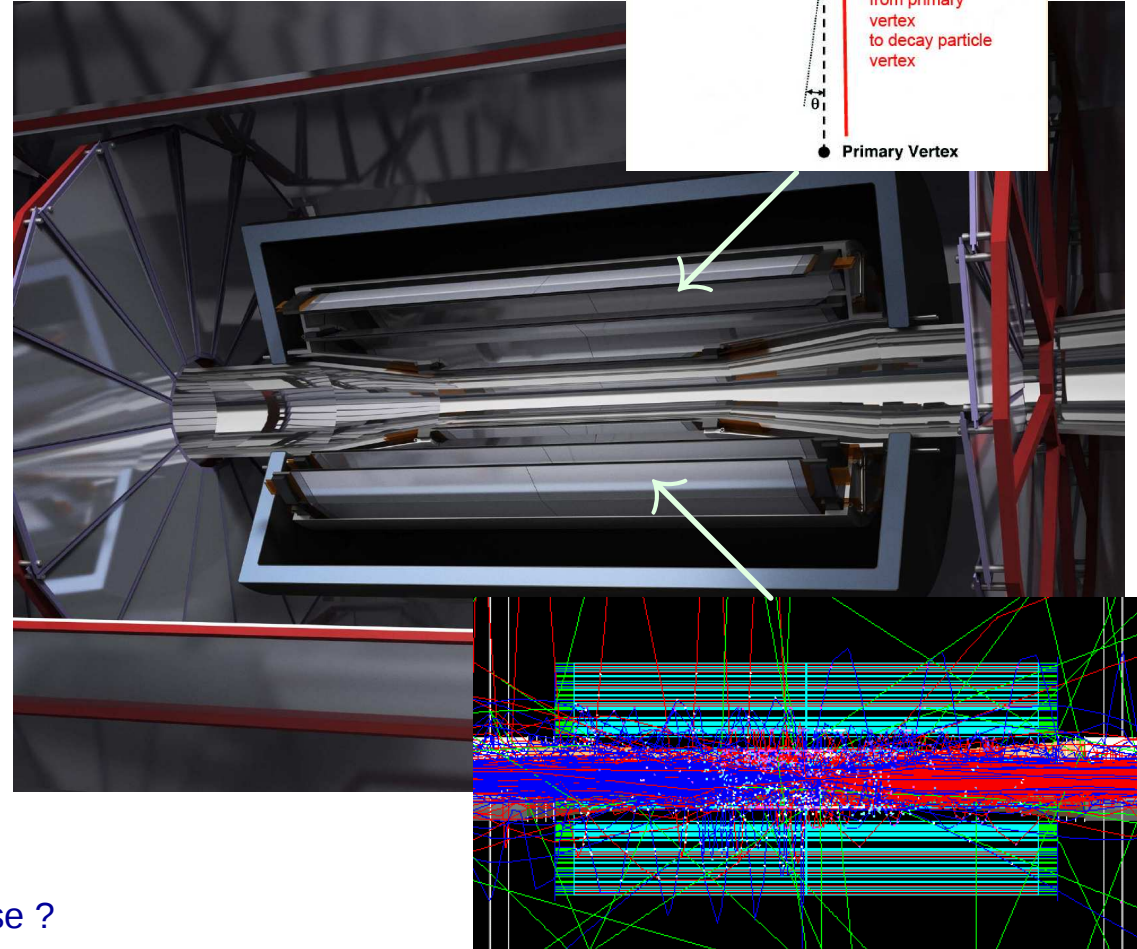
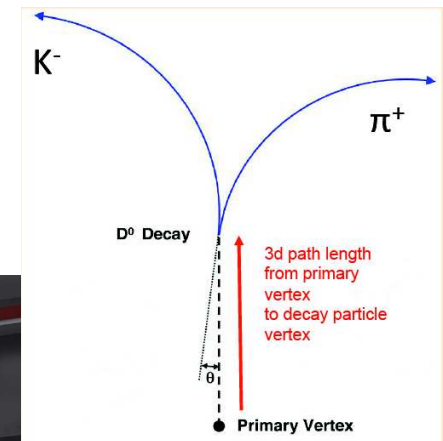
- rigid, ultra-light, heat but not electrically conductive, mechanical supports, possibly with $C_{\Delta t} \simeq C_{\Delta t}^{Si}$
- very low mass, preferably air, cooling system
- micron level alignment capability

- ✧ **EM compliance :**

- power cycling in high B field $\Rightarrow$ F(Lorentz)
- higher mode beam wakefield disturbance $\Rightarrow$ pick-up noise ?

- ✧ **Radiation load and SEE compliance at T_{room}**

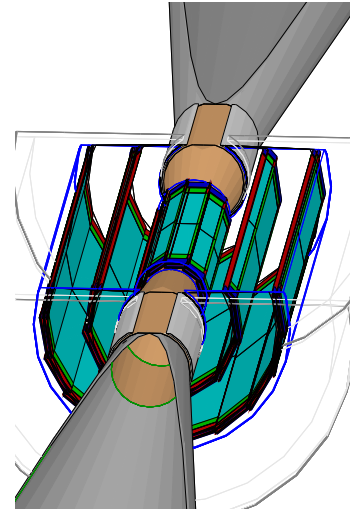
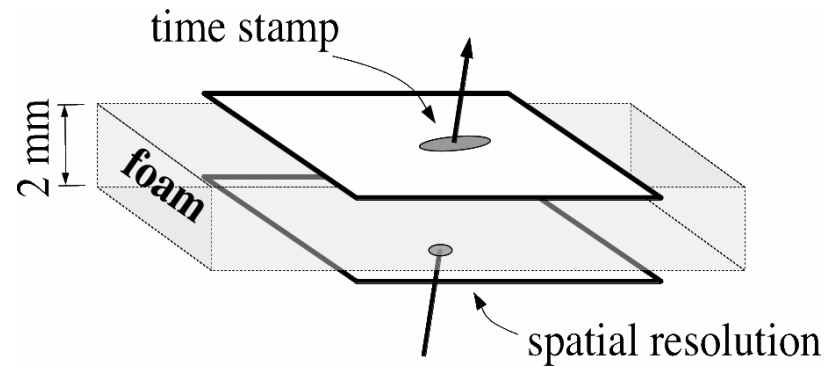
$\Rightarrow$ reduced material budget



The RoleS of the "Vertex" Detector

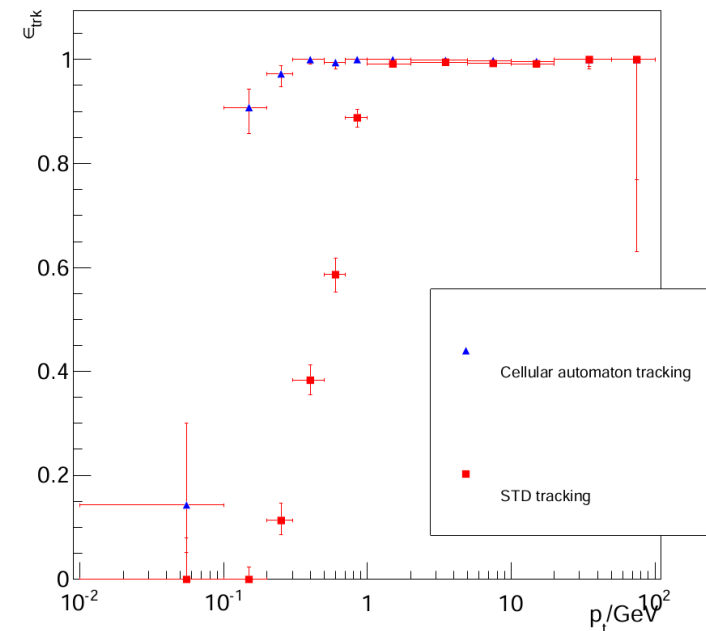
DISPLACED VERTEX RECONSTRUCTION AND CHARACTERISATION :

- reconstruction of collision point
- reconstruction of D-meson and τ -lepton vertices
- reconstruction of b-quark decays in (top-quark) jets
- determination of displaced vertex electrical charge
- etc.



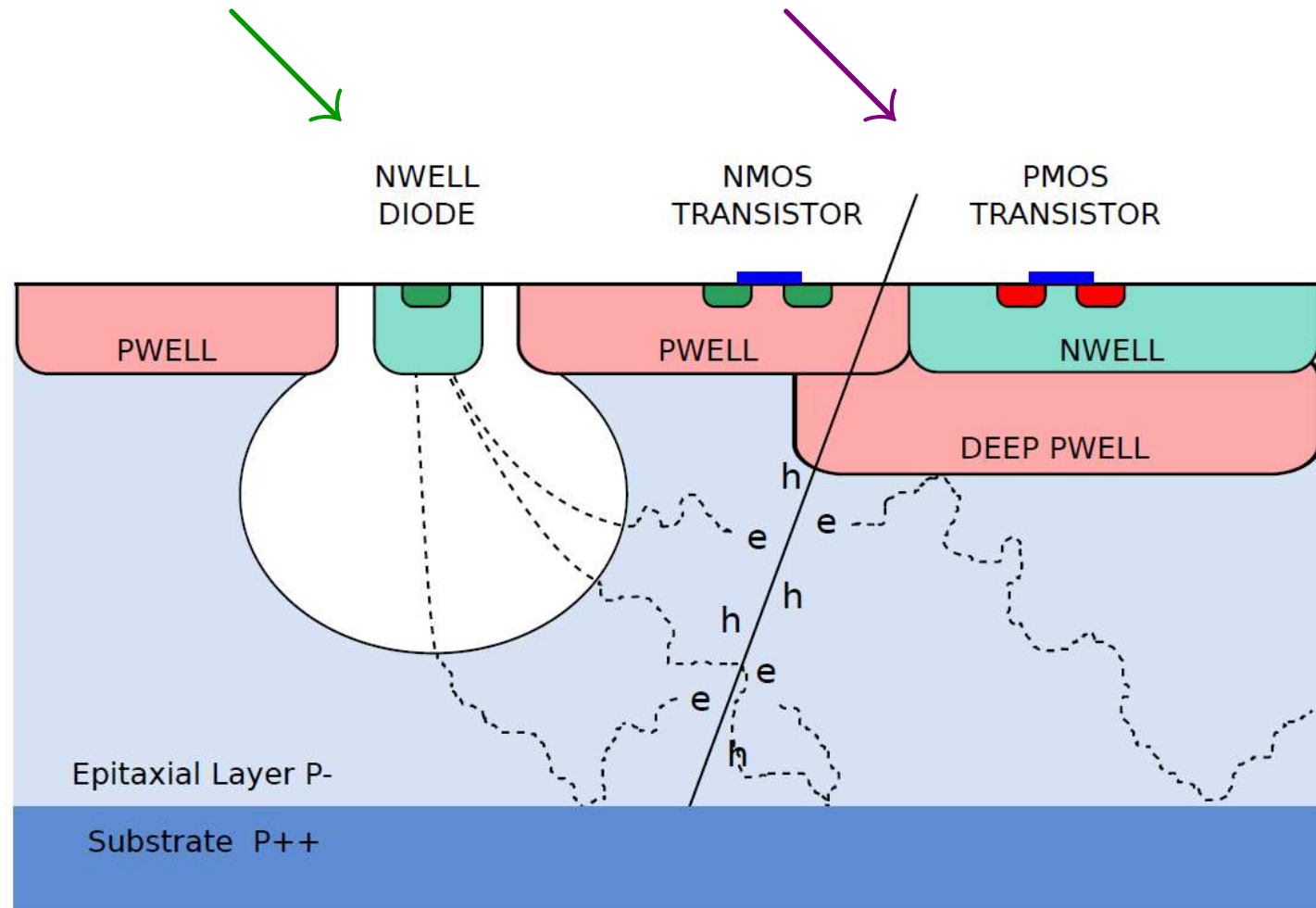
ROLE IN THE TRACKING :

- track seeding (depending on main tracker)
- low P_t track reconstruction
- track momentum determination (in particular low P_t)
- fake tracks mitigation (E_{miss} determination)



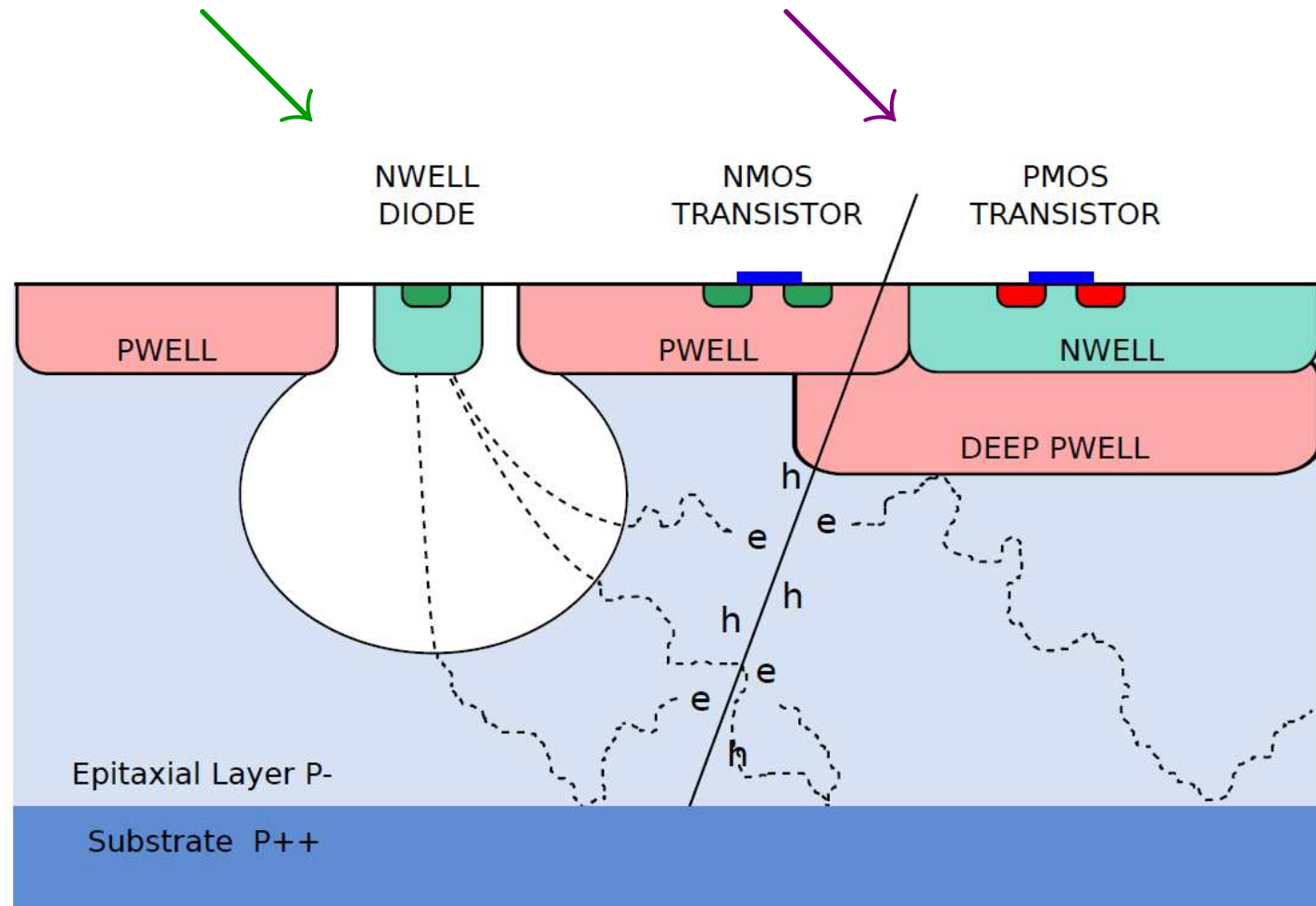
CMOS Pixel Sensors (CPS): Main Features

- CMOS Pixel Sensors $\equiv$ **Detector** $\oplus$ **Front-End Electronics** in same die



CMOS Pixel Sensors: Main Features

- R&D addresses **Sensing Element** $\oplus$ **Read-Out μ circuitry**



Sensing Node & VFEE Optimisation

- **General remarks on sensing diode :**

- should be small because : $V_{signal} = Q_{coll}/C$; Noise $\sim C$; $G_{PA} \sim 1/C$
- BUT should not be too small since $Q_{coll} \sim CCE$ (important against NI irradiation)

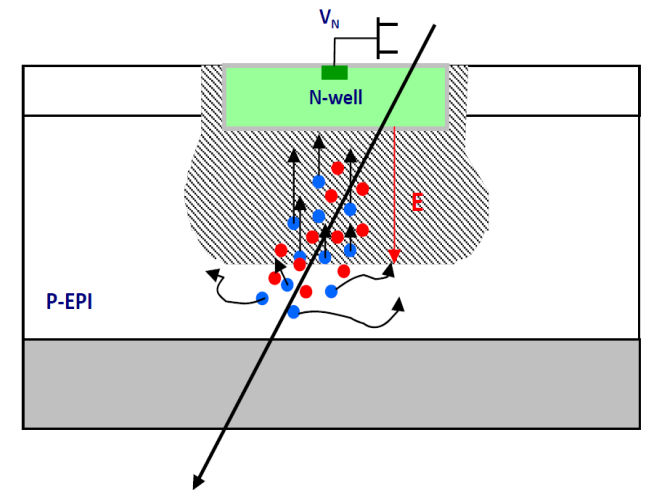
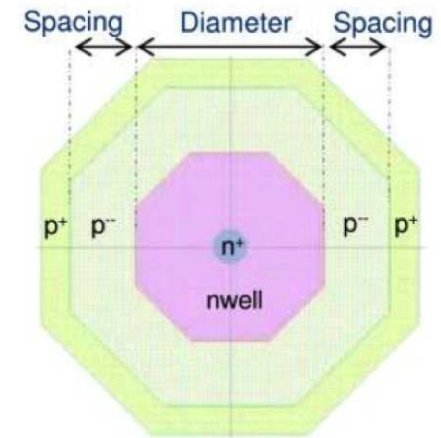
- **General remarks on pre-amplifier** connected to sensing diode :

- should offer high enough gain to mitigate downstream noise contributions
- should feature input transistor with minimal noise (incl. RTS)
- should be very close to sensing diode (minimise line C)

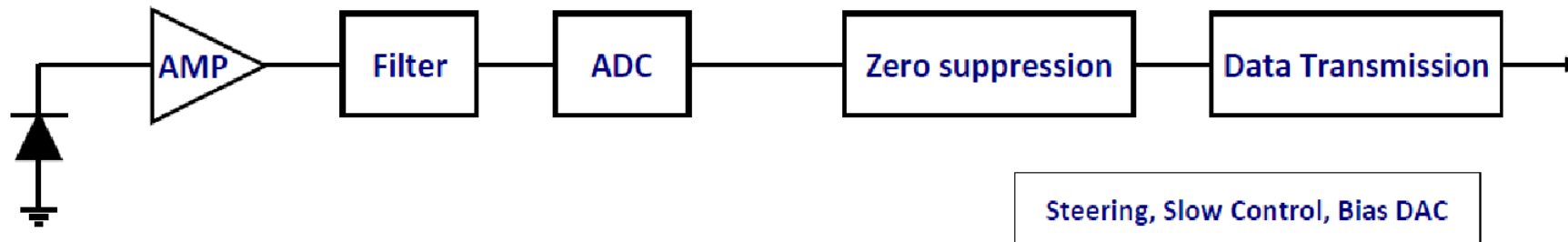
- **General remarks on depletion voltage :**

- apply highest possible voltage on sensing diode
preserving charge sharing $\mapsto \sigma_{sp}$
- alternative : backside/reverse biasing

⇒ **Multiparametric trade-off to be found,
based on exploratory prototypes rather than on simulations**



Main Components of the Signal Processing Chain



● Typical components of read-out chain :

- **AMP** : In-pixel low noise pre-amplifier
- **Filter** : In-pixel filter
- **ADC** : Analog-to-Digital Conversion : 1-bit $\equiv$ discriminator
 - may be implemented at column or pixel level
- **Zero suppression** : Only hit pixel information is retained and transferred
 - implemented at sensor periphery (usual) or inside pixel array
- **Data transmission** : O(Gbits/s) link implemented on sensor periphery

● Read-Out alternatives :

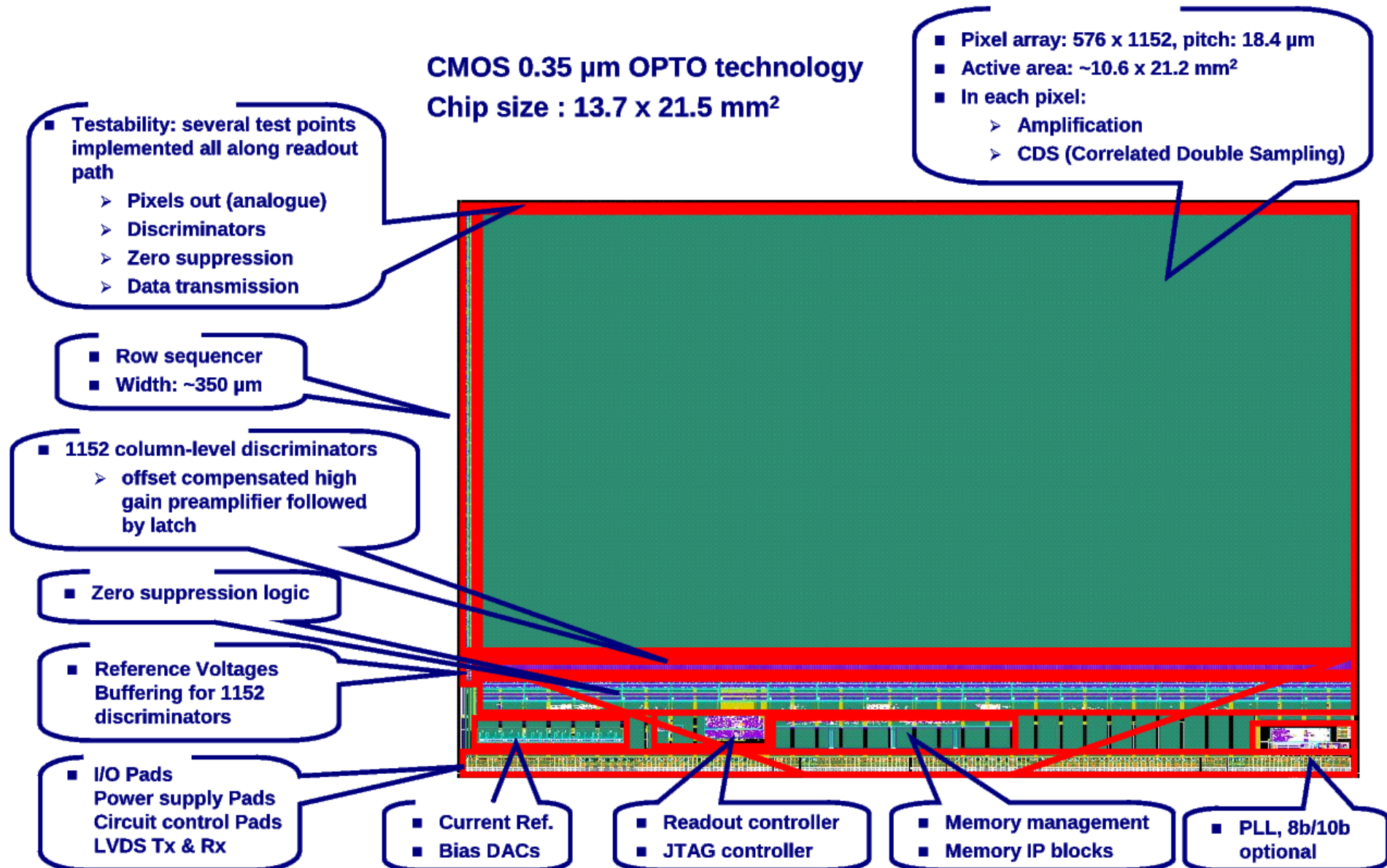
- **Synchronous** : rolling shutter architecture
- **Asynchronous** : data driven architecture

● Rolling shutter : best approach for twin-well processes

- trade-off between performance, design complexity, pixel dimensions, power, ...
- MIMOSA-26 (EUNET), MIMOSA-28 (STAR), ...

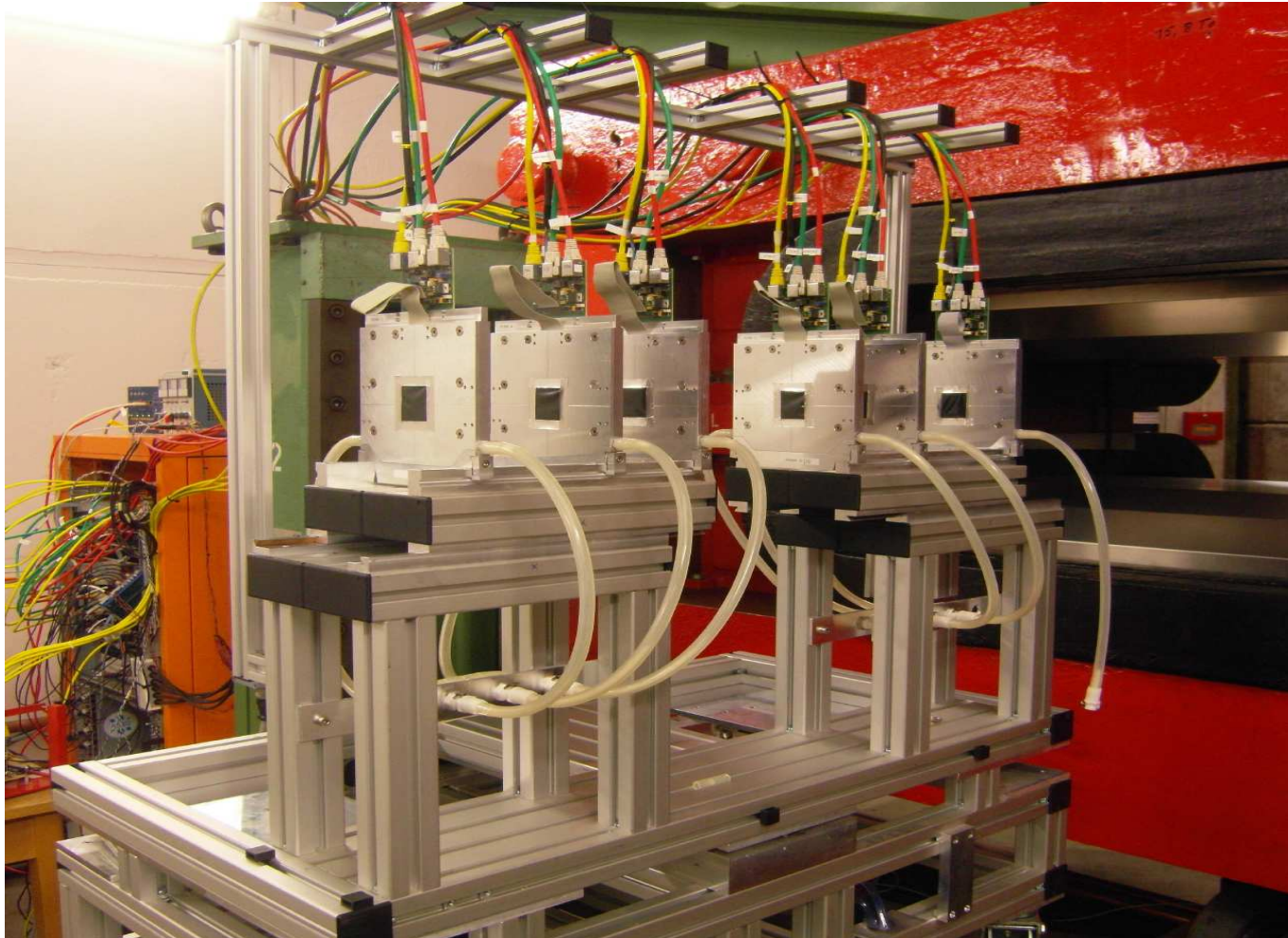
MIMOSA-26: Established Architecture

- Rolling shutter architecture applied to 1st generation of CPS applications



Widespread Application of MIMOSA-26

- EUDET Beam Telescope : adapted to sub-GeV electron beams

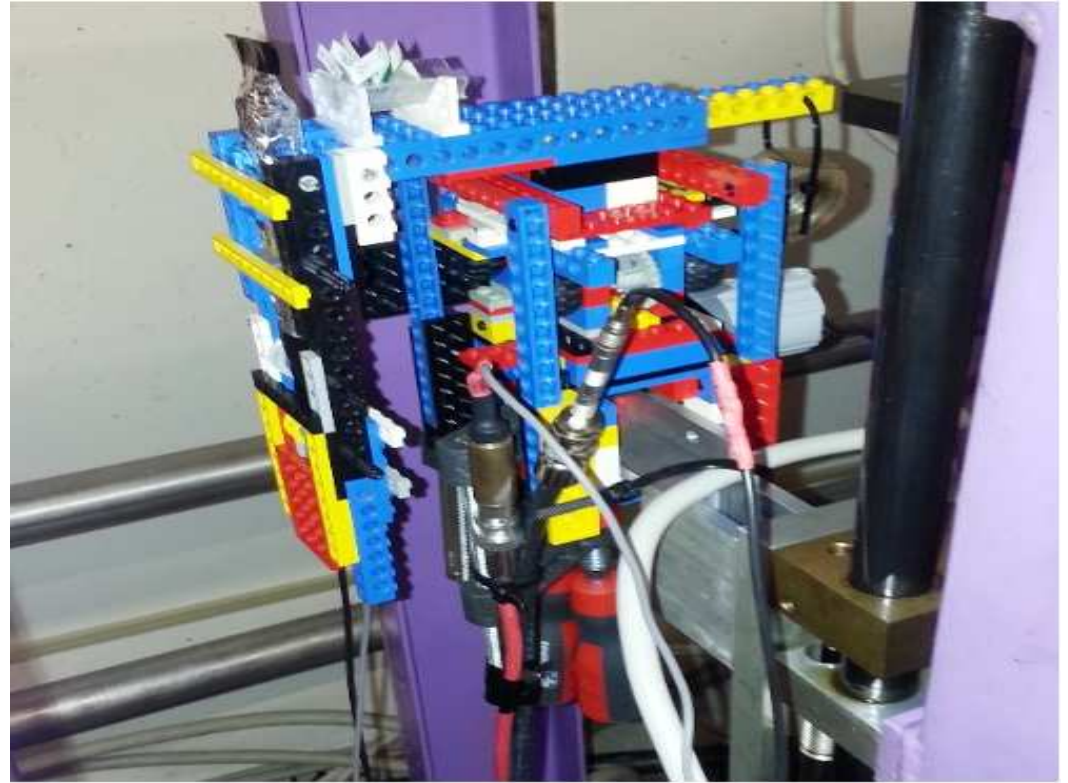


- about 10 copies or similar devices used at DESY, CERN, SLAC, TRIUMF, ...

Other Applications of MIMOSA-26

- Ex: Vertex Detector of NA61/SHINE Heavy Ion Experiment at CERN
(<http://ph-news.web.cern.ch/content/first-pb-beam-na61shine>)

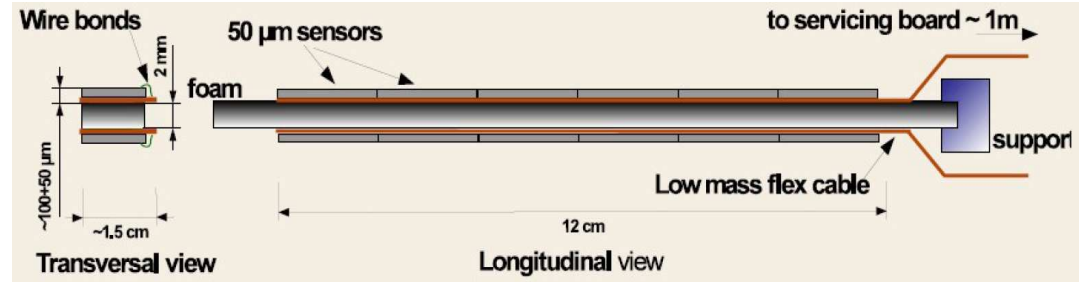
- MIMOSA-26 sensors being exposed to radiation tolerance tests with $1.2 \cdot 10^{10}$ Pb ions/cm² on H2 beam at CERN



- Several other applications: FIRST/GSI, NA-63/CERN, CBM-MVD-demo./FAIR, hadrontherapy, X-Ray imager demo., etc.

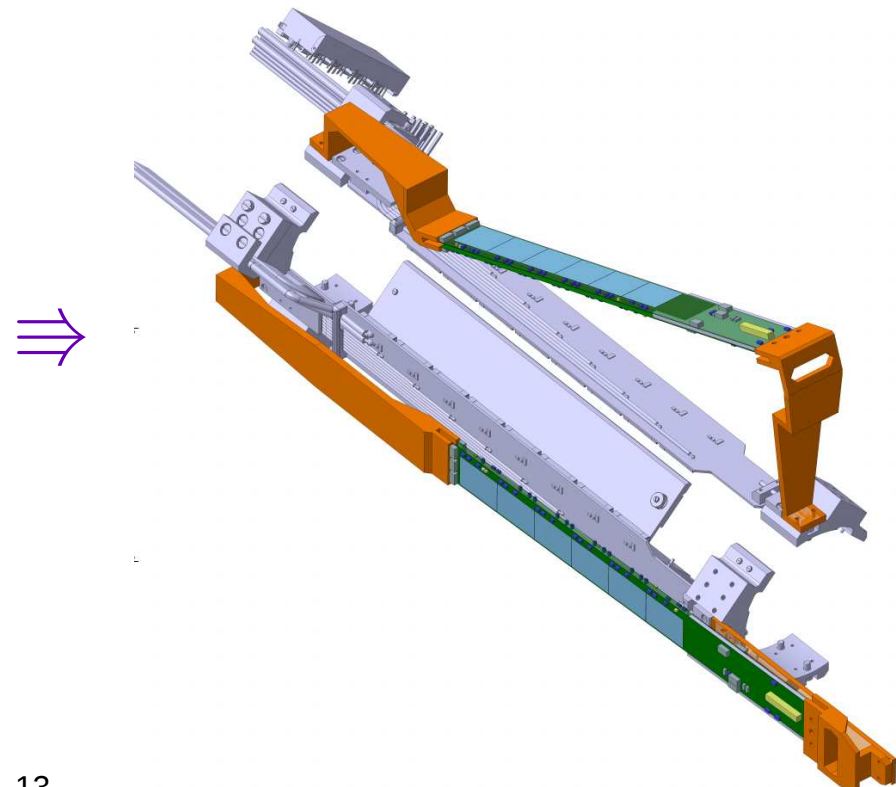
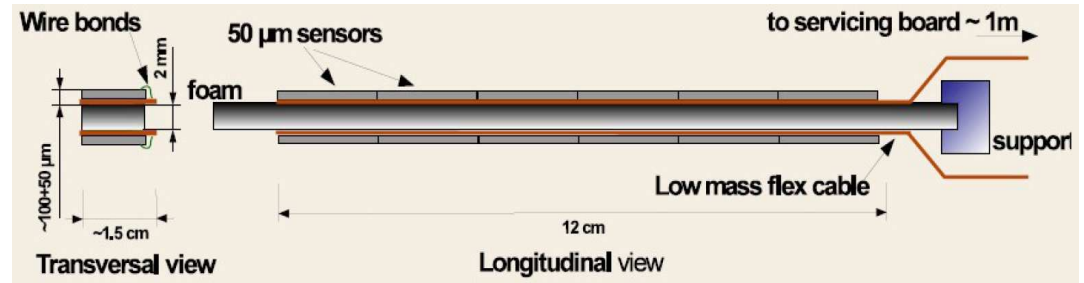
PLUME Double-Sided Ladder Based on 12 MIMOSA-26

- ILC vertex detector triggered R&D on ultra-light double-sided ladder with $\lesssim 0.3\%$ X0 material budget
- **PLUME ladder :**
2x6 MIMOSA-26 ($50\ \mu\text{m}$)

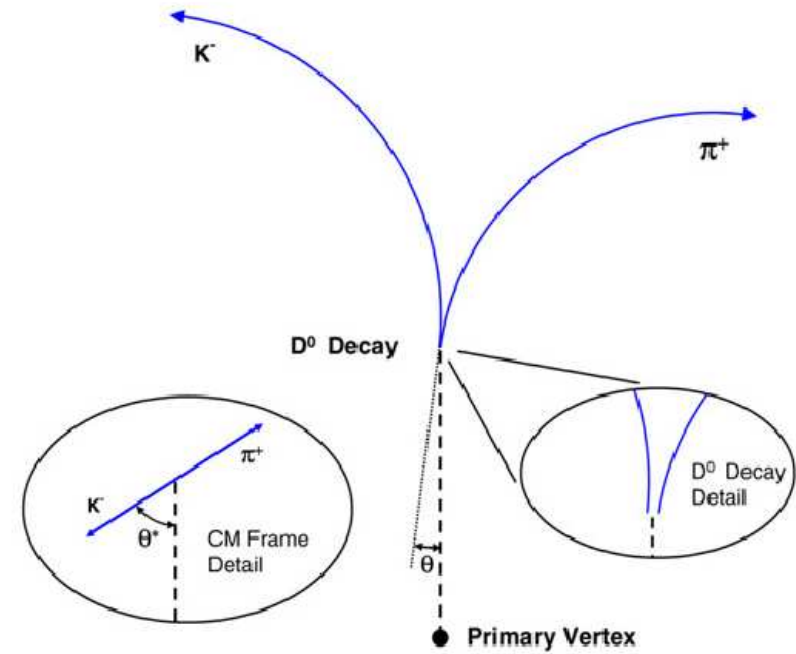
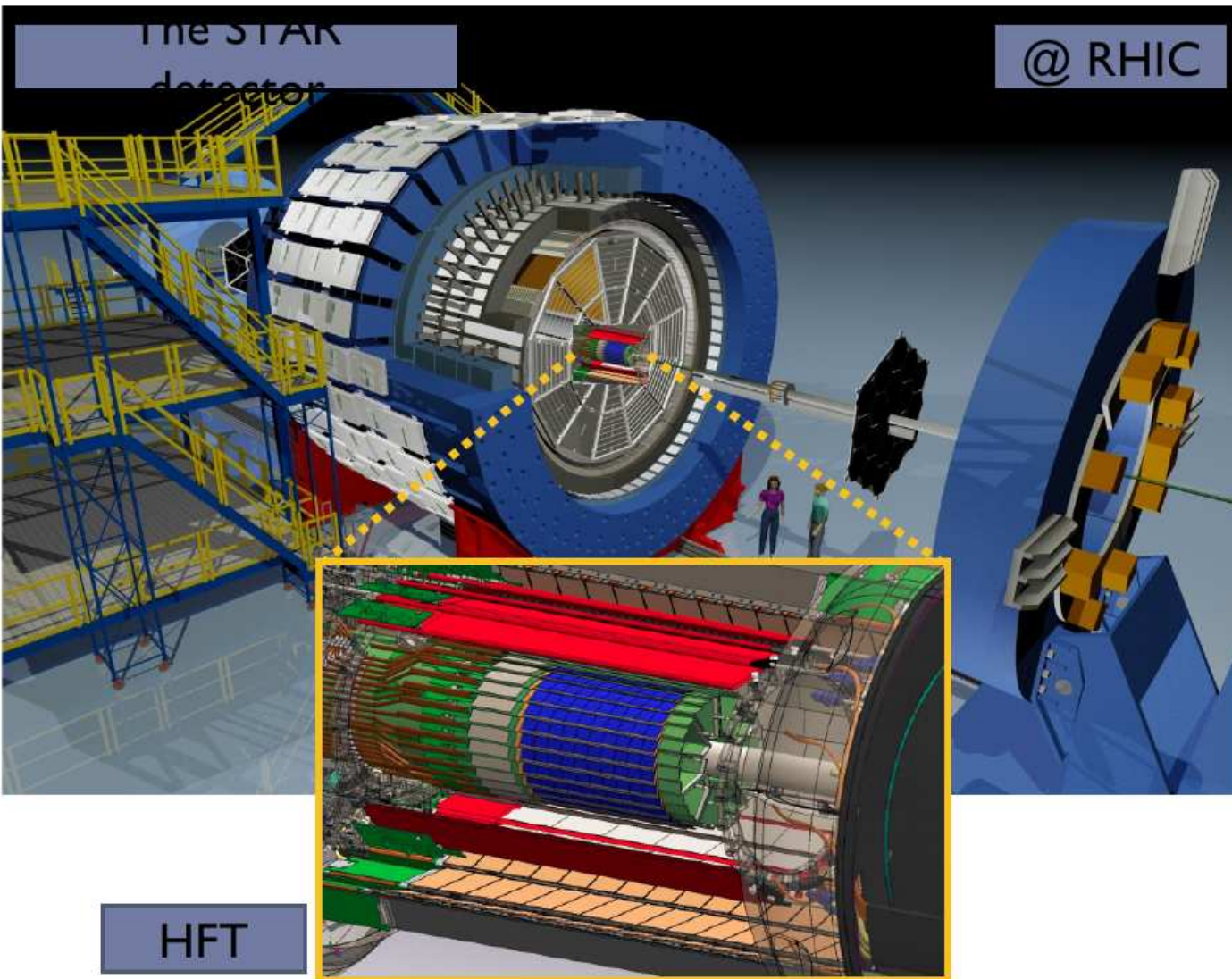


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- ILC vertex detector triggered R&D on ultra-light double-sided ladder with $\lesssim 0.3\%$ X0 material budget
- **PLUME ladder :**
2x6 MIMOSA-26 ($50\ \mu\text{m}$)
- Most recent application :
BEAST-II at SuperKEKb with
2 PLUME ladders (0.4% X0) equipping
IP environnement to characterise
beam related background using
mini-vectors $\Rightarrow$ rate & direction
- **Data taking starting in 2017**



State-of-the-Art : STAR-PXL

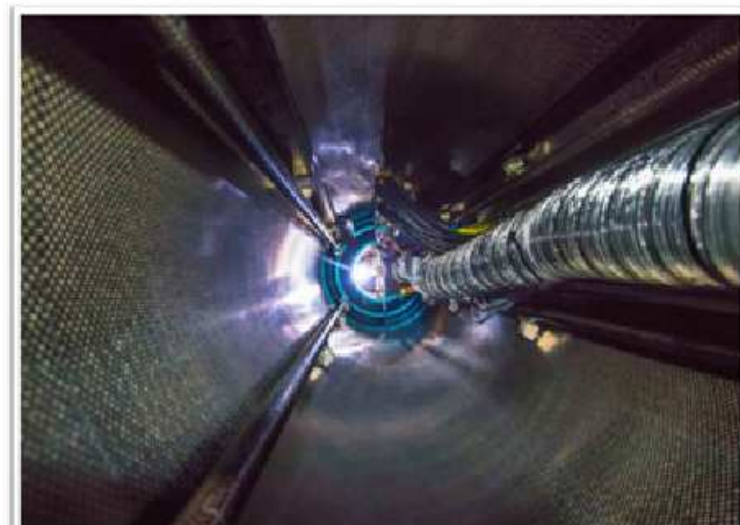


200 GeV Au+Au collisions @
RHIC

$dN_{ch}/d\eta \sim 700$ in central events

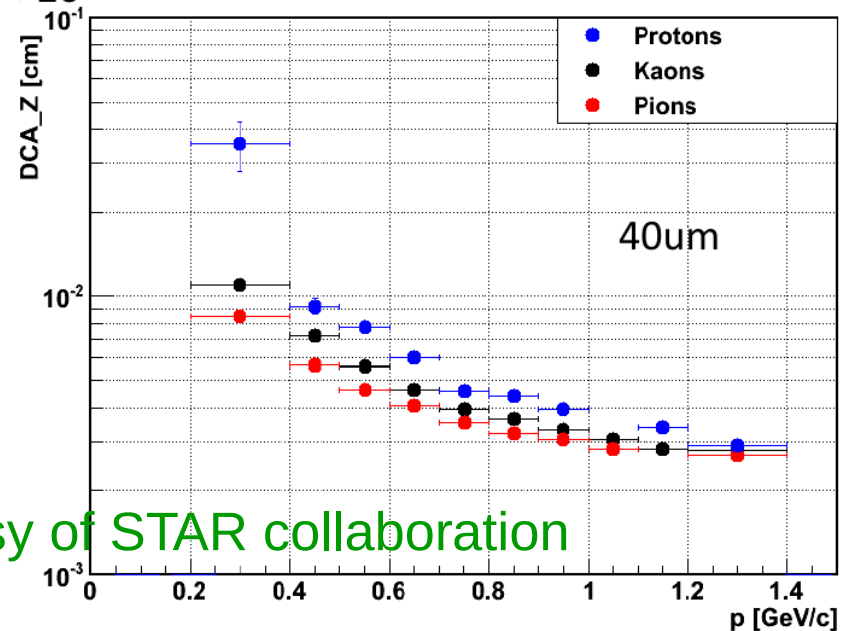
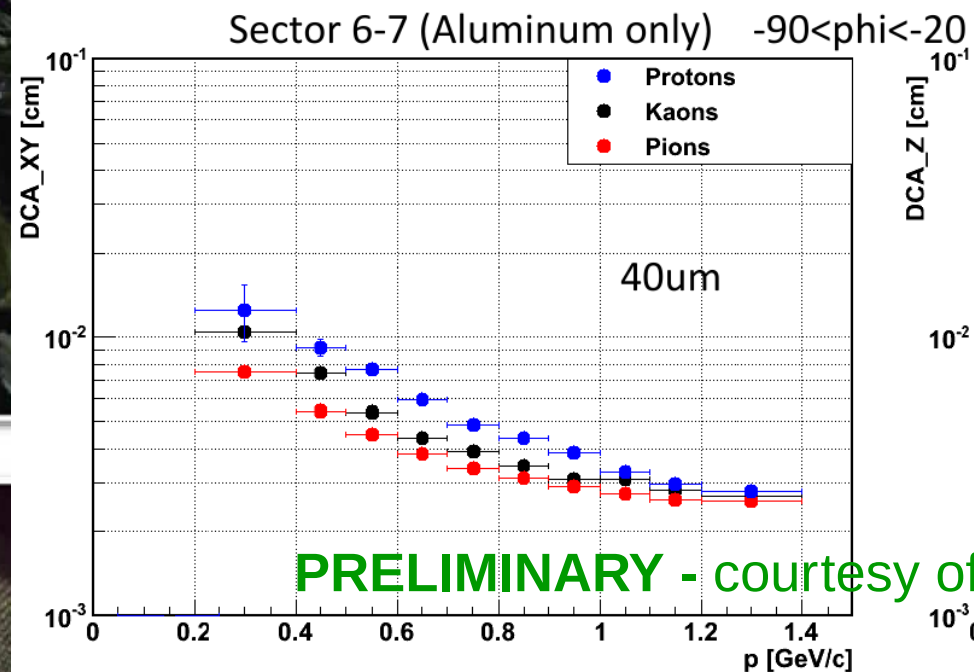


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Data taking from March-June 2014

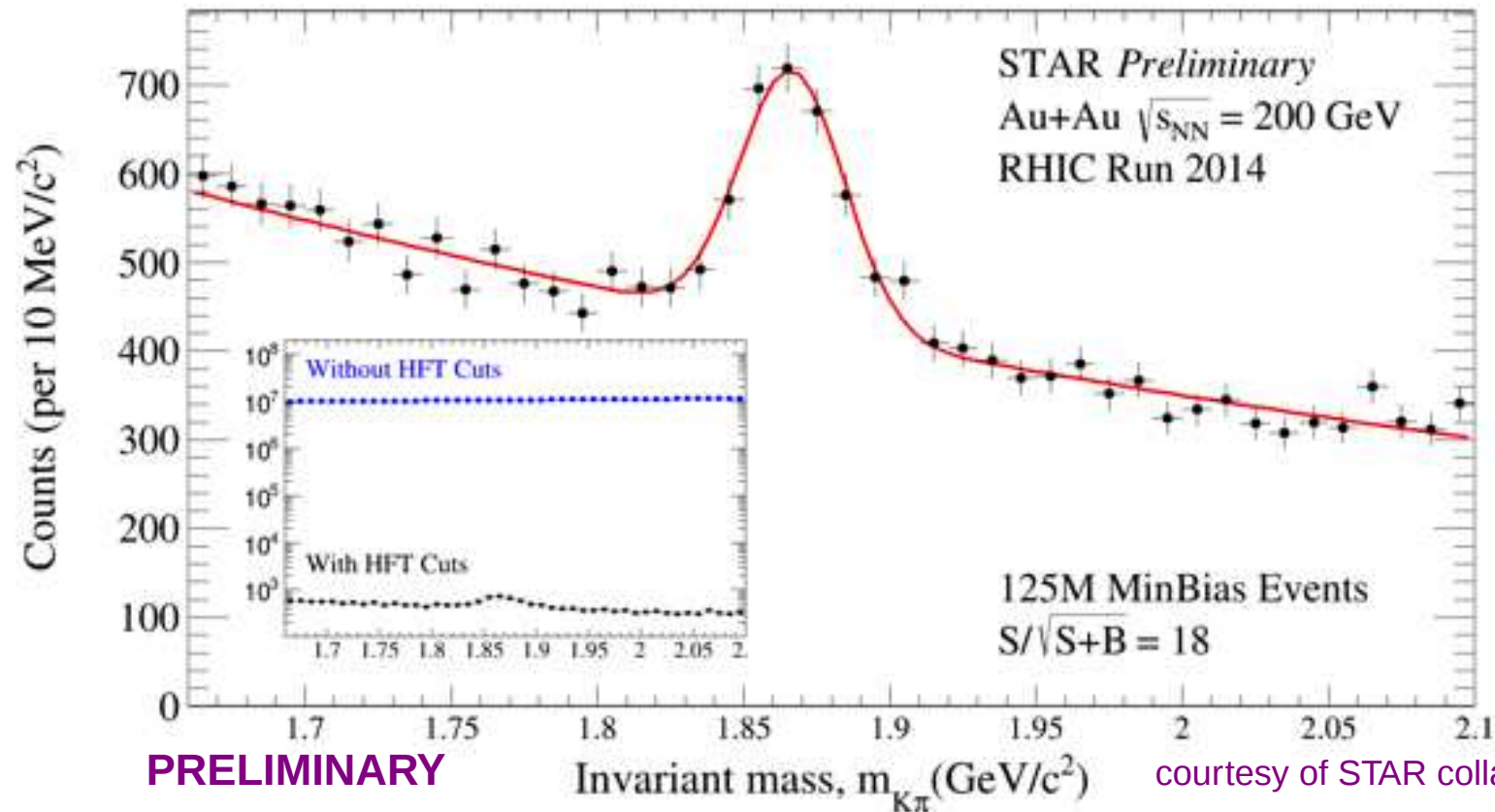


Validation of CPS for HEP (25/09/14 : DoE final approval, based on vertexing performance assessment)

MIMOSA28
(ULTIMATE)

State-of-the-Art : STAR-PXL

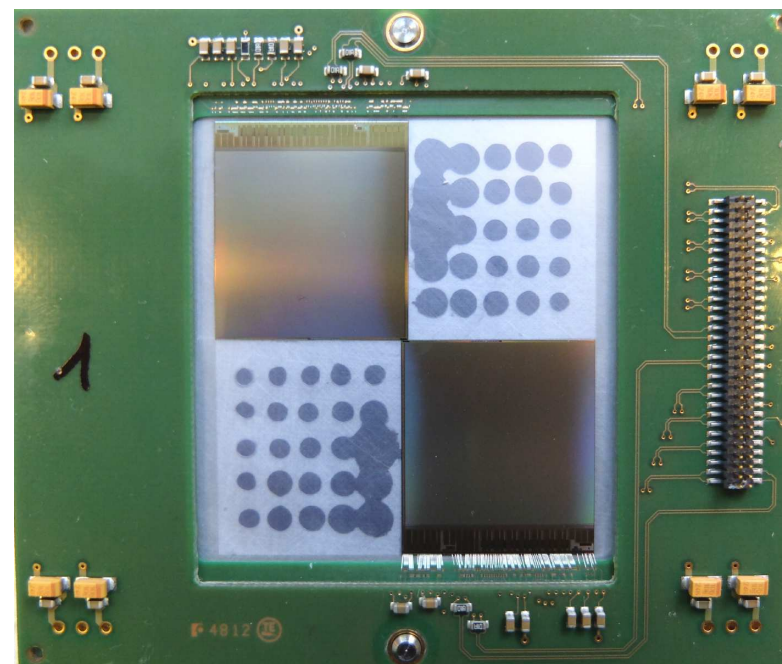
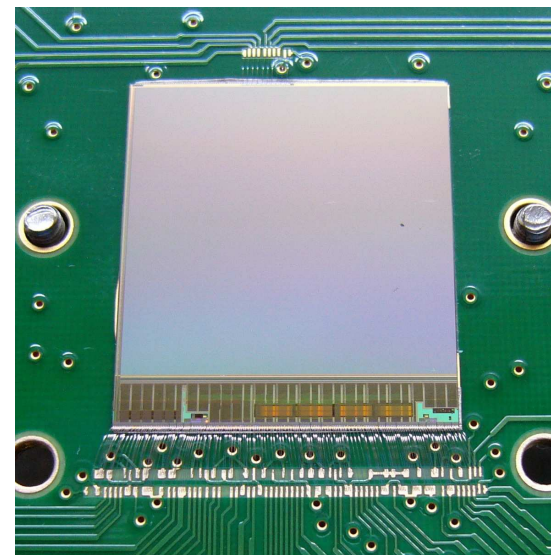
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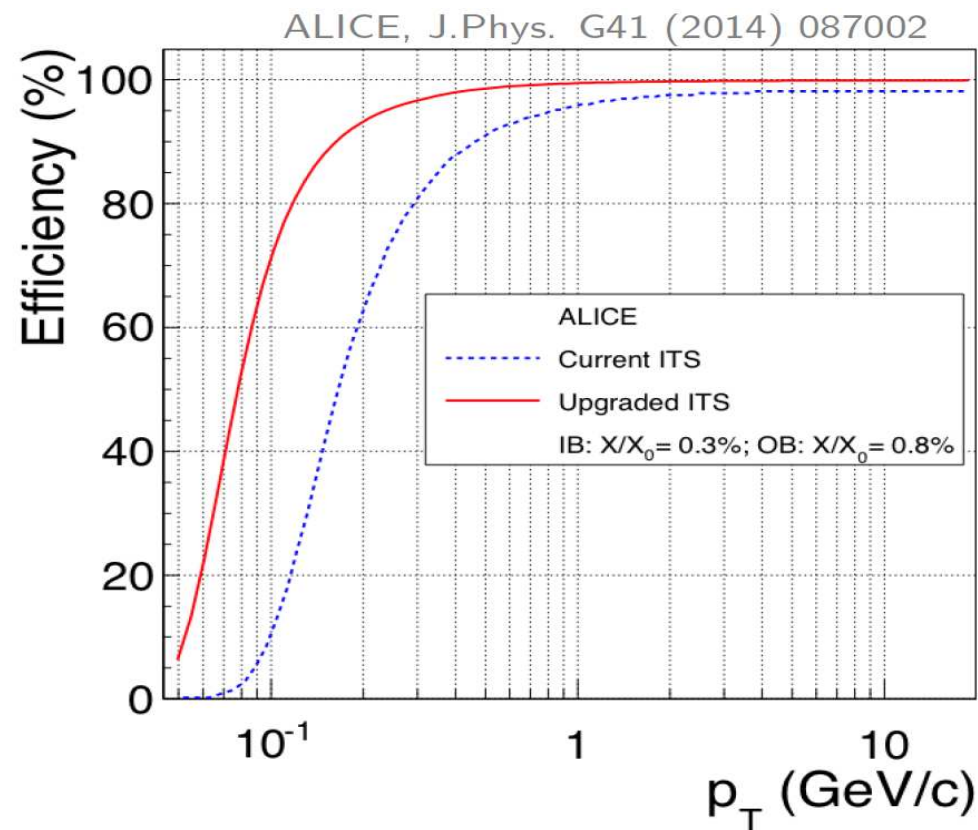
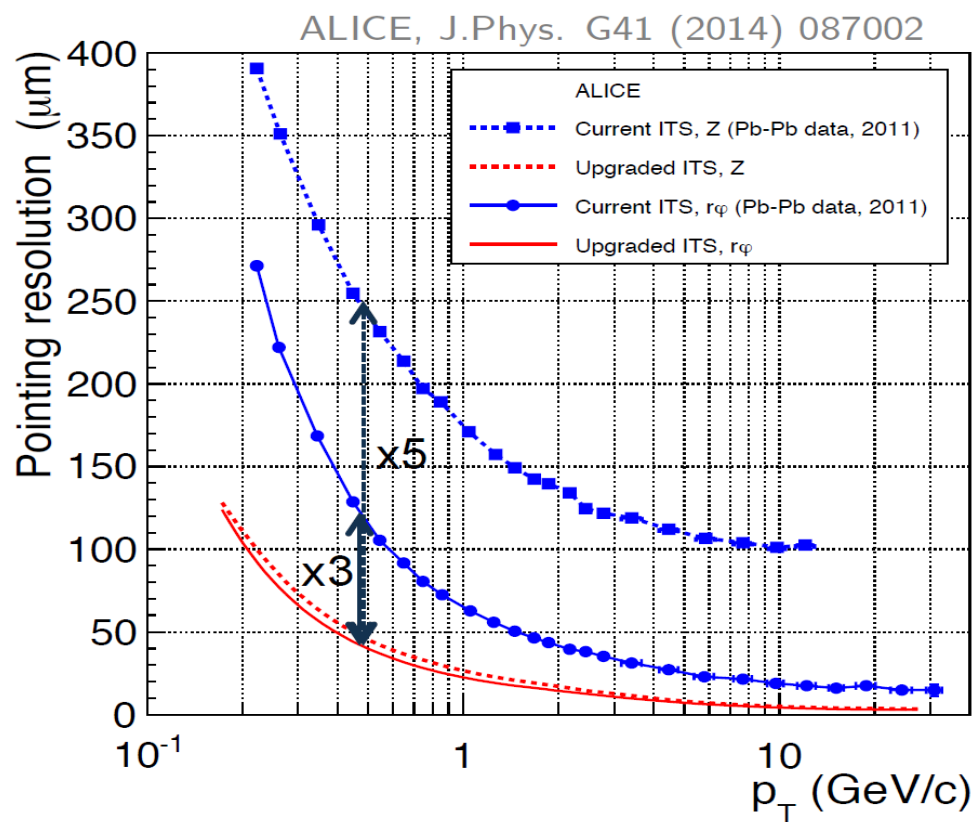
Applications of MIMOSA-28/ULTIMATE

- Beam Telescope from hadrontherapy (ex: GSI)
- Frascati Beam Telescope (0.05 % X0/plane)
 - adapted to 450 MeV electrons $\Rightarrow$
 - becoming part of facility equipment
- AIDA (EU-FP7)
 - Single Arm Large Area Telescope (SALAT)
 - 4 MIMOSA-28 sensors per plane $\Rightarrow$
 - $\ll 0.1\%$ X0 per plane
- Prototype of an inner tracker
 - reference requirements : BESIII upgrade
 - 3 layers (see LIU Quinyuan's talk)
 - 120 sensors thinned to $50\ \mu m$

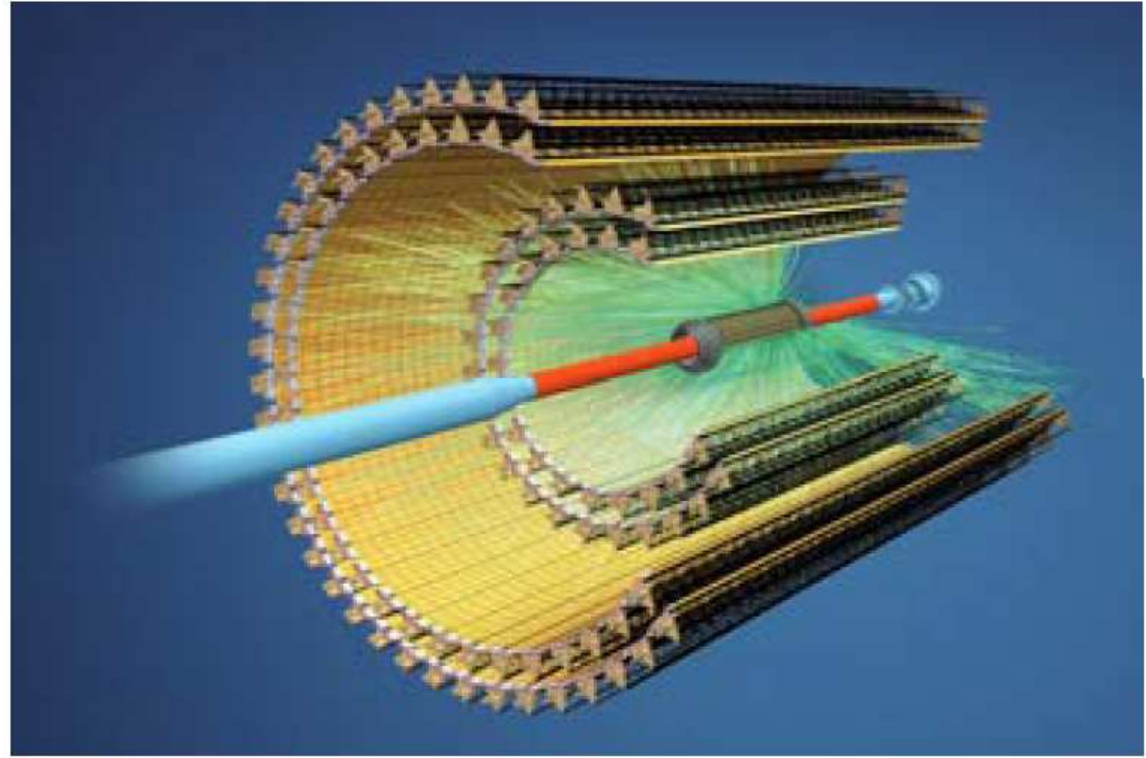
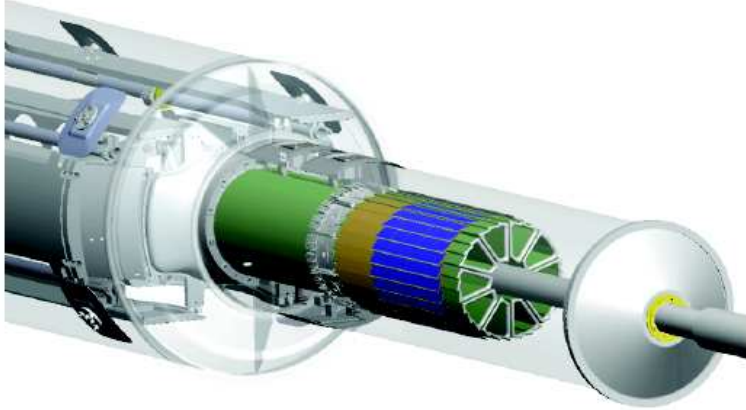


Next Step : Upgrade of ALICE-ITS

- ALICE Inner Tracking System (ITS) foreseen to be replaced during LS2/LHC
 - higher luminosity ($\equiv$ collision rate), improved charm tagging (see talk of G. Martinez)
- Expected improvement in pointing resolution and tracking efficiency



From STAR/RHIC to ALICE/LHC



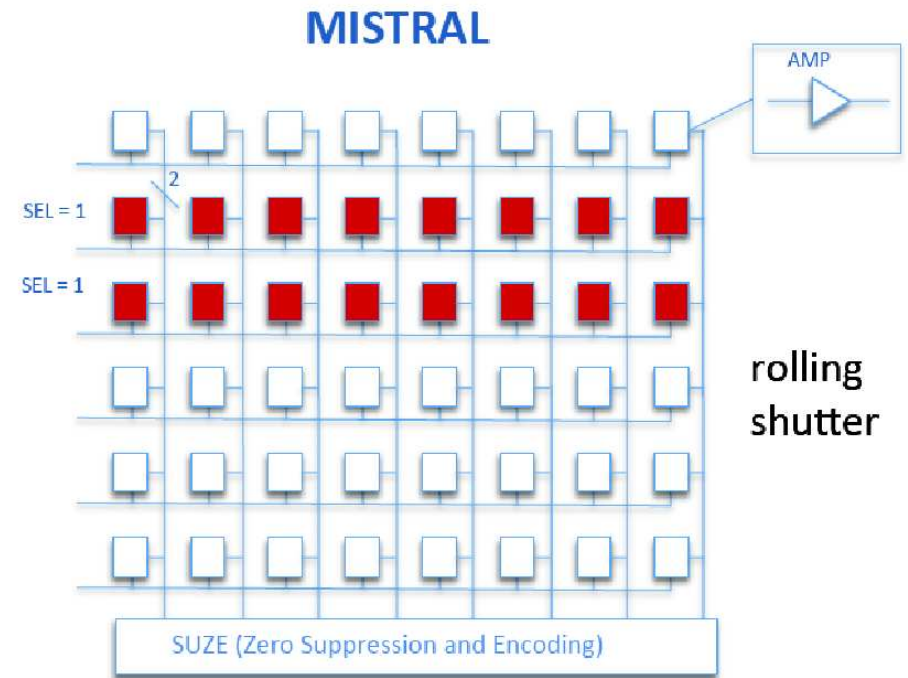
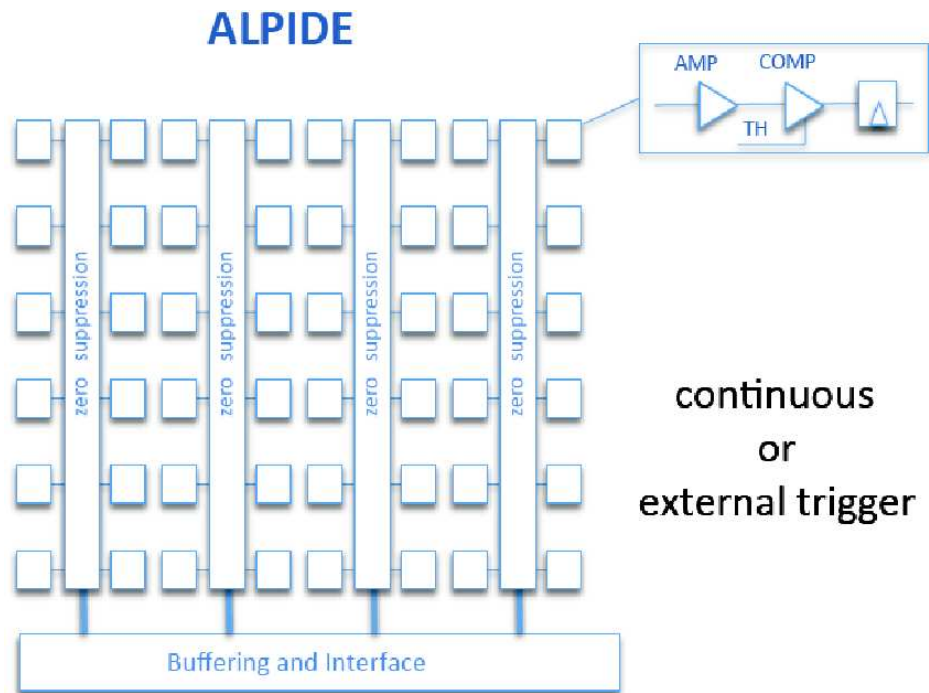
● CHALLENGES:

- nearly 100 times larger sensitive area : 400 sensors (0.15 cm^2) $\rightarrow$ $25 \cdot 10^3$ sensors ($> 10 \text{ m}^2$)
- ~ 10 times faster read-out
- somewhat higher radiation tolerance

$\Rightarrow$ investing a new CMOS fabrication process (imposed by requirements):

AMS- $0.35 \mu\text{m}$ (twin-well) $\rightarrow$ Tower- $0.18 \mu\text{m}$ (quadruple-well)

ITS Pixel Sensor : Two Architectures



Pixel dimensions $27\mu m \times 29\mu m$
Event time resolution $< 10\mu s$
Power consumption $< 50mW/cm^2$
Insensitive area $\gtrsim 1mm \times 30mm$
Nb(T) inside pixel ~ 200

Pixel dimensions $36\mu m \times 65\mu m$
Event time resolution $20\mu s$
Power consumption $\lesssim 90mW/cm^2$
Insensitive area $1.5mm \times 30mm$
Nb(T) inside pixel ~ 15

- Both chips have identical dim. (15mm x 30 mm) as well as physical and electrical interfaces:
 - * position of interface pads
 - * electrical signaling
 - * steering, read-out, ... protocols

Main Features of the Final Prototypes

- **Full scale sensor building block :**

- ✧ complete (fast) read-out chain $\simeq$ ULTIMATE
- ✧ pixel area ($\sim 1 \text{ cm}^2$) $\simeq$ area of final building block
- ✧ same nb of pixels (160,000) than complete final tracker chip
- ✧ fabricated with $18 \mu\text{m}$ thick high-resistivity EPI
- ✧ BUT : pixels are small ($22 \times 32.5 \mu\text{m}^2$) and sparsification circuitry is oversized (power !)
- ✧ **Tested at DESY (few GeV e^-) in June'15 and CERN-SPS (120 GeV "pions") in Oct. '15**

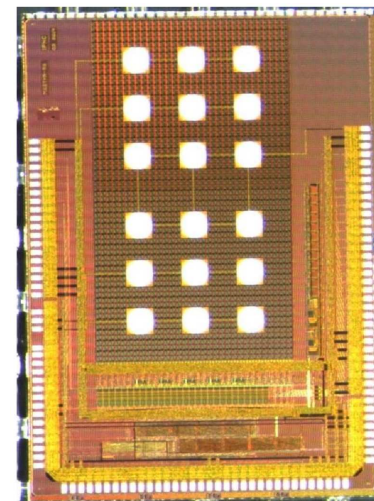
FSBB-M0bis



- **Large-pixel prototype without sparsification :**

- ✧ 2 slightly different large pixels :
 - $36.0 \mu\text{m} \times 62.5 \mu\text{m}$
 - $39.0 \mu\text{m} \times 50.8 \mu\text{m}$
- ✧ pads over pixels (3 ML used for in-pixel circuitry)
- ✧ fabricated with $18 \mu\text{m}$ thick high-resistivity EPI
- ✧ BUT : only $\lesssim 10 \text{ mm}^2$, 4,000 pixels, no sparsification
- ✧ **Tested in Frascati (450 MeV e^-) in March & May'15**

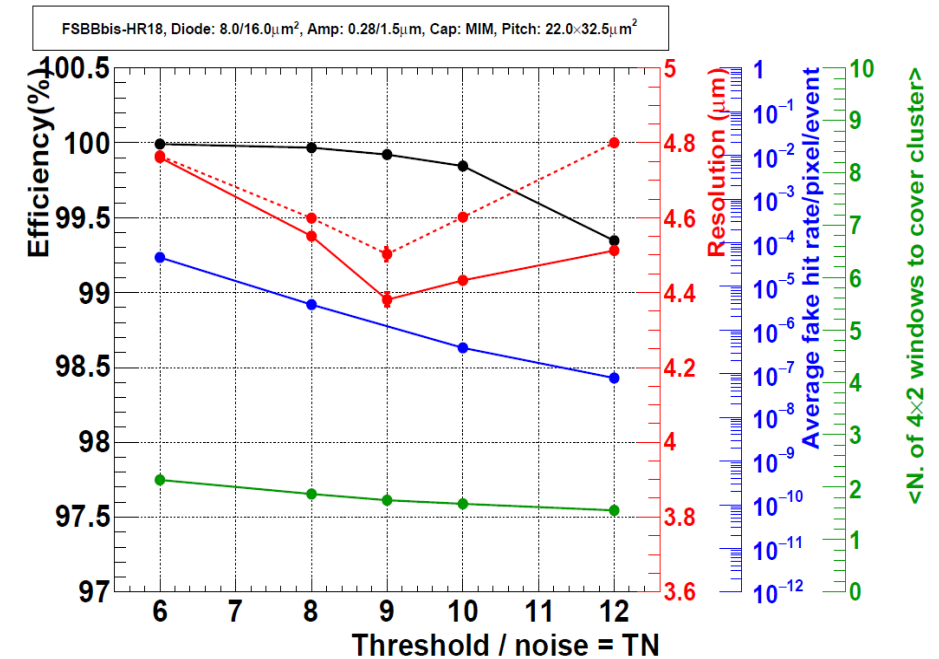
MIMOSA-22THRb



Detection Performances of the Final Prototypes

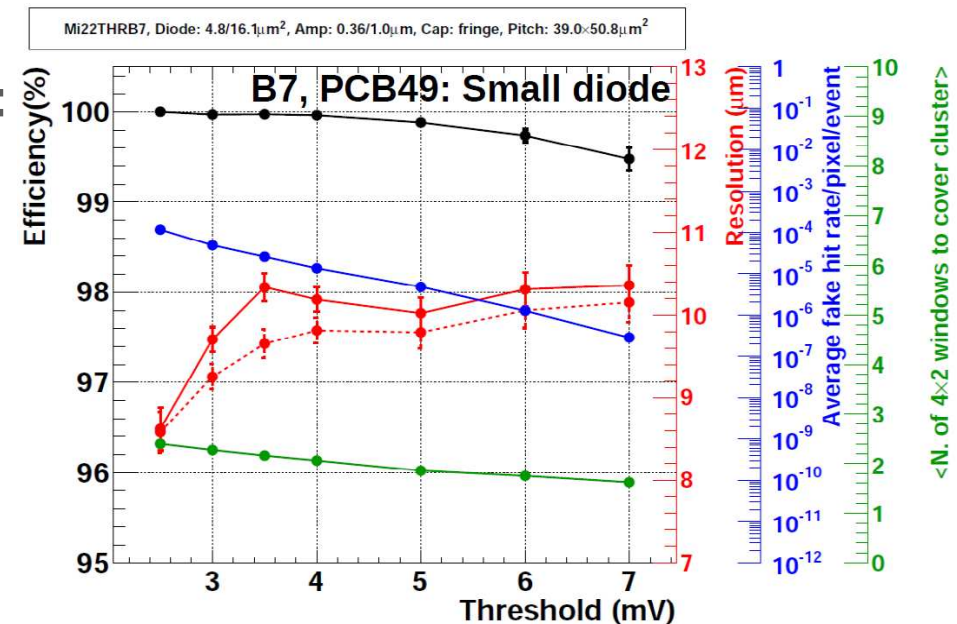
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Vertex Detector at CEPC

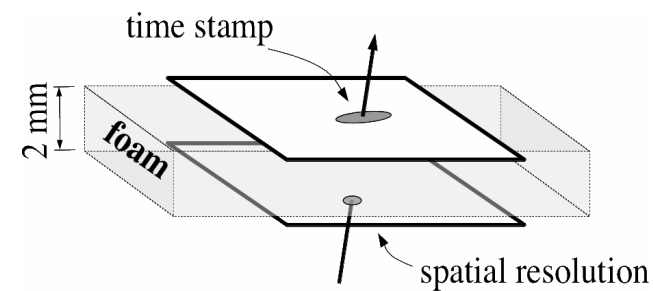
- Comparison between CEPC (240 GeV) and ILC (500 GeV) requirements
 - Physics performance driven requirements equivalent for both machines
 - Running conditions driven requirements may be similar (design dependent, still under study)
 - ↪ both machines induce beam related background in the detector dominating physics signal by several orders of magnitude

- Some typical requirements:

Detector	σ_{sp}	t_{int}	Dose (30°C)	Fluence (30°C)
ILD-VXD/In	$< 3 \mu m$	50/10 μs	< 100 kRad	$\lesssim 10^{11} n_{eq}/cm^2$
ILD-VXD/Out	$\lesssim 4 \mu m$	100 μs	< 10 kRad	$\lesssim 10^{10} n_{eq}/cm^2$

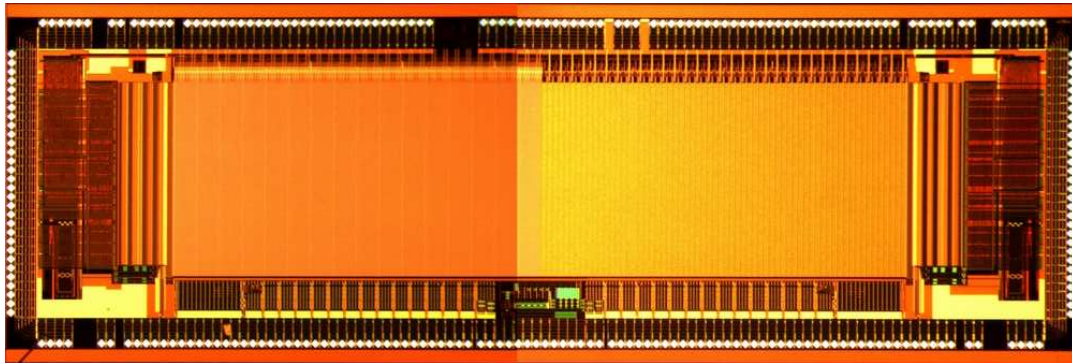
- Special attention: power < 50 mW/cm² (power cycling required ?)

Validation of CPS for ILD Vertex Detector

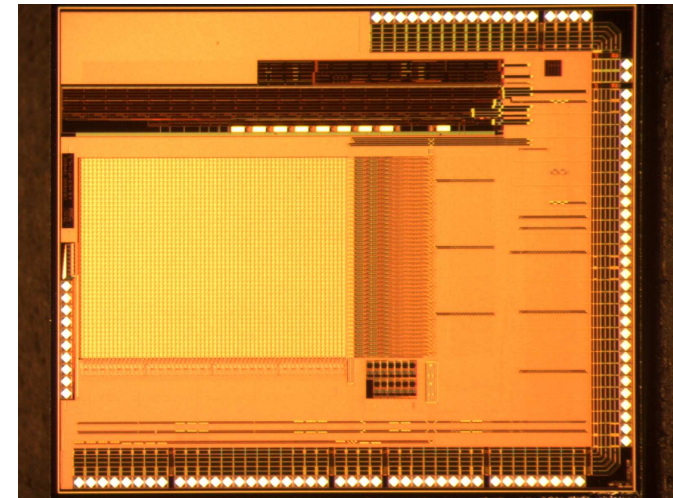


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- Medium-size proto. of each sensor fab. in AMS-0.35 μm process (2012)



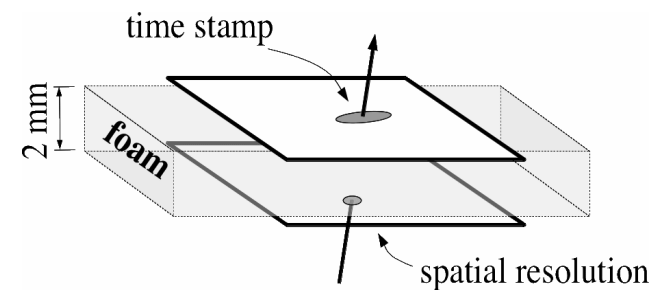
- ILD-VXD/In: accurate / swift



- ILD-VXD/Out: power saving

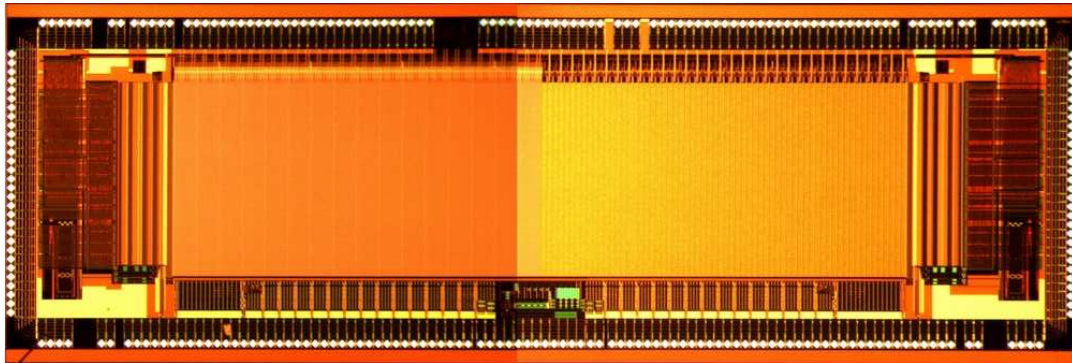
⇒ All measured performances comply with requirements

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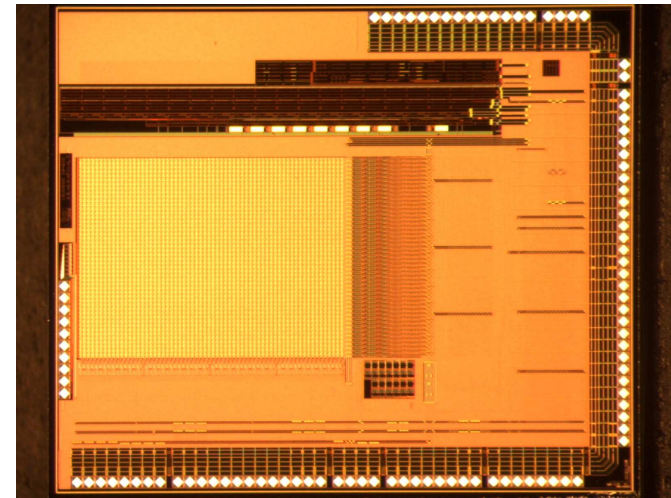


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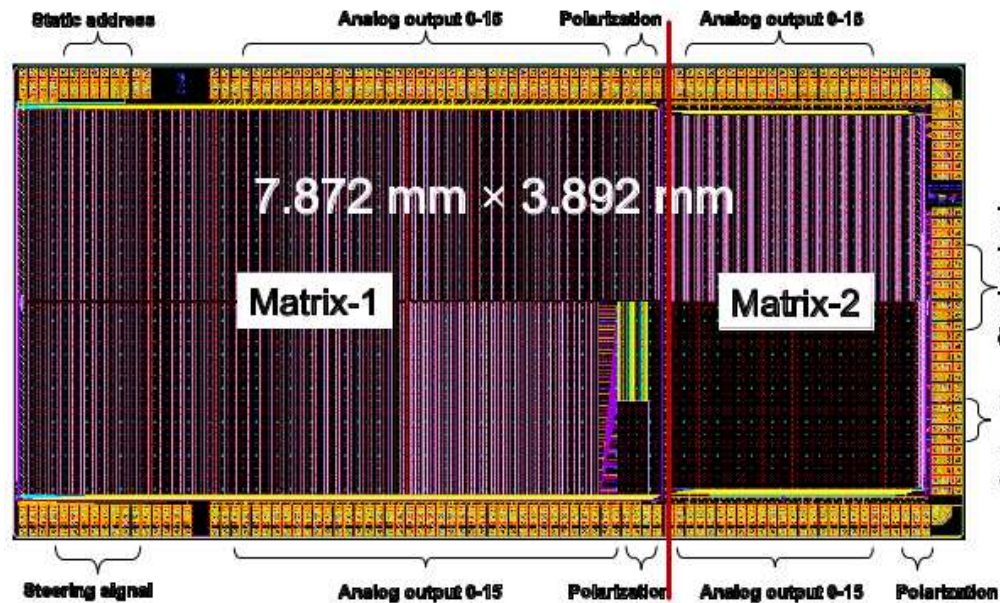
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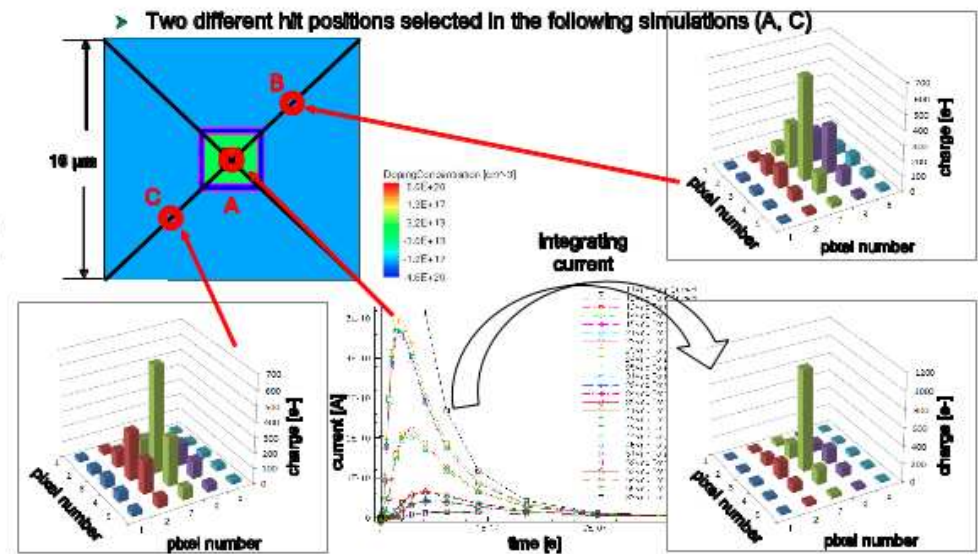
- BUT requirements provide little safety margin (lumi, BG), no track seeding, ...**

CPS for CEPC

- CMOS PIXEL SENSORS RETAINED FOR R&D WITH INITIAL FUNDING FROM IHEP :
 - 1st joint MPW submission with IPHC in Novembre 2015 → expected back in April'16
 - Goal: understand charge collection performances vs diode geometry & epitaxial-layer properties

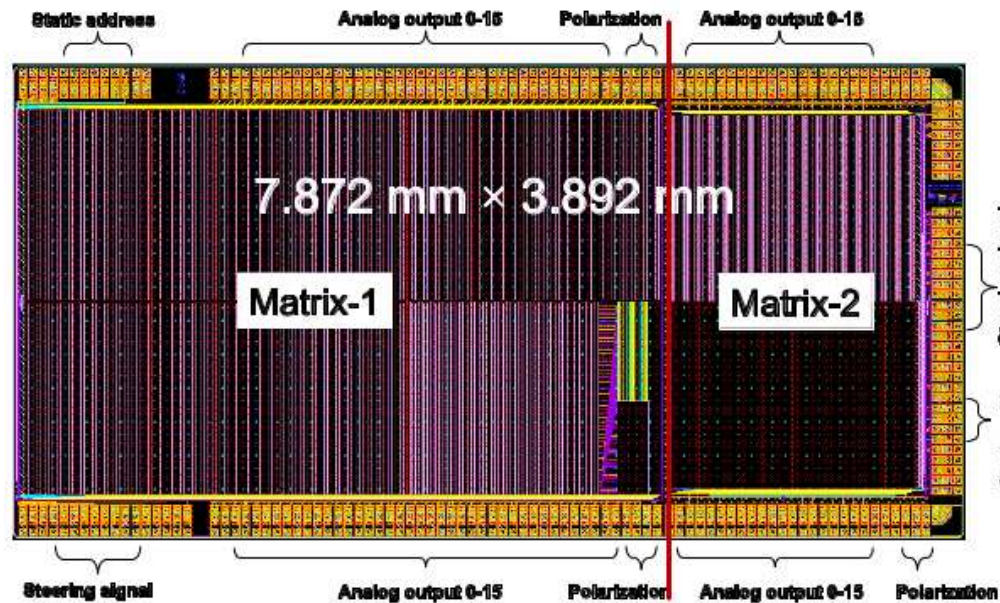


TCAD simulation

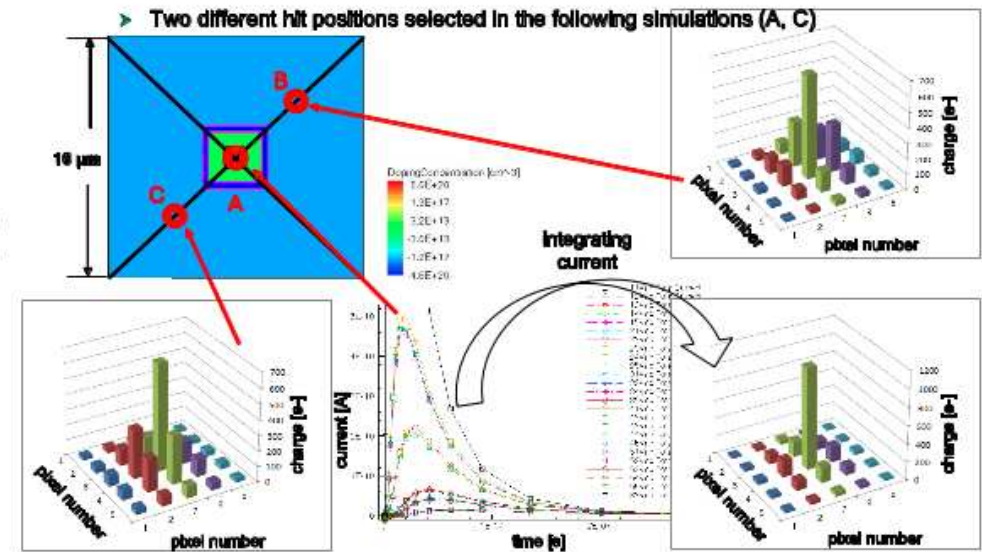


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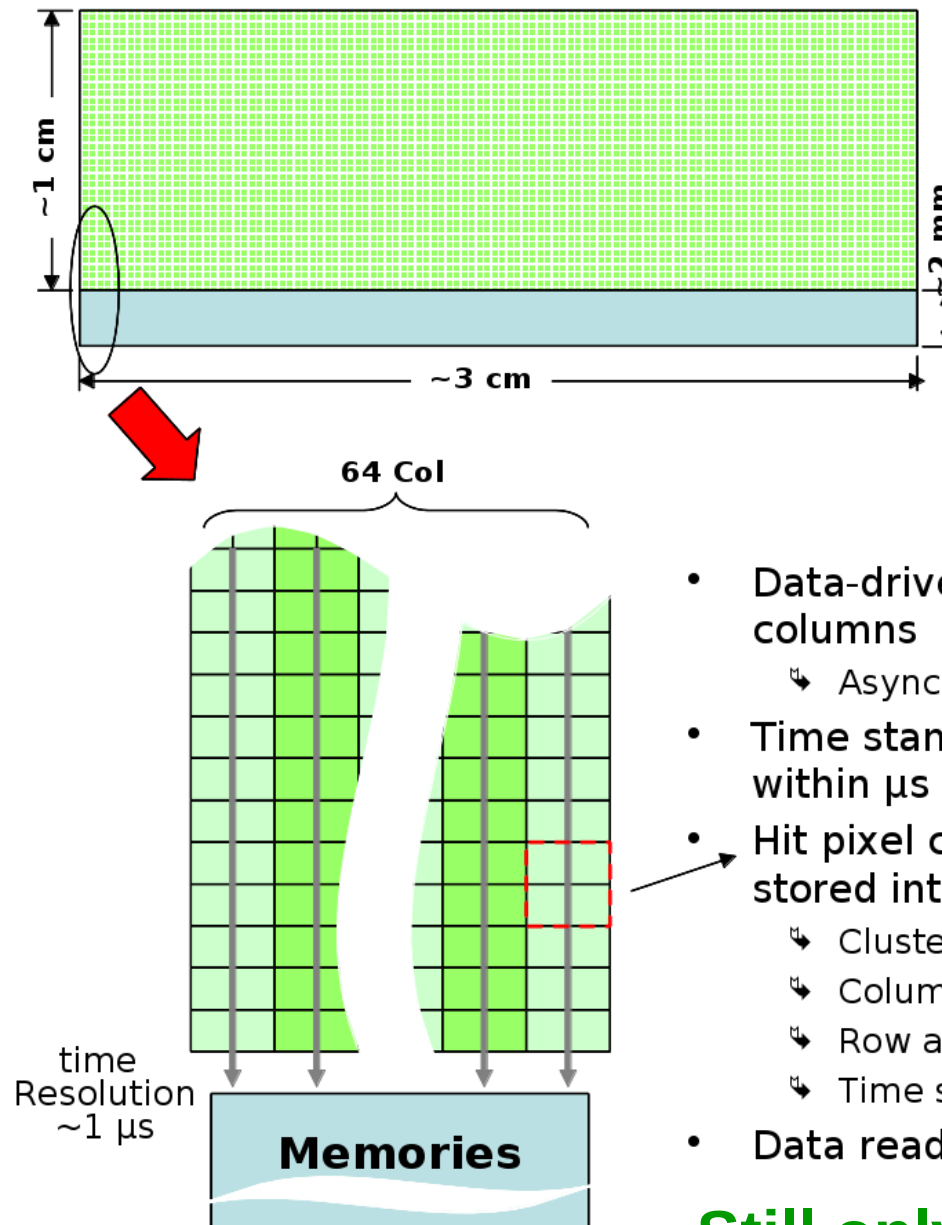


TCAD simulation



- Funding request sent to MOST for next steps
- Collaboration of 4 groups from IHEP, Shandong Univ., Wuhan and IPHC
- ALSO: EXPLORING THE TECHNOLOGY POTENTIAL FOR TRACKING SUB-SYSTEMS
 - large pixels $\rightarrow 10 \mu\text{m}$ resolution
 - $\ll 1\% X_0$ per layer

Noria Based CPS Architecture for ILC&CEPC Double&Single Bunch Id.



- Pixel dimensions $\sim 20 \times 20 \mu\text{m}^2$
 - ↳ $\sigma_{\text{sp}} \sim 3 \mu\text{m}$
- In-pixel amplification-shaping
 - ↳ integration time $< 1 \mu\text{s}$
- In-pixel digitisation
- Organised in N sub-matrices of 64×512 pixels

- Data-driven pixel readout in every pair of columns
 - ↳ Asynchronous readout
- Time stamp at the bottom of pixel array within μs
- Hit pixel clusters of each column pair are stored into memories (possibly after cluster selection)
 - ↳ Cluster format 2×2 pixels
 - ↳ Column address
 - ↳ Row address
 - ↳ Time stamp (structure)
- Data readout in a few ms after end of train

Still only a concept, not yet a design

SUMMARY - CONCLUSION

- **CPS tend to comply with an increasing range of applications privileging highly granular & thin (low power) pixel devices :**
 - ⇒ STAR-PXL, CBM-MVD1, ILD-VXD(500), ..., ALICE-ITS, ILD-VXD(1000)
(also attractive for large areas $\rightarrow$ cost, power)
 - ⇒ Architectures developed in AMS-0.35 μm CMOS process comply with present requirements of an ILC vertex detector (not including seed tracking)
- **Faster (low power) read-out** would alleviate vulnerability to unknowns associated to beam related background $\Rightarrow$ major motivation for further R&D in CPS, single bunch tagging being the ultimate (realistic) goal

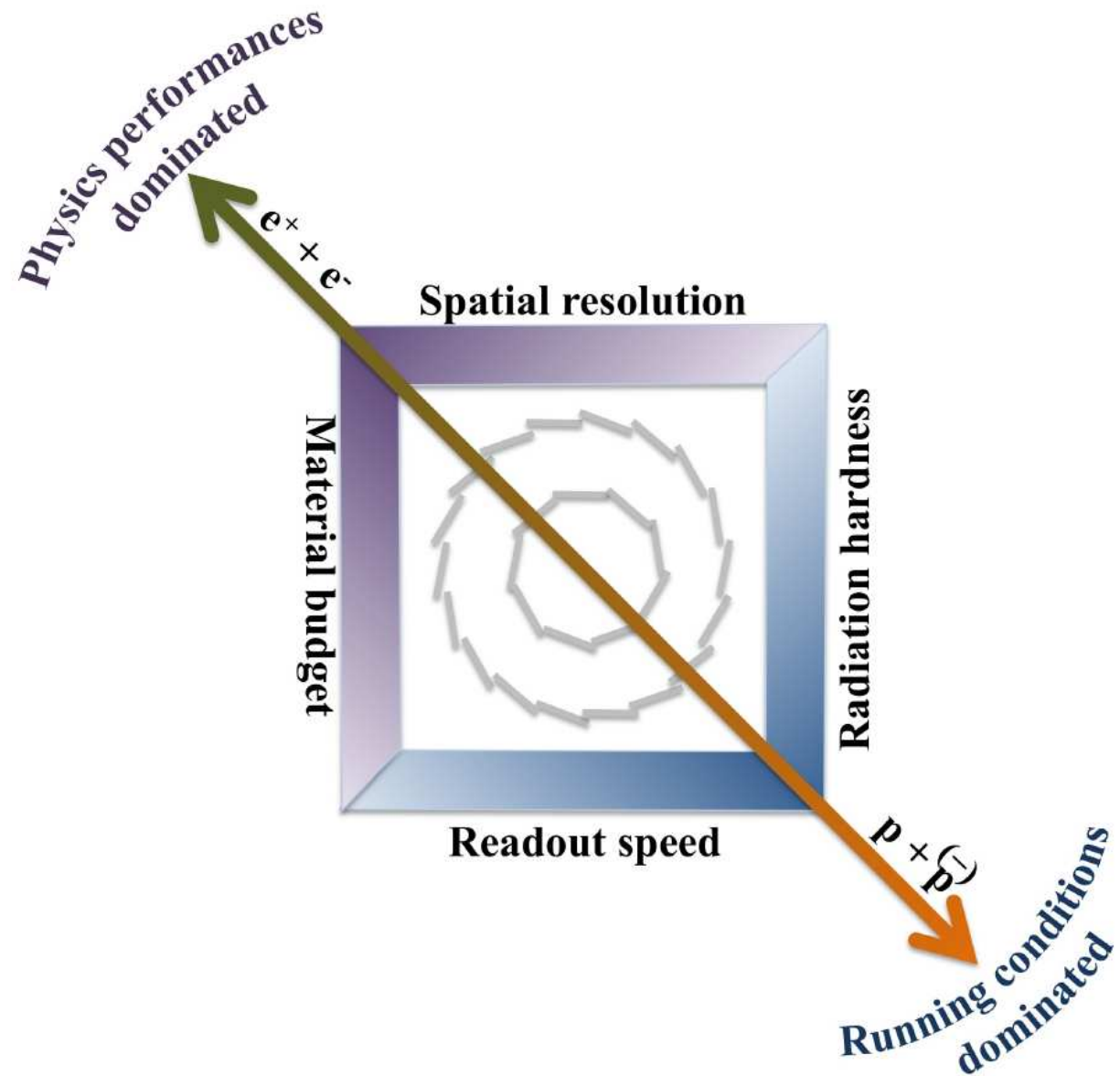
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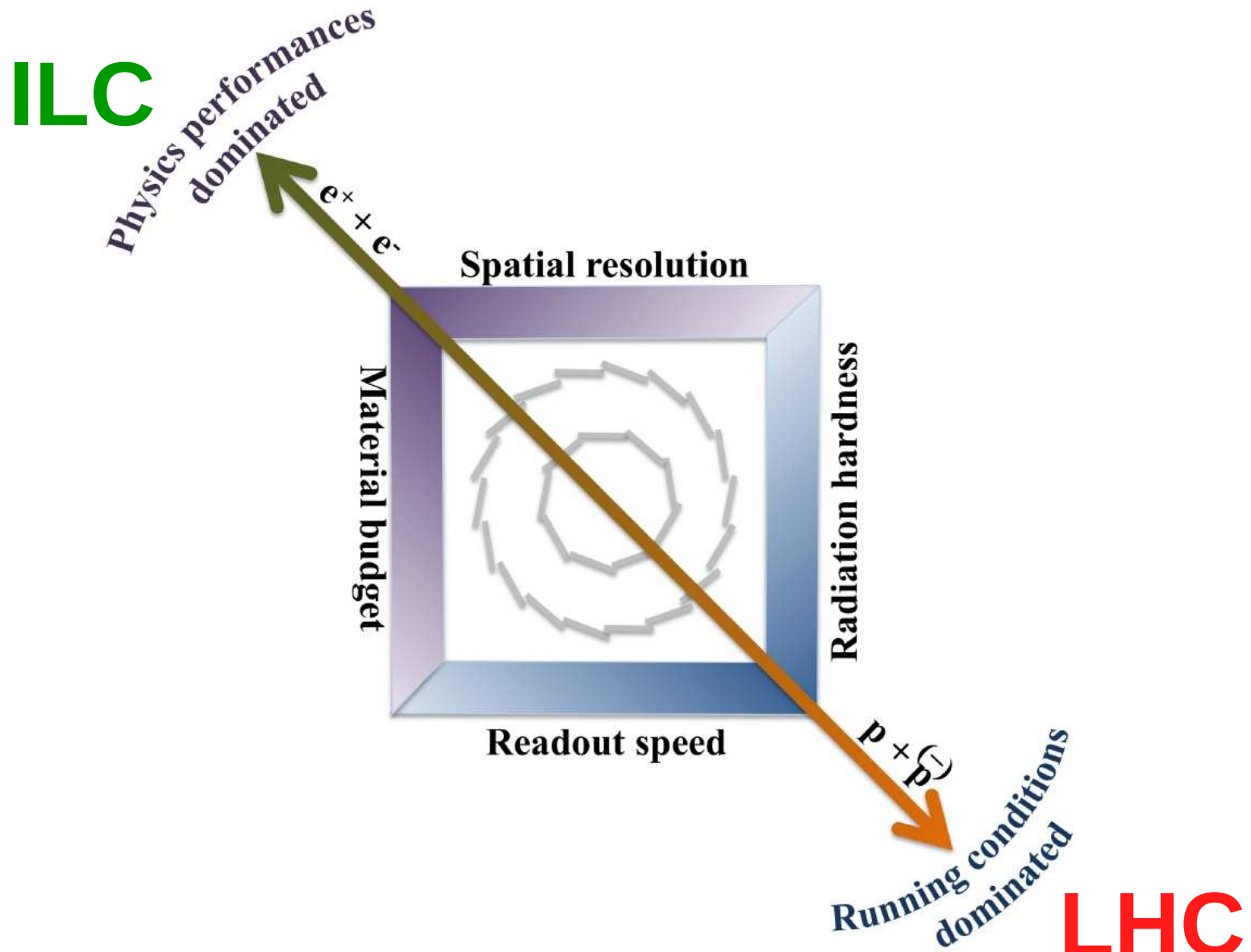
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- Numerous spin-offs expected: imaging (single photon counting), cancer therapy (beam monitor, on-line imager), ..., large scale soldering inspection, ...

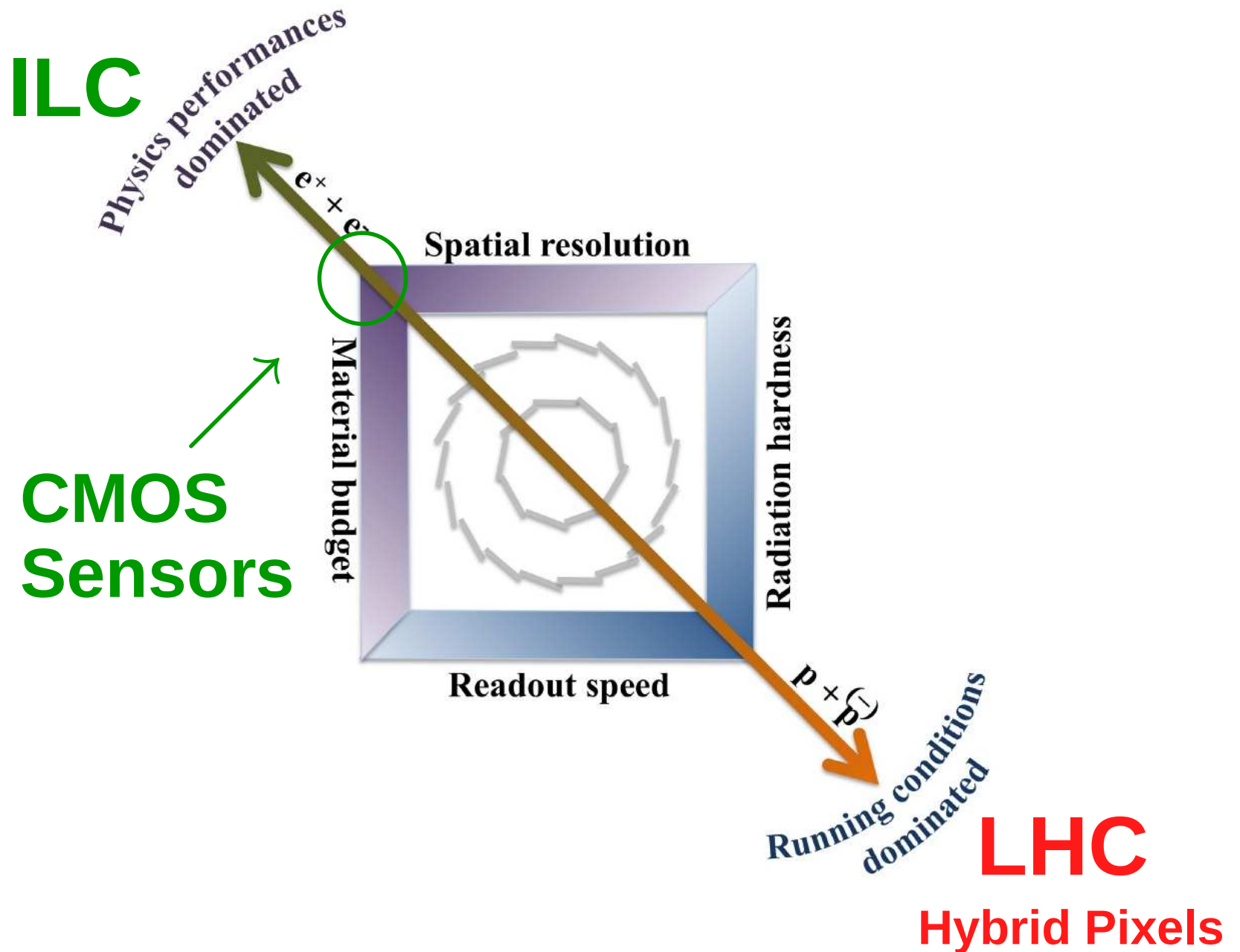
Motivation for High Precision CMOS Sensors



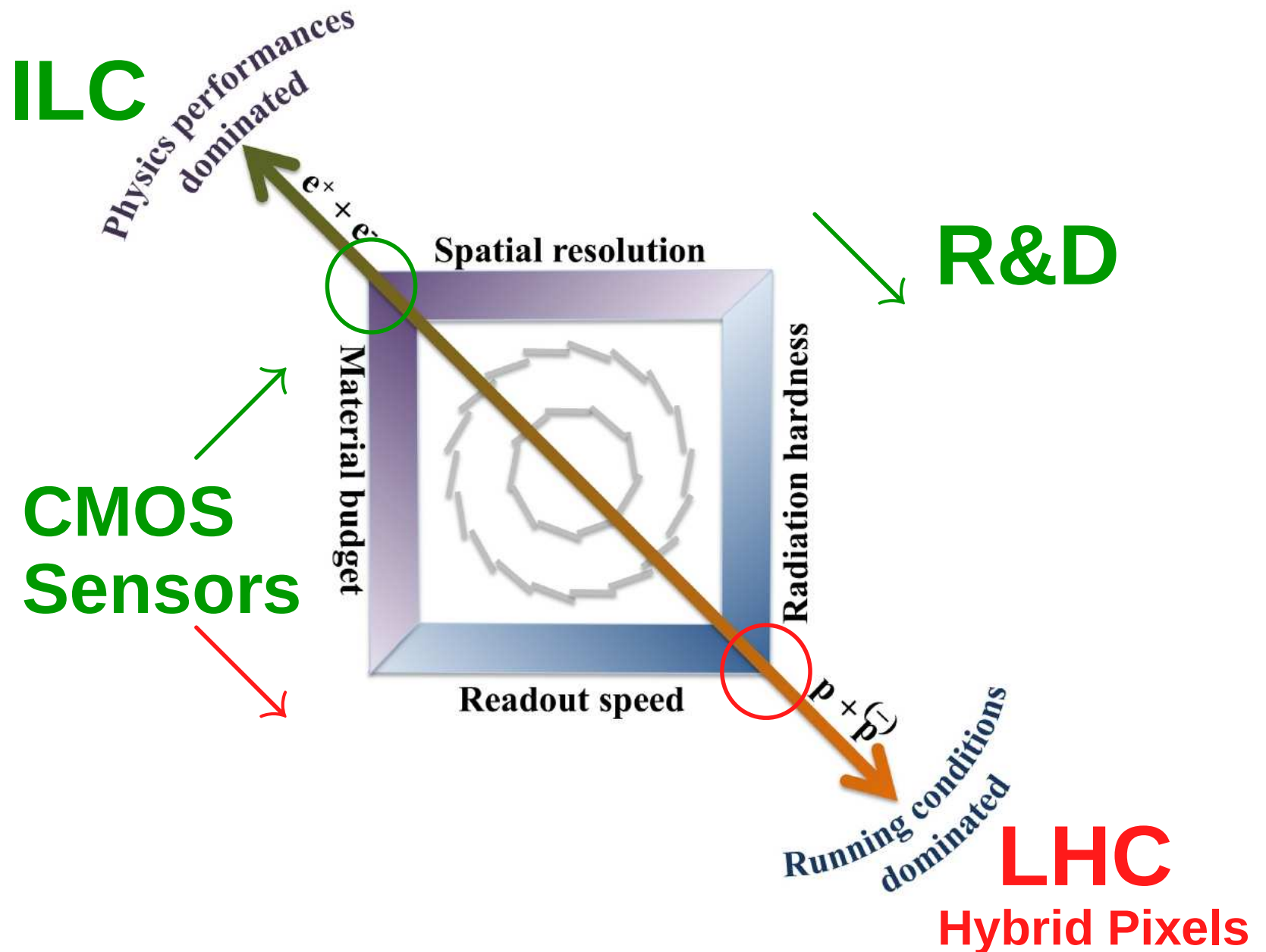
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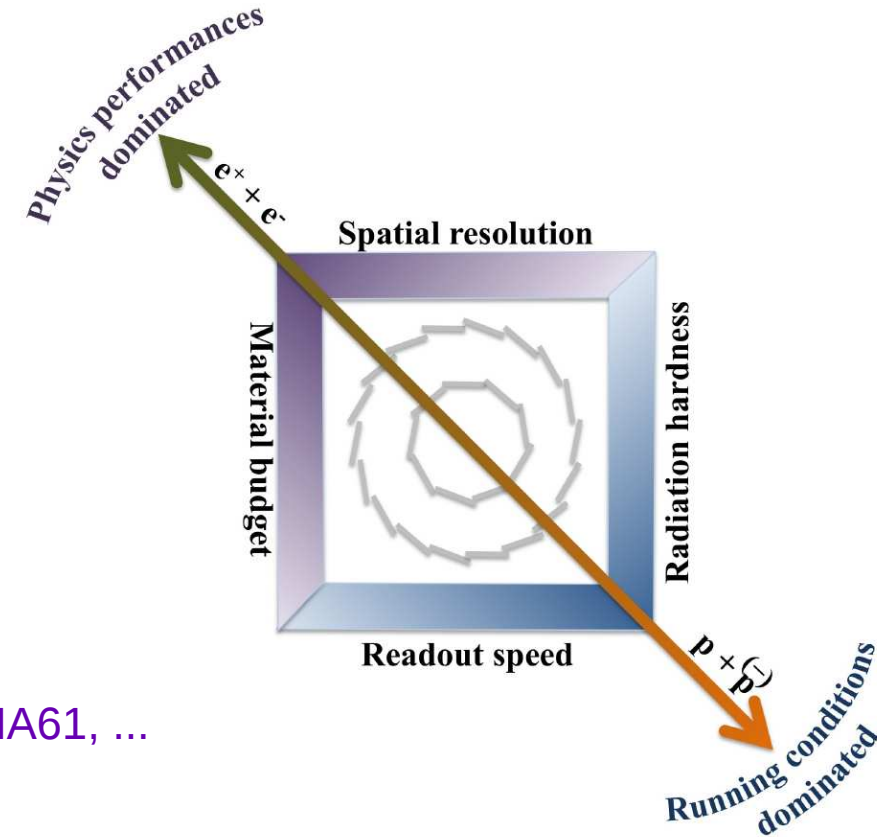
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Motivation for Developing CMOS Sensors

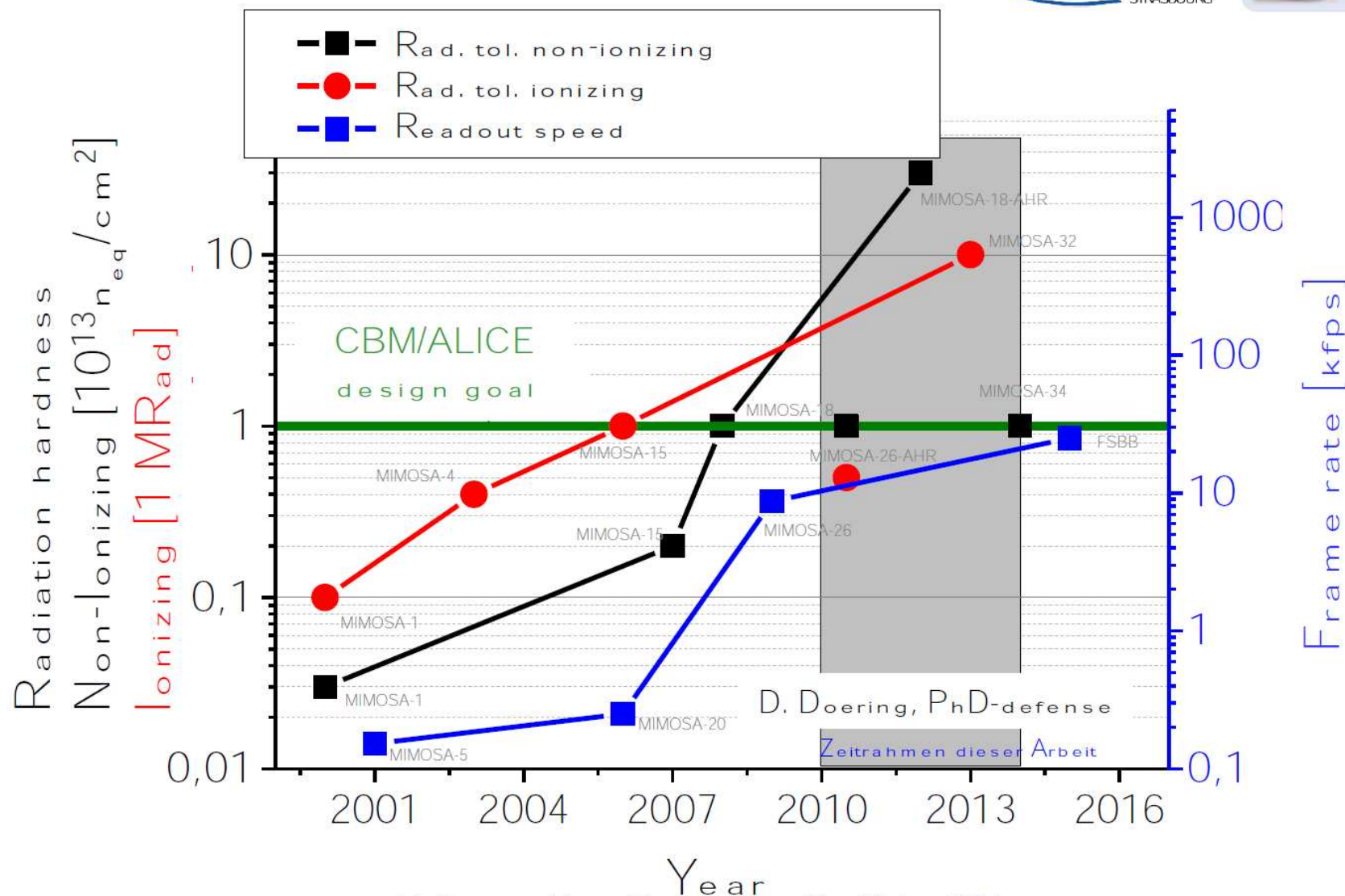
Quadrature of the Vertex Detector

- CPS development triggered by need of very high granularity & low material budget
- Applications exhibit much milder running conditions than pp/LHC
 - ⇒ Relaxed speed & radiation tolerance specifications
- Increasing panel of existing, foreseen or potential application domains :
 - Heavy Ion Collisions : STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
 - e^+e^- collisions : ILC, BES-3, ...
 - Non-collider experiments : FIRST, NA63, Mu3e, PANDA, ...
 - High precision beam telescopes adapted to medium/low energy electron beams :
 - ↪ few μm resolution achievable on DUT with EUDET-BT (DESY), **BTF-BT (Frascati)**, ...



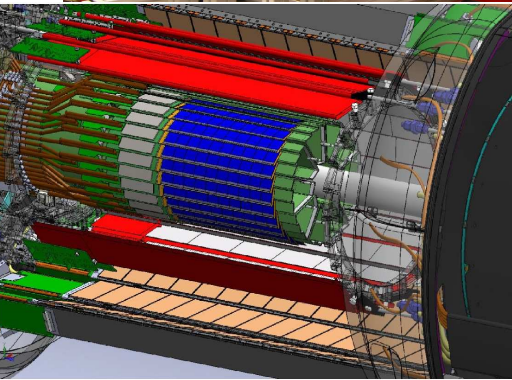
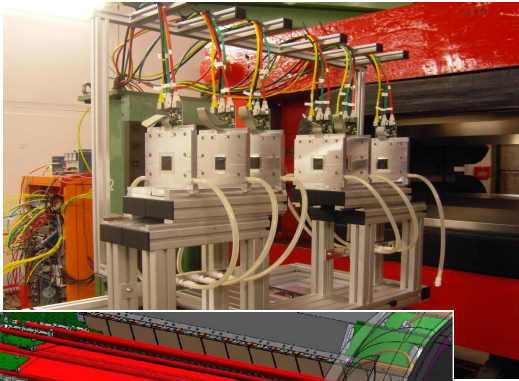
Radiation Tolerance

Material budget: $0.05\% X_0$
 Spatial resolution: $\sim 3\text{-}5\ \mu\text{m}$



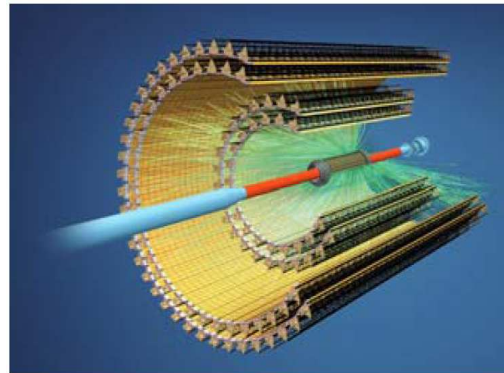
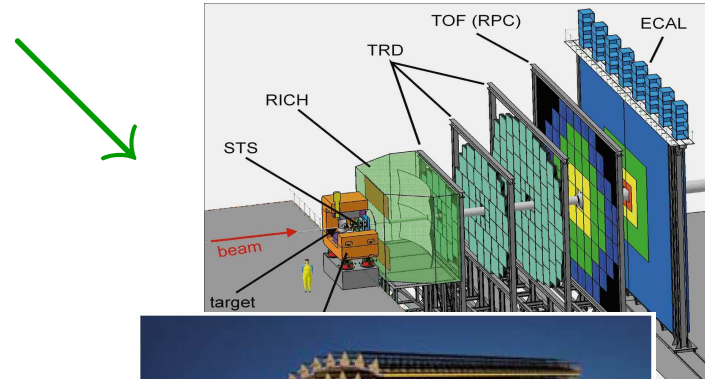
Improving Speed and Radiation Tolerance

$O(10^2) \mu s$

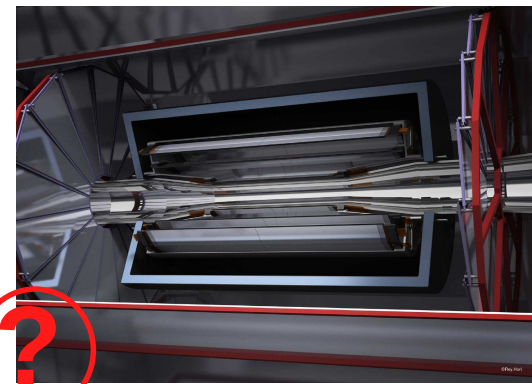


*How to improve speed & radiation tolerance
while preserving 3-5 μm precision & $< 0.1\%$ X_0 ?*

$O(10) \mu s$



$O(1) \mu s$



EUDET/STAR

2010/14



ALICE/CBM

2015/2019



?X?/ILC

$\gtrsim 2020$

Speed vs Pixel Dimensions

- Pixel dimensions govern the spatial resolution at the expense of read-out speed
 $\Rightarrow$ Trade-off to be found specific to each application

Pixel pitch	$< 10 \mu m$	$\gtrsim 15 \mu m$	$> 20 \mu m$	$\gtrsim 25 \mu m$	$\lesssim 50 \mu m$
Nb(T)	2–3	15	$\gtrsim 50$	$\gtrsim 200$	HV: few 10^2
$\sigma_{sp} [\mu m]$	$\lesssim 1 \times 1$	$< 3 \times 3$	$< 5 \times 5$	$\lesssim 5 \times 5$	$\gtrsim 10 \times 10$
$\Delta t [\mu s]$	10^3	$\lesssim 30/200$	$\gtrsim 10-15$	< 10	10^{-2}
Pre-Amp+Filter	Out	In-Pix	In-Pix	In-Pix	In-Pix
Discrimination	Out	Out	In-Pix	In-Pix	In-Pix
Sparsification	Out	Out	Out	In-Pix	In-Pix
Ex.(chip)	Mimosa-18	ULTIMATE/MISTRAL	ASTRAL	ALPIDE	HV-CMOS
Depleted	No	No	No	Yes	YES
CMOS Process	AMS-0.35	AMS-0.35/Tower-0.18	Tower-0.18	Tower-0.18	AMS-0.35/0.18
Ex.(appli.)	Beam Tele.	STAR-PXL/ALICE-ITS	ALICE-ITS	ALICE-ITS	LHC ?

Sensor Development Organisation

MISTRAL RO Architecture ASTRAL RO Architecture Diode + in-pixel amplification Optimisation

