OMEGA microelectronics Overview 2015

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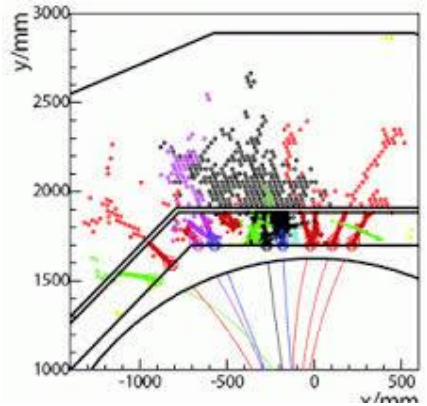
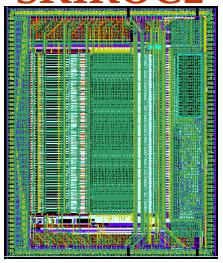
http://omega.in2p3.fr

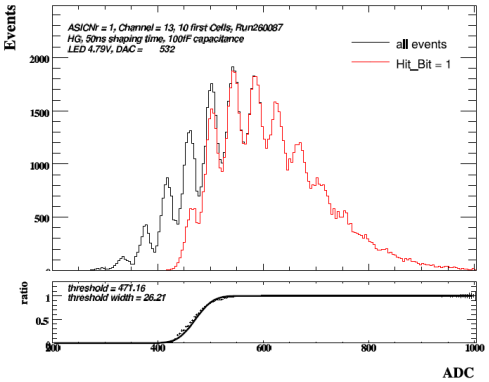
Organization for Micro-Electronics desiGn and Applications

- R&D on imaging calorimetry
  - Particle Flow Algorithms [Brient, Videau]
  - Electronics crucial (low noise, low power, fully integrated)
  - Several innovative features (power pulsing, SiPM…)
  - Validation of technological prototypes
  - Worldwide collaboration

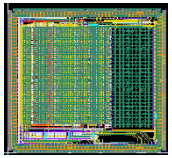


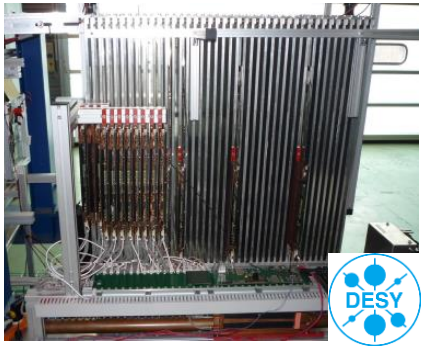
SKIROC2

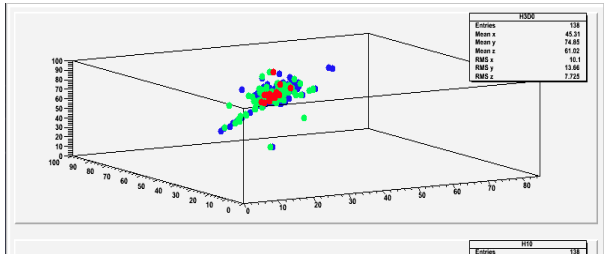




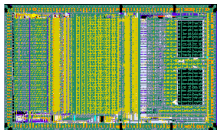
SPIROC2



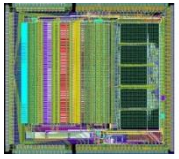




HARDROC2

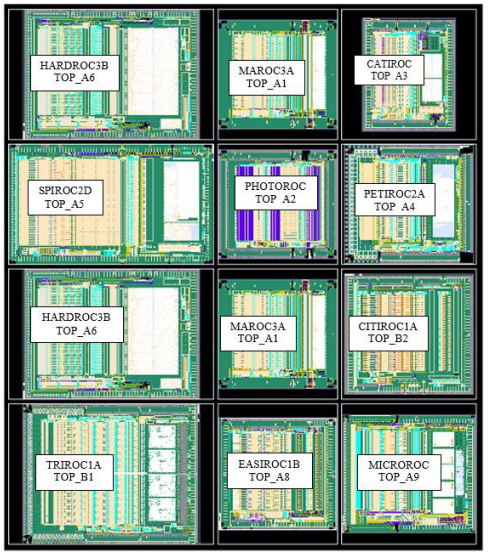


MICROROC



Production Run : Feb 2015

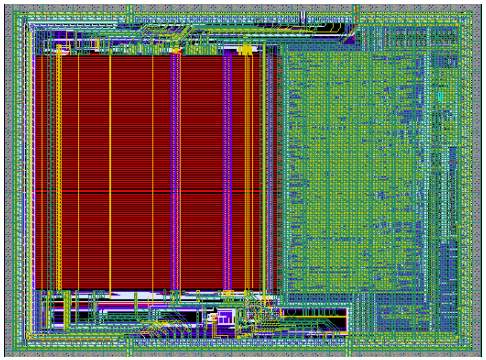
- 10 chips submitted feb 2015 (~250 k€)
  - Masks : 140 k€
  - 6 wafers : 30 k€
  - Découpe, transport… : 20 k€
  - + Packaging : 60 k€, tests…
  - Manpower ~4 FTE = 300 k€



chip	resp	cost	#chips	cost /chip		experiment	funding	IN2P3 user	ext user
CATIROC	Gisèle	14 360 €	360	39,89		JUNO/LHAASO	R&D	APC, IPNO	IHEP
CITIROC1A	Stéphane	14 360 €	360	39,89		CTA	WEEROC	IMNC	INAF
EASIROC1B	Ludovic	13 986 €	360	38,85		E40 KEK	RPB		KEK
HARDROC3A	Frédéric	44 875 €	720	62,33		CALICE DHCAL	AIDA+IPNL	IPNL	
MAROC3A	Sylvie	26 327 €	720	36,56		JUNO, CLAS12	RPB	APC, IPHC	INFN
MICROROC1	Nathalie	15 258 €	360	42,38		CALICE DHCAL	LAPP	LAPP	Weissman
PETIROC2A	Nathalie	14 360 €	360	39,89		medical + muons	R&D	IPNL,LPCF	
PHOTOROC	Damien	12 066 €	360	33,52		valo	RPB	LLR	
SPIROC2D	Ludovic	20 568 €	360	57,13		CALICE AHCAL	DESY+AIDA	LLR	DESY, KEK
TRIROC1A	Salleh	23 840 €	360	66,22		TRIMAGE	WEEROC		INFN
Total		200 000 €	4320	46,30					

CALICE à OMEGA en 2015

- **Fabrication de HARDROC3B (sDHCAL)**
  - Premier ASIC de 3ème génération pour ILC : final specs
  - AIDA1 WP9 milestone
  - 600 chips produits pour le démonstrateur de l'IPNL
  - Coût : 60 k€ (18 k€ IPNL + 32 k€ AIDA1 + 10k RPB)



- **Fabrication de SPIROC2D (AHCAL)**
  - 300 chips produits pour le AHCAL testbeam module at DESY
  - Coût : 30 k€ (23 k€ DESY + 7 k€ AIDA1)

- **Report fabrication de SKIROC2A (ECAL) (pas de financement)**
  - ~200 SKIROC2 chips provided to CMS HGCAL

- **Budget**
  - Reçu 3 k€ IN2P3
  - Dépensé (en plus des chips) : 18 k€ =12 k€ missions +6 k€ materiel
  - 2.1 FTE (Stéphane, Frédéric, Ludovic, Nathalie)

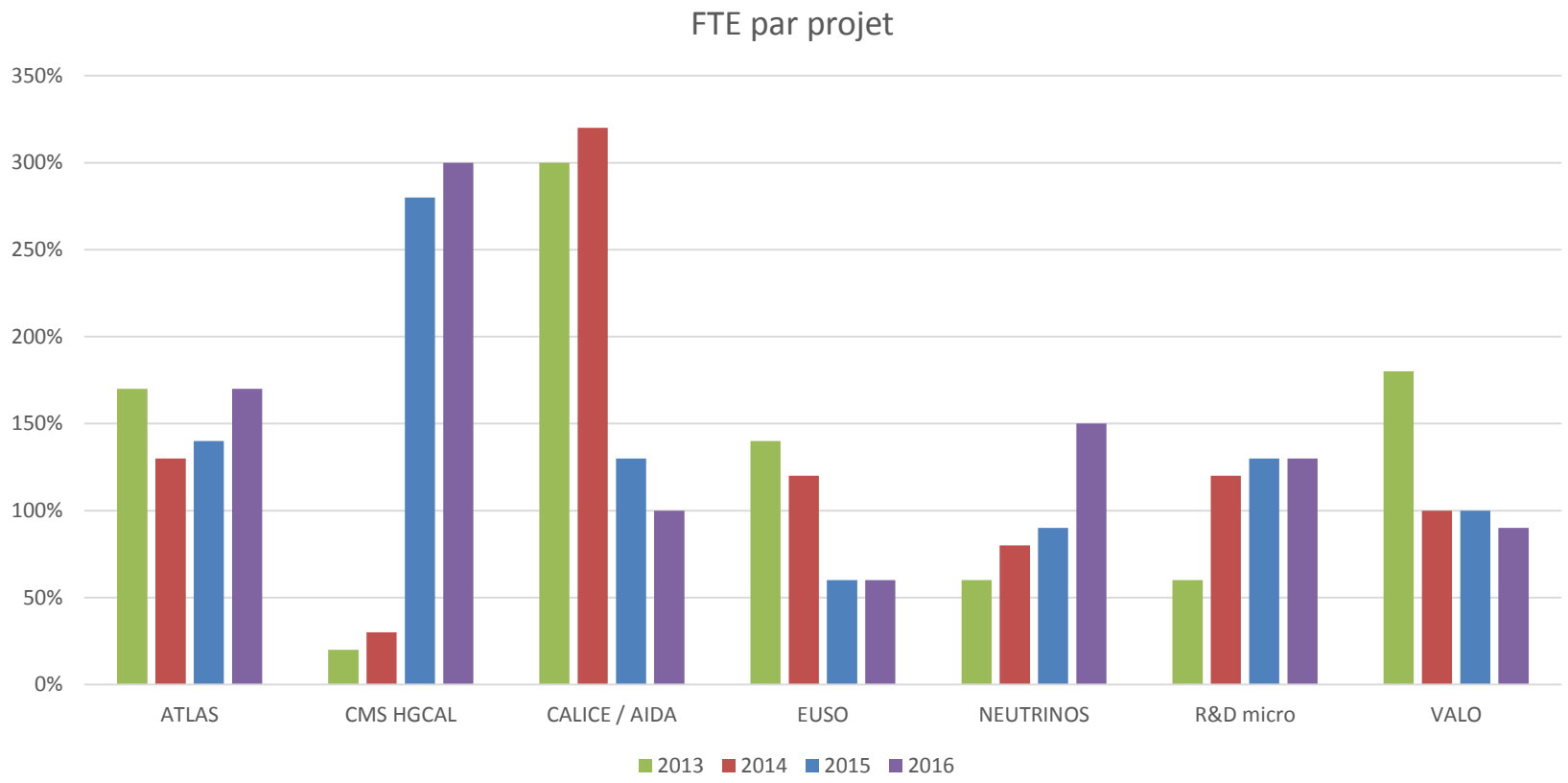
AIDA2020 WP4 microelectronics

- WP Coordinators: Christophe de la Taille, Valerio Re
- Goal : provide chips and interconnections to detectors developed by other WPs

- Task 1: Scientific coordination (CNRS-OMEGA, INFN-UNIBG)
- Task 2 : 65 nm chips for trackers (CERN)
  - Fine pitch, low power, advanced digital processing
  - Deliverable : full wafers for task 4 (cost ~1M$)
- Task 3 : SiGe 130nm for calorimeters/gaseous (CNRS-OMEGA)
  - Highly integrated charge and time measurement
  - Deliverable : SPIROC3 for WP12 and PETIROC3 fro WP13
  - Selection of technology in 2016.
- Task 4 : interconnections 65 nm chips /pixel sensors (INFN)
  - TSVs in 65 nm CMOS wafers, bonding of 65 nm chips to sensors, exploration of fine pitch bonding processes

Plan de charge 2016

- Consolidation LHC phase 2
- Evolution à étudier en astro/neutrinos



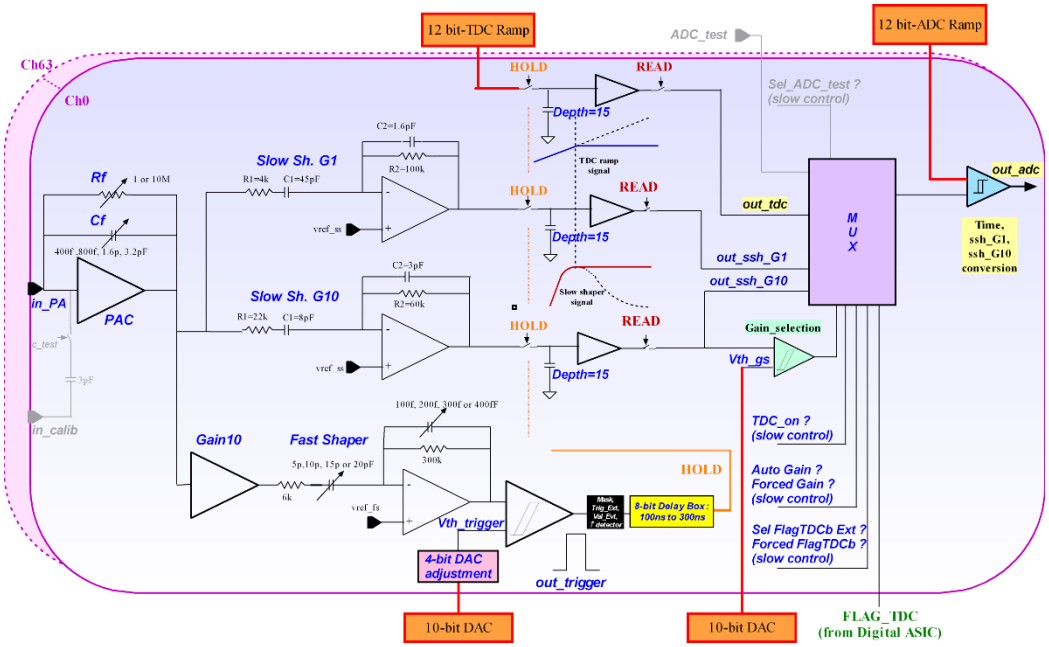
CALICE 2016

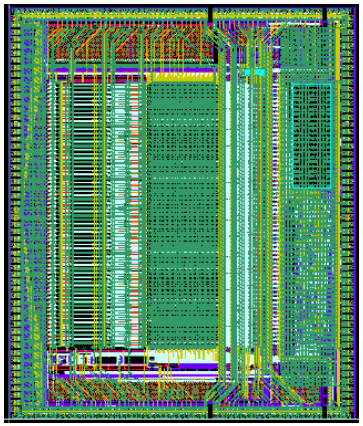
- Activité fortement réduite
  - Pas de financement à part AIDA2020 (SPIROC3)
  - Tester d'abord la 3ème génération (HARDROC3 sDHCAL IPNL)
  - Possible évolution de technologie (65/130 nm or SiGe)

- Demande 2016 :
  - Soutien aux activités testbeam du sDHCAL (5 k€ missions)
  - Participation au CALICE management (electronics coordination) : 3 k€
  - Possible production d'un SKIROC2A avec CMSHGCAL

HGCAL tests for electronics

- Development of a SKIROC2A for CMS
  - Optimized version for CMS testbeam, pin to pin compatible
  - Dual polarity charge preamplifier
  - Faster shapers (25 ns instead of 200 ns)
  - 40 MHz circular analog memory, depth= 300 ns
  - TDC (TAC) for ToA and ToT , accuracy : ~50 ps
  - Submission end 2015 SiGe 350nm
- Will replace SKIROC2 on modules for timing studies



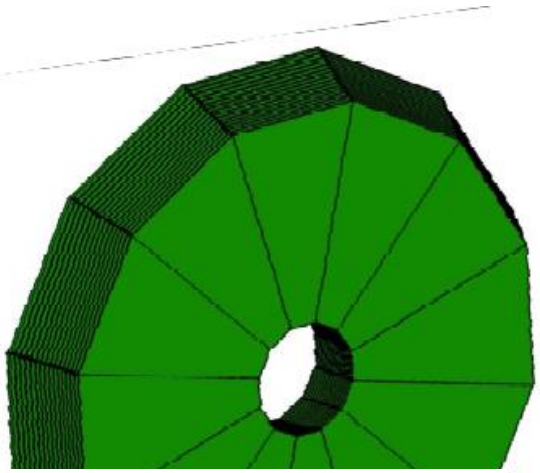


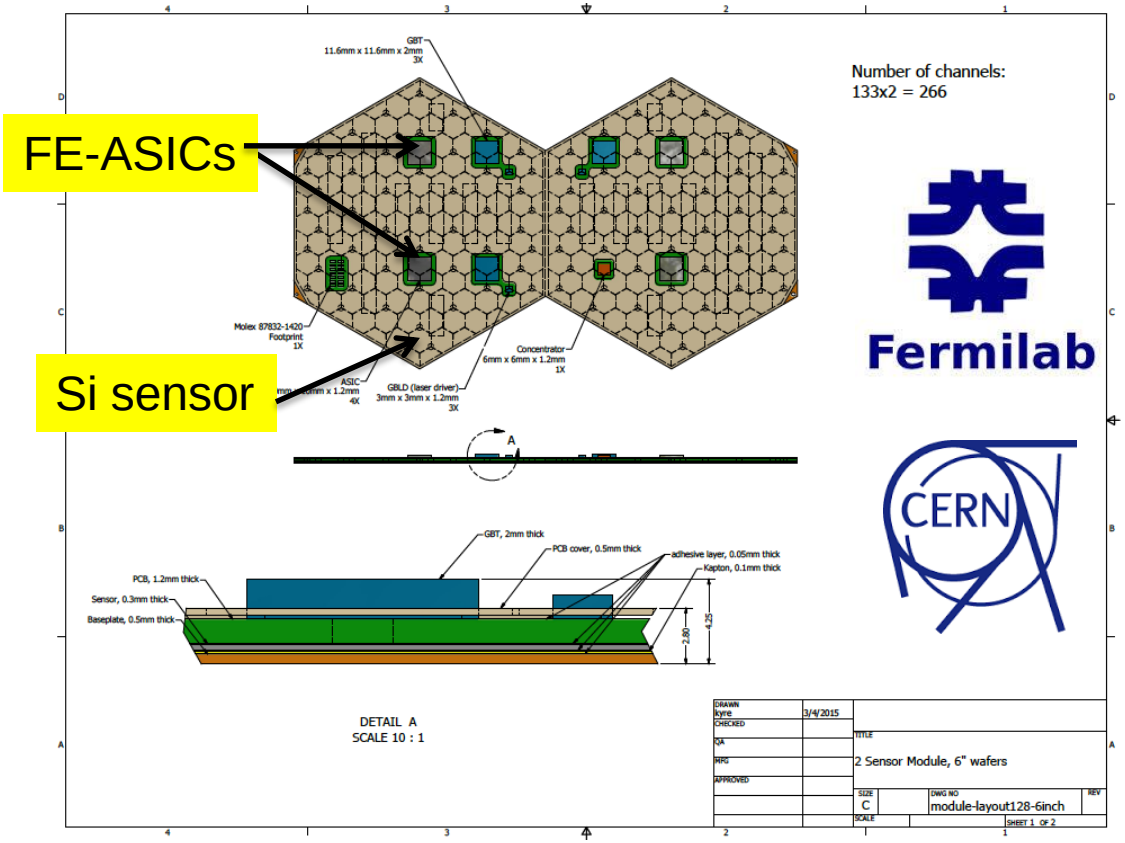
SKIROC2

Backup

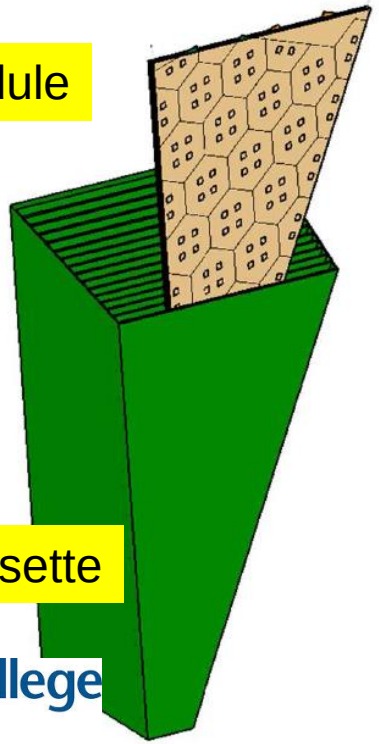
Detector overview

- Stringent requirements for Front-End Electronics
  - Low power (few mW), low noise (<2000 e-)
  - High radiation (200 Mrad, $10^{E}16$ N)
  - System on chip (digitization, processing…)
  - High speed readout (5-10 Gb/s)





Module



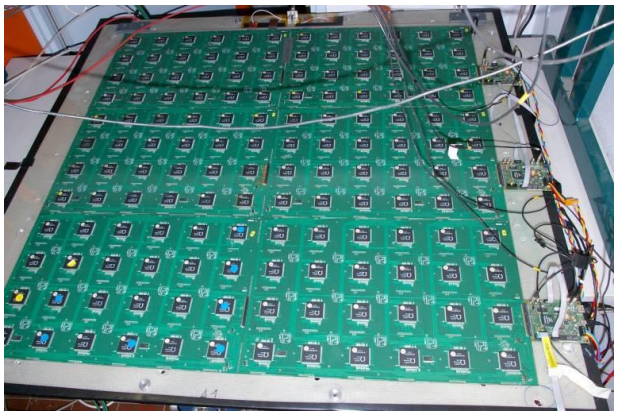
Cassette

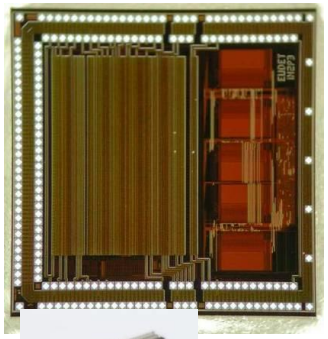
Imperial College London

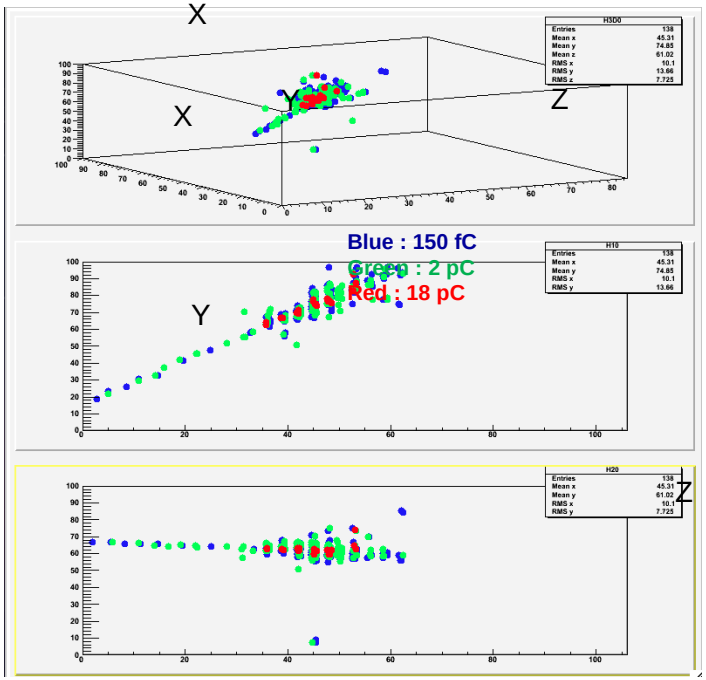
HARDROC2 for RPC readout

- **HARDROC2: 64 channels (RPC DHCAL)**
  - preamp + shaper+ 3 discris (semi digital readout)
  - Auto trigger on 10fC up to 20 pC
  - 5 0.5 Kbytes memories to store 127 events
  - Full power pulsing => 7.5 µW/ch
  - Fully integrated ILC sequential readout
  - 10 000 chips produced to equip 400 000 ch
  - SDHCAL technological proto with 40 layers (5760 HR2 chips
    - Successful TB in 2012 : 40 layers with Power Pulsing mode

Cosmic hadronic shower



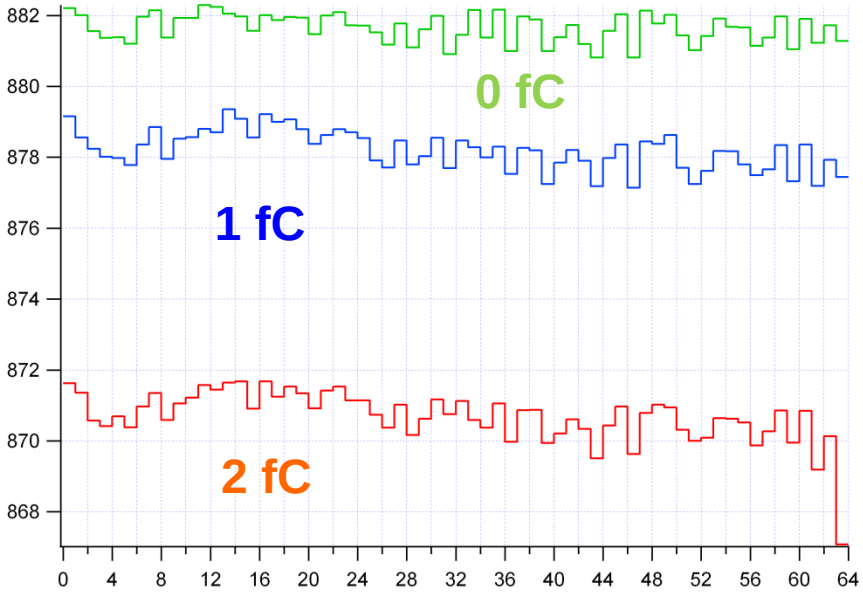




Variant: MICROROC

MICROROC: 64 channels for µMegas (DHCAL ILC)

- ❑ Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- ❑ Noise: **0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- ❑ Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- ❑ **HV sparks protection**
- ❑ 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m2 in TB



@LAPP Annecy

1m2 equipped with 144 MICROROC

SKIROC : SiECAL chip

- 64 ch Si readout chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits
  - Time measurement 1 ns