R&D autour d'un Si-W ECAL

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Grant ANR-2010-0429-01

Time line

Physics prototype

Technological prototype

ILD@ILC ; CMS@LHC ; x@CPEC ; WAGASCI@T2K ?

Proof of concept

- Linearity
- Resolution
- Sensors
- Very front-end

1500 channels/dm^3

Feasibility of design options

- Compactness
- Granularity
- Front-end
- Low Power (power pulsing)
- 2m Long SLAB

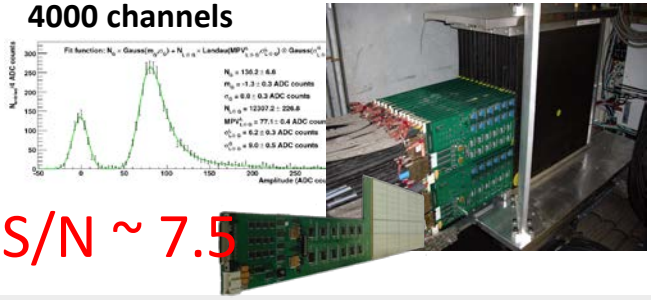
5000 channels/dm^3

Construction

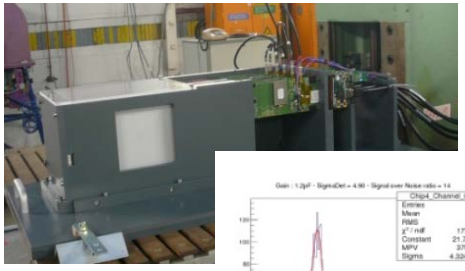
- Integration
- Environement
- Services
- Industrialization
- Tooling
- Project org.

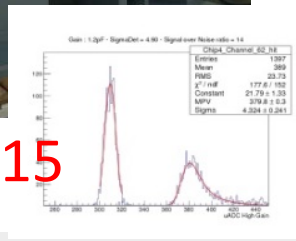
...10000 channels/dm^3

2004-2008
30 layers
4000 channels



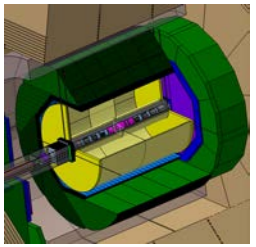
S/N ~ 7.5



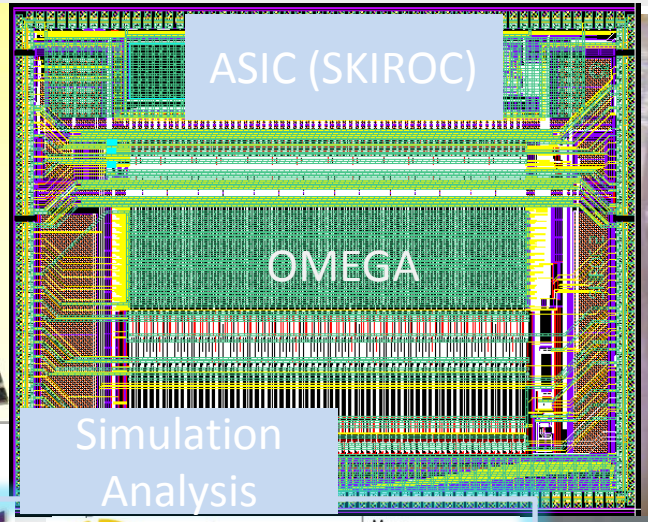


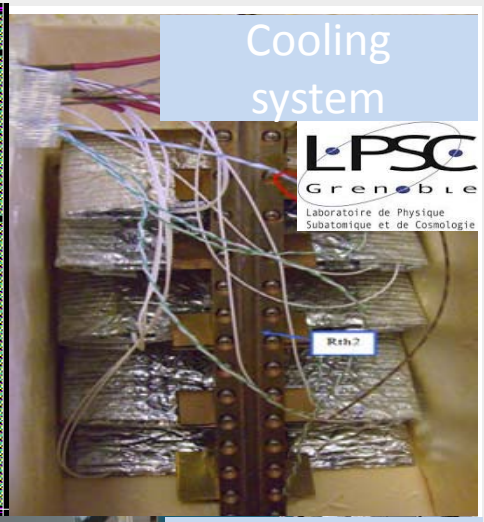
S/N ~ 15

~24 X0, 20 cm thick
~2500 m^2 active detectors
~100M readout channels

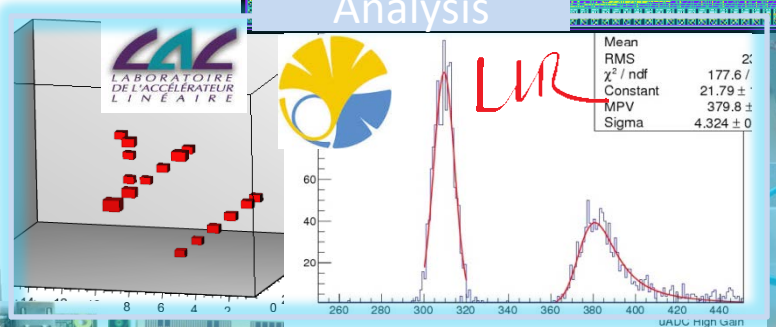


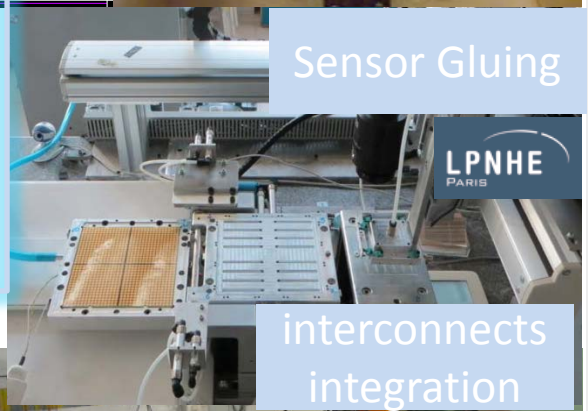
Prototyping : who is doing what

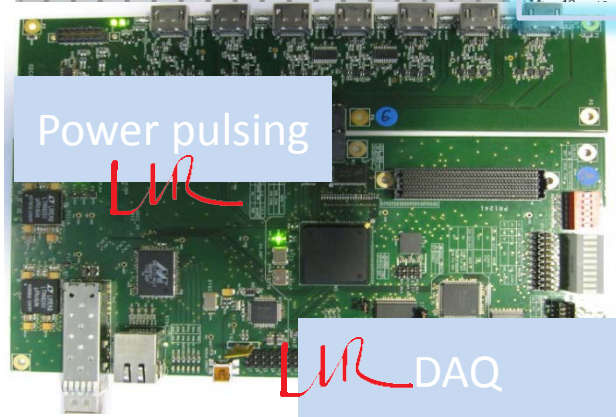


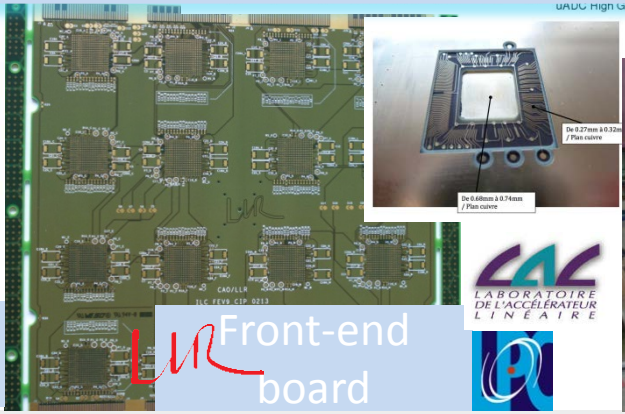


Simulation Analysis

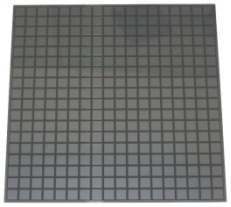


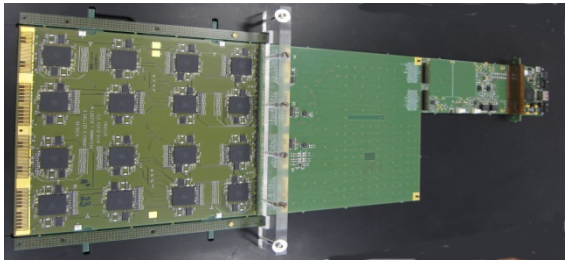


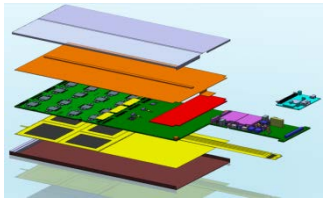


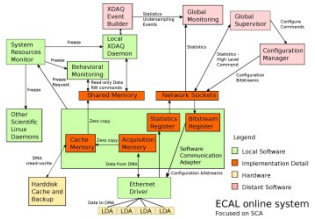


Activities at LLR (CALICE)



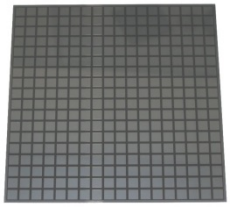


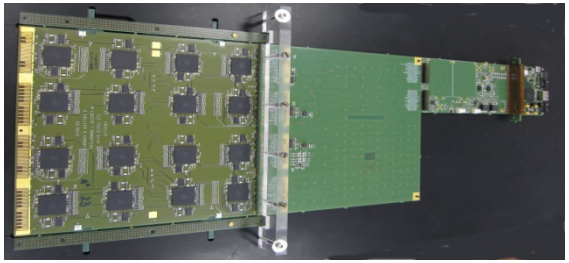


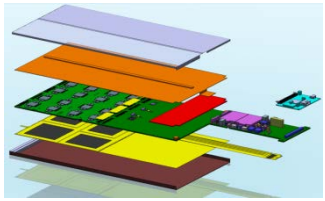


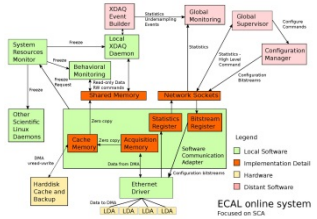
	Sensors	VFE & FE boards	DAQ	Integration & super-structures	SW ecosystem for ECAL
<2015	-Large size 9cm -Couplings with GR & opt. (HPK) -Test tools	-VFE : 256 chn, not opt -Universal Det. Interface -Test tools (w/o gluing)	-Universal DAQ for small throughput -Moderate power	Prototypes -Composite struct. -Single layer slab -Cooling, Gluing	- configuration & raw data storage Det & test bench
2015	-Larger size13cm -LFoundry -Small prod tests	-VFE : 1024 chn. -Long slab (4 boards) -Partial Opt. of PSRR & interchip couplings	-Partial inclusion of DIF functionalities: towards a local controller 100kchn	-Small prod of ASUs -Test with cosmics -Slim slab design	-Extended with data logger, pre-processing, run control
future	-Harvesting new manufacturers -Mass tests tools	-Longer slab (8 boards) -System redesign (PSRR) -Power distribution		-Design update -Long slab -Consolidated proto. -Tools -Beam tests	-Connexions to other sub-syst. -Event bulding

Project activities (mid term)







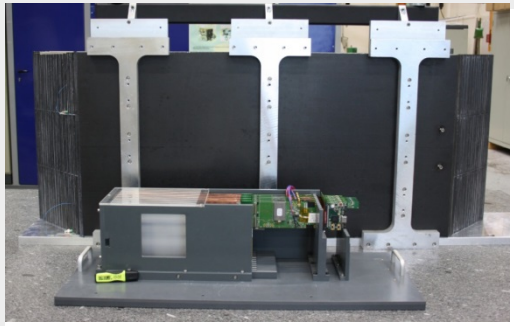


	Sensors	VFE & FE boards	DAQ	Integration & super-structures	SW ecosystem
outcome	-HPK w/o GR	-performance of single (few) channel(s) with power pulsing and SK2	-Modular system for Small setups	Prototypes -Composite struct. -Single layer slab -Gluing	-Modular SW -Diffusion among partners
ongoing	-Lowering dead area	-understand self couplings -Performance with beam -		-Semi-automated Integration bench	-Add function.
issue	Rad. Hard. New GR struct. (larger panel of manuf.)	-System redesign for SK2: PSRR, PP -New chip ? -Chip on board	-Higher level data Concentrator - Real low power -LV & HV distribution -DCS and system	-reproducibility -Full integration with cooling, top of module elec. & structure	-Double layer slab -Long slab -Consolidated proto. -Tools -Beam tests

Long term activities

- Scaling to an experiment depends…on the experiment (not the scope of current activities)
- But: on going R&D based on requirements for ILC (since 2006) for the demonstration of the concept
- Gain of credibility with a well integrated prototype (was EUDET prototype)
  - Needs funds and manpower (buy sensors, intrinsic cost of serious hardware, prototyping iterations, etc…)
  - Needs a definition of the project and its management
  - Many spin-off (LLR): CMS/HGCal, T2K, JUNO, CPEC, ILC…
  - Demonstration in the following:

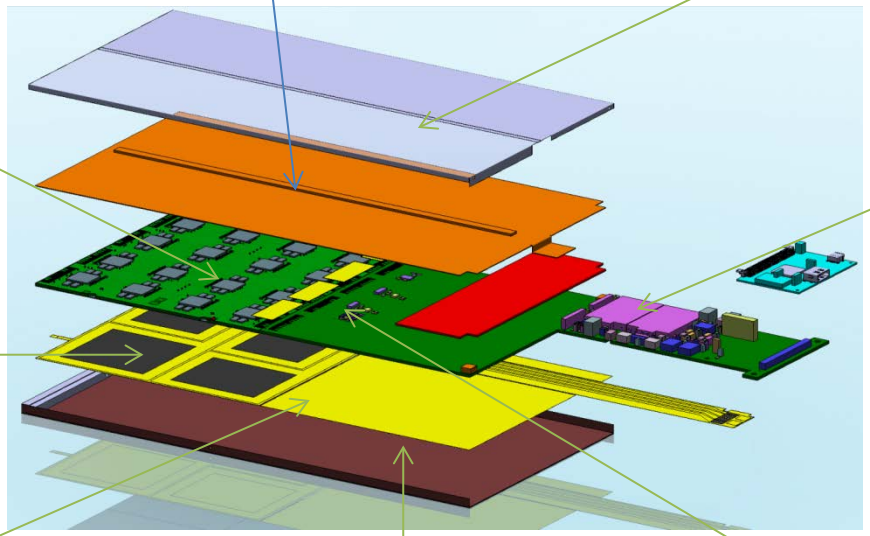
A detector module + composite structure



Coper sheet for cooling

Cover (EMI shielding)

PCB
1024 chn.
16x skiroc2



Power pulsing circuitry (400 mF)

Si PIN diodes

Front-end, DAQ, TFC Not shown

HV kapton

A “short SLAB”

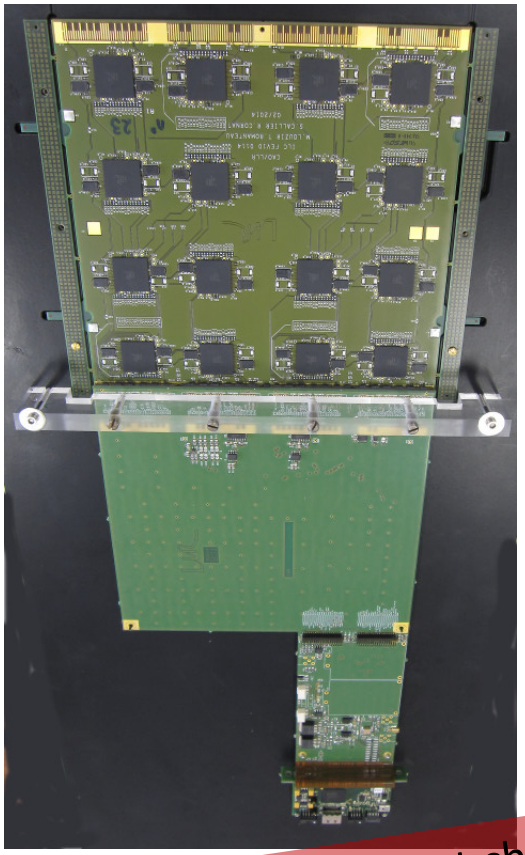
large source of inspiration for CMS/HGCal.

Stiffener, Absorber
Carbon fiber + W

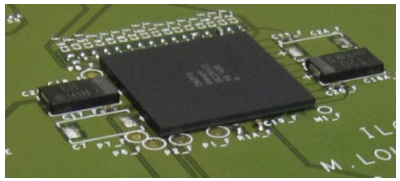
FCC Interconnects

Next version(s) of VFE board

18 x 18 cm^2 front-end board includes 1024 channels (16 chips),
almost perfect flatness required for gluing the sensors : 1.6mm symmetrical stacking



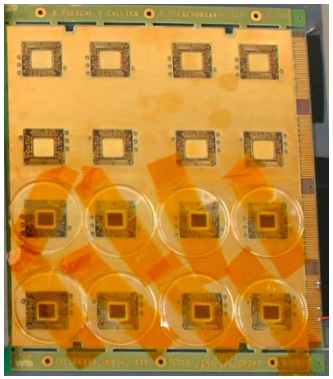
LFBGA packaged chips
and Panasonic Sp-CAP CX series
⇨ 1.1mm thick components envelop



With packaged chips version the overall module thickness would be 5.5 mm (+absorber) : >4600 ch/dm^3

Naked die version would provide optimal module thickness (<4mm in total, >6000 chn/dm^3)

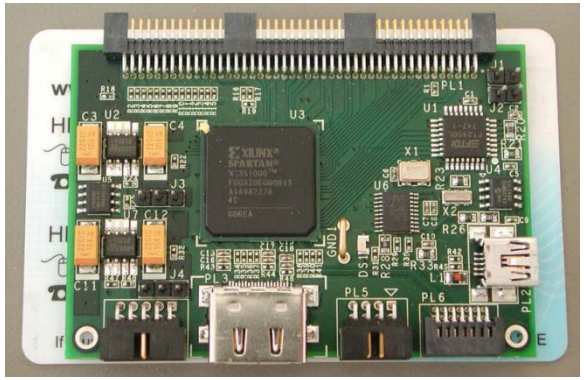
Electrical tests are ok but flatness is incompatible with sensor gluing.

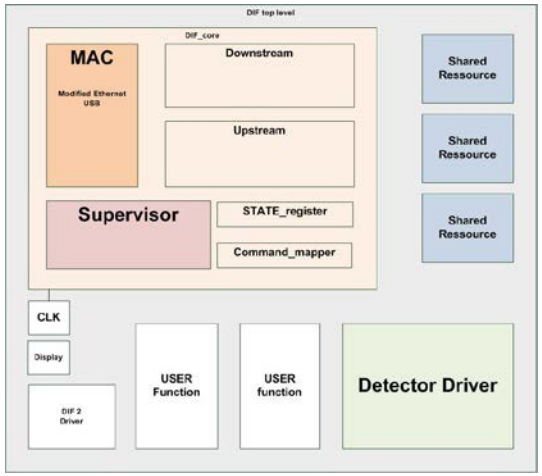


Copy (with a different chip) for T2K/WAGASCI + study of MPPC arrays

DAQ

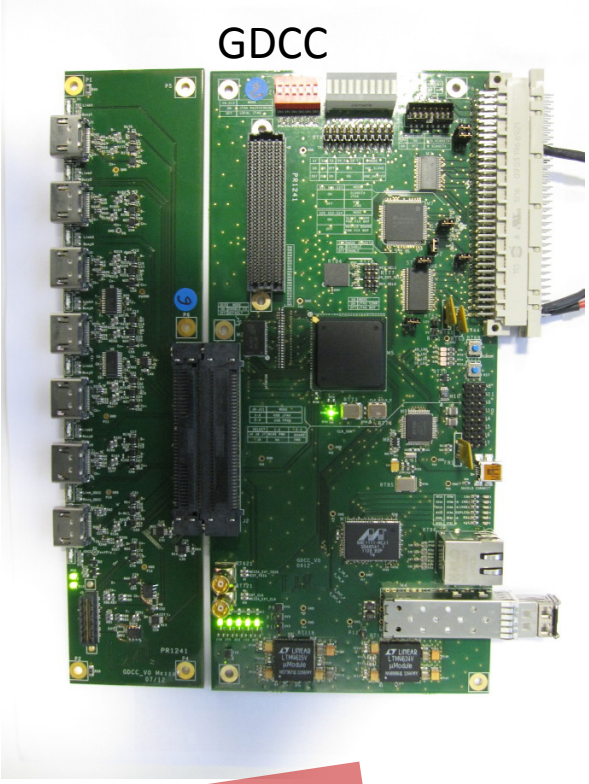
DIF





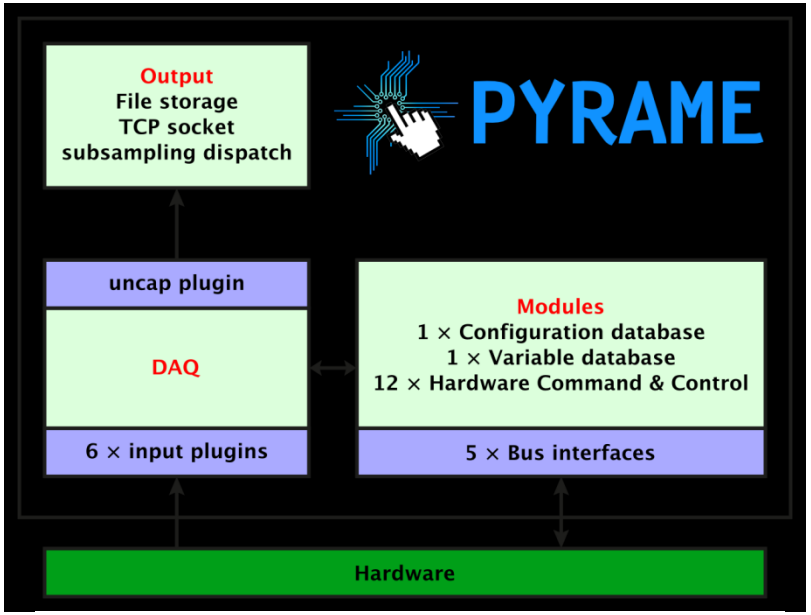
DCC

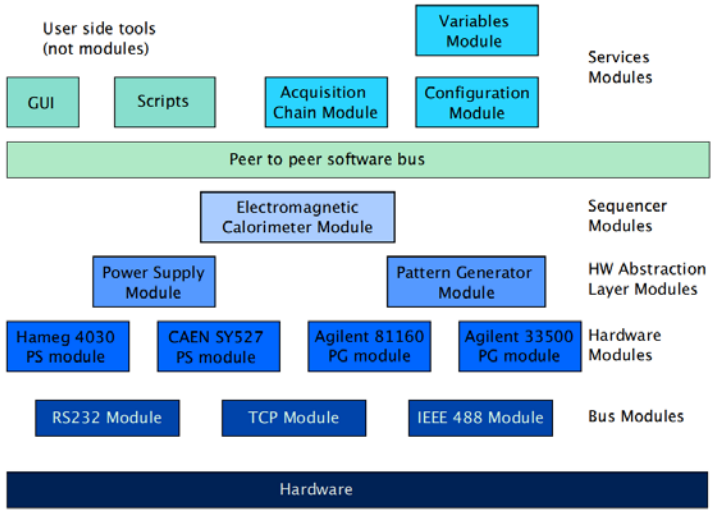
GDCC



Baseline for T2K/WAGASCI
+ JUNO/Trigger-DAQ
Read out of SKIROC2, SPIROC2,
MAROC3, EASIROC…

SW http://llr.in2p3.fr/sites/pyrame/





Prototyping framework for online systems.
Heavily modular for control-command or data acquisition.
Flexible and providing lots of options, allowing the system to evolve as fast as the testbench.

Baseline for T2K/WAGASCI

Used on P2IO/captinnov platfom

Used on CILEX/Galop

Used on CTA/NectarCam test benches

Proposed to CMS/HGCal and JUNO (small setup DAQ)

Used on many LLR testbenches
And at LAL & Japan for ECAL test benches

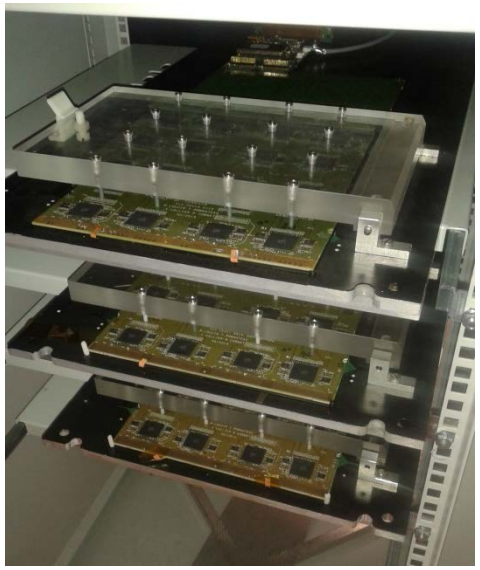
Latest news @LLR

Long slab with 4096 channels :
Configuration ✓ok
Read-out ✓ ok

Study of long transmission lines with high capacitive load : × on going
Study of power distribution : × on going

Preparation of a test beam setup @CERN (Nov. 4-16 2015) :
3 planes ✓ok
Slow control & Read-out ✓ ok

Study of long transmission lines with 4th plane : × on going
Calibration : × on going



Follow up of generic R&D 2016-17 @LLR

- Merging of DIF&(G)DCC : generic read-out HW , addressing issue of syncho, time stamping and time measurement.
- Designing long detector modules (CALICE as a study case) : R&D on transmission lines with high capacitive loads, power distribution (sim & proto), power pulsing
- Integrating the “EUDET” module : simulations of heat dissipation, miniaturized connections, stress tests of composite structures, slab design (CMS, ILC, CEPC)
- Toward the completeness of the online software : event building + integration with other frameworks (XDAQ, EUDAQ, etc…) and standards (OPCUA, IPBus,…)

IT Manpower at LLR

Nom	Sujet	Generic (CALICE)	Specific
Michael Frotin	Intégration	10%	40% (CMS)
Marc Anduze	Structures	10%	25% (CMS)
Frédéric Magniette	Online SW	20%	80% (CMS)
Miguel Rubio-Roy	Online SW	20%	80% (LLR)
Jérome Nani	Instrumentation, DAQ	50%	50% (LLR)
Franck Gastaldi	DAQ	10%	90% (T2K, JUNO)
Rémi Cornat	Instrumentation, DAQ	40%	40% (JUNO, CTA)
		1.6 FTE	

R Manpower at LLR

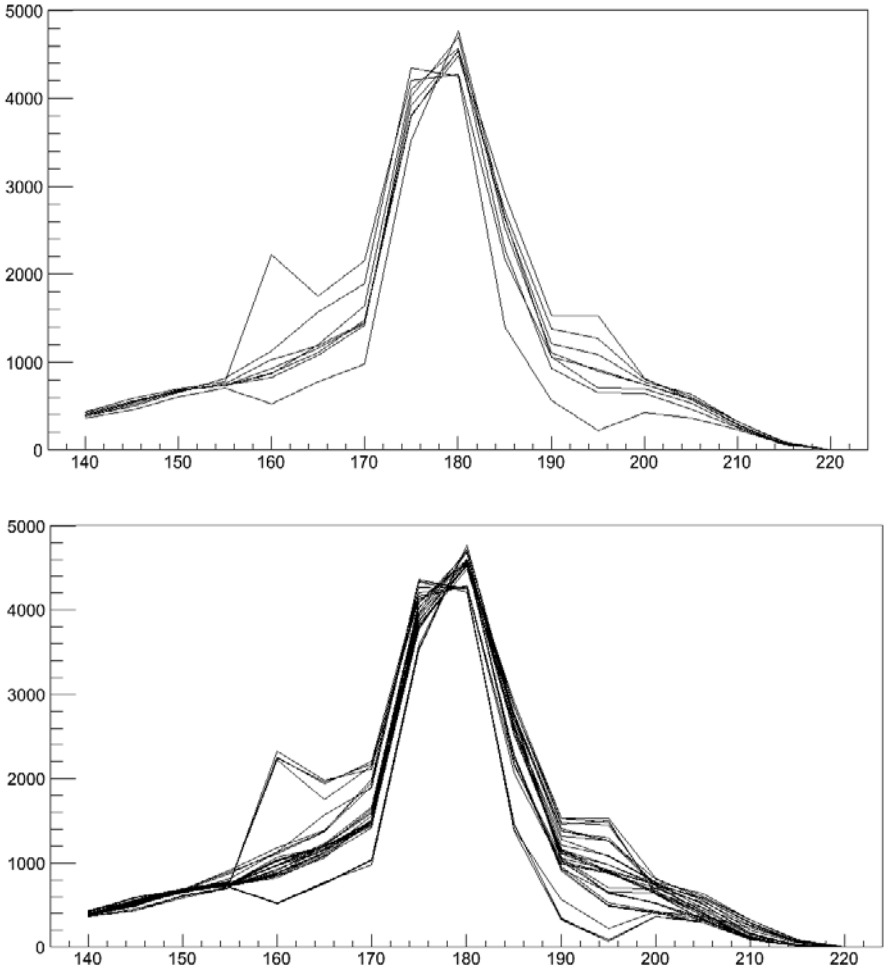
Nom		
Vladik Balagura		100%
Vincent Boudry		100%
Henri Videau		100%
Jean-Claude Brient		10%
Kostya Spack	PhD.	100%
Dan Yu	PhD.	100%
Trong Hieu -> Bo Li	PostDoc	100%
		3.1 + 3 FTE

2015 Results

I.2 Sensitivity to noise from other chips

Rough Scurves of a few selected reference channels on a reference chip

0, 8, 16 then 32 channels/chip are made noisy (trigger enabled + threshold set at 180 maximum toggling of internal triggers)



➔ Reference Scurves remains the same whatever the number of noisy channels is

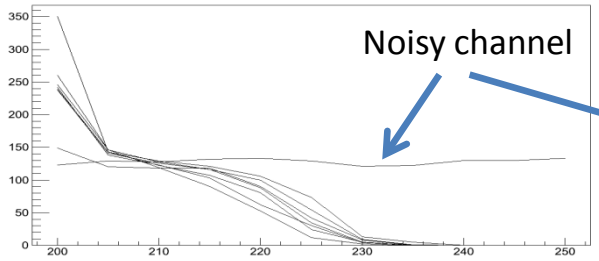
Courtesy of J. Nanni (LLR)

I.3 Internal noise

Before masking

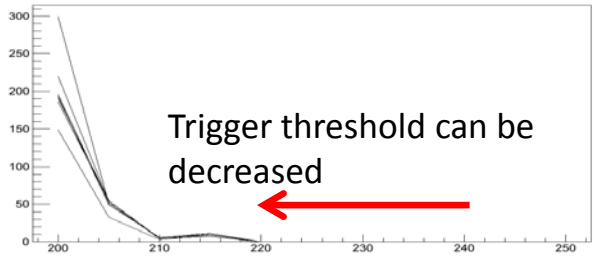
After masking

Scurves with all channels enabled



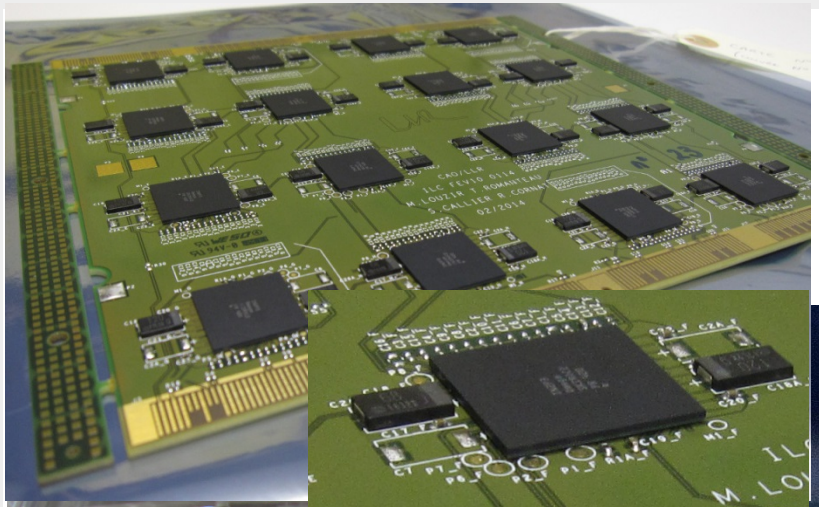
Masked channel

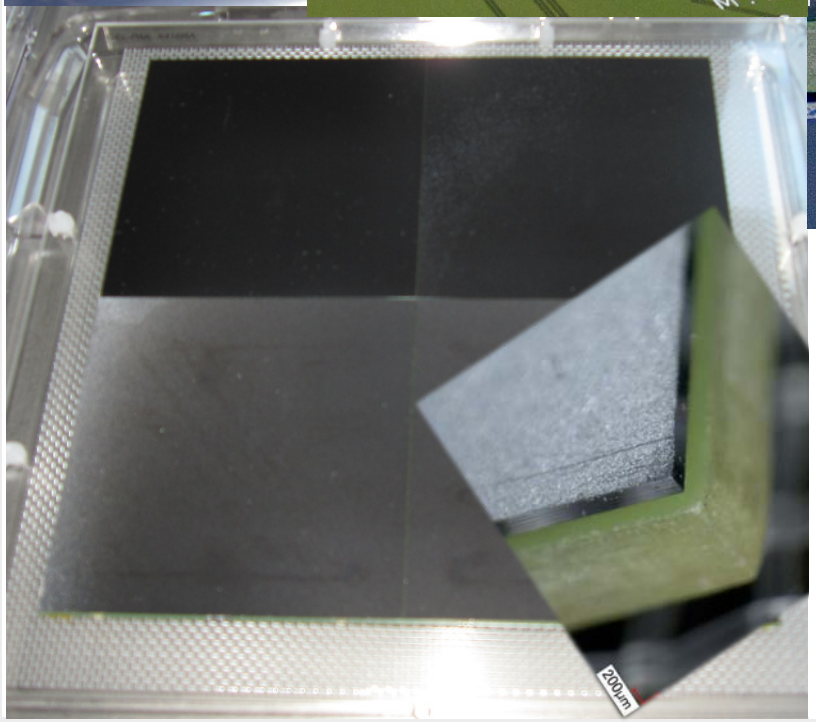
Scurves with noisy channel masked (preamp. remains powered)



➔ Digital noise due to generation of internal triggers

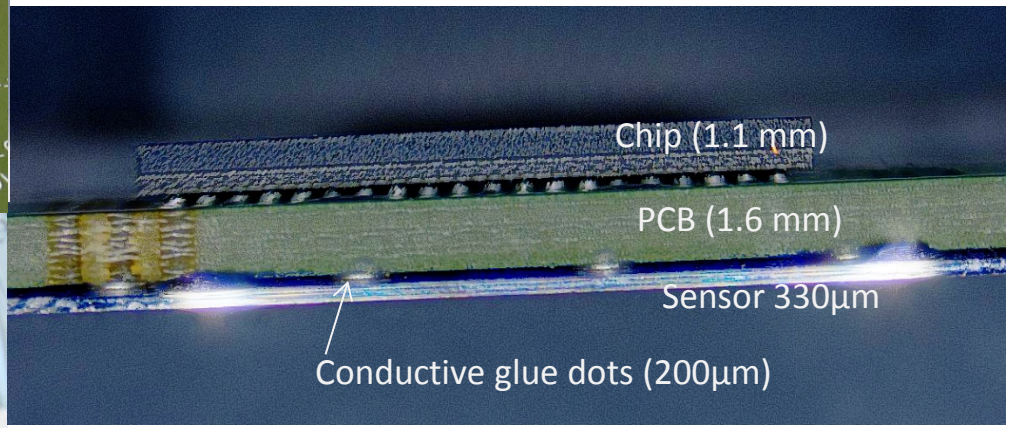
Detector module assembly





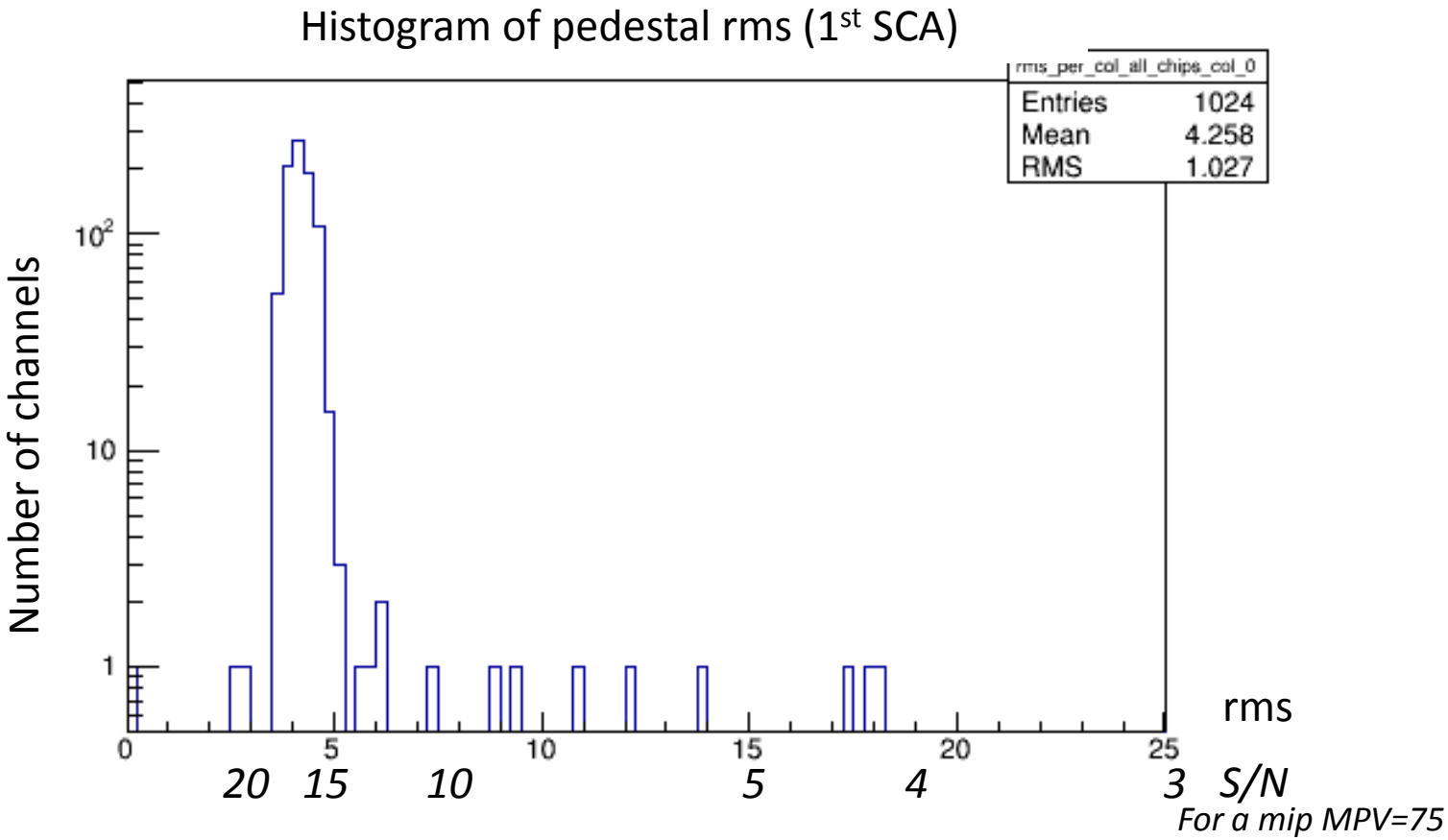
Robots for gluing sensors are developed (LPNHE)

⇨ First step towards industrialization



4 wafers 9cm x 9 cm wide can be glued with a 20 µm precision and a reproducible process. Glue is dispensed then pressed in order to form 200 µm thick dots

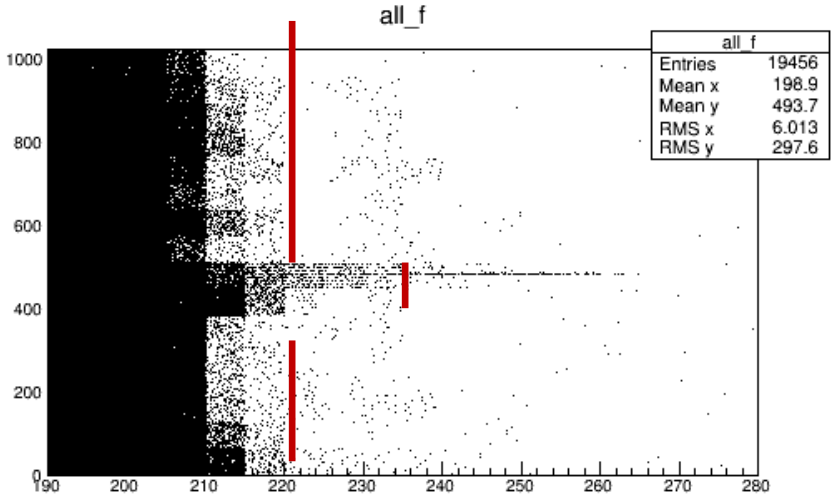
II.1 Pedestals with glued sensors

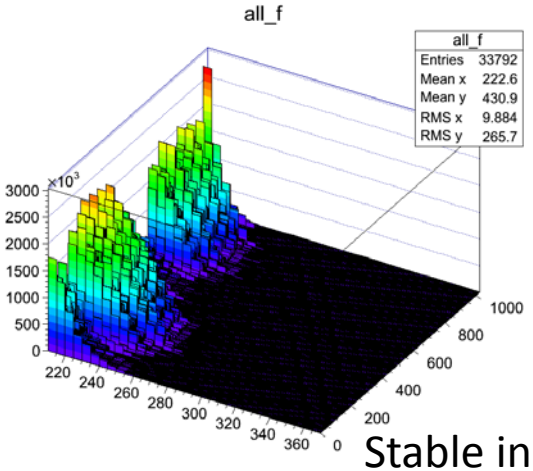


II.2 Scurves

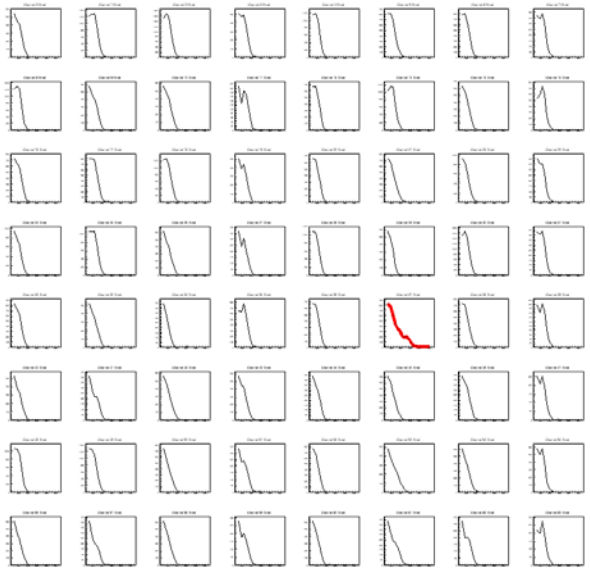
New cabling of the power supplies , isolated room

Uniform threshold arround 220-230 DACu possible





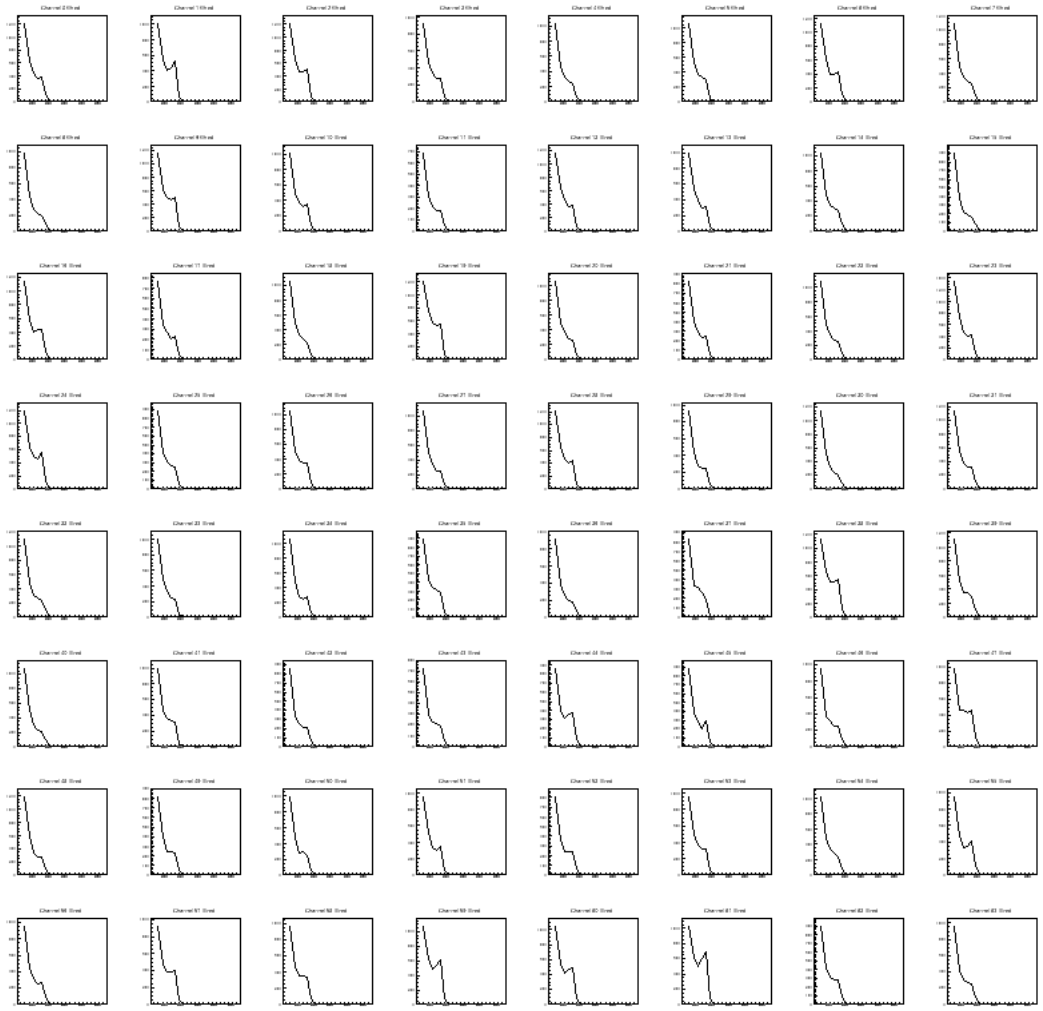
Few noisy channels…



Stable in time using the same test setup

II.2 Scurves

Probable effect of internal digital noise

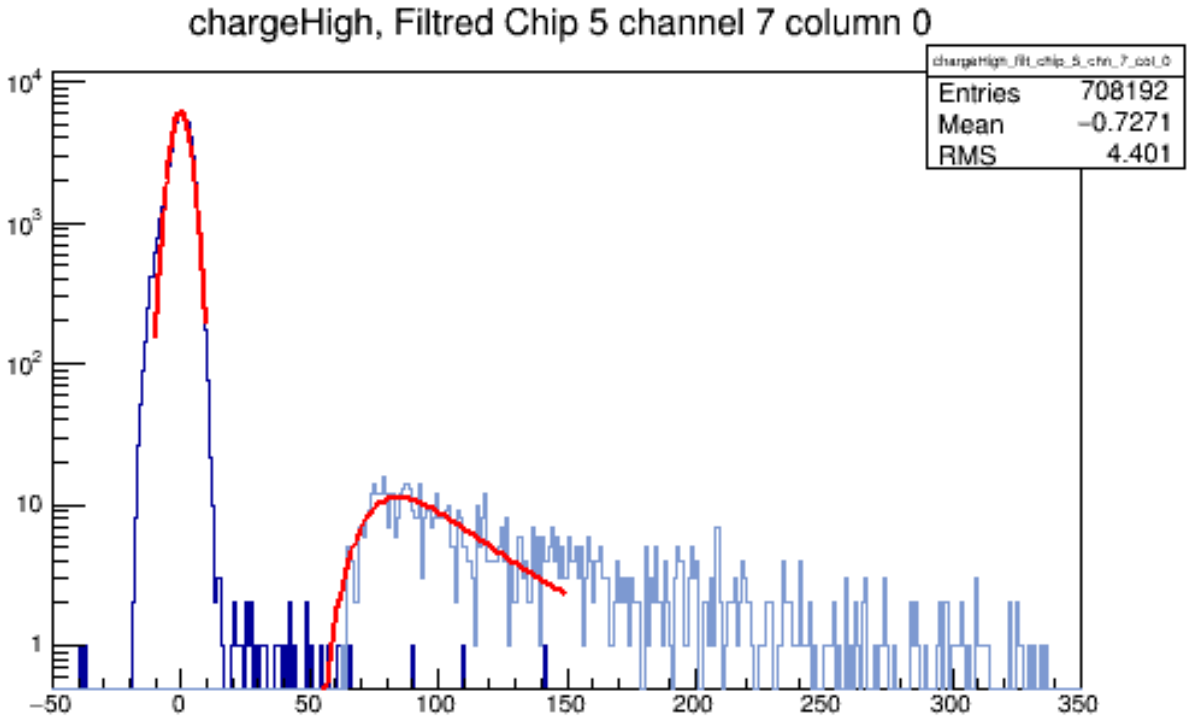


II.3 Cosmics data taking

50 hours,
Spill at 10 Hz, duty cycle 60%
DIF in TestBeam mode

Gain : 1.2 pF (high)

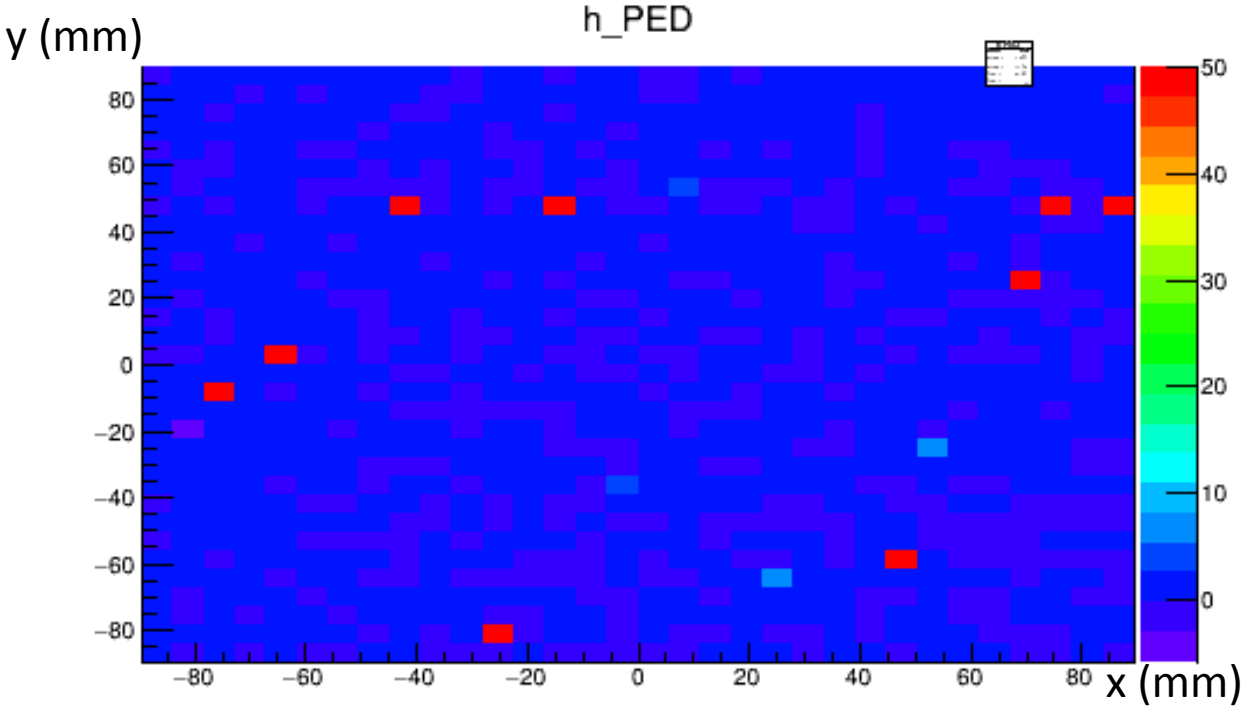
Typical channel



II.3 Cosmics data taking

5 cosmics run taken, ~consitent

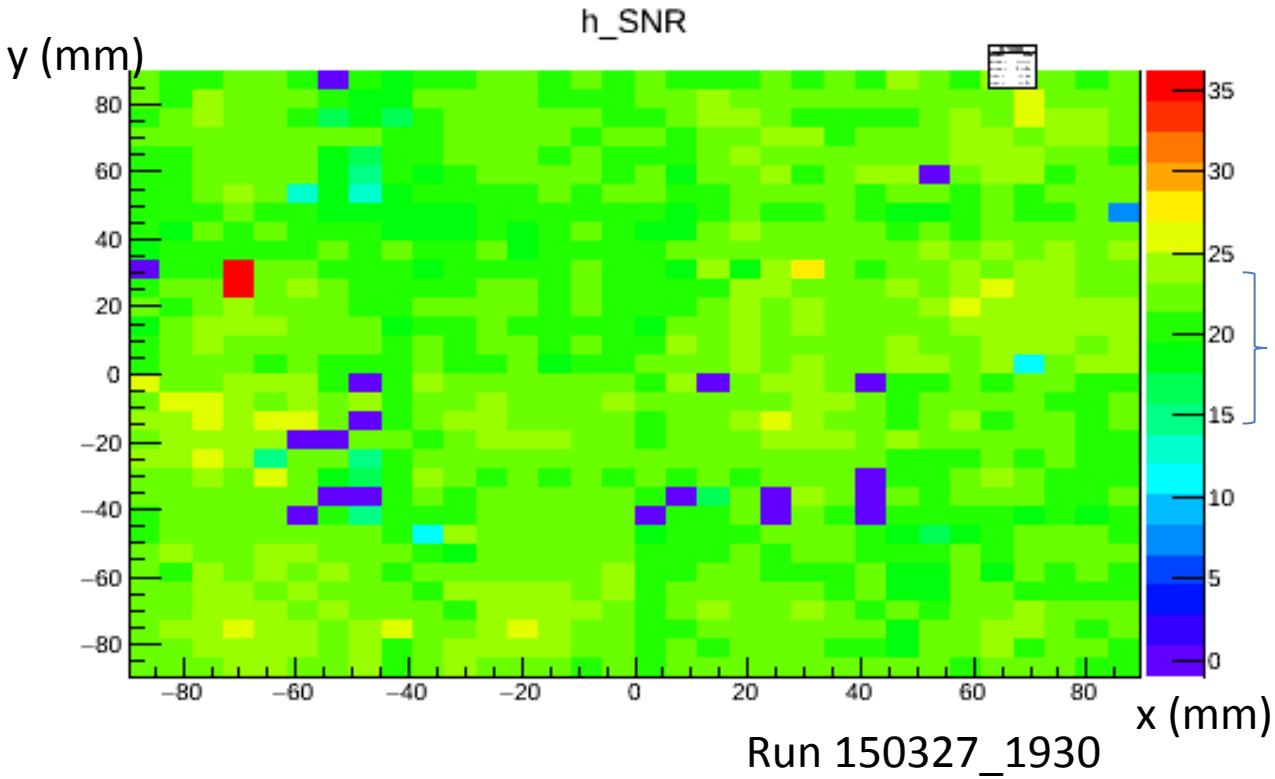
Pedestal uniformity after
correction (= mean of gauss fit)



II.3 Cosmics data taking : SNR

Some fit error + missing channels (to be verified)
Quality of fits not checked
Part of landau can but cut (high threshold) : overestimation of MPV

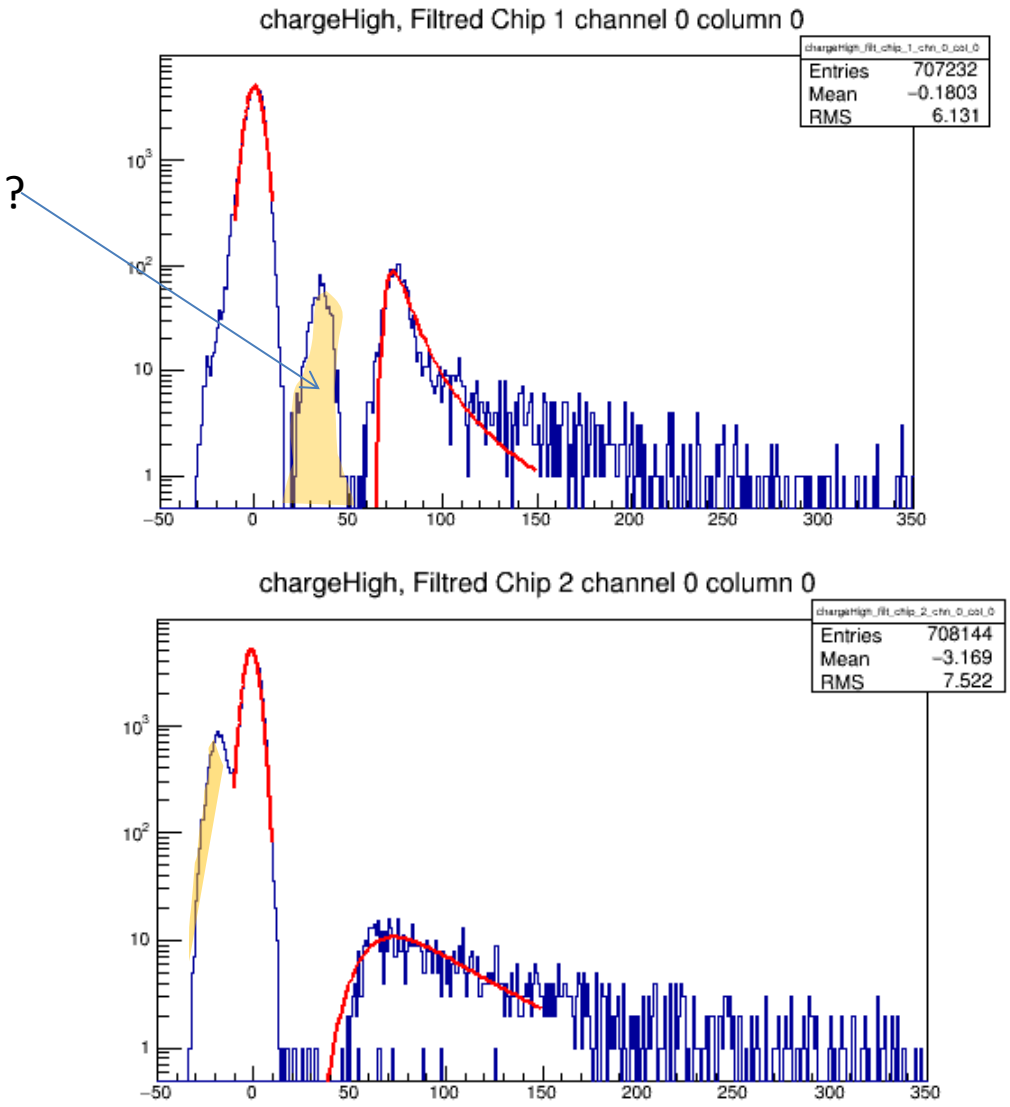
… but preliminary results are encouraging!



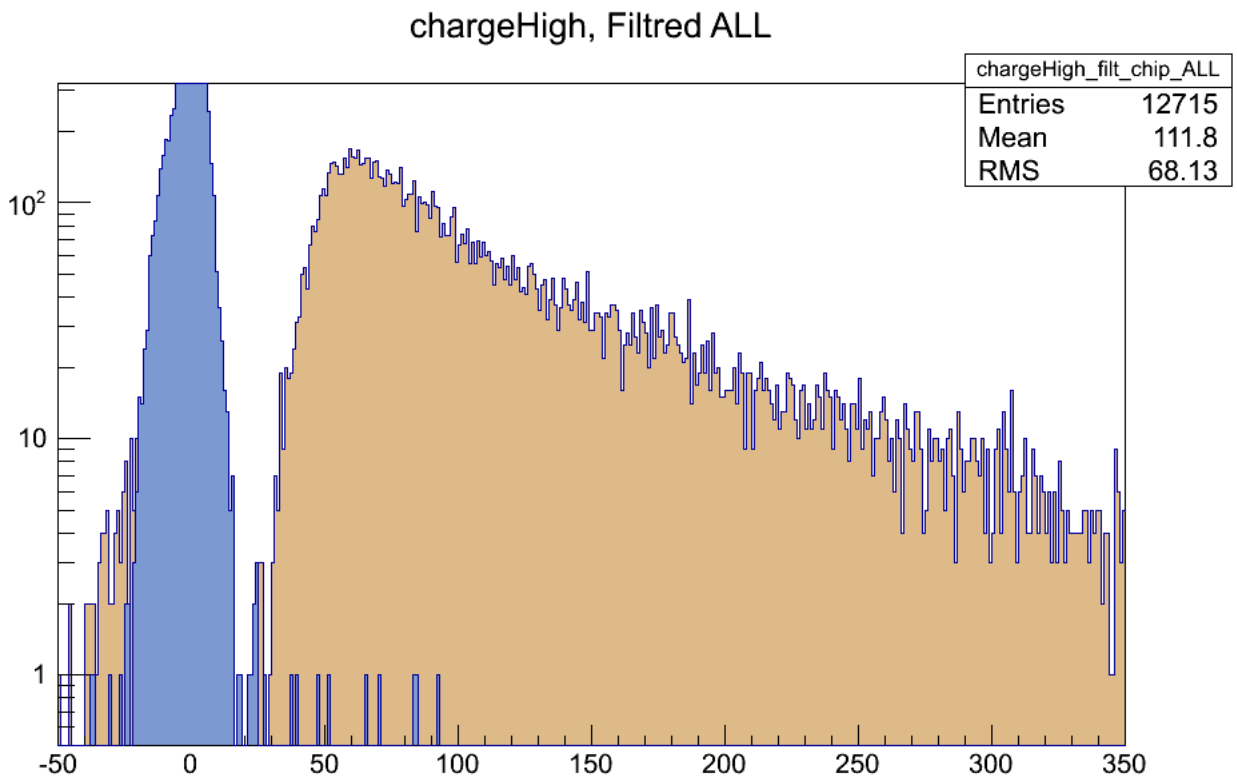
Run 150327_1930

II.3 Cosmics data taking

Somme effects to understand



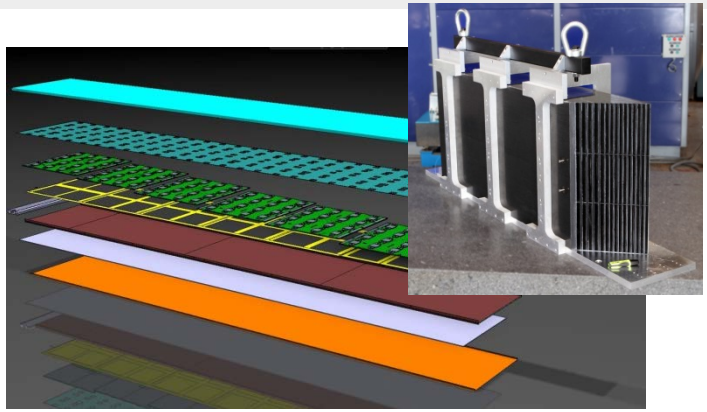
All channels of a chip merged together (raw data with no cut)



Toward a full length module

In principle, front-end boards will be chained forming up to 2m long detector SLAB, most of signals in bus

Issue 1 : clock distribution (5 & 50 MHz)
Interconnects are not impedance controlled (FFC)
One clock line may be loaded by 40 to 80 ASICS

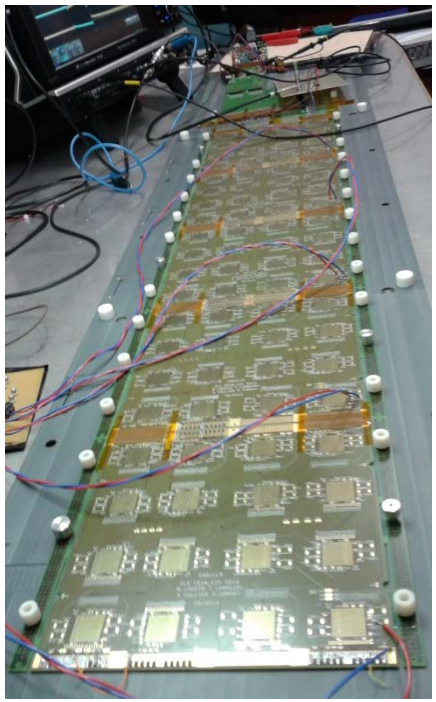


large C-W structure exists

⇨ Use of MLVDS adapted with 100 Ω on both sides, 100 mVpp remaining signal at the end
(6 Ohms loss/board, 20-40 pF/board, up to 10 boards)

⇨ Next version ASIC will have a PLL generating the highest frequency

Issue 2 : Power distribution (12 A pulses) & blocking capacitors (tested with FET switches as loads)



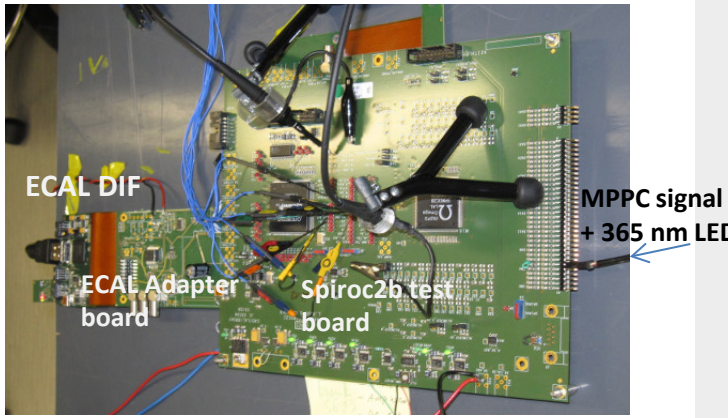
⇨ Current taken from a 800mF super cap (16mΩ ESR) + 2mF/board

Along 6 boards, static loss is 250 mV due to connectors (w/o chips).
May foresee to distribute power in a star topology.
4 boards SLAB being assembled at LAL

V. Extension to other chips (T2K, JUNO)

Test setup with a spiroc2b

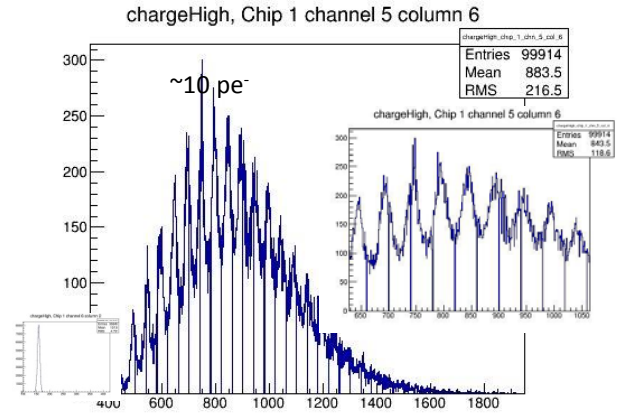
- Use of a modified test board from Omega
- Fpga bypassed by an ECAL DIF
- ~same DIF firmware as for ECAL (modified pin-out and signal levels)
- MPPC + LED pulser (16 pulses within a spill)



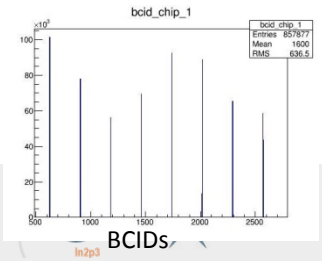
Combined tests

- Added an ECAL slab in the setup
- Common data acquisition as soon as SPILL signal is sent
- CCC : Same SPILL, same slow clock
- Events not in time (LED on one side, noise on the other) but cosmics would have been.

- Easiroc and Maroc will be added soon (started)



Pedestal ~at scale

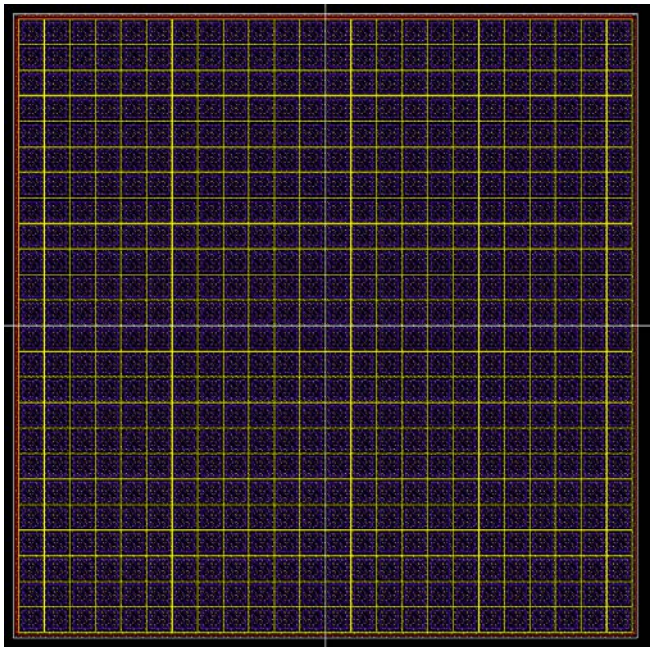


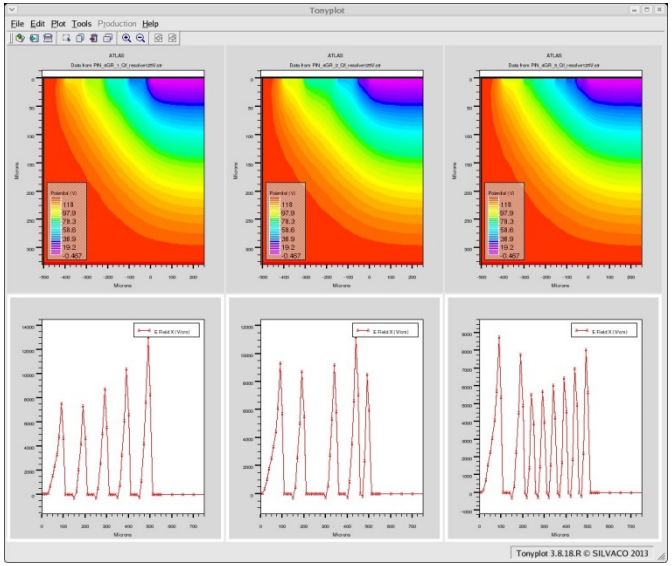
BCIDs

Wafer R&D

Large size matrix burned on 8’ wafers

- Ordered (LFOUNDRY)
- 700, 500 or 300 µm thickness
- 13.5 cm large
- 24*24 pixels

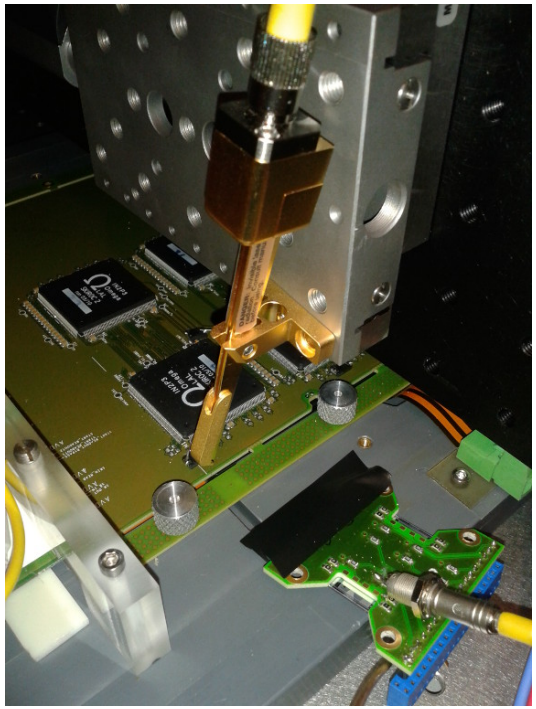




Segmented guardrings

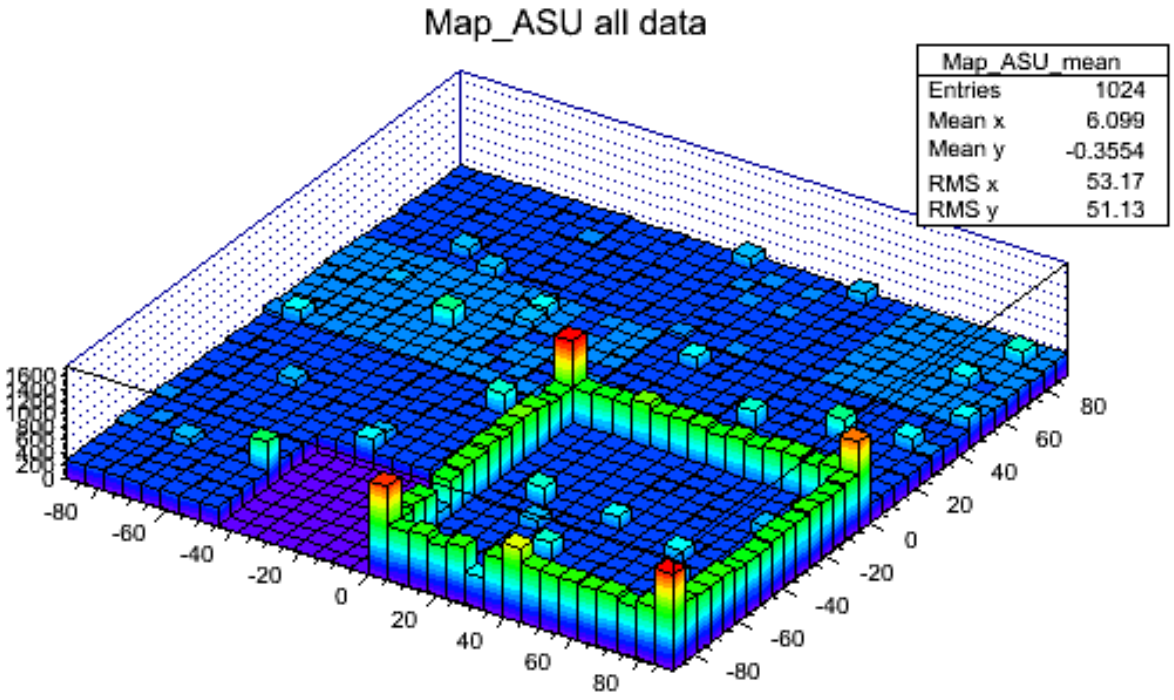
- Layout done at LLR
- From previous designs (baby wafers)
- Attempt to optimize structure by simulation

II.4 Square events

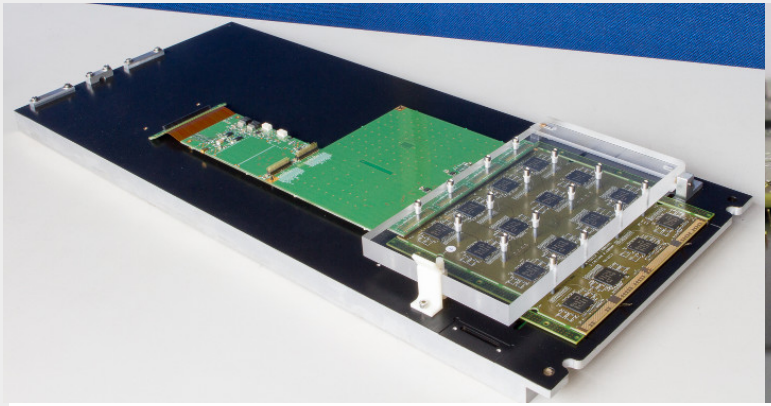


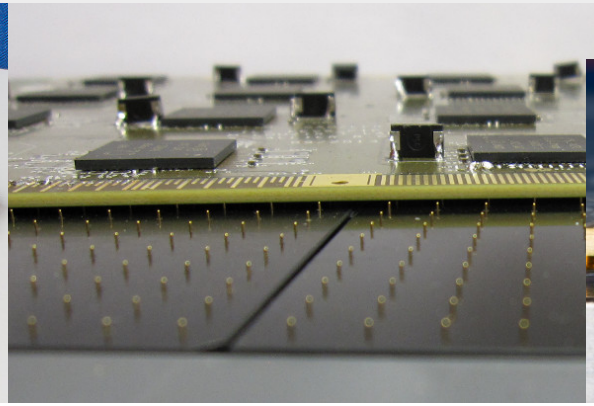
Infrared laser + fibre
20 ps light pulse
FEV10 board + glued sensors (from 2009 batch)

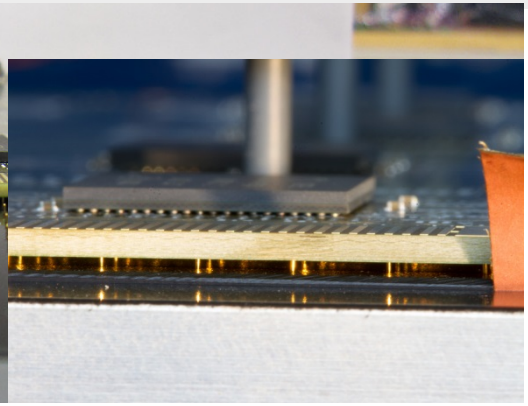
All channels enabled (no masking), power pulsing
Gain : 1.2 pF, Threshold : 400



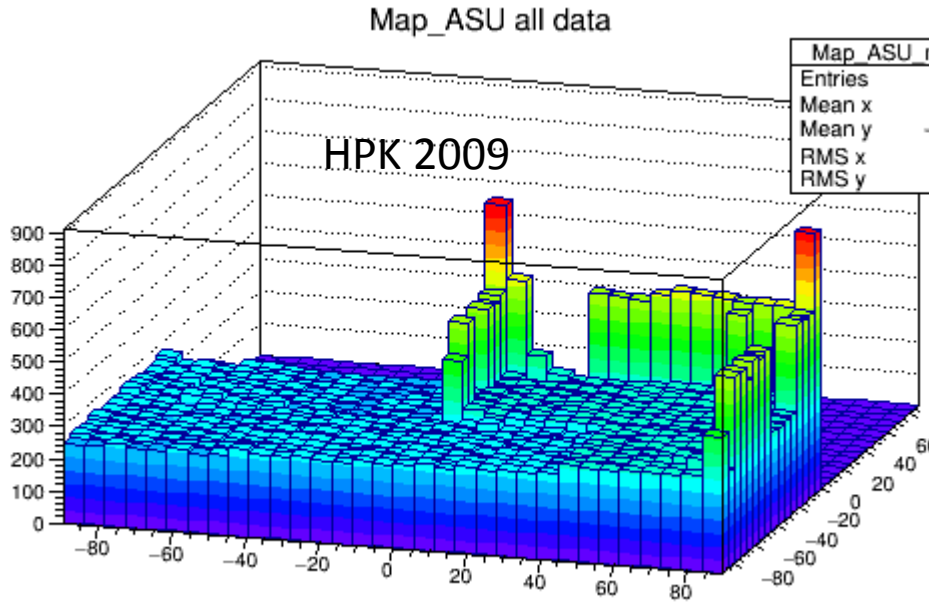
III. Desktop test setup with unglued sensors

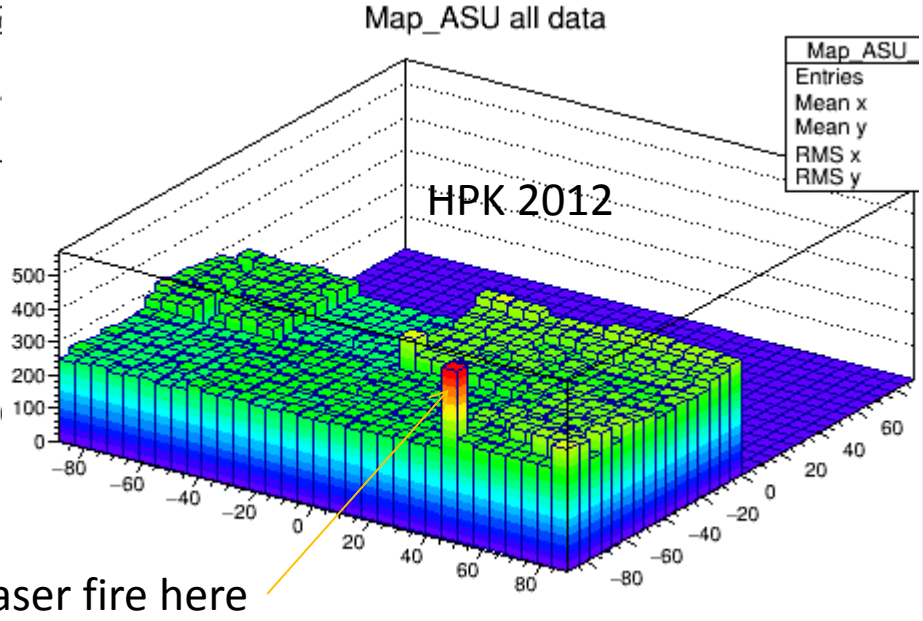




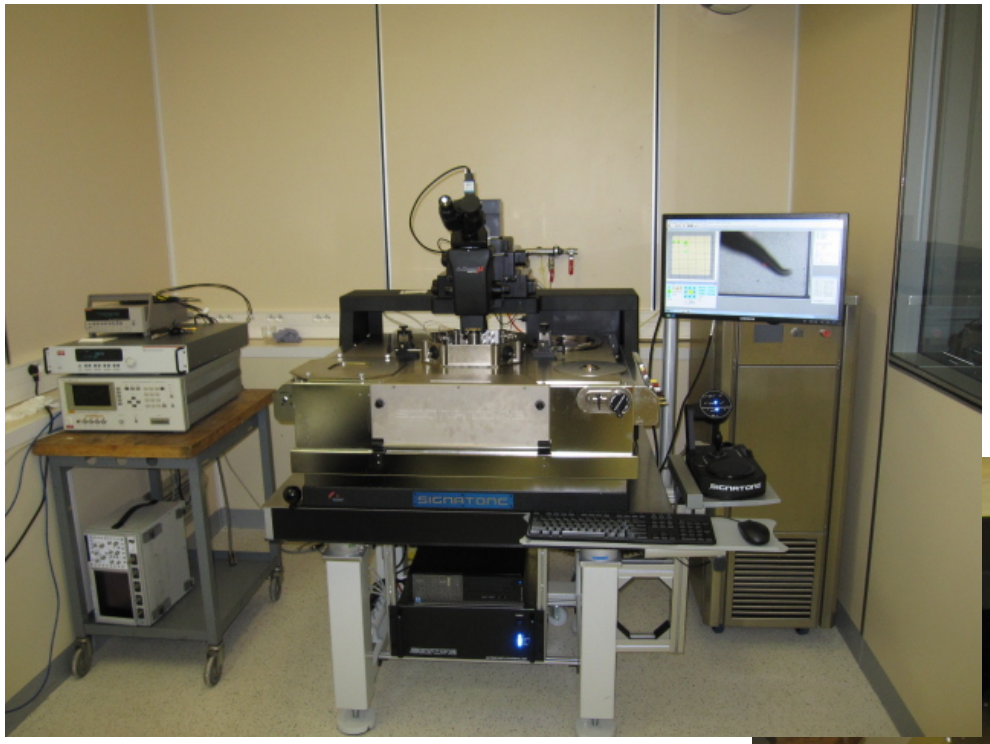


Comparison of 2 different wafer design (with/witout guard rings)
Missing signals (bad contacts with springs ?)

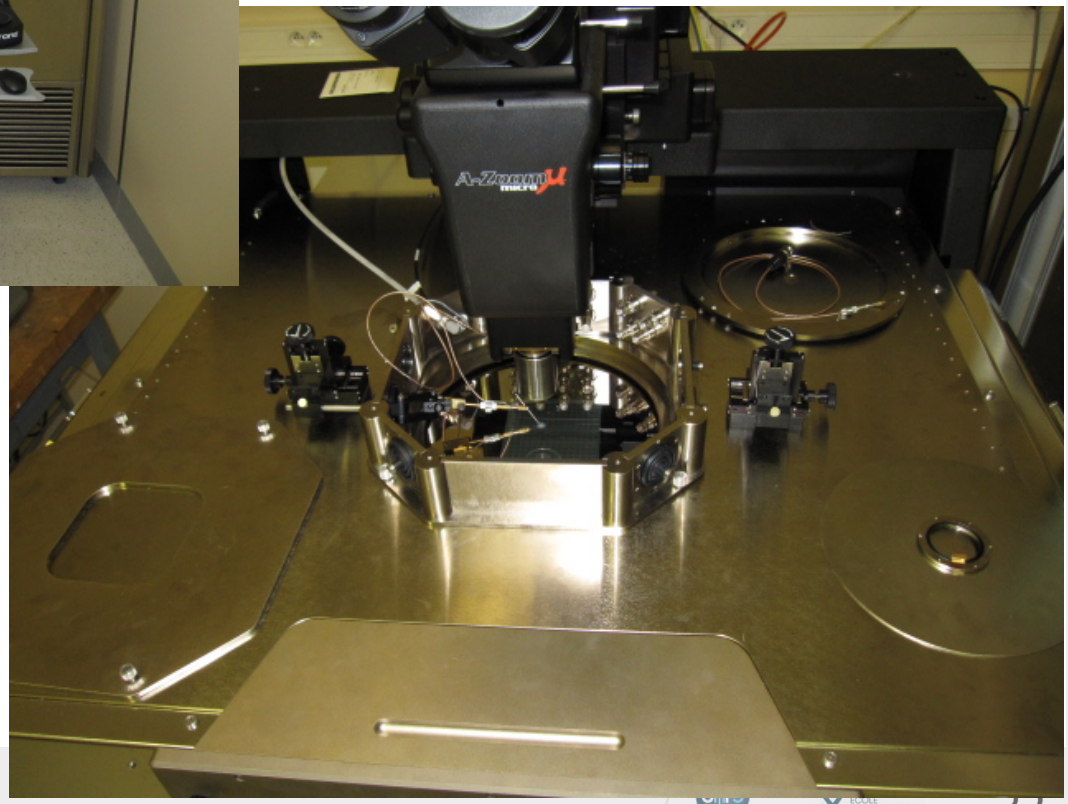




P2IO/Captinnov Platform



A semi-automated test machine

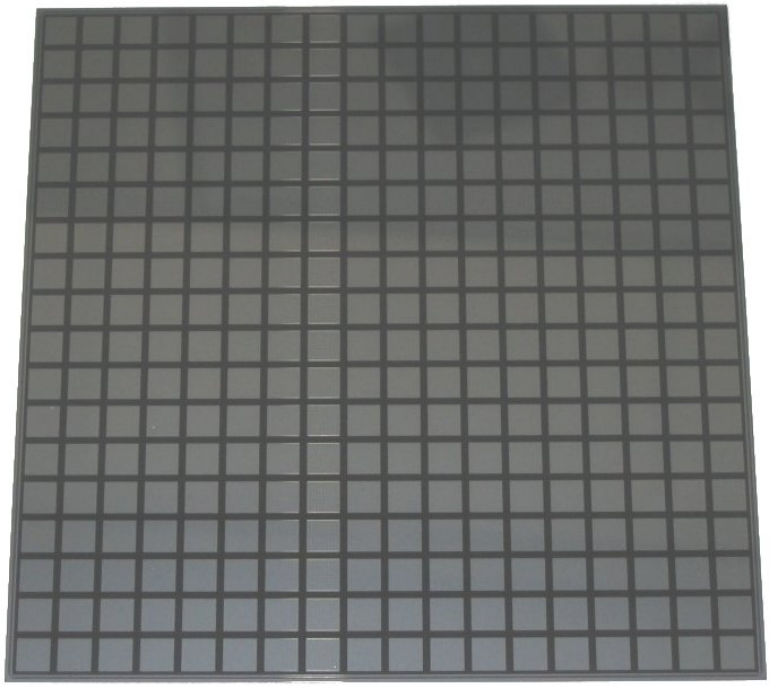


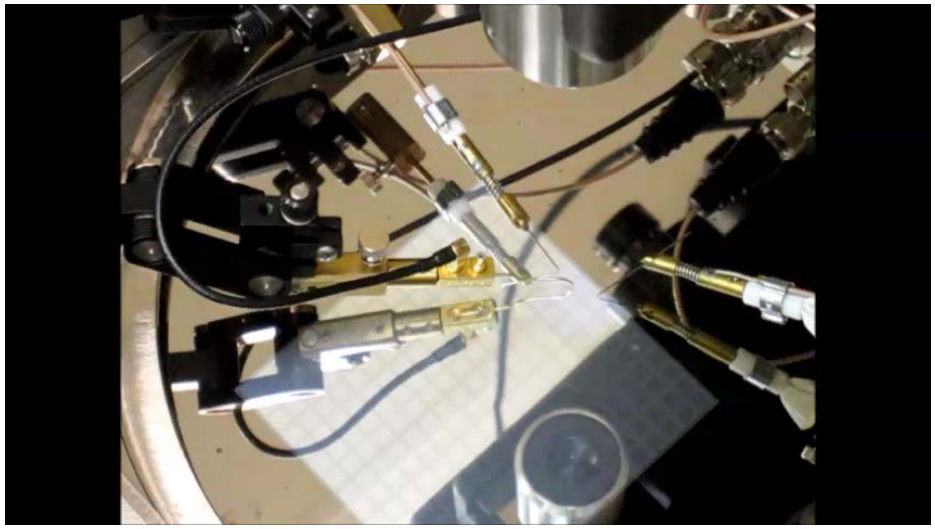
Project of platform driven by CALICE developments (+ATLAS@LAL)

Interest from STM

Example of an application

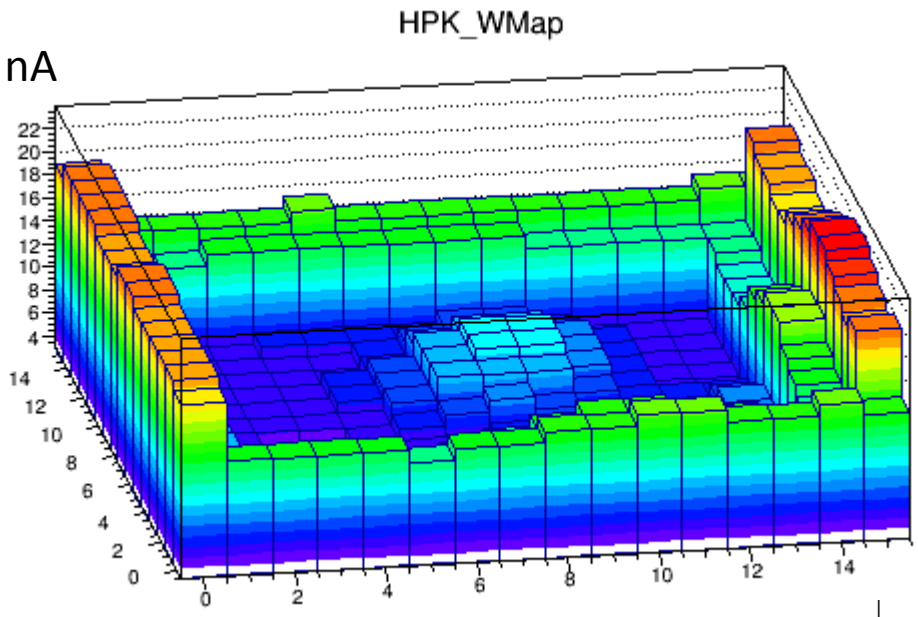
Map of leakage current of the 16 x 16 (9x9 cm^2) PIN diodes detector for the CALICE/ILD Si-W ECAL



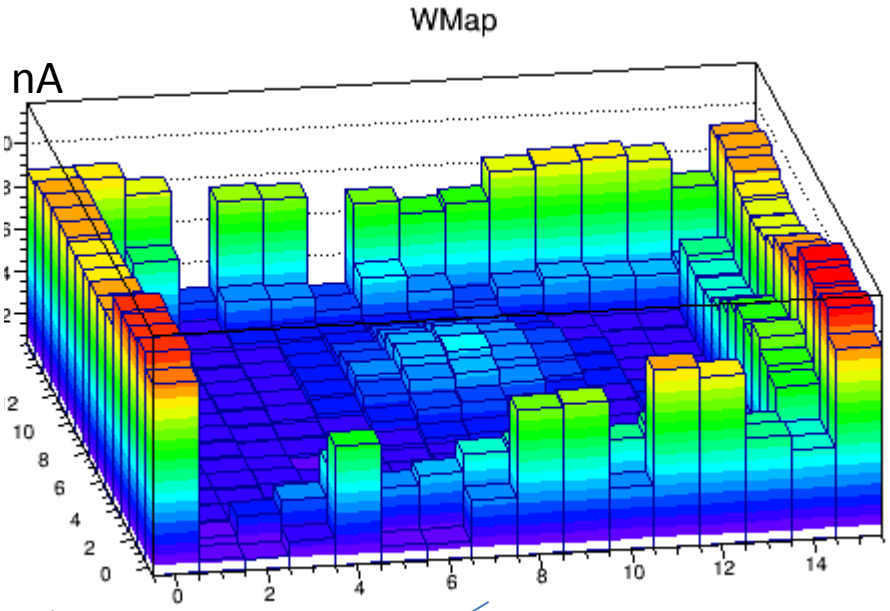


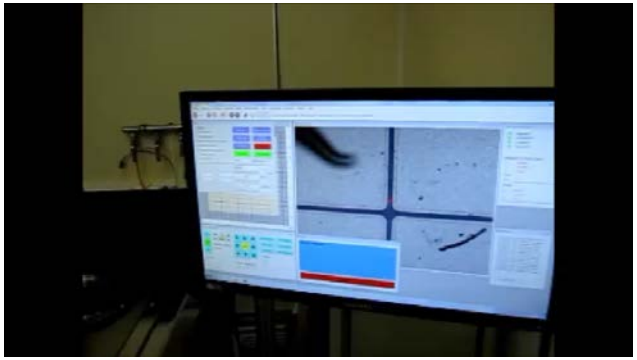
The scan is fully automated and the measurements are synchronized with the machine,
Duration of the scan : 30 minutes for 256 diodes.

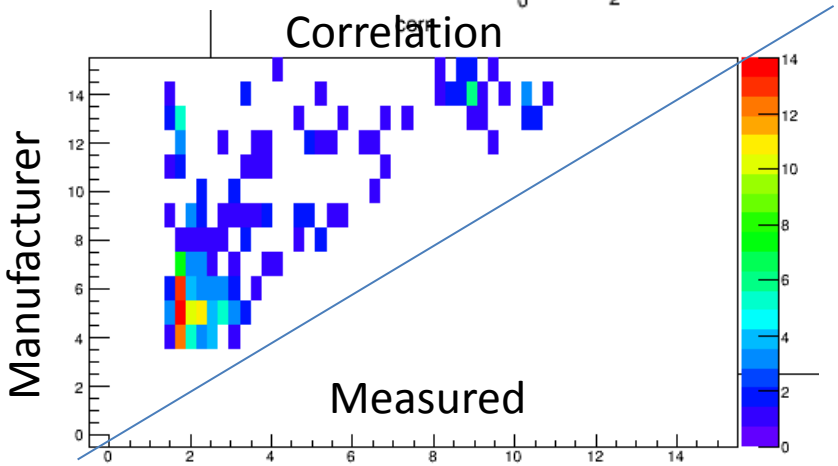
Map from the manufacturer (2011)



Measured map (09/06/2015 –preliminary–)



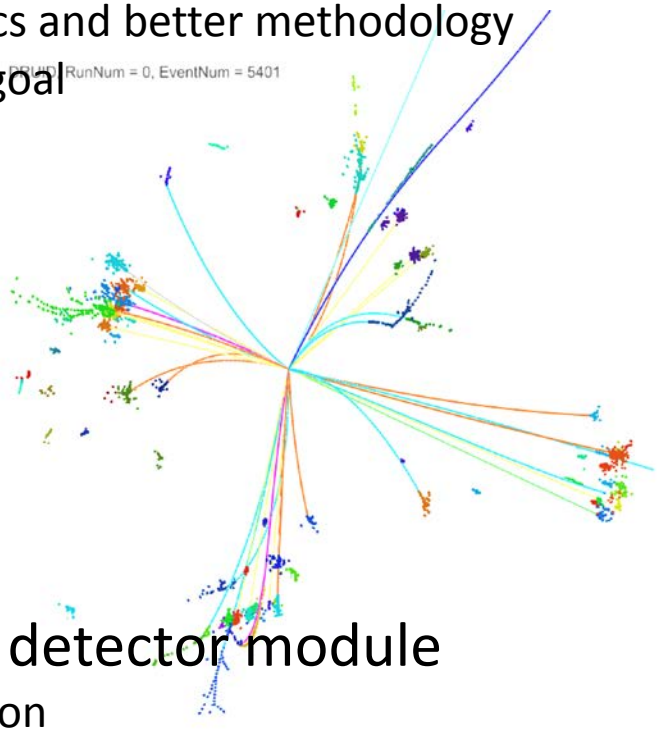




Conclusion

Preliminary tests of the first front-end board

- All results should be checked will higher statistics and better methodology
- Signal over noise ratio seems to exceed design goal
- 98% of channels are responding (cosmics)
- Successful operations with **full** power pulsing
- Missing : linearity, crosstalk etc…



Production of a small batch of 8 slabs

- Gluing of sensors planed for end of May/June
- Assembly of slabs : September

Next engineering step is building a long detector module

- Requires specific studies of the power distribution
- Already tested 2 front-end boards together