Ecal activities at LAL

Roman Pöschl

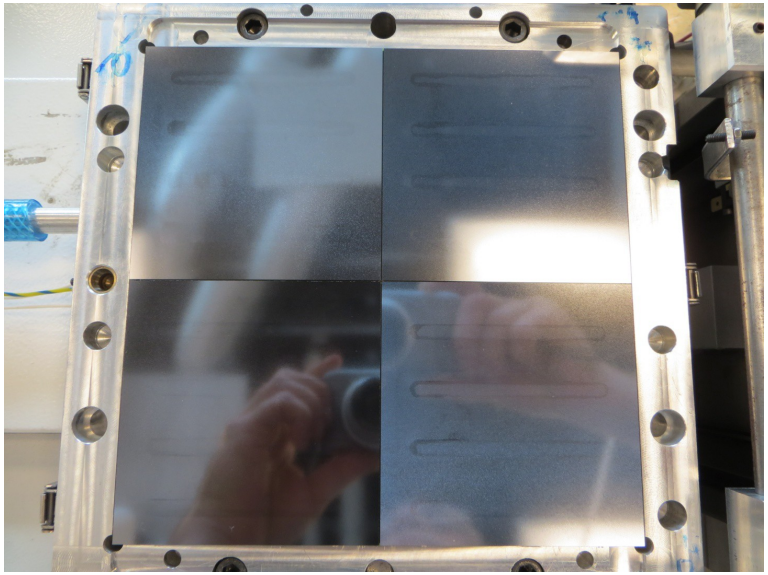
- Ecal Assembly
- R&D for PCB
- Analysis
- Budget 2016

Reunion CALICE France – April 2015

Comments on Assembly

- Development by the LAL team
  Julien Bonis, Patrick Cornebise, Alice Thiebault, Marco Fernandez
  (Consultation by Christian Bourgeois and Alexandre Gonnin)
  All steps allow assembly in a fully controlled manner with very little human 'contact' with detector devices

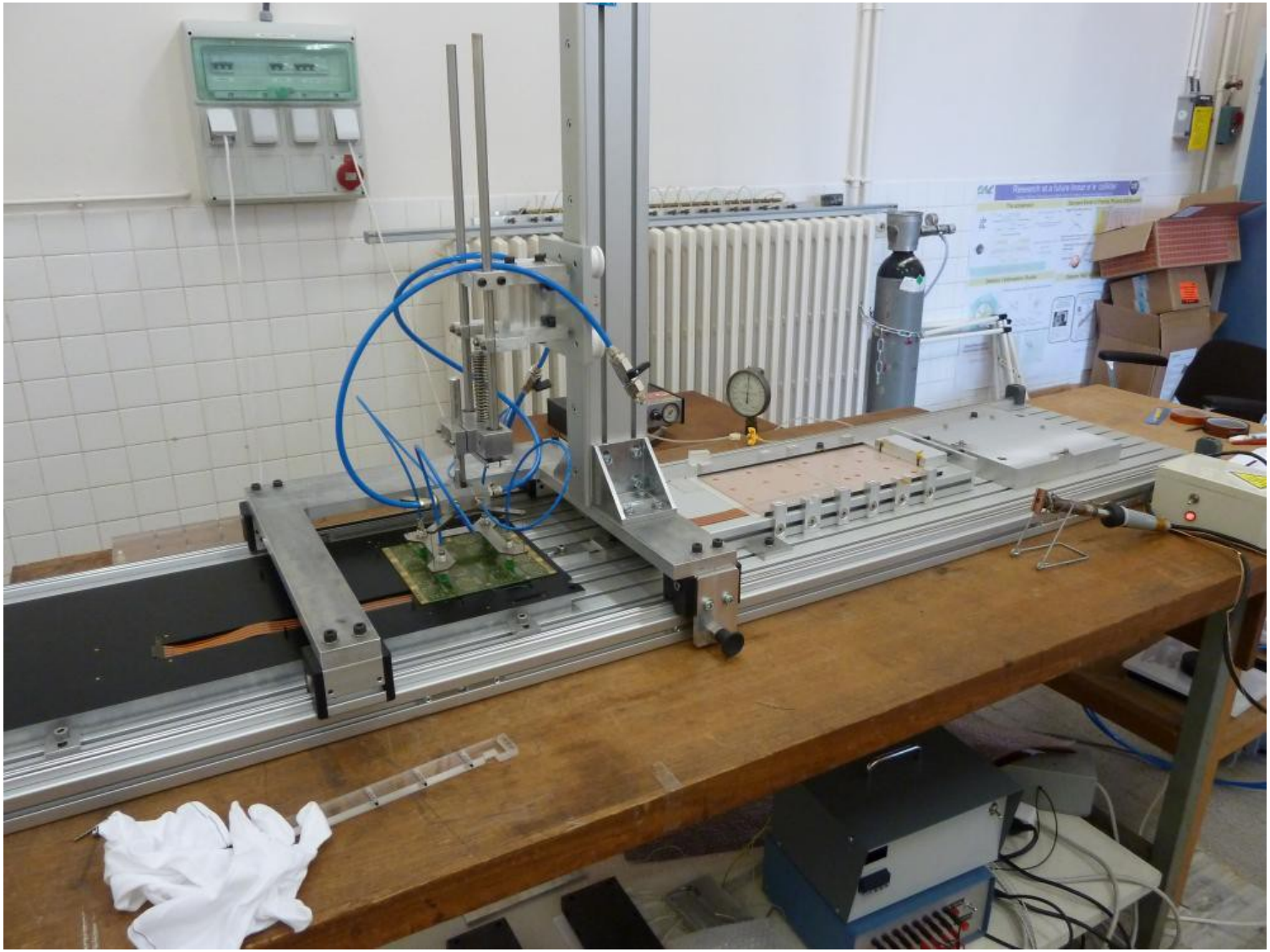
- For the tests, training an ASU with false SiWafers was used



Assembly of SiW Ecal layers

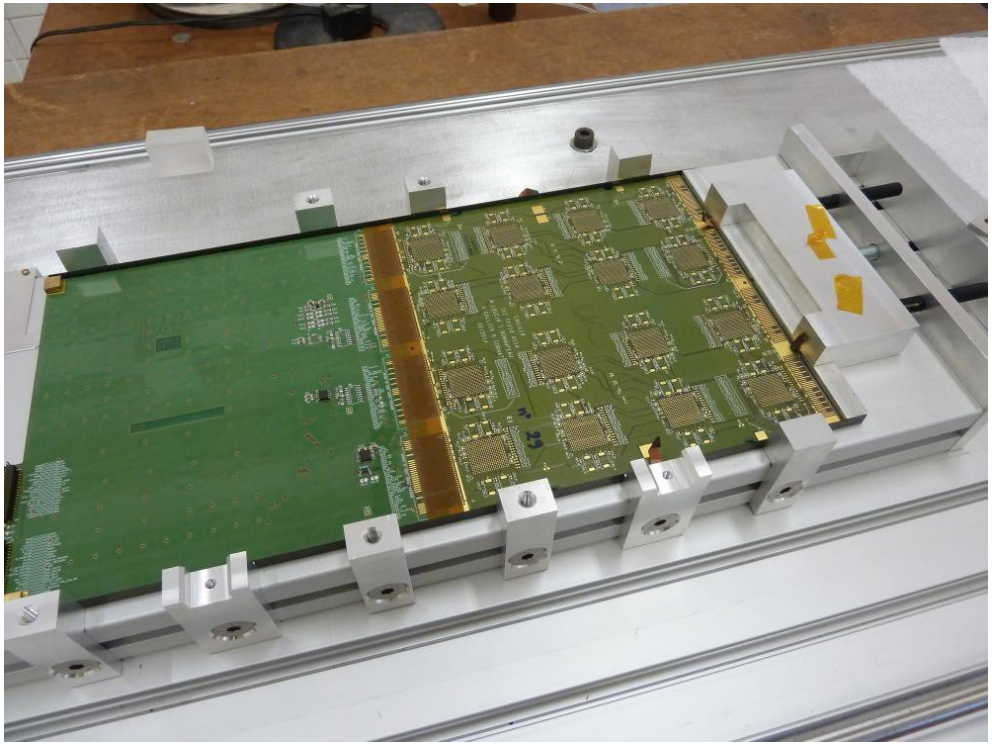
Assembly bench in LAL Workshop

Assembly bench from a different angle

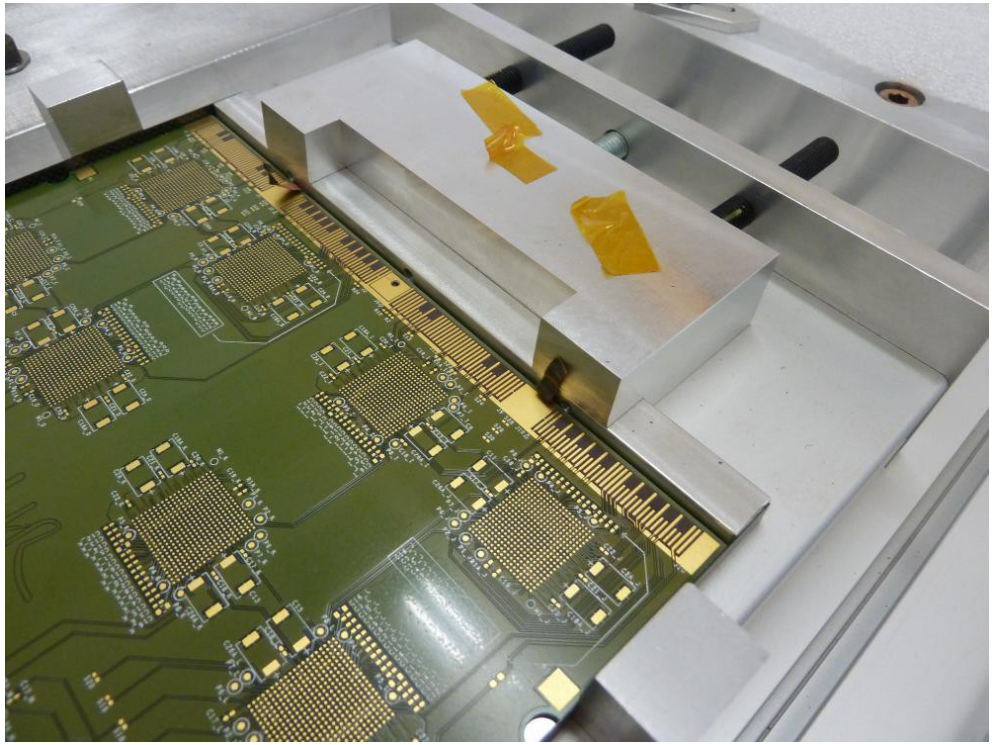


Steps of assembly

8. Finishing



Interconnection pair Adpater card/ASU



Connection of HV straps

Not shown: Placing of thermal copper drain and closing with Aluminum cover

Ready for use: a) Leakage current b) Tests with data

Comments

- All steps of assembly procedure have been exercised with an experimental model

- New w.r.t. FEV8 (2012)
  Four wafers, interconnection in mechanical structure

- Technically ready to receive and assemble 'real' layers
  Important step to stabilise effort at LAL (We are sitting at the end of the chain)

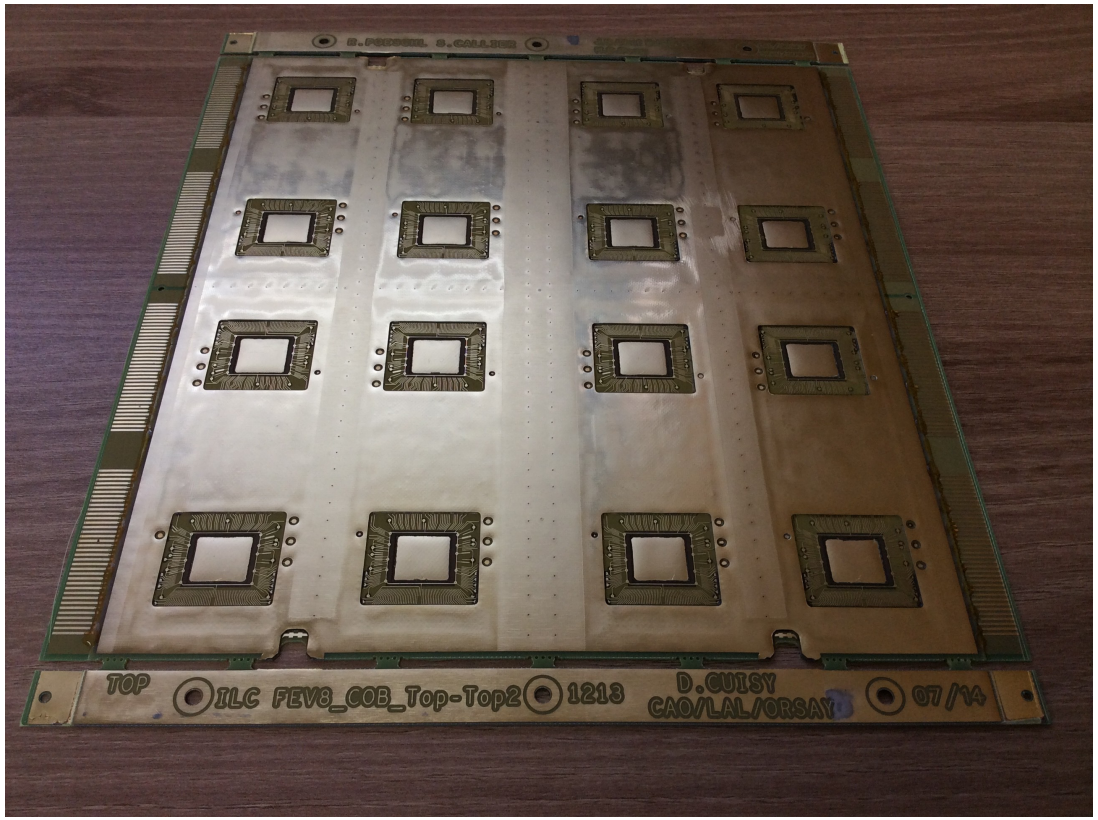
- Assembly of short layers takes about 1 day
  * including polymerisation => parallelisation
  * do not expect much longer for long layer (provided enough automatisation)

- **AIDA-2020** will help to scrutinise procedure further
  - Further reduction of human intervention
  - Interconnection is maybe most delicate step that needs automatisation and monitoring (in particular in view of long slabs)

- LAL Assembly bench will also serve as starting point for ATLAS studies!!!
  Contact assured by Dirk Zerwas

FEV8_COB

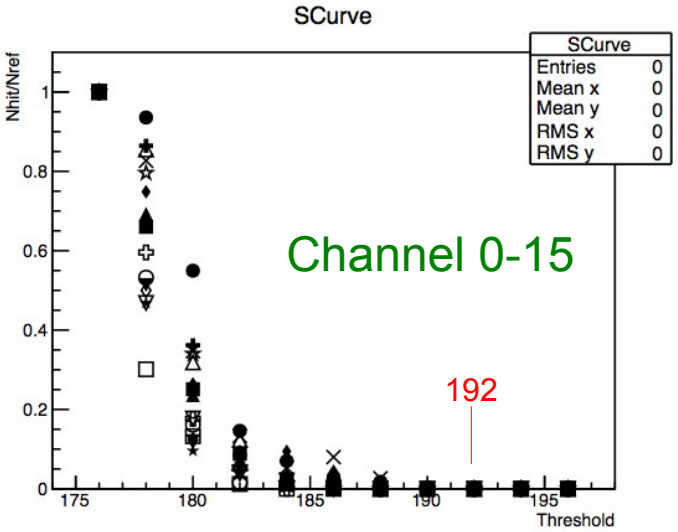
- Produced by EOS Company South-Korea under supervision of SKKU/OMEGA/LAL
  Production autumn 2014
- Metrology
  Thickness ~1.1mm
  Planarity not overwhelming 1,0mm and 1,4mm of bending
  Still within industrial limits
- Did see mechanically better boards during meeting with EOS company

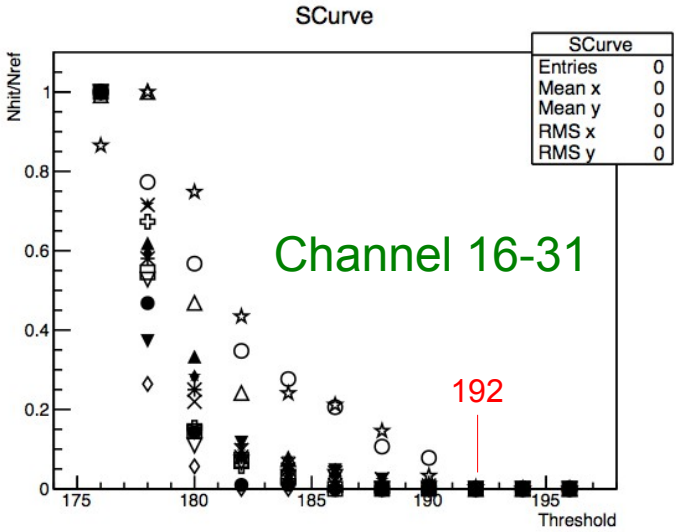


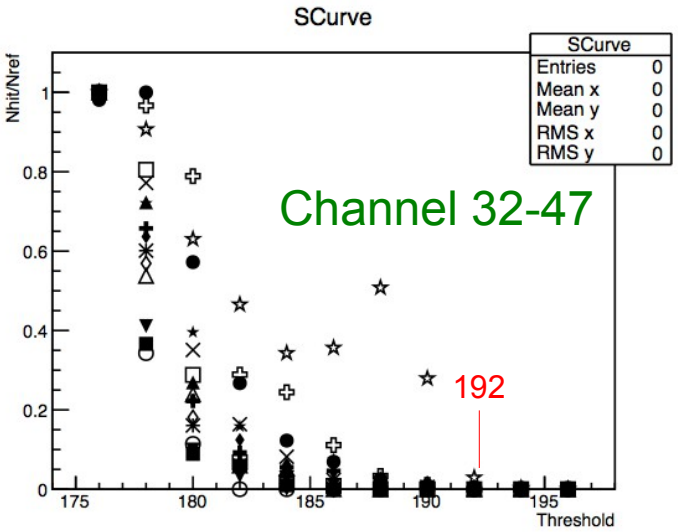
Support by:

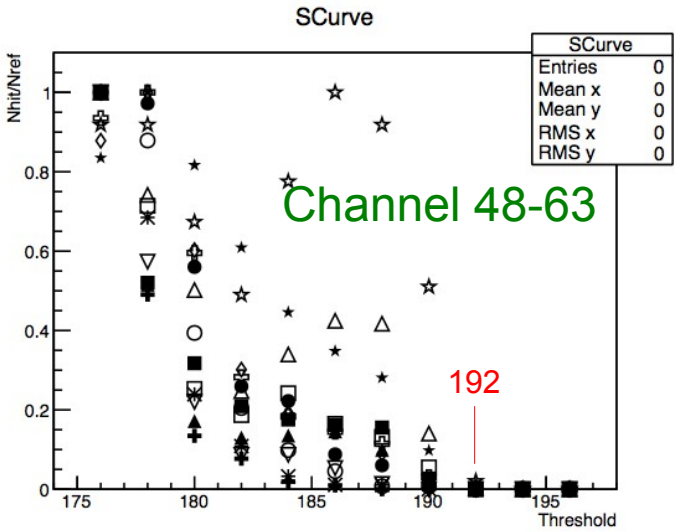
The first S-Curves

Chip0 after disabling of 7 channels: No charge injection









- S-Curves for Chip0 look reasonable up to excellent

- 192 DAC Counts is Common threshold for this ASIC (~1 – 1.5 MIPs)

- Remark: Tests with a better shielded Setup

  -> 5-10 DAC counts smaller threshold

FEV_COB Team – September 2015

Intensive debugging during September 2015

Visit of two students from SKKU and one form Kyushu
Possible thanks to FKPPL

Team from SKKU (Korea), OMEGA, LAL and Kyushu

FEV_COB Next steps

- Characterisation of available PCBs
  2 EOS Boards,
  One PCB has short cut after bonding (?), need to understand why
  Once understood -> can equip spare boards
  1 Protechno Board, 1 Exception Board (since 2013)
  S-Curves, charge injection, etc.

- Progressive improvement of experimental setup to scrutinise results

- Expect first solid conclusions by ~Xmass

- If results satisfactory: Equip PCBs with Si Wafers

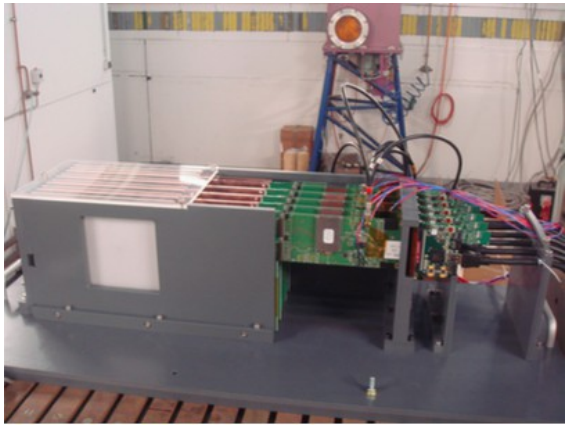
- Prepare production of new PCBs for Spring 2015
  - Proper shielding of ASIC pre-amps (current board still contains this bug)
  - (More) emphasis on mechanical properties
  - FEV8 -> FEV11 scheme
  - Strive for all-Korean solution

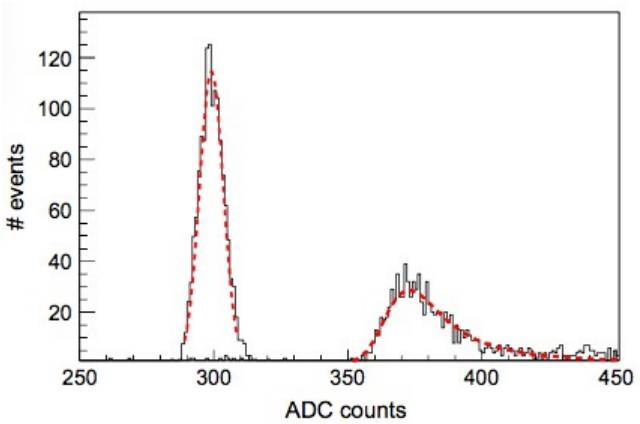
Data Analysis and papers

Two papers since last CALICE France Meeting:

SKIROC2 performance in 2012 beam test (NIM A 778 (2015) 78

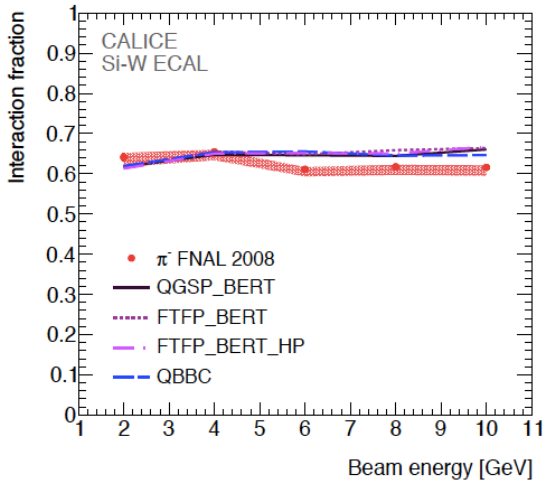
SiW Ecal group: Main author Thibault Frisson (IN2P3 Postdoc LAL, afterwards CERN)

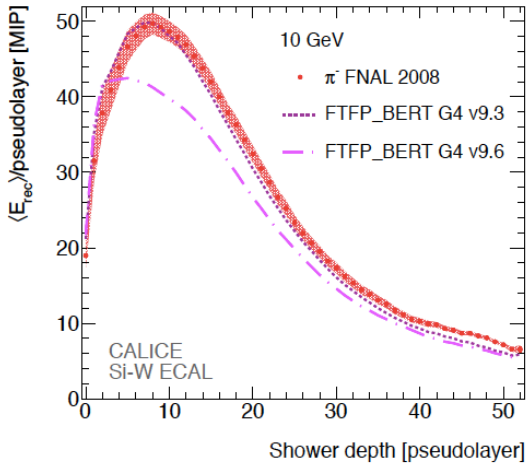




Hadrons in Ecal, FNAL data 2008 (NIM A 794 (2015) 240

CALICE Collaboration: Main author Naomi van der Kolk** (Postdoc P2IO [LAL/LLR], now MPP Munich)



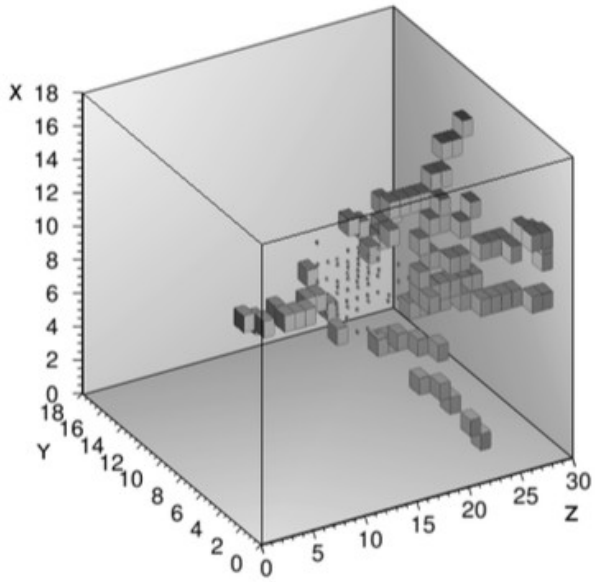


- Intensive discussion with G4 team!
- Seems that G4 Is too much tuned on scintillator!!!

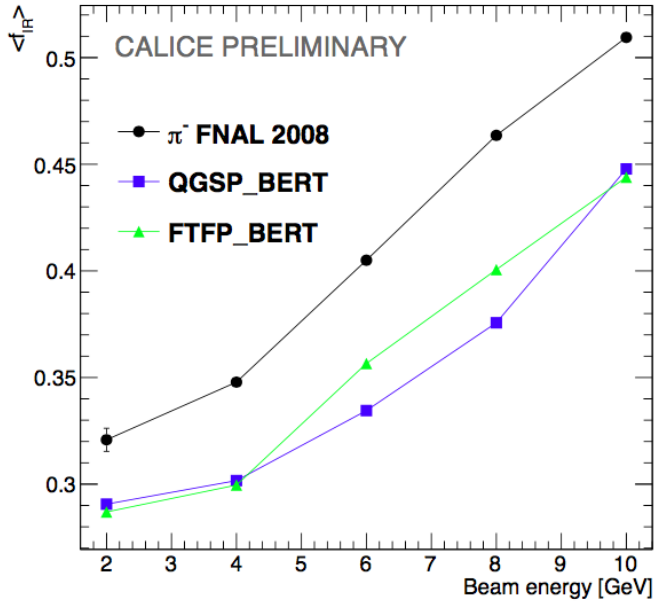
Ongoing Analysis

- Tracking in SiW Ecal
  SiW is one of the (maybe the) worldwide best devices to study first hadronic interaction

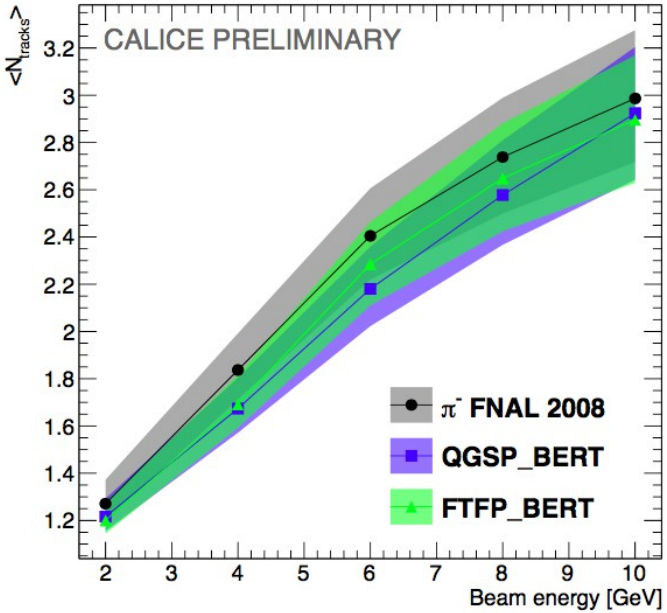
- Analysis by PhD Student Sviatoslv Bilokin (based on FNAL 2008 data set)



- Separation between Interaction zone and Outgoing tracks



- Energy deposition in interaction zone



- Number of tracks In SiW Ecal

- Novel analysis, will reveal details of G4 simulation and of role in Ecal in PFA

- Analysis note for CALICE Preliminary request in CALICE Editorial Board

Budget 2016

Personnel in 2016:

Chercheurs:

R.P. (100%)
S. Bilokin (100%)
D. Zerwas (50%)
F. Richard (100%)
E. Kou (30%)
F. LeDiberder (30%)

=> 4.1 FTE

Ingénieurs et Techniciens :
J. Bonis (40%)
A. Thiebault (40%)
P. Cornebise (30%)
C. Bourgeois (30%)
A. Gonnin (20%)
B. Mercier (10%)
C. Prevost (10%)
M. Fernandez (20%)
D. Breton (20%)
=> 2.2 FTE

Budget 2016

Demandes AP:

- Optimisation/Motorisation du banc d'assemblage : **15 kEUR**

- Cartes d'interface simplifiées, faux wafers pour tester l'assemblage: **5 kEUR**

- Contribution à l'achat des FEVN : **8 kEUR**

- Kapton HV pour couches longues et kapton d'interconnexion: **7 kEUR**

- Révision cartes lecture numérique et distribution pour multi-slab: **10 kEUR**

=> Démandes a l'in2p3 AP: 45 kEUR

Budget 2016

Démandes Missions 2016:

- Sémaine omnibus ILC en Europe : 4x1000 EUR = **4 kEUR**
- Réunion CALICE en Amérique du Nord : 2x2000 EUR = **4 kEUR**
- Réunion CALICE en Europe : 4x1000 EUR = **4 kEUR**
- LCWS16 en Asie : 2x3000 EUR = **6 kEUR**
- Test en faisceau au CERN 2x2 sémaines
  3 ingénieurs pour une sémaine chacun (mise en operation):
  3x1000 EUR = **3 kEUR**
  3 chercheurs pour couvrir ~ 6 sémaines
  6x500 EUR = **3 kEUR** (+ 6x500 EUR par AIDA2020 TA)
- Divers (Top workshop, CALICE Elec. And DAQ Meeting, JCL 2016, etc.)
  5000 EUR (forfaitaire) = **5 kEUR**
- Intégration ILD
  3000 EUR (forfaitaire) = **3 kEUR**

=> Démandes à l'in2p3 Missions: 32 kEUR

Budget 2016

Démande PostDoc de trois ans:

1) Travaux pour Prototype technique de l'Ecal (Testbeam, Labtests etc.)
2) Intégration du nouveau système de lecture
3) Synérgie avec ATLAS (à préciser)

Démande Thésard:

1) Analyse données test en faisceau
2) Sujet de physique (à préciser)

Démande ingénieur sous contrat (Niveau IE, à voir avec le SERDI du LAL):

- Etudes système de lecture numérique (0.5 – 1 FTE)

Summary and outlook

- LAL team is preparing for assembly of short layers
  Synergies with ATLAS (and CMS) to be developed/extended

- Important exercise with experimental model of a layer
  Many different steps that have to be mastered!!!
  Experience will be input to further automatisation (objective of AIDA-2020)
  Assembly has to become integral part of detector design!

  LAL team is fragile but skillful!

- Continuing R&D on Chip on Board solution

  Continuation with profound debugging until end of the year
  Then equipment with wafers and new production
  Need sustained support
  FKPPL cannot remain the only source of funding !
  MOU with SKKU? what else ... ?

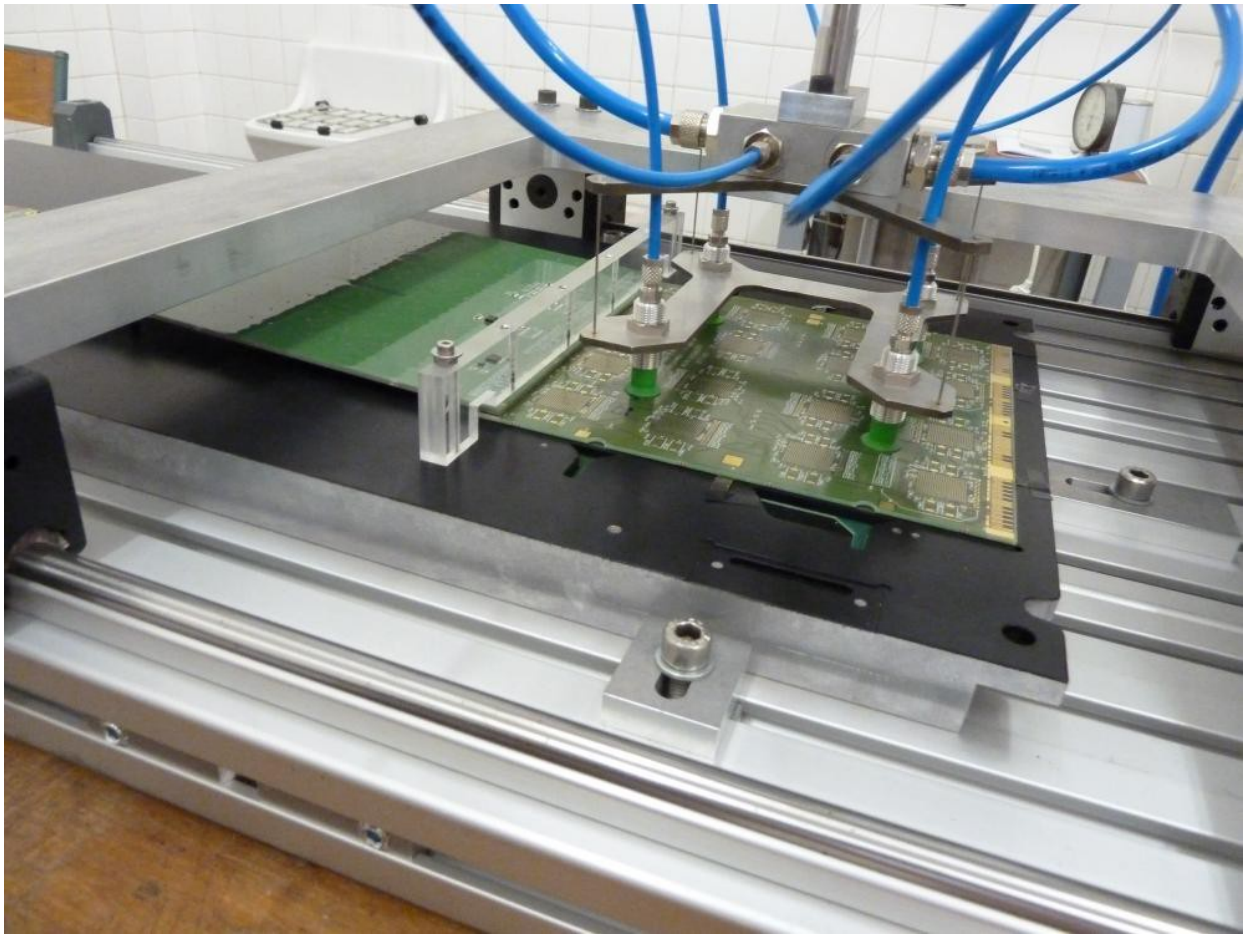
- Continuing wiht data analysis
  Two published papers since last CALICE France Meeting
  Ongoing analysis on Tracks in Ecal

- Request 2016 to IN2P3 (Not only on Ecal/CALICE matters)
  45 kEUR (AP), 32 kEUR Missions, Manpower

Backup

Steps of assembly

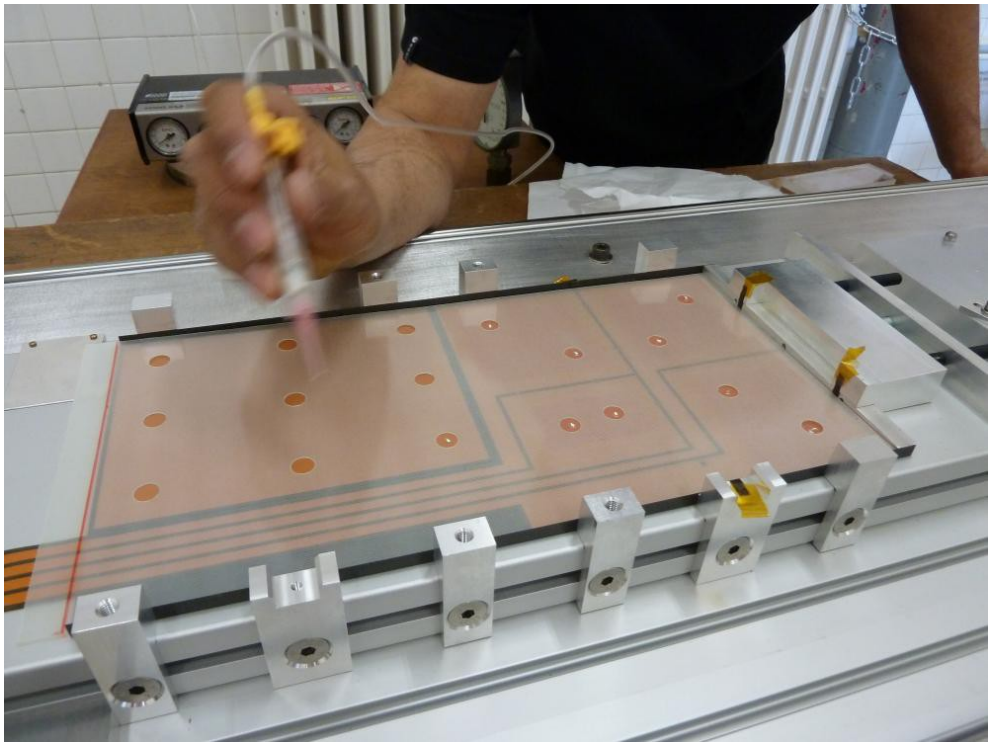
2. Picking PCB from delivery plate



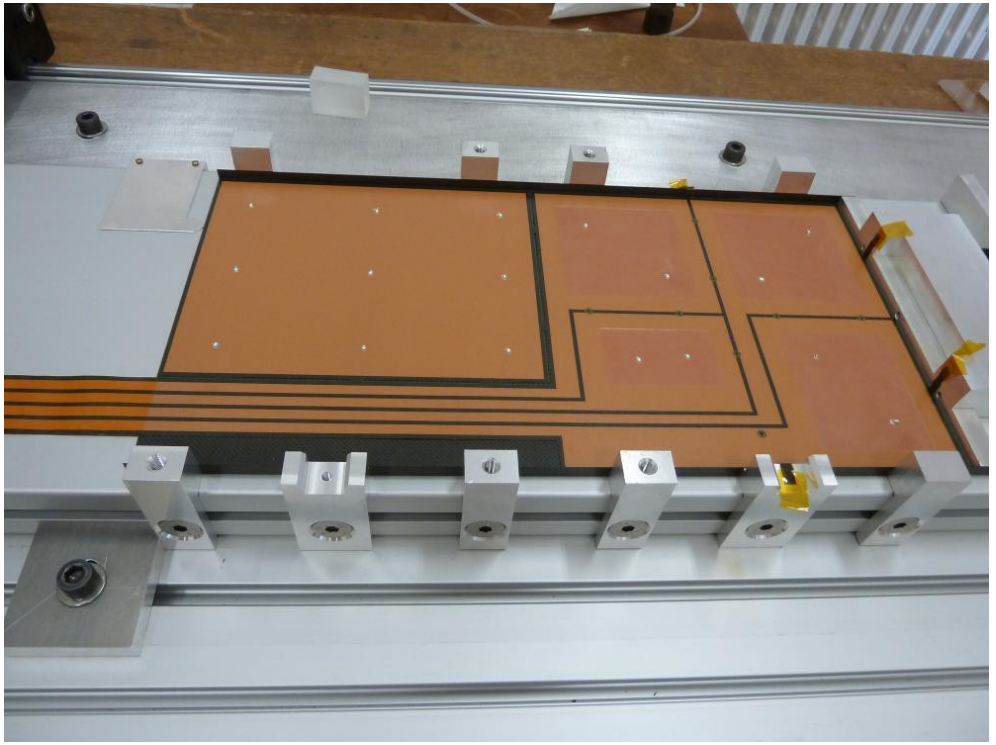
Steps of assembly

3. Preparing the HV Kapton

Placing glue dots for connection SiWafer – HV Kapton



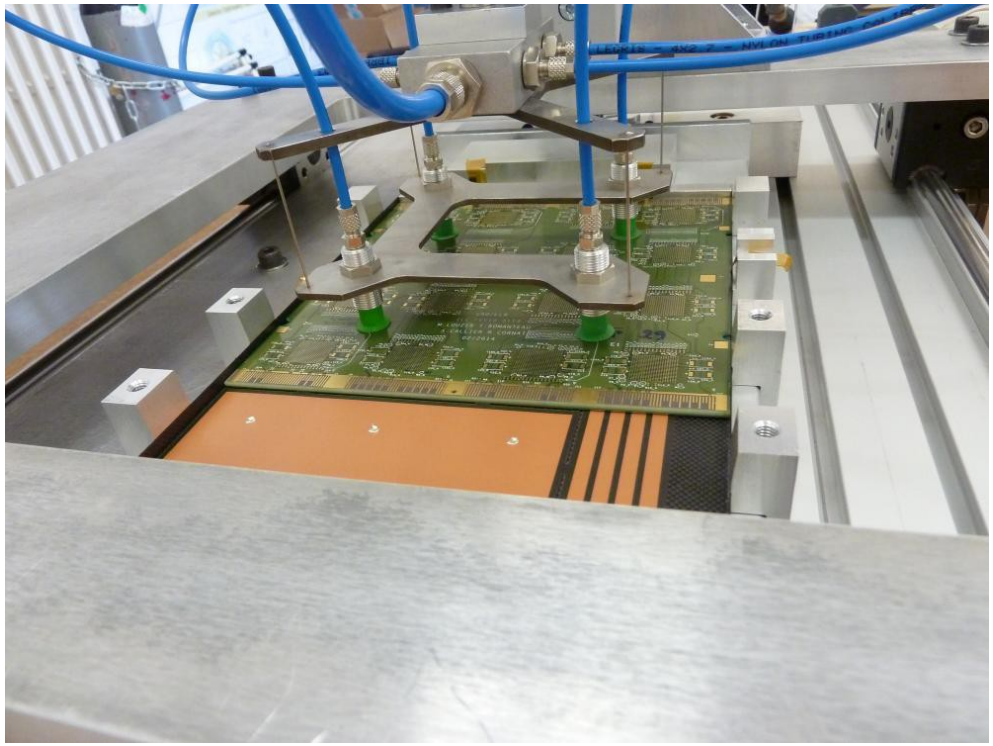
Well controled paramters at well defined spots

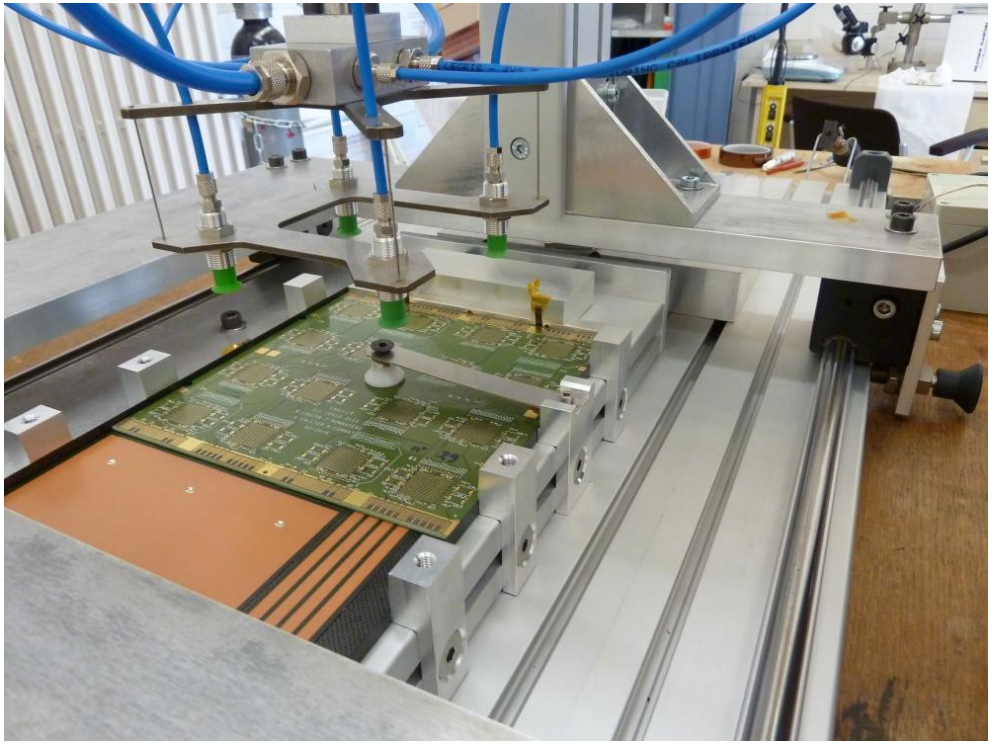


Proper grid of glue dots

Steps of assembly

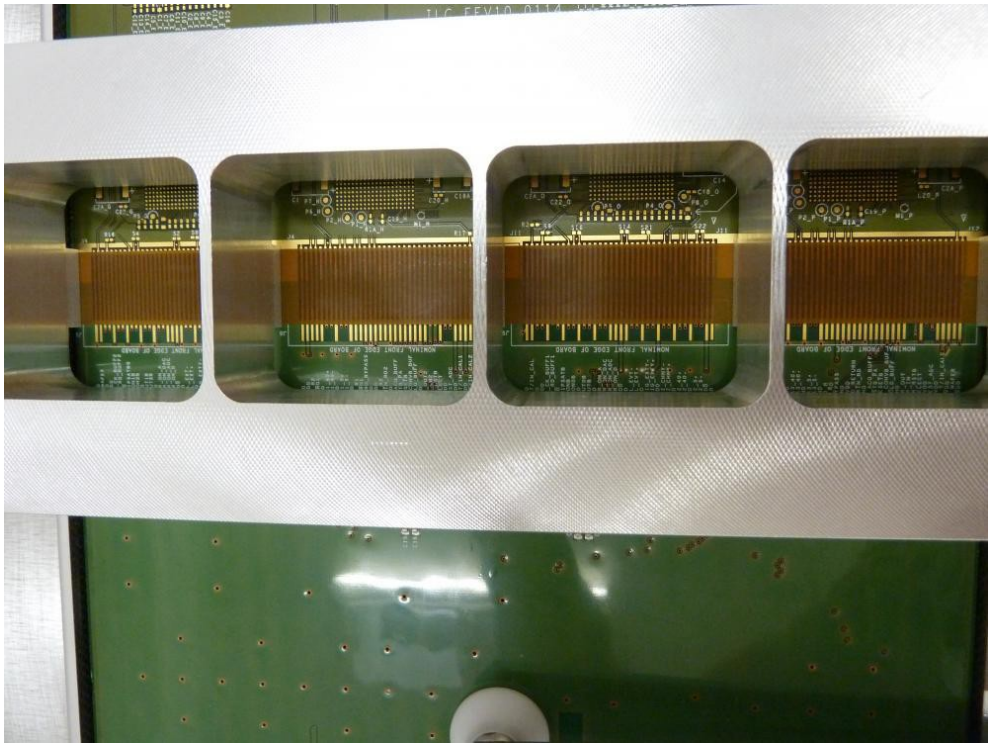
4. Placing and fixing





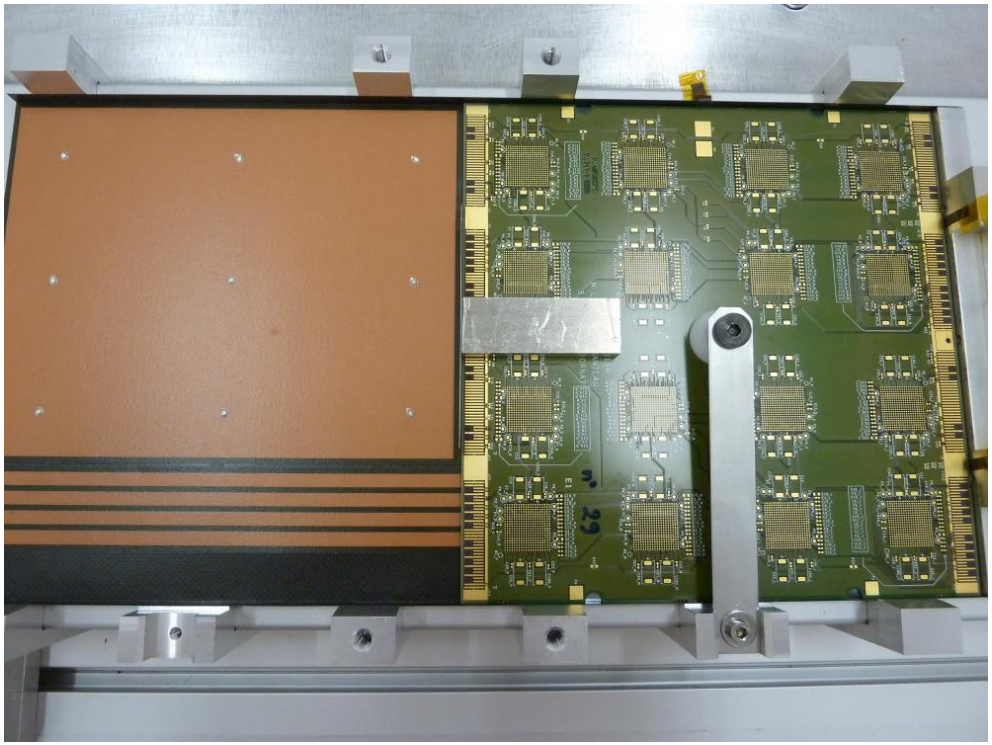
Steps of assembly

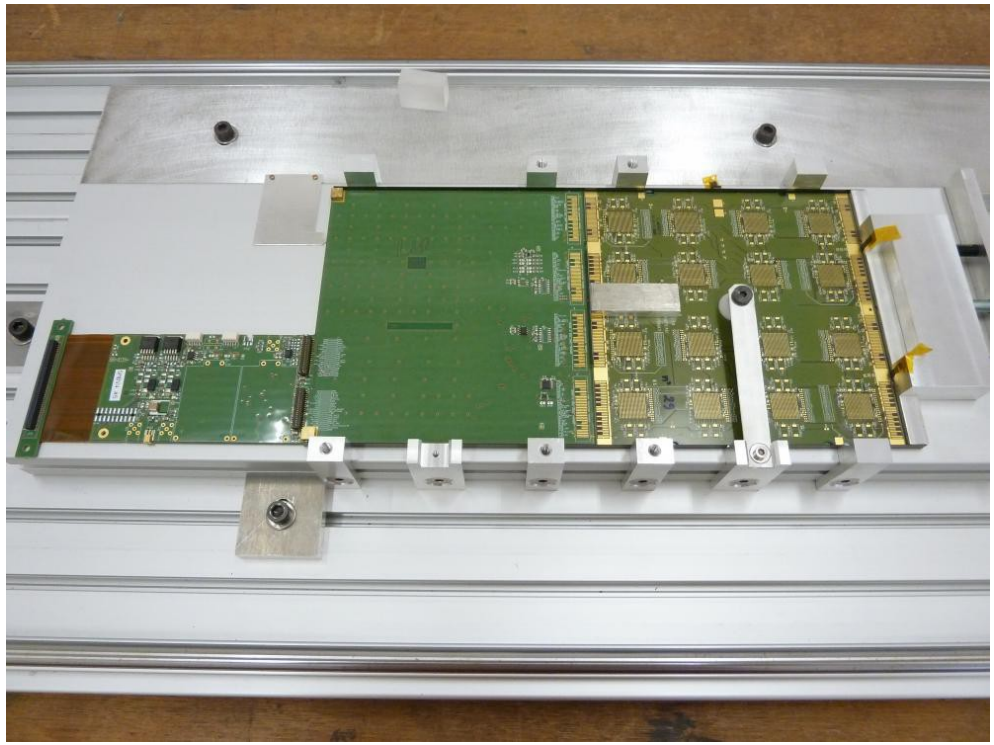
6.1 Interconnection – Placing the frame



Steps of assembly

5. Adapter card alignment (applies also for further ASUs)

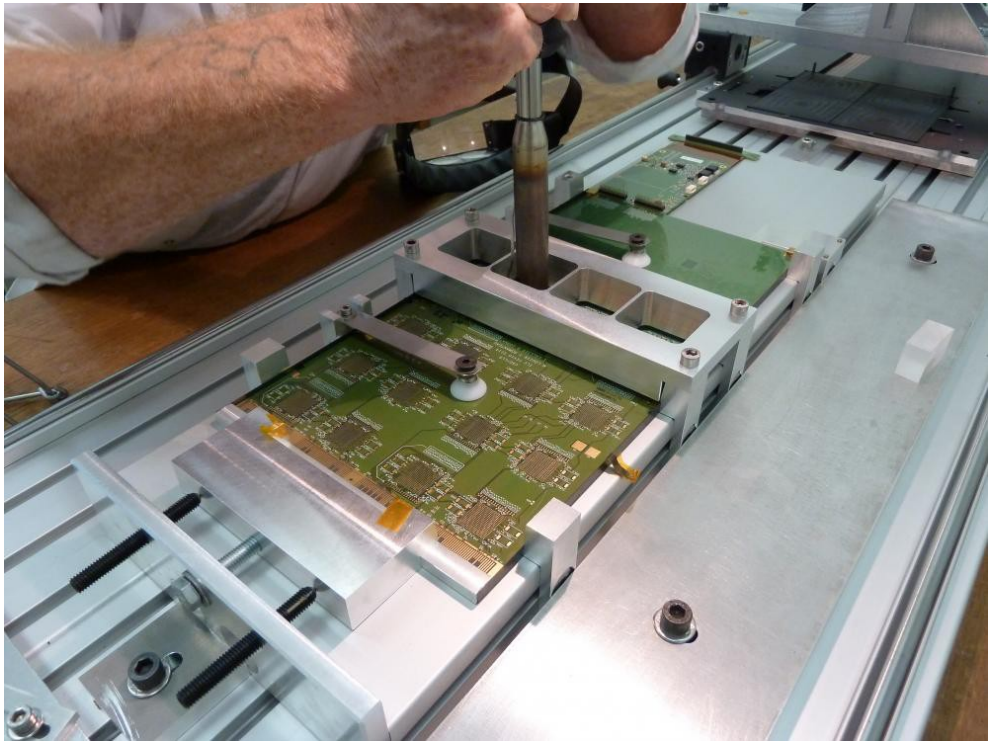




6.2 Interconnection – Do the job

... following carefully studied specifications

Interconnection in/on assembly bench

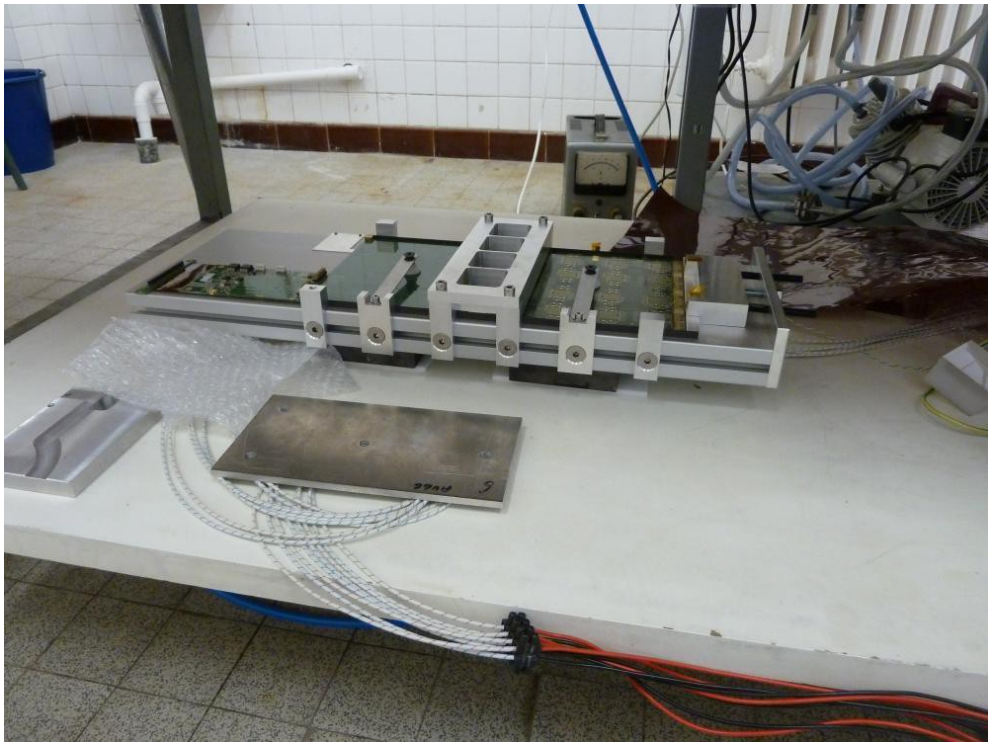


Human being to be “replaced” by robotic procedure (AIDA-2020)

- This part of the assembly has to be very carefully integrated into planning of detector design!!!

Steps of assembly

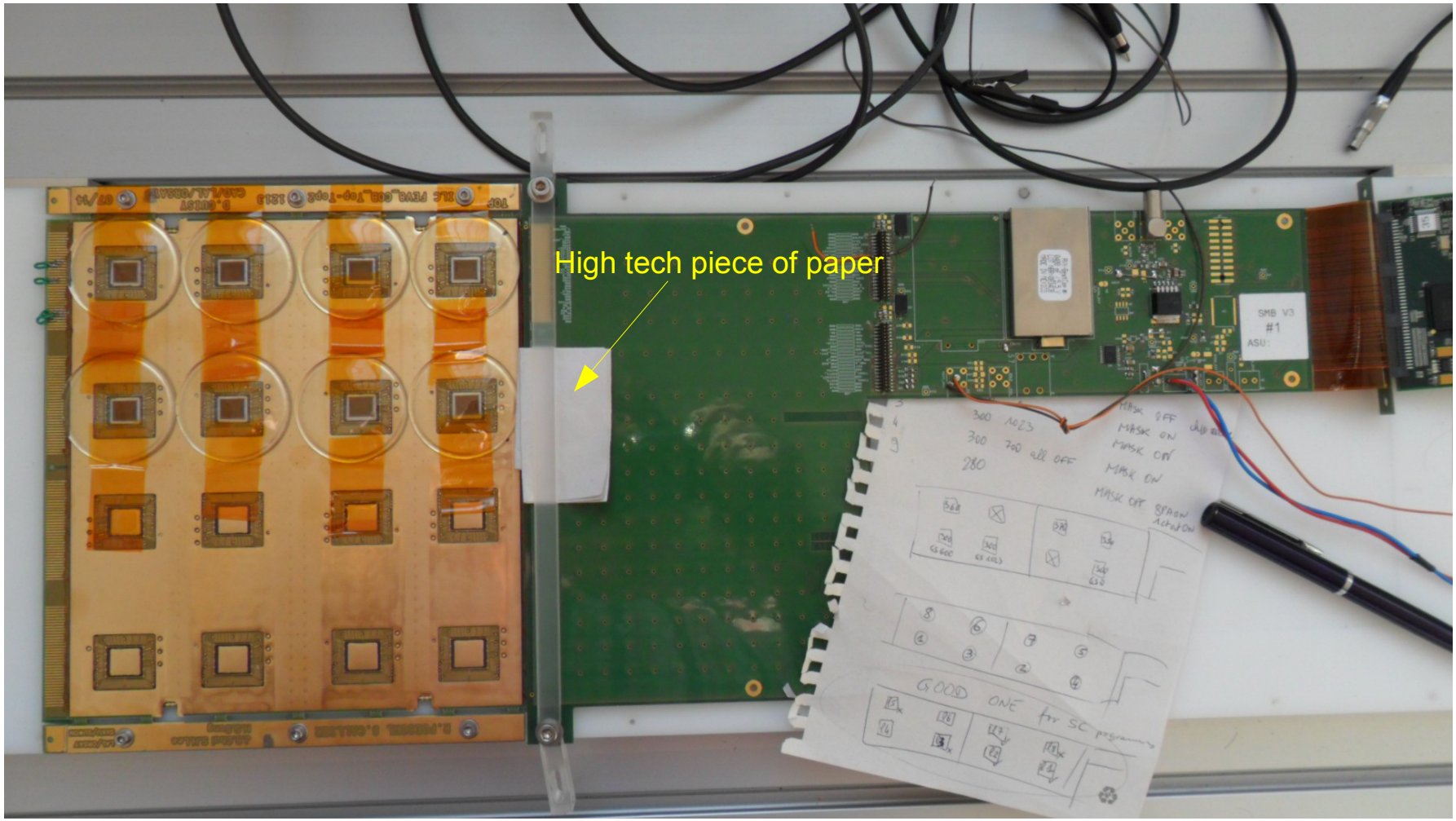
7. Polymerisation (Gluing PCB – HV Kapton)



Layer remains in cradle during polymerisation

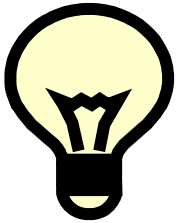
Polymerisation for about 1/2 day at 40° C
(Check time with experts)

FEV8_COB – On test bench



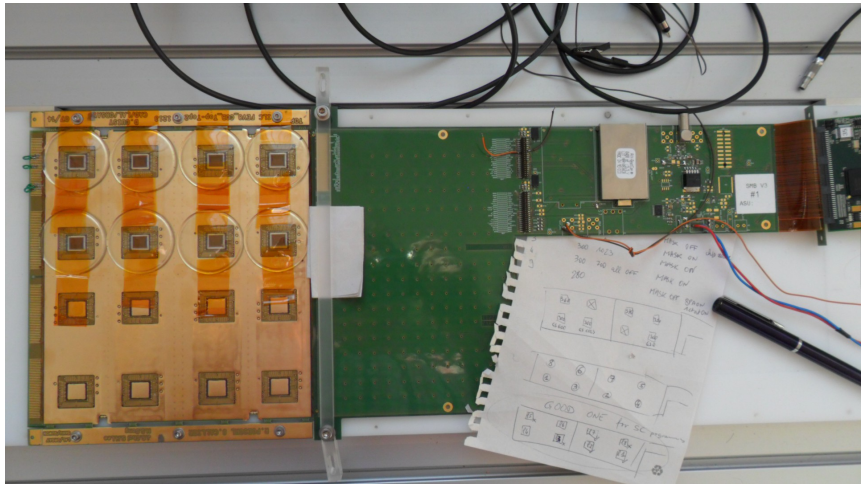
Integrated smoothly with existing hardware and current version of calicoes/pyrame software

A bright idea ...

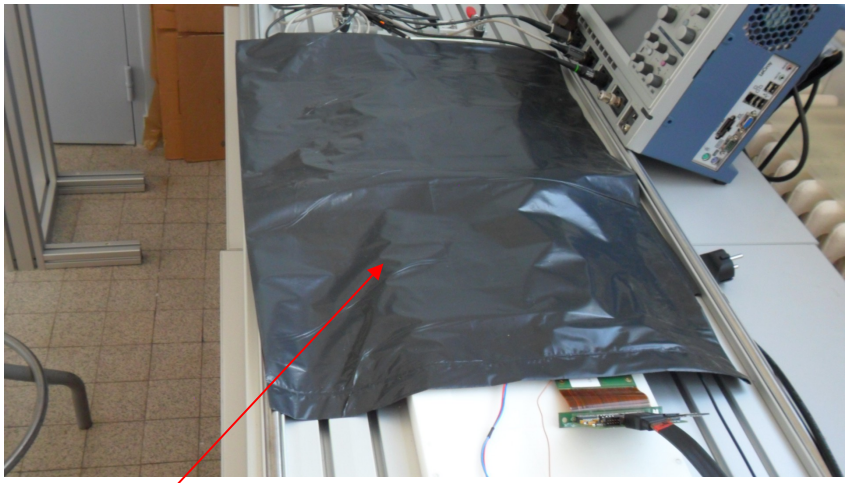


... by Christophe: Put set-up into dark environment

Doesn't work!



Works !



Black plastic waste bag

Lesson: Naked dies are very sensitive to ambient light