



## Generic Electronics for TPC Architecture

**Generic electronic system going from the front end to data storage**

journée annuelle détecteurs gazeux - 10 septembre 2015 - Subatech, Nantes

# GET Collaboration

Faisal Abu-Nimeh<sup>4</sup>, Shebli Anvar<sup>1</sup>, H. Baba<sup>5</sup>, Pascal Baron<sup>1</sup>, Daniel Bazin<sup>4</sup>, Chiheb Belkhiria<sup>2</sup>, Bertram Blank<sup>2</sup>, Joël Chavas<sup>1</sup>, Patricia Chomaz<sup>1</sup>, Eric Delagnes<sup>1</sup>, Frederic Druillole<sup>1</sup>, Jerome Giovinazzo<sup>2</sup>, Patrick Hellmuth<sup>2</sup>, Cedric Huss<sup>2</sup>, Eugene Galyaev<sup>4</sup>, Bill Lynch<sup>4</sup>, Wolfgang Mittig<sup>4</sup>, Tetsuya Murakami<sup>5</sup>, Laurent Nalpas<sup>1</sup>, Jean-Louis Pedroza<sup>2</sup>, Emanuel Pollacco<sup>1</sup>, Riccardo Raabe<sup>3</sup>, Jérôme Pibernat<sup>2</sup>, Bruno Raine<sup>3</sup>, Abdel Rebi<sup>2</sup>, Atsushi Taketani<sup>5</sup>, Frederic Saillant<sup>3</sup>, Patrick Sizun<sup>1</sup>, Daisuke Suzuki<sup>4</sup>, Nathan Usher<sup>4</sup> and Gilles Wittwer<sup>3</sup>.

<sup>1</sup> IRFU/SPhN, CEA-Saclay, Cedex 91191 Gif-sur-Yvette, France

<sup>2</sup> CENBG, Chemin du Solarium, 33175 Gradignan Cedex, France

<sup>3</sup> GANIL, Bd Henri Becquerel. BP 55027, 14076 Caen Cedex 05. France

<sup>4</sup> NSCL, MSU, 1 Cyclotron, East Lansing, Michigan 48824-1321, US

<sup>5</sup> RIKEN, 2-1 Hirosawa, Wako, Saitama 351-0198, Japan

# PROJECTS TESTING OR DEPLOYING GET

- TPC in Magnets

-  SPIRIT(RIKEN, MSU)\*,#

- E52 (J-PARC, Jp)#

-  AT-TPC (FRIB, US)\*#

- IBS-TPC (IBS, Kr)

- Pusan National Univ (Kr)

-  IKS-TPC(Be)

- Solid-State Devices

- FARCOS (INFN-Catania, IT)

- TRACE/GASPARD/ ...  
(IRFU, IPNO, INFN-Padova, IT)

\* - System Developers

# - System Building

- Funding

22 systems in 6 countries

80k channels built to date

 erc

- Beam Trackers

- CAST (IRFU, Fr)

- n\_ToF (IRFU,CERN)#

- S<sup>3</sup> (SPIRAL2, Fr)#

- Spectro (IPN-Orsay,Fr)#

- Spectrometer (IRFU, TAMU)

- FALSTAFF (IRFU)

- TPC

- AstroBox (IRFU, TAMU, IFIN)#

- *2p-TPC (CENBG, GANIL, Fr)\*#*

- Active-Targets

- TexAT-P (TAMU,US)#

- *ACTAR-TPC(SPIRA2, Fr)\*,#*

- Lanzhou-TPC (IMP,Cn )

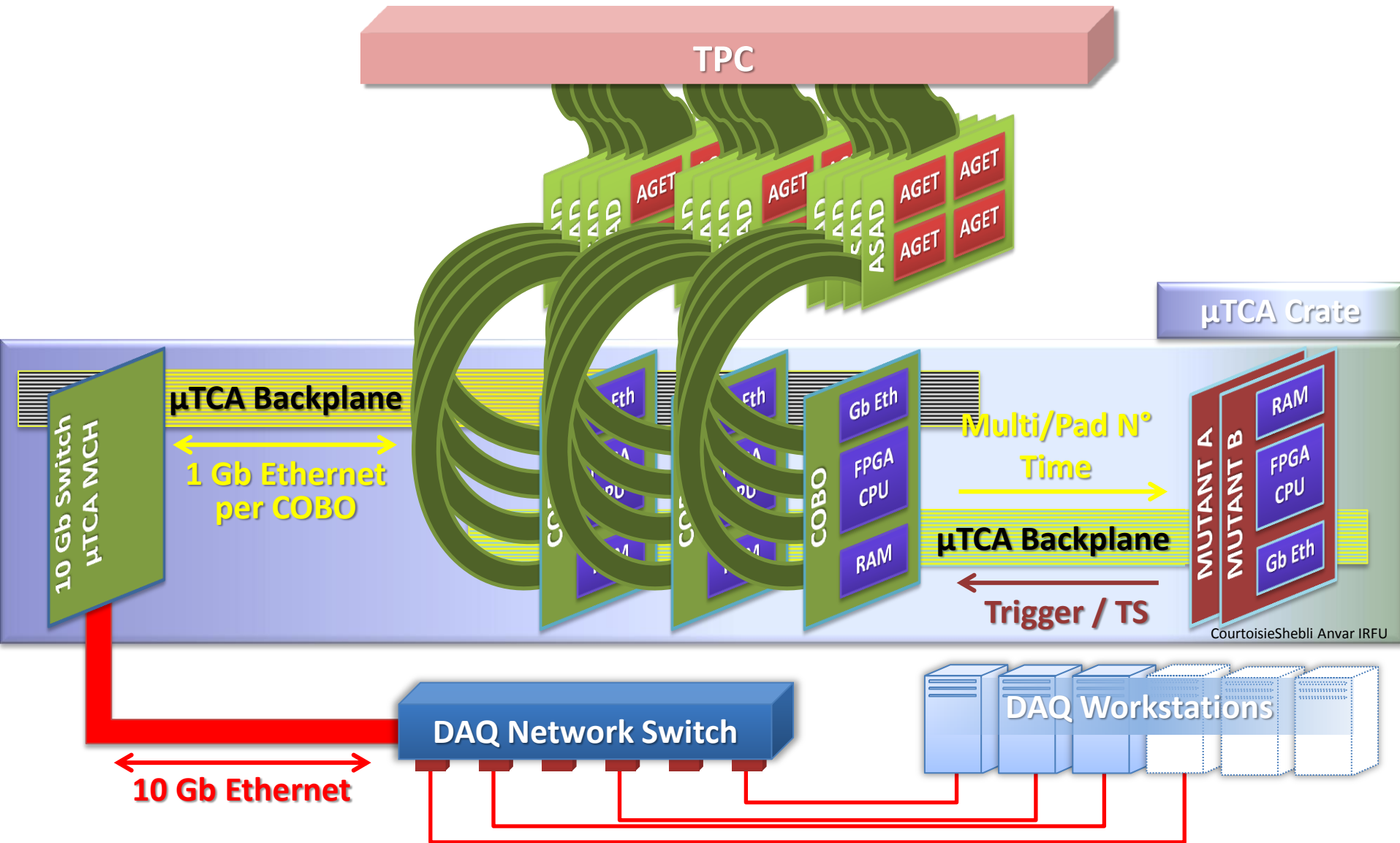
- Tokyo-TPC (Jp)#

- iTPC (SINAP, Cn)

 erc

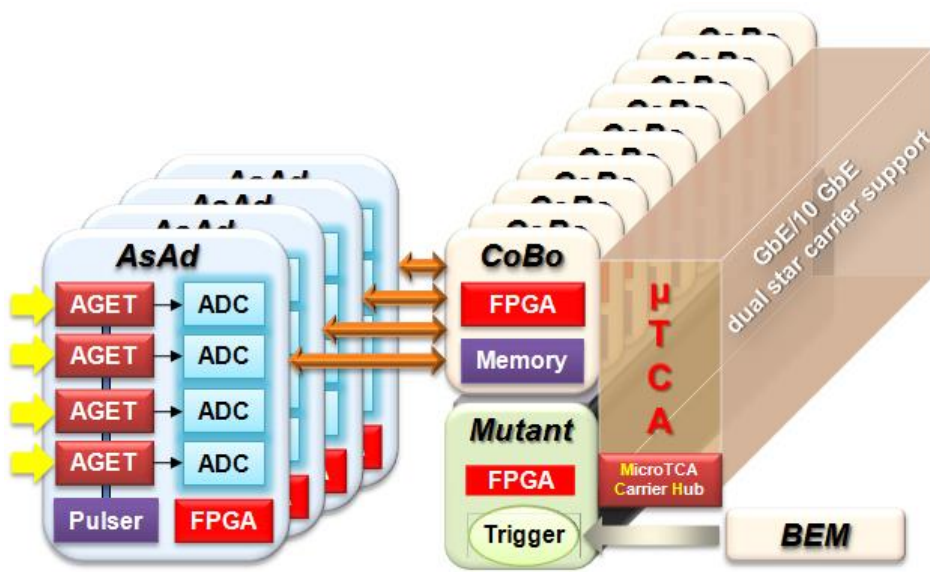
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# Hardware Architecture

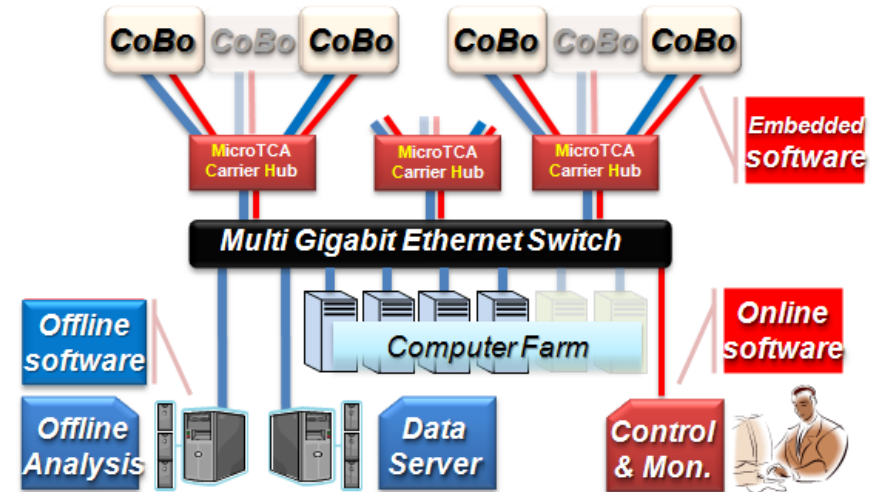


CourtoisieShebli Anvar IRFU

# Hardware Architecture (2)



*GET conceptual design*



*Network topology*

## AGET

**ASIC** based on AFTER chip [ref.1]  
New features [self-triggering, readout time ...]

## AsAd

(ASIC Support & Analog-Digital conversion)  
4 **AGETs**,  
4x12-bit ADC,  
Pulser.

## CoBo

(Concentration Board)  
4 **ASADs** control stamp,  
Zero suppress, Data compression.

## MUTANT

(Multiplicity Trigger And Time)  
10 **CoBos** control Multiplicity,  
Trigger building,  
Clock distribution.

## BEM

(Back-End Module)  
Interface with other ancillary equipment.  
time stamping,  
remote master trigger.

***μTCA crate***: 1 Mutant & 10 CoBos => 10240 channels [3 *μTCA* crates for 30 k channels]

# Asic AGET

## Mean features

Input current polarity: positive **or** negative

**64** analog channels

**4** charge ranges/channel: 120 fC, 240 fC, 1 pC & 10 pC

**16** peaking time values: 70 ns to 1  $\mu$ s

**512** analog memory cells / channel

Fsampling: 1 MHz to 100 MHz; Fread: 25 MHz

**Auto triggering** : discriminator + threshold (DAC)

**Multiplicity signal**: analog OR of the 64 discri. Outputs

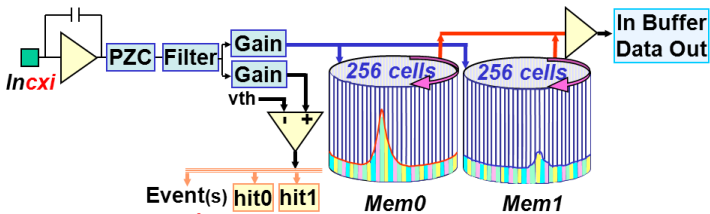
## Main features for the readout

- Address of the hit channel(s)

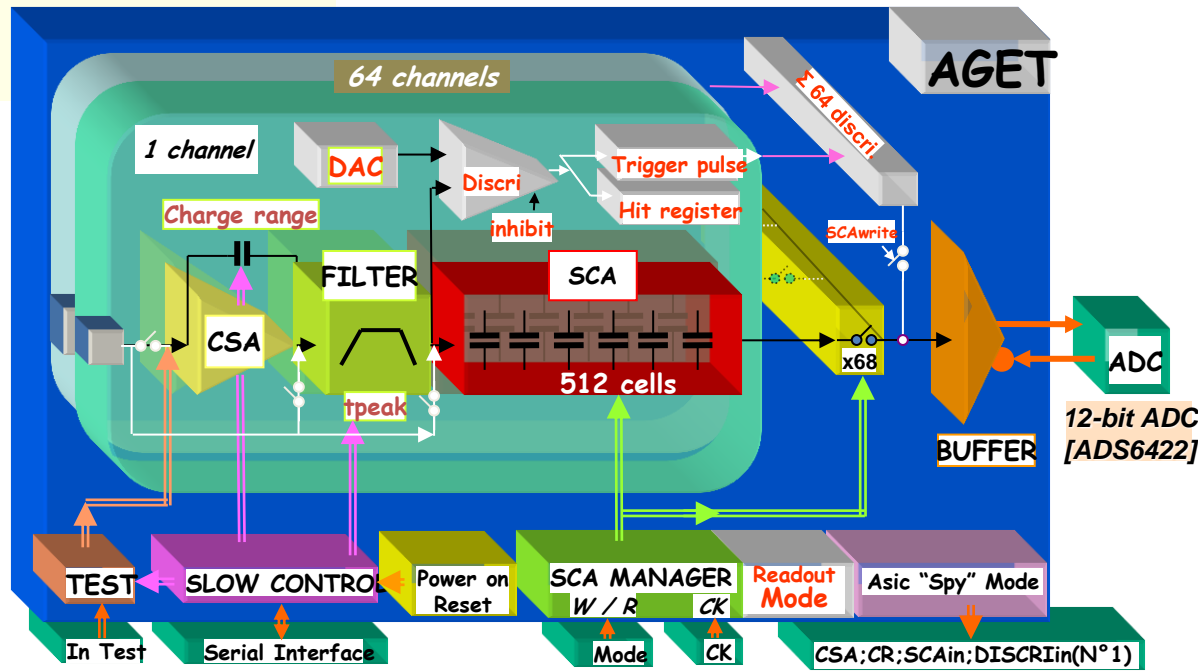
- 3 readout modes:

All, hit or specific channels

- Predefined number of analog cells / trigger (1 to 512)

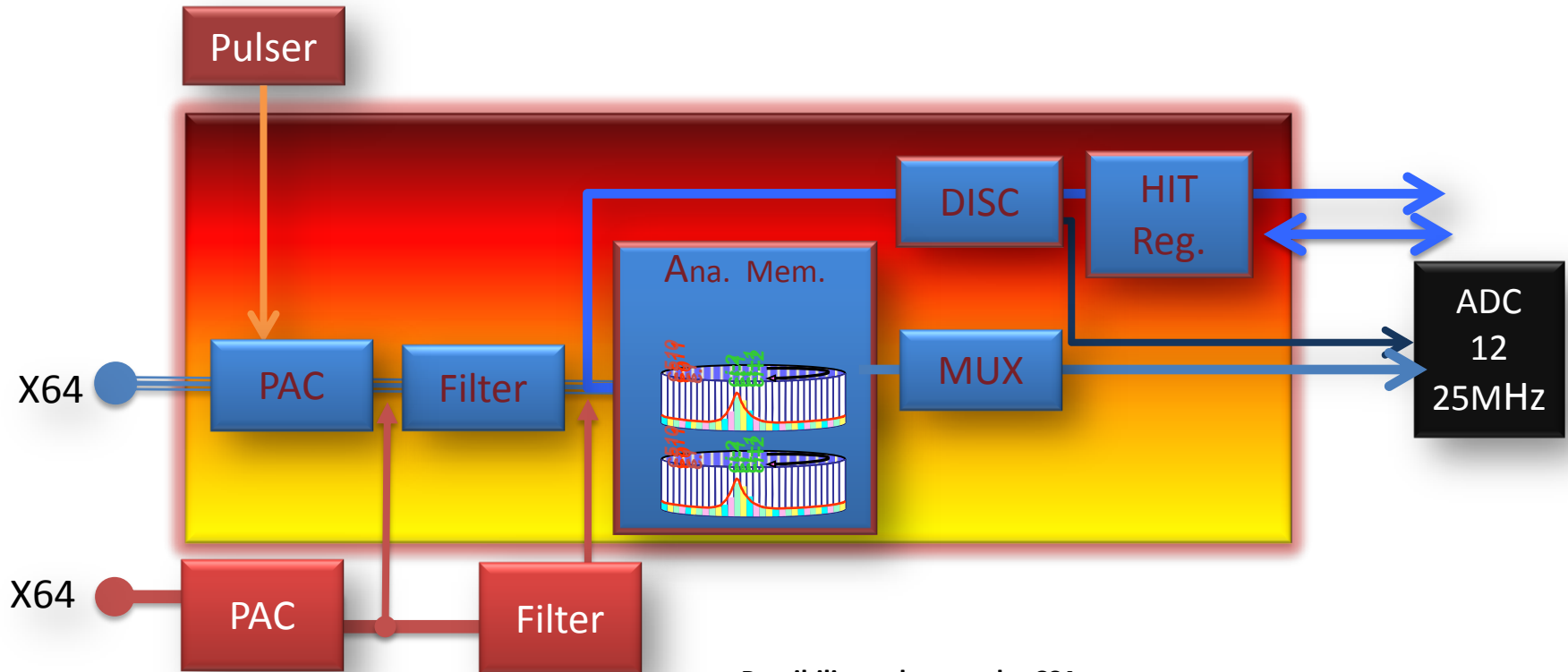


SCA : memory can be split in 2 x 256 cells



E. Delagnes – P. Baron

# AGET-MUX



**Possibility to bypass the CSA**  
*enter directly into the RC2 filter or SCA inputs*

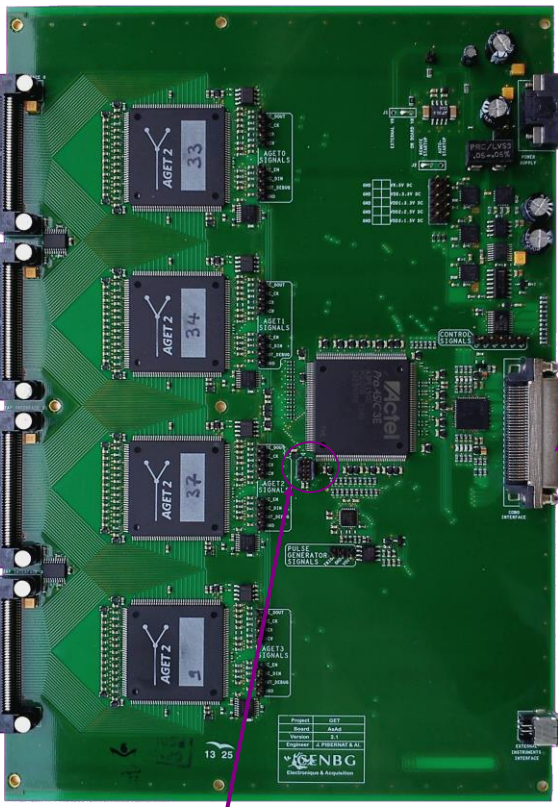
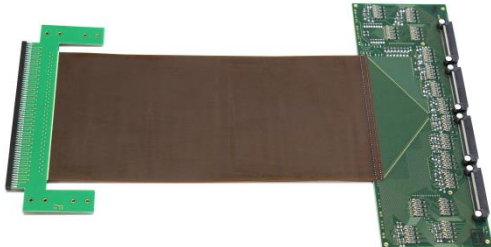
CSI, DSSSD...

# AsAd FRONTEND

- 10 layers Class 6/7 PCB (Double Europe standard)
- More than 700 components, mounted on one side only
- 2200 connections
- Firmware, developed in VHDL implemented on a FPGA

## Input interface

- 64 Channels
- 8 Ground connections
- 4 P.S. direct connections
- 4 P.S. switch-controlled connections
  - 2 for ZAP protection bias
  - 2 for channels disconnections



## Power interface (Molex μD)

- 3.6V – 5W standard power supply

## Control/Data interface (VHDCI68 / cable of 3m)

- 1 AsAd-control serial port
- 4 AGET-control serial ports
- 4 ADC-data serial ports
- AGET sampling/readout control
- Power control

## Instruments interface (Molex firewire)

- 2 Digital inspection lines
- External trigger for step voltage generator

## Programmer interface

- Firmware and serial number upload

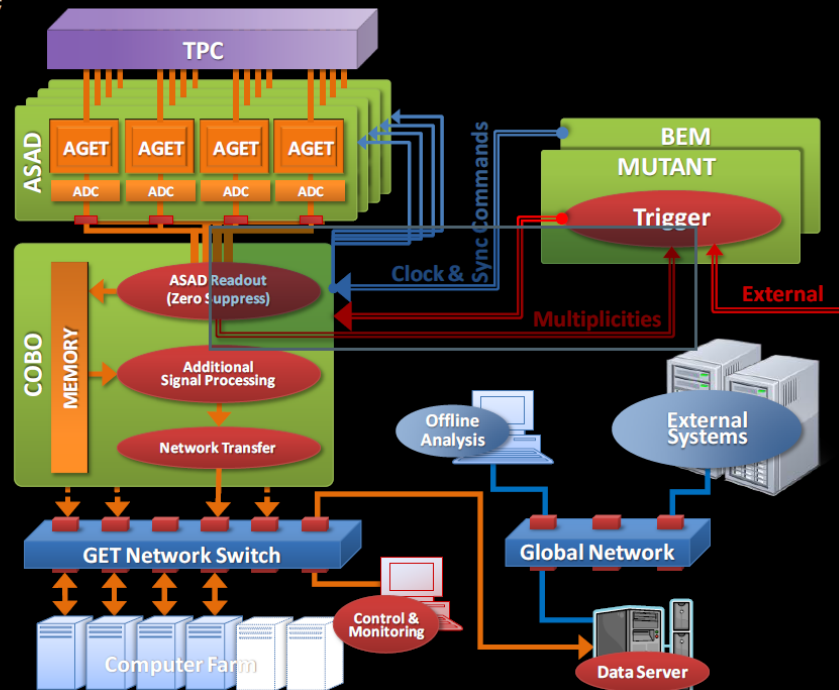
GET GM VI St Avit 09/2014 J. Pibernat



# CoBo

## Concentration Board

- Data sink and interface between AsAd and network
  - Perform data reduction and formatting from AsAd ADC serialized output
  - Buffering to maximize throughput
  - Time stamp for synchronization
  - Relay multiplicities and hit patterns to MuTanT for trigger decision
  - Perform slow control setting of AGET, AsAd and CoBo registers

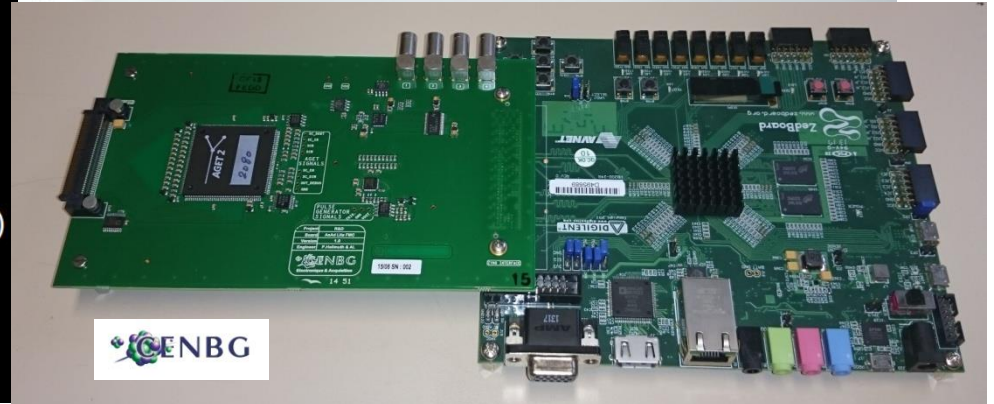


Daniel Bazin

# RCoBo

## Reduced CoBo

- Can pilot one AsAd board only (256 channels)
- New adapter board now tested with AsAd v2.1
- Future of ML507?
  - No longer manufactured
  - Virtex5 now old generation (Virtex7 and Virtex Ultrascale already out)
  - Move to ARM technology (Zynq)
  - Use FMC standard on adapter board (compatible with all evaluation boards)



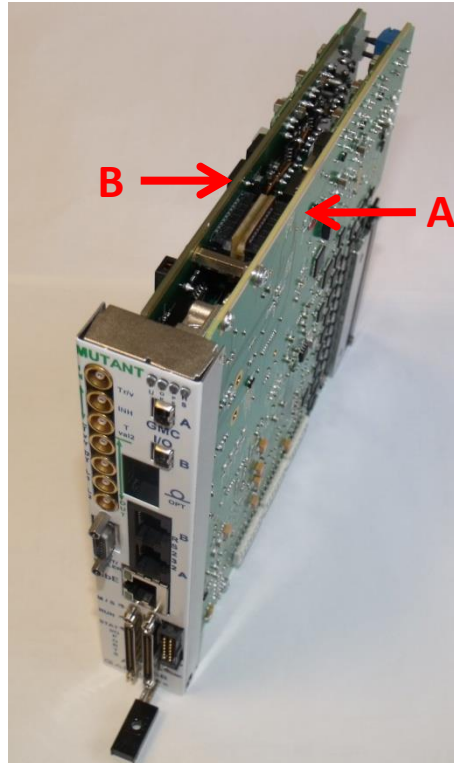
# 1 module – 2 boards

## MuTanT

Multiplicity

Trigger  
(L0,L1,L2)

and Time  
(+ Event Number)



Board B: - Trigger/timestamper engine

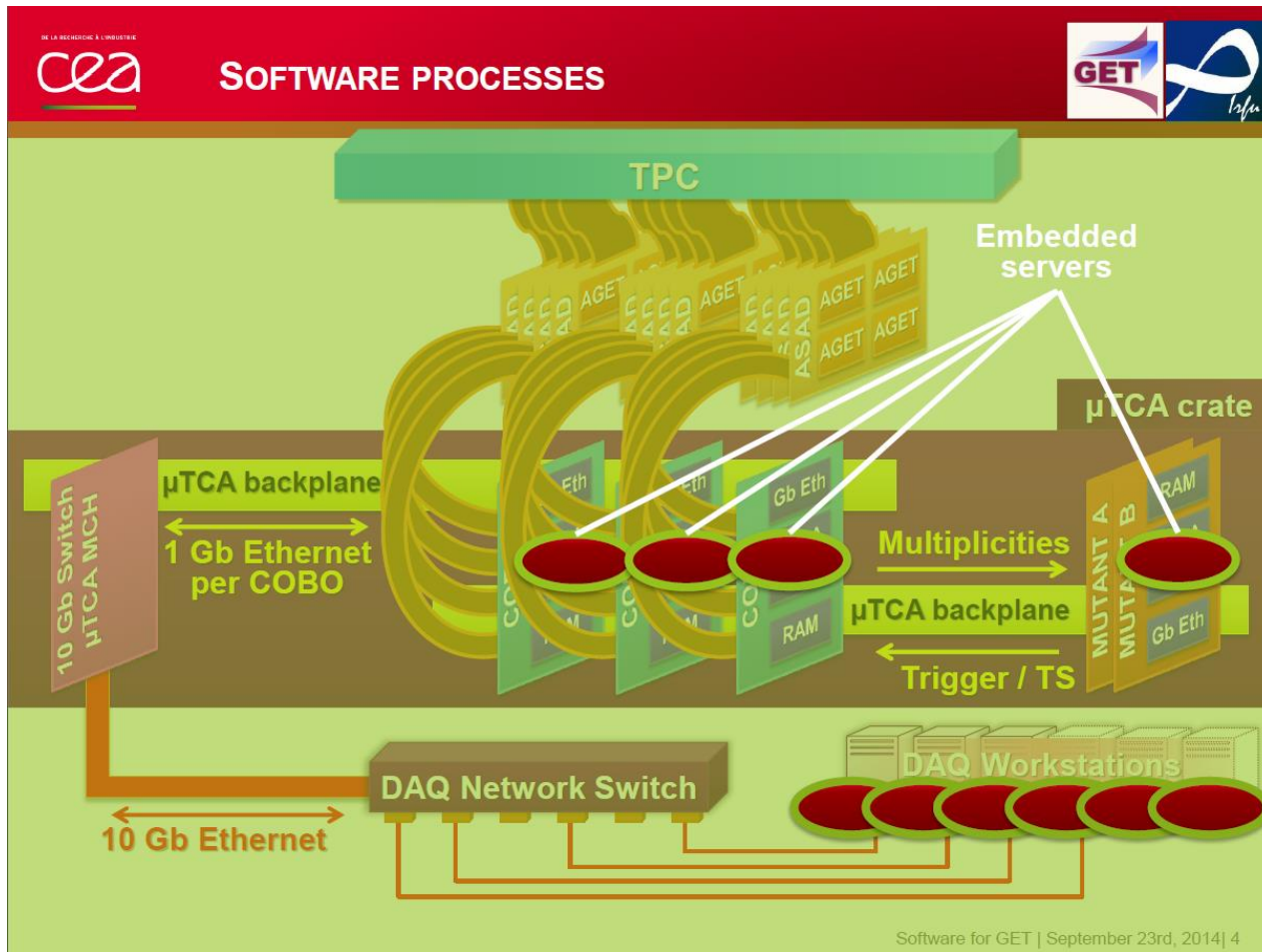
Board A: - GMC/WSCA distribution  
- Embedded system (Linux)

- L0: External trigger
- L1: Multiplicity trigger
- L2: Trigger on hit pattern



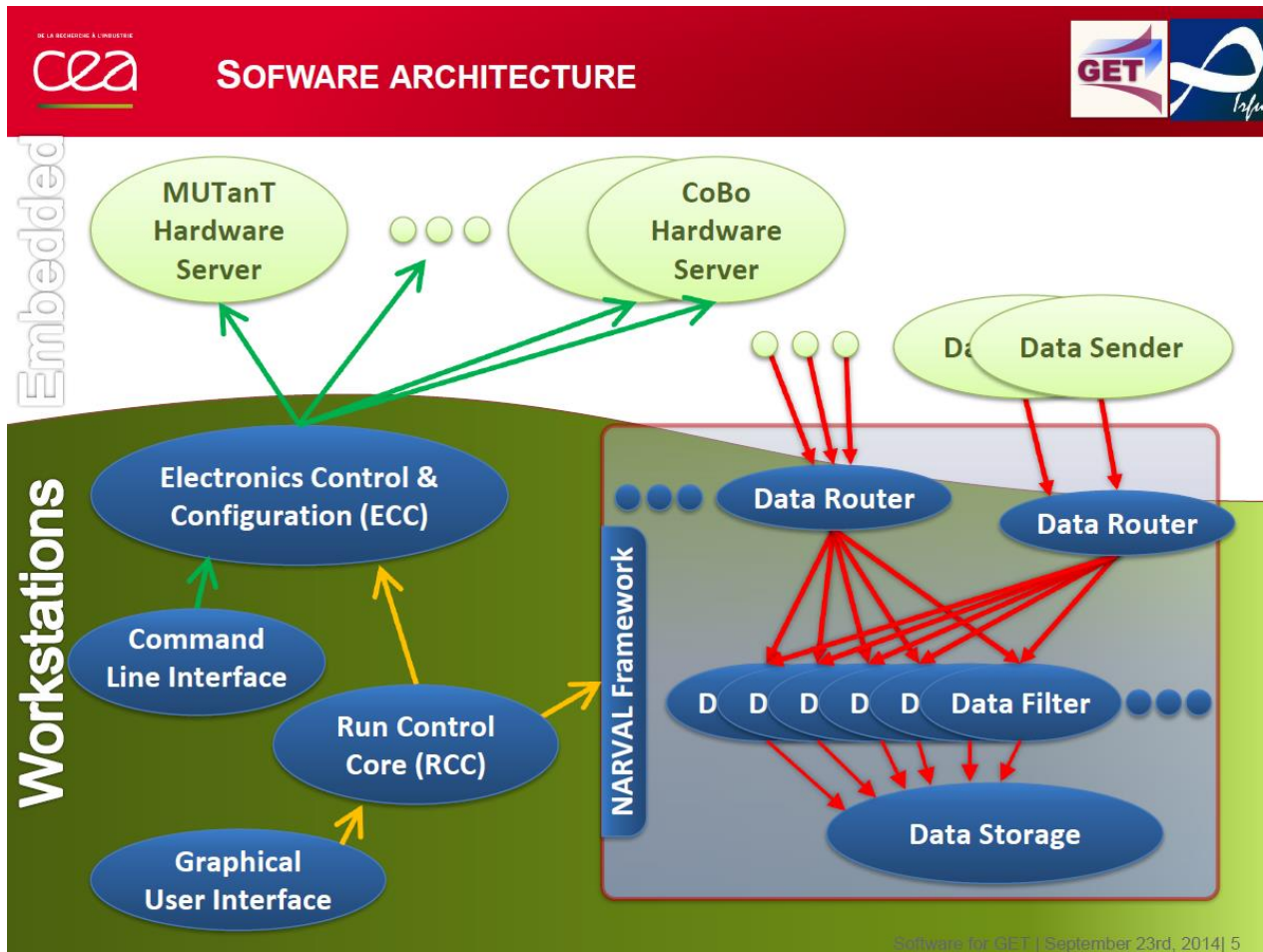
Gilles Wittwer

# Software architecture



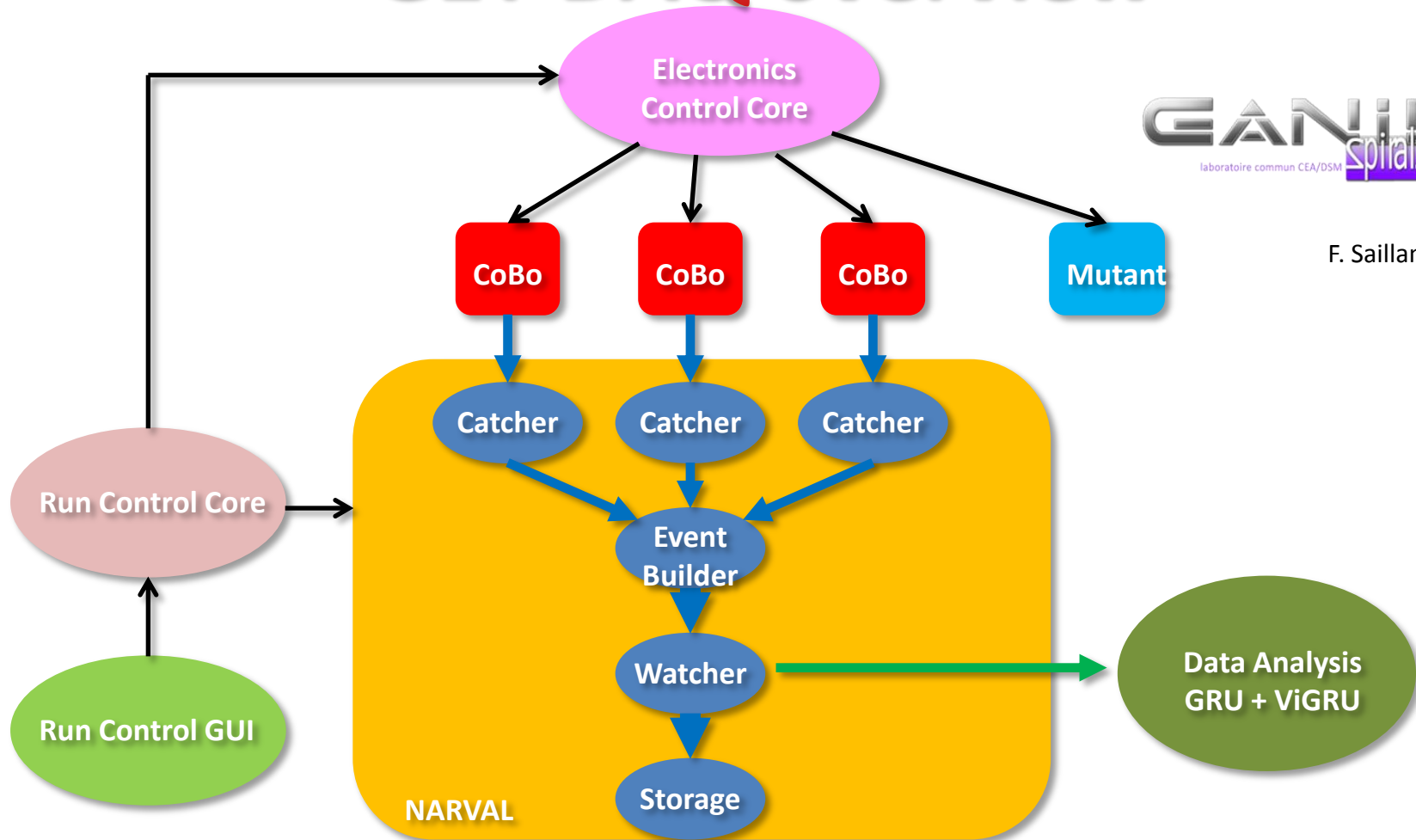
Sh. Anvar P. Sizun

# Software architecture (2)

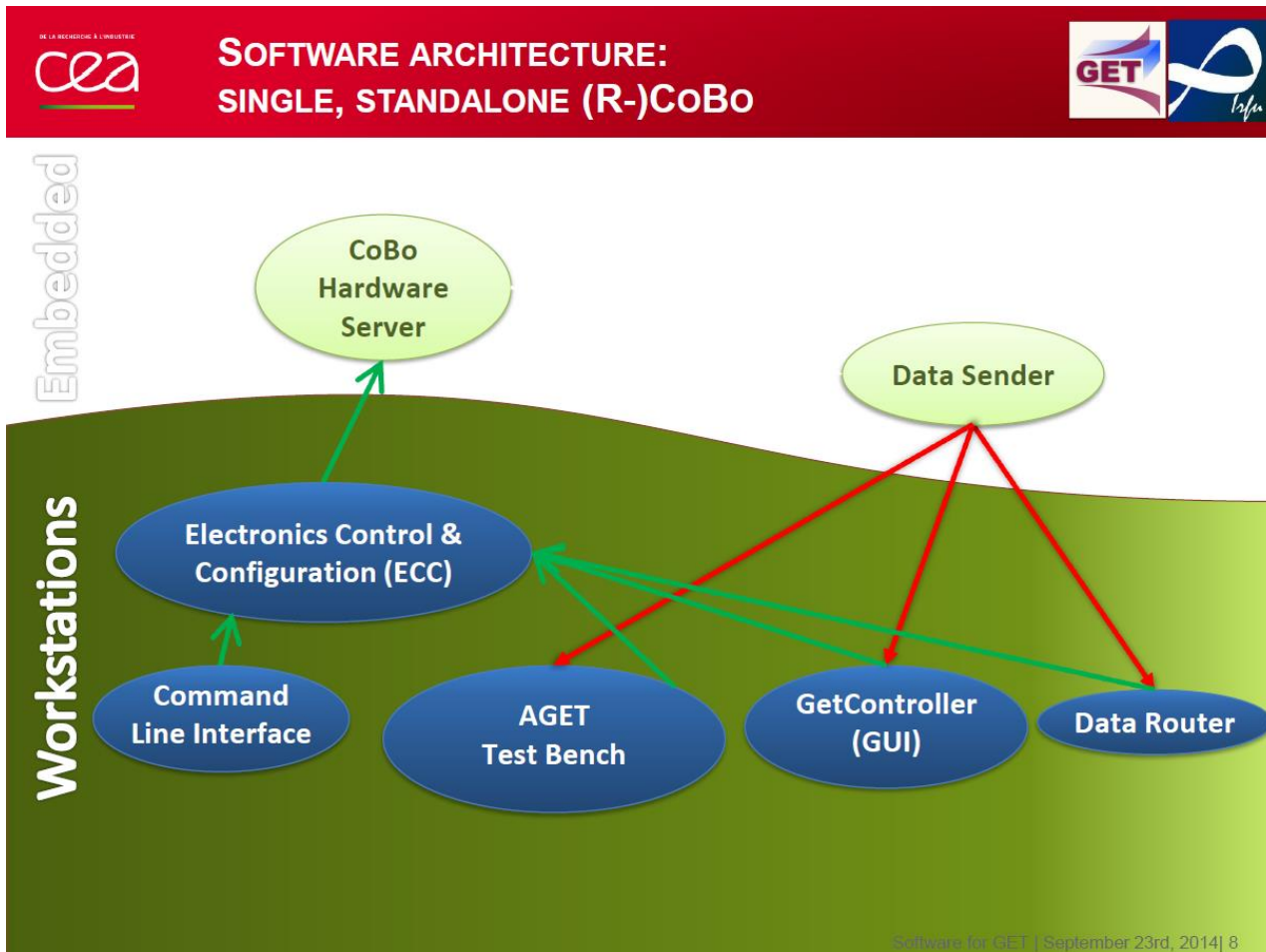


Sh. Anvar P. Sizun

# GET DAQ overview



# Software architecture (3)

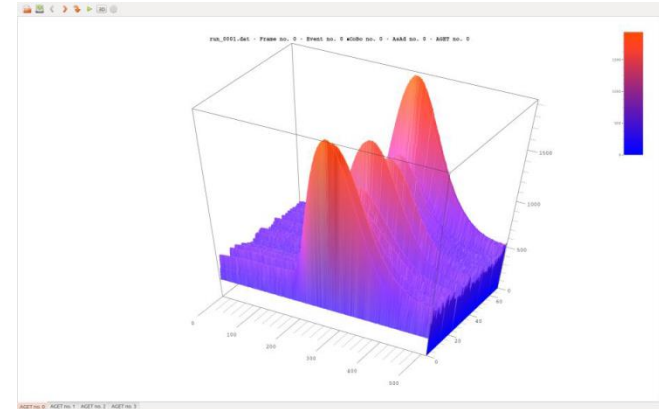


Patrick Sizun

# GETController

Edit test conditions

Name	Value	Unit	Range
<b>ECC</b>			
<b>CoBo[*]</b>			
isActive	172.16.115.80	false	
<b>Module</b>			
nbEvent	1000		
frameType	standard		{standard, test, threeBytes, zeroSuppression}
isAcqTestMode	false		
enableWriteHittedregister	false		
enableMemZpMode	false		
multiplicityThreshold	1		
multiplicityThreshold_2p	50		
multWindowSize	10		
triggerMode	external		{external, external_2p, noTrigger, onMultiplicity, onMultiplicity_2p, onReque...
triggerPeriod	5000 ms		
triggerDelay	800		
triggerDelay_2p	800		
triggerTimeOut_2p	800		
triggerDeadTime_2p	800		
triggerTime_2p	800		
writingClockFrequency	100.0		{6.25, 12.5, 25.0, 50.0, 100.0}
readingClockFrequency	25.0		{6.25, 12.5, 25.0}
readDataDelay	14		
writeReadDelay	0		
scwMultDelay	50		
<b>CircularBuffer[*]</b>			
<b>AsAd[*]</b>			
<b>Control</b>			
<b>Clocking</b>			
<b>ADC</b>			
<b>Generator</b>			
<b>InspectionLines</b>			
<b>Monitoring</b>			
<b>Agnet[*]</b>			
<b>Control</b>			
<b>Global</b>			
<b>channel[*]</b>			
isActive	true		
isSelectedForTestMode	false		
TriggerInhibition	none		{inhibit_channel, inhibit_trigger_data, inhibit_trigger_function, none}
LSBThresholdValue	0		{0, 15}
Gain	1pC		{10pC, 120fC, 1pC, 240fC}



GET Controller

Information

Log Headers AsAd no. 0 Control

Test Identity

Name: fonctionnal

Type: StdAcquisition

Servers

ECC: 172.16.115.4:46002

DAQ: 172.16.115.4:46005

Target: 172.16.115.80:46001

Paths

Hardware: soStandAlone.xcfg

Conditions: fonctionnal.xcfg

Data:

Event no. 34 - AsAd no. 0 - AGET no. 0

Amplitude

Time Bucket Index

AGET no. 0 AGET no. 1 AGET no. 2 AGET no. 3

Control

Load Hw

Configure

Start

Stop

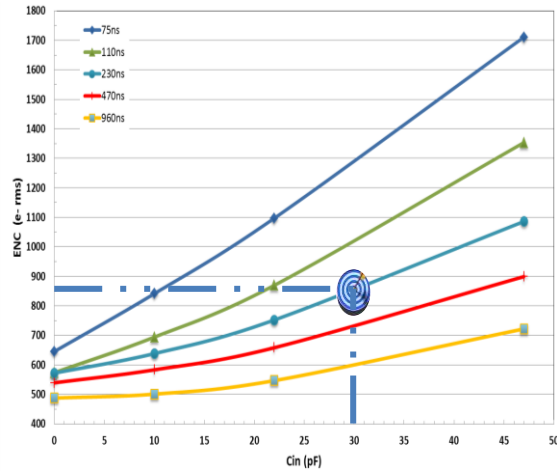
Reset

109 frame(s)

The figure shows a line graph with 'Amplitude' on the y-axis (ranging from 0 to 3500) and 'Time Bucket Index' on the x-axis (ranging from 0 to 600). The graph displays a single prominent peak centered around a Time Bucket Index of 100, with an amplitude of approximately 3200. Multiple overlapping lines in different colors represent different data series. To the right of the graph is a vertical list of colored dashes corresponding to indices 0 through 17. Below the graph, there are tabs for 'AGET no. 0', 'AGET no. 1', 'AGET no. 2', and 'AGET no. 3'. On the far right, there is a 'Control' panel with buttons for 'Load Hw', 'Configure', 'Start', 'Stop', and 'Reset', along with a dropdown menu showing '109 frame(s)'.



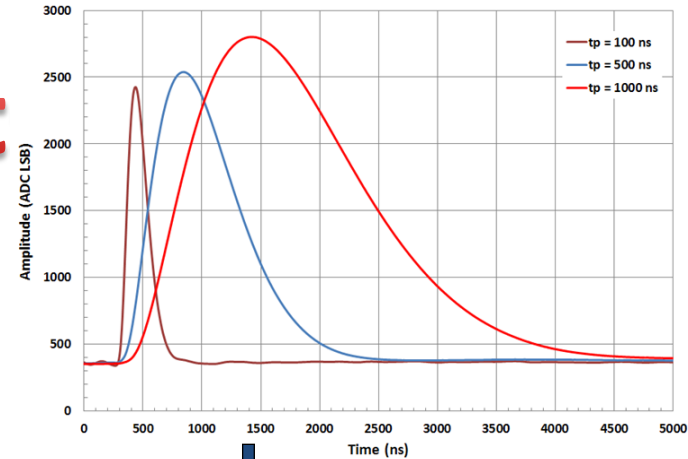
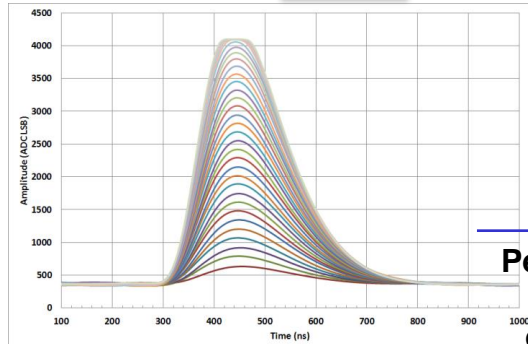
## Charge resolution versus peaking time & input capacitor



Pascal Baron AGET GM VI

# Main result

INL < 2%



Peaking time code

Tpeak [5% to 100%]

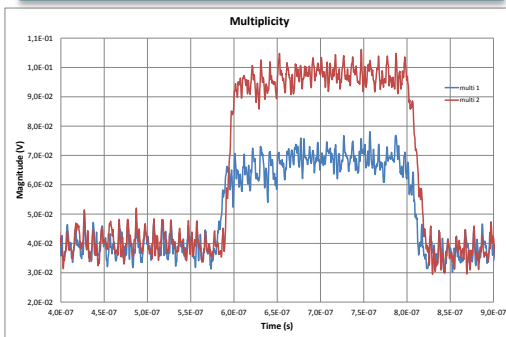
Tfall [100% to 5%]

T FWHM

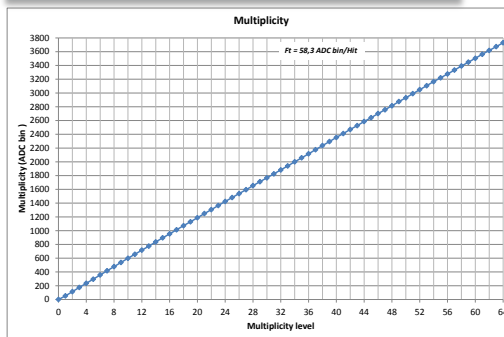
Range (fC)	Simulated value (mV / fC)	Measured value (mV / fC)
120	17	15.16
240	8.88	8.61
1000	1.864	1.976
10000	0.1874	0.194

Peaking time code	Tpeak [5% to 100%]	Tfall [100% to 5%]	T FWHM
1	75 ns	130 ns	100 ns
2	110 ns	270 ns	175 ns
3	230 ns	580 ns	390 ns
4	270 ns	710 ns	460 ns
5	330 ns	810 ns	550 ns
6	370 ns	920 ns	620 ns
7	470 ns	1250 ns	820 ns
8	520 ns	1370 ns	890 ns
9	540 ns	1290 ns	920 ns
10	580 ns	1390 ns	980 ns
11	690 ns	1670 ns	1170 ns
12	740 ns	1800 ns	1220 ns
13	790 ns	1960 ns	1340 ns
14	820 ns	2060 ns	1400 ns
15	940 ns	2400 ns	1590 ns
16	960 ns	2500 ns	1650 ns

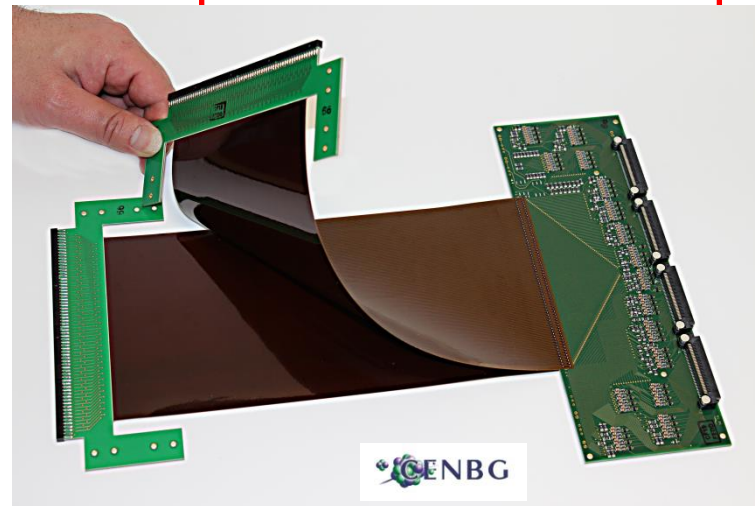
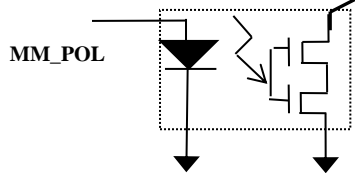
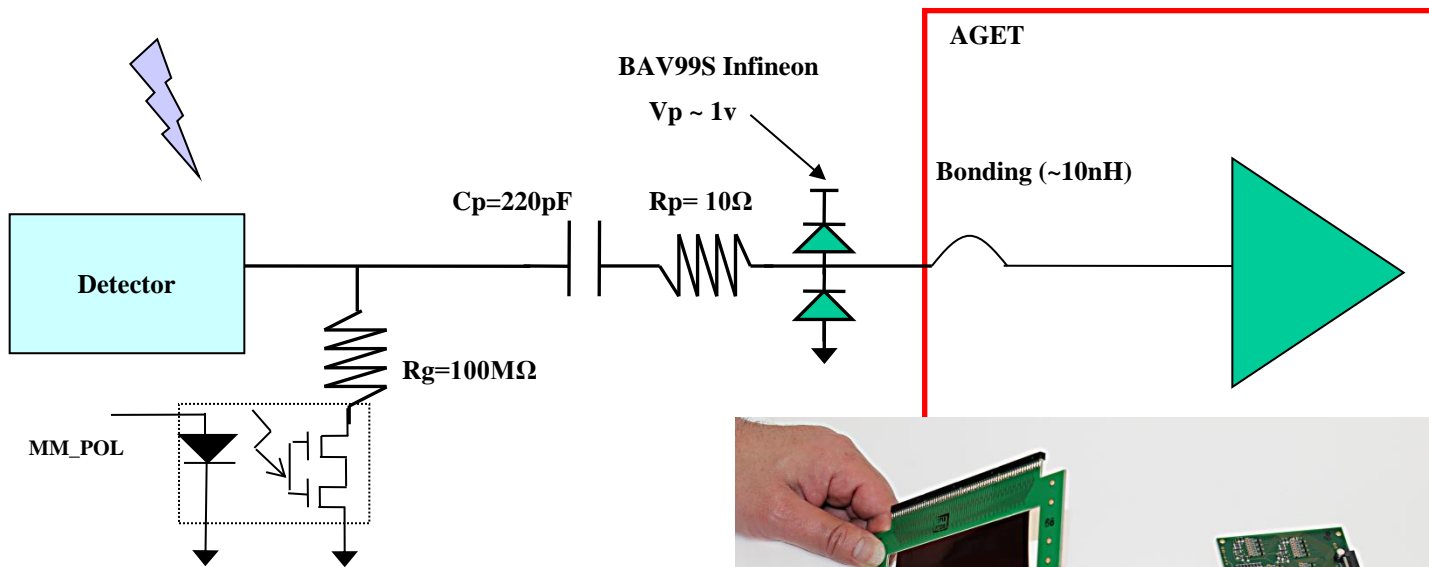
## Quality of the signal (multiplicity 1 & 2)



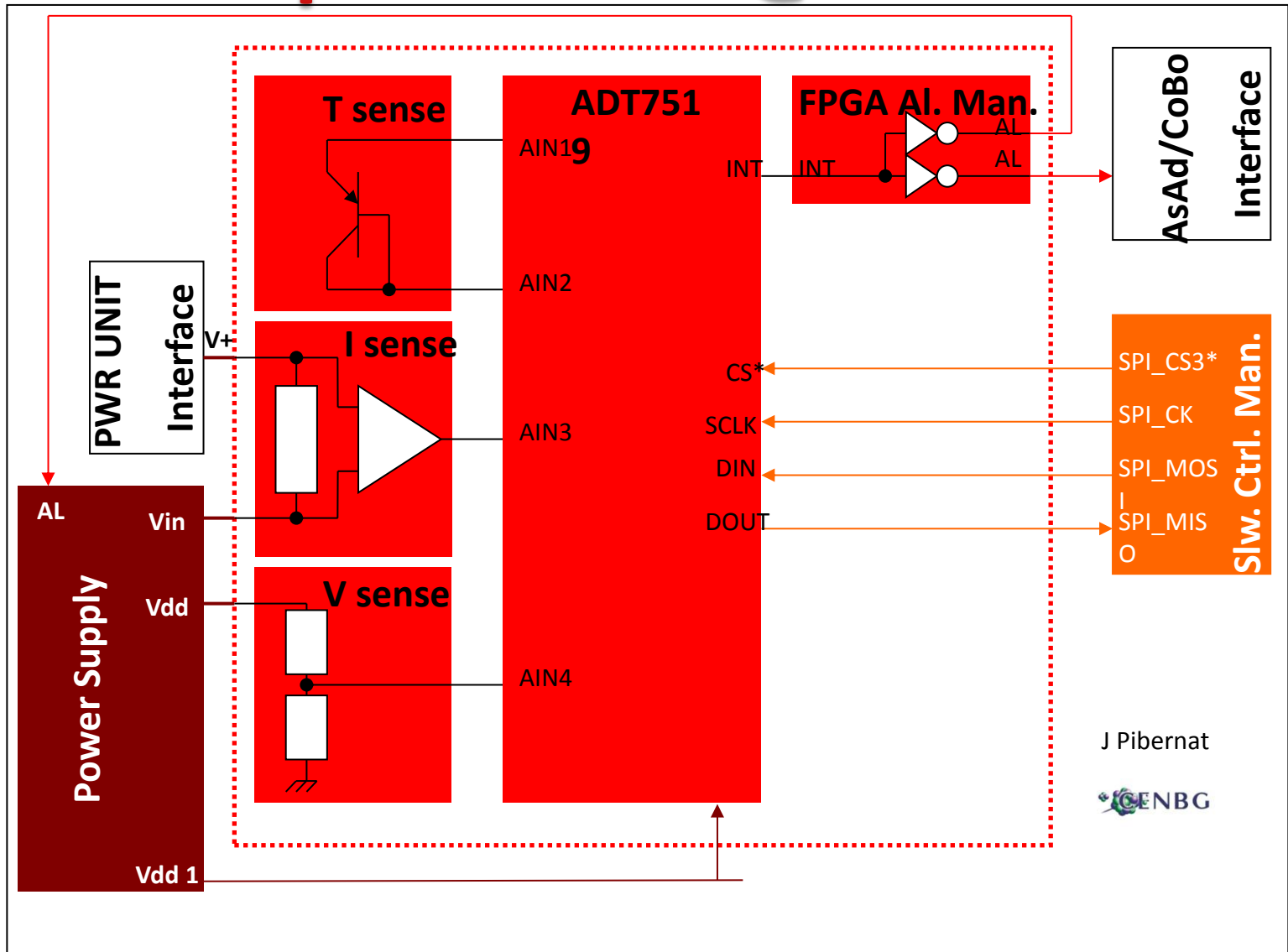
## Transfer Function # 58,3 ADC bin / Hit



# Frontend protection @ detector level

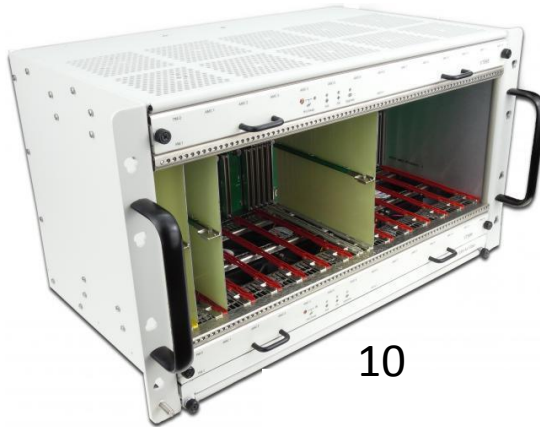


# Frontend protection @ board level

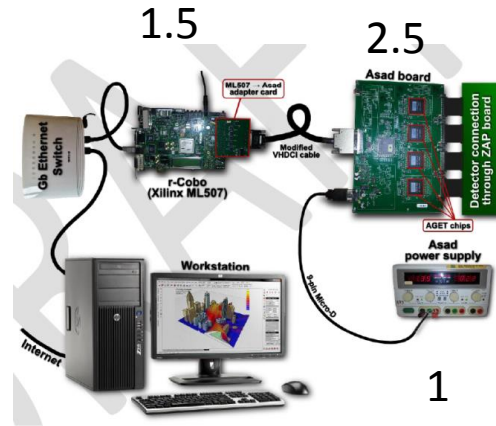


# Budget overview

5



10



1.5

2.5

1



1



2

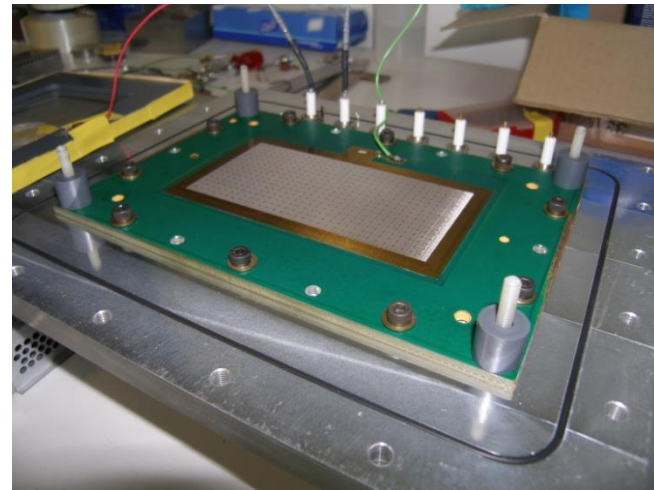
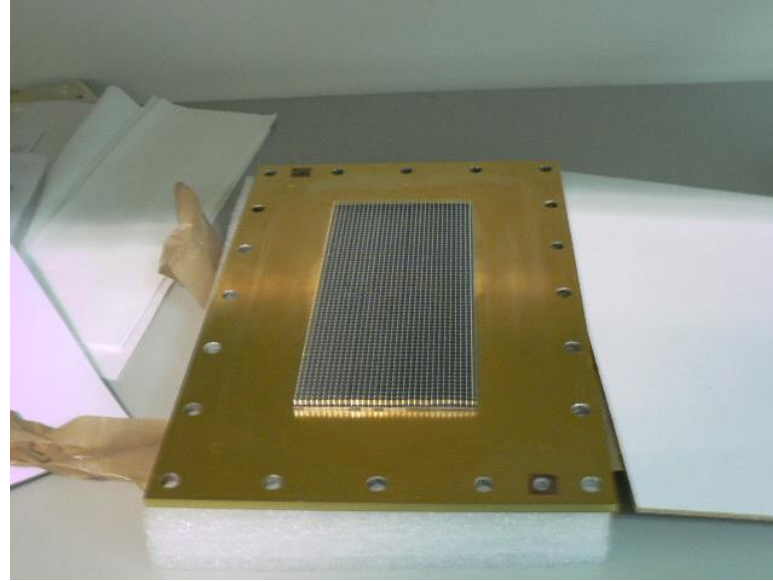
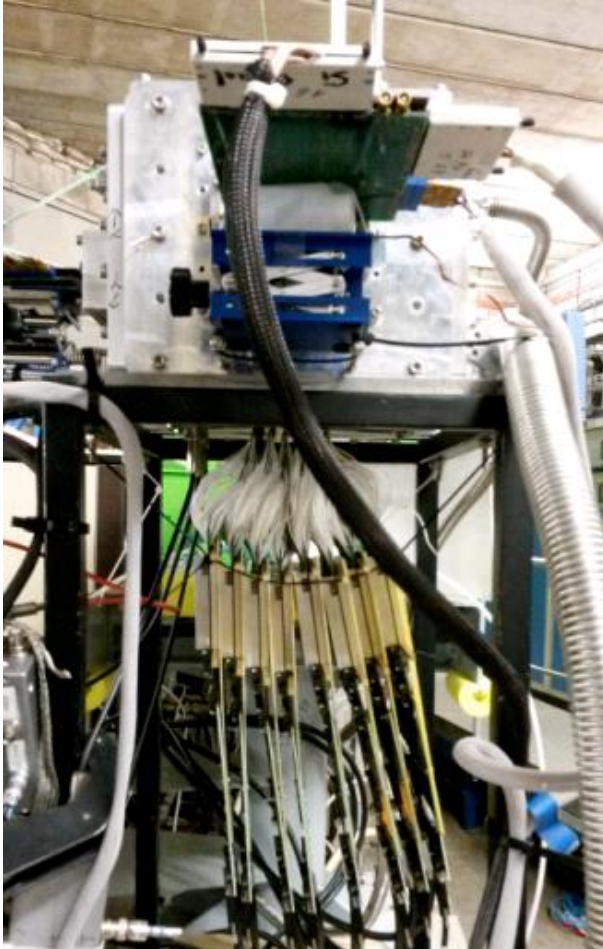
10

Rcobo 256 Channels 20 €/channel

1 crate = 10 CoBo + 40 AsAd + 1 MUTANT      10 Kchannels 16 €/channel

3 crates = 30 CoBo + 120 AsAd + 3 MUTANT      30 Kchannels 14 €/channel

# Thank you...



GANIL

GENBG