

Satus on Front-End Readout Electronics → The FATALIC Project ←

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Clermont-Ferrand – France

Tile Upgrade Week
– Wednesday 10th of June 2015 –

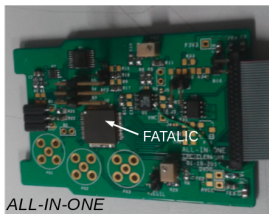


Overview

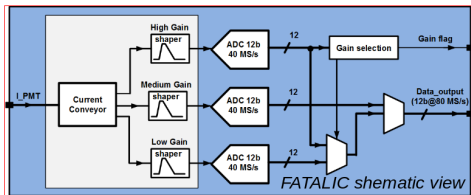
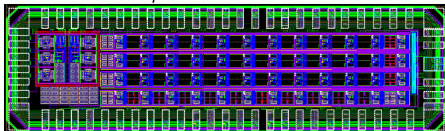
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- 2 The Clermont-Ferrand Test Bench
- 3 Study of The Photomultiplier Output
- 4 Study of The Shaper Output
- 5 Study of The Digitized Output
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Front-end ATLAS tile Integrated Circuit

FATALIC chip embedded in the "All-in-One" FE board



FATALIC microscop view



Main characteristics of FATALIC:

- A 3-gain PM-signal **analog processing** (current conveyor + 3 shapers)
- 3 embedded **12-bit ADCs** (one per gain)
- An **auto gain-selection** (MEDIUM and {HIGH or LOW})
- A **12-bit data output bus** with the data of the 2-selected gain multiplexed

FATALIC strength: low noise

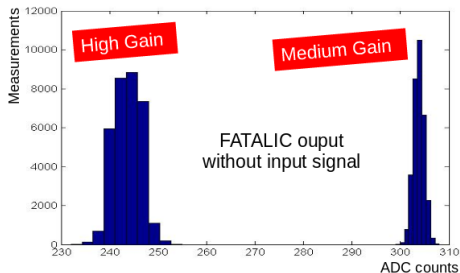
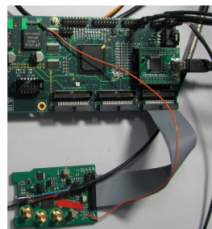
Noise Requirement :

"the smallest signal of interest from the detector, expressed in terms of **equivalent input charge** delivered to the front end electronics, is **24 fC**. The intrinsic noise of the electronics, as measured through the digitization path, expressed in terms of equivalent input charge, **shall not be greater than 12 fC rms at pedestal.**"

FATALIC noise measurement

Medium Gain : Std Deviation = 1.23 LSB → 42 fC rms

High Gain : Std Deviation = 2.74 LSB → 9.4fC rms



Why a low noise chip ?

→ Thanks to the **digitalization** of the analog signal **inside Fatalic**

- (a) no sensitivity to the noise induced by the main board
- (b) no sensitivity to EMC properties of the interface-flat cable

The CF Test Bench

Computer/interface to drive the tests

Low voltage power supply



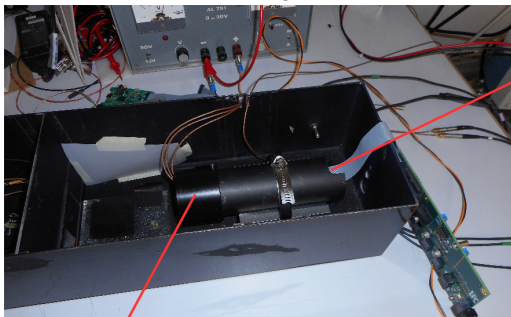
Scope to measure analog signal

LED driver (emulate the light produced by the tiles)

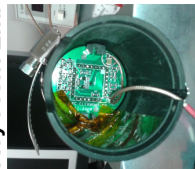
High voltage power supply

The CF Test Bench

LED + PM + very Front-End



very Front-End



Possibility to follow the signal through the whole chain (see next slide)

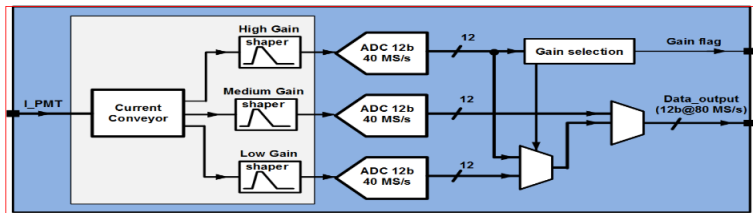
LED + PM



- 3 LEDs to simulate a realistic physics conditions:
- incoming particle = pulse
 - out-of-time pile-up = second pulse time-delayed
 - in-time pile-up = constant light

For the discussed studies : only one pulse

How to follow the signal ?



PM

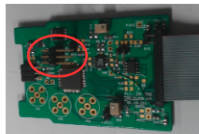
1. FATALIC input



direct readout getting the PM output through the Active Divider

Shaper

2. Analog signal (shaper output)

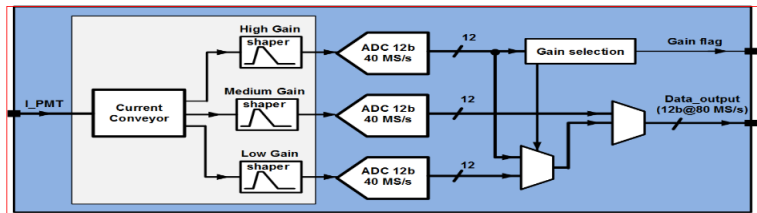


All-In-One with additional access for the shaper

ADC

3. Digitized signal (ADC output)

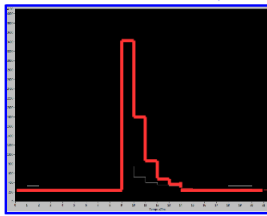
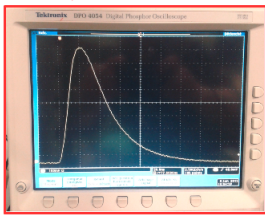
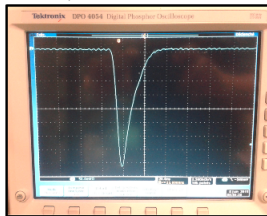
How to follow the signal ?



PM signal

Shaper signal

ADC signal

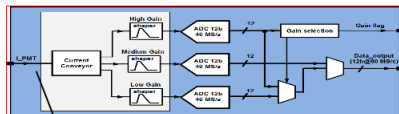


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PM signal quick look

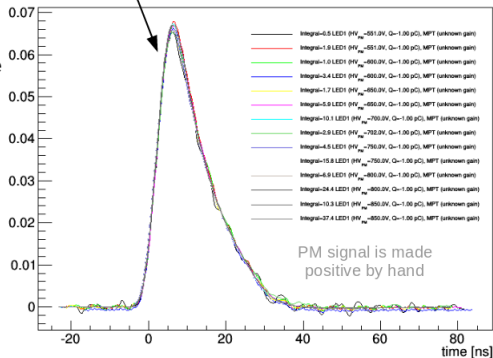
1. Analysing the shape of the PM response for different HV



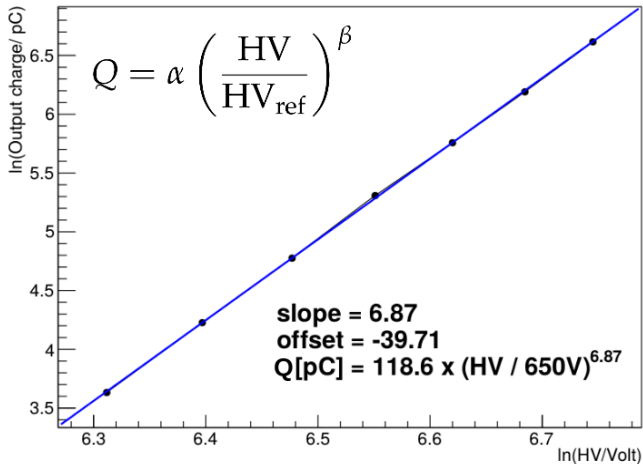
2. The PM : **absolute** charge source
(Scope impedance = 50 Ω)

$$Q = \int \frac{V_{\text{scope}}(t)}{R_{\text{scope}}} dt$$

→ useful for calibration test
(complete charge injector tool)



PM as absolute charge source

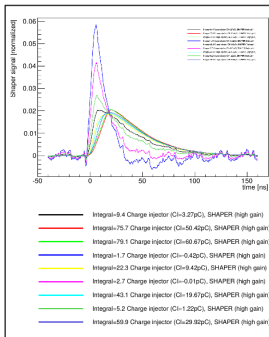
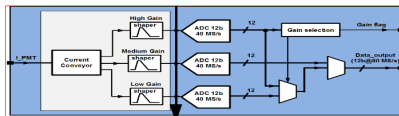


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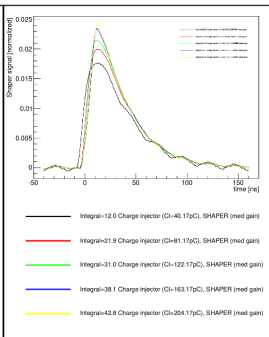
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Signal shape comparison

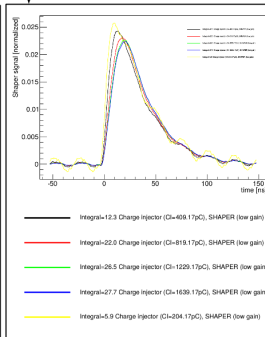
Comparing the **shape of the analog signals** for different injected charge.
Essential for the **optimal filtering**
(using the **charge injector**)



high gain



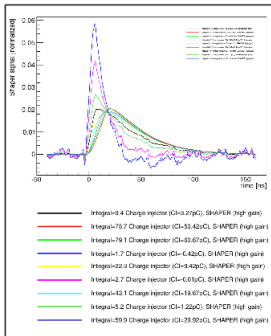
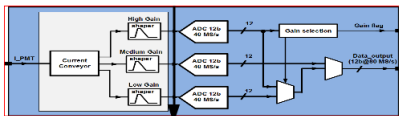
medium gain



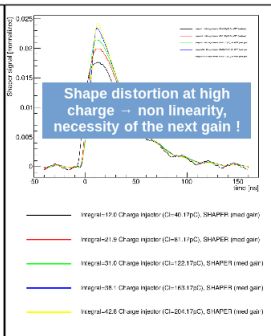
low gain

Signal shape comparison

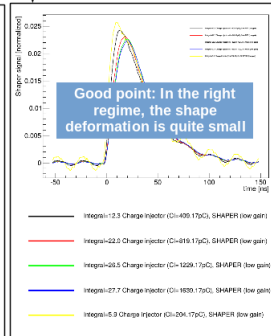
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high gain



medium gain

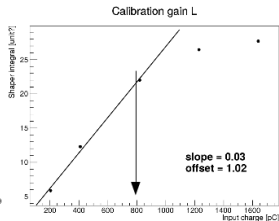
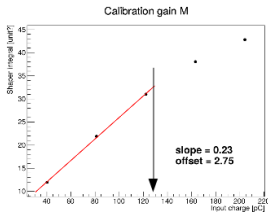
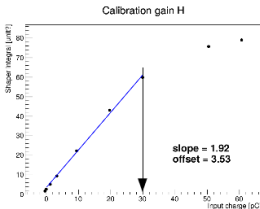
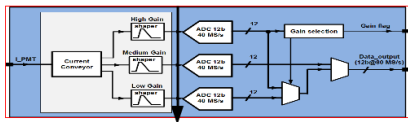


low gain

Calibration with the Charge Injector

Calibrating each gain and estimating when the linearity breaks (using the charge injector)

→ working quite well in each validity domain



Gain ratio:
- H/M = 8.3
- M/L = 7.6

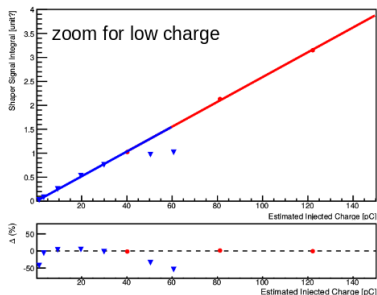
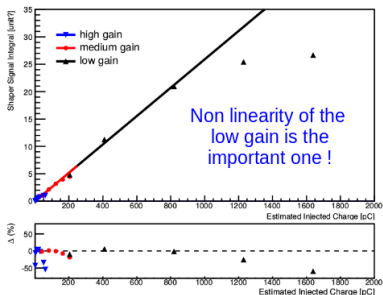
Important caution : the input charge is simply an estimation since the Charge Injector not precisely calibrated (**non linearity**).

Calibration with the Charge Injector

To **overlay** the response of the 3 gain on the same plot:

- remove the offset for each data point
- scale the slope by the gain ratio

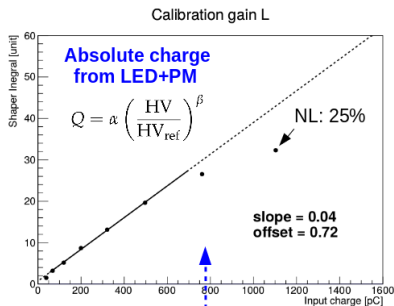
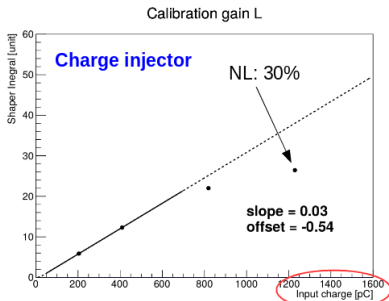
This is an illustrative plot
more than a physics one !



Important caution : the input charge is simply an estimation since the Charge Injector not precisely calibrated (**non linearity**).

Calibration: Charge Injector VS LED+PM

Important caution : the input charge is simply an estimation since the Charge Injector not precisely calibrated (**non linearity**).

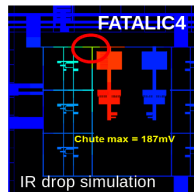
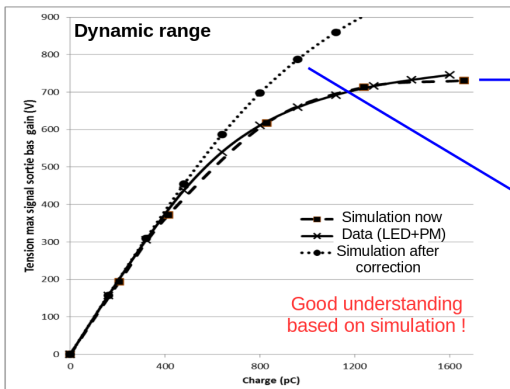


If the charge injector has some **non linearity**, this measurement is **biased** ! Use a **well calibrated** charge source, like **LED+PM**

Linearity improvement: FATALIC4b

For high energy events, the input peak current reaches tens of mA. In FATALIC4, this current induces a 200mV-voltage drop of the power supply, **limiting the input dynamic range**.

This **problem has been fixed in FATALIC4b** with larger power rails.

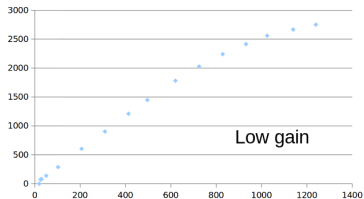
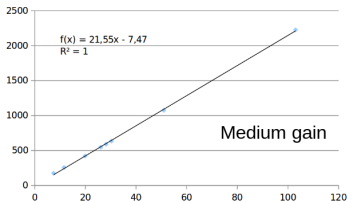
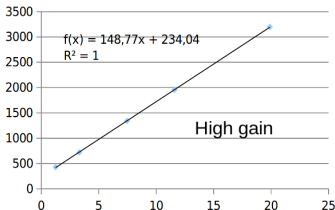
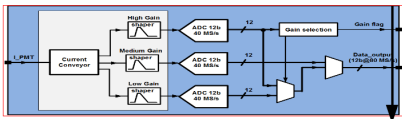


Comment : this problem was not presented in Valencia because it was only seen in a dynamic regime (**pulse**), tested later.

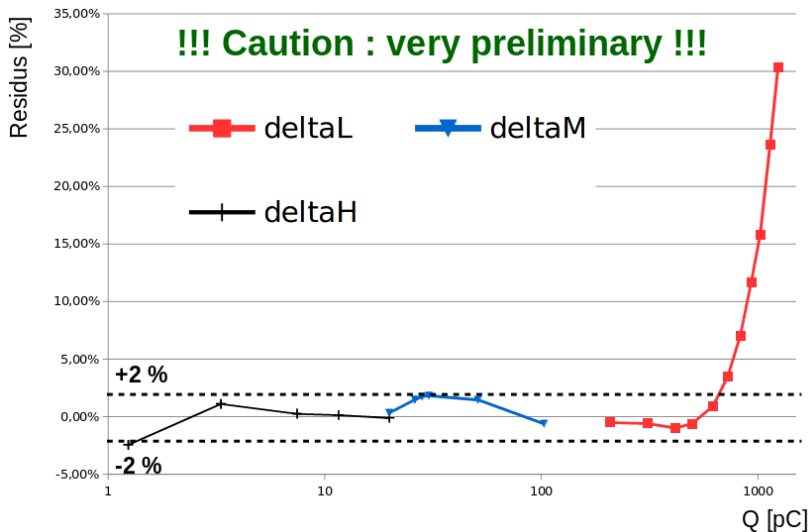
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Calibration with the Charge Injector



Non linearity: residus



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Summary And Outlooks

Summary

- Performed deep tests to characterize FATALIC4 in a **dynamic regime**
- Scrutinize the signal at each step: PM, shaper, ADC
- Very good signal-to-noise results
- FATALIC4 has an overall good response (linearity) over the three gains

Main progress: reveal/improve weakness visible in dynamic regime only

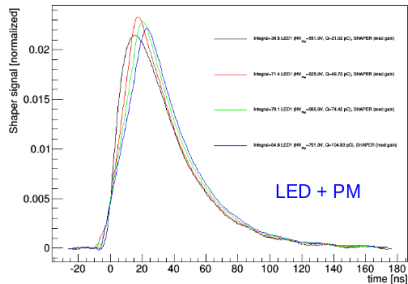
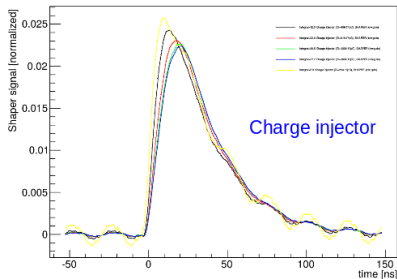
- Identification of a **non-linearity** at high input charge, **only in dynamic**
- Very well **understood** with the simulation and **solved** → **FATALIC4b**

Outlooks

- Currently: **linearity precision limited by the source** calibration
- A new test board, with an embedded **14-bit precision ADC**, has been designed to **calibrate input signal** of Fatalic with **high precision**
- **Test FATALIC4b** (currently under production)

Backup Slides

Low gain shape distortion: CI vs LED+PM



Non linearity precision: discussion

A precise calibration of the charge injector linearity is a key point to properly characterize the chip linearity ...

From François Vazeille ✨

13/04/2015 16:19

Subject: **Linearity of the CIS**

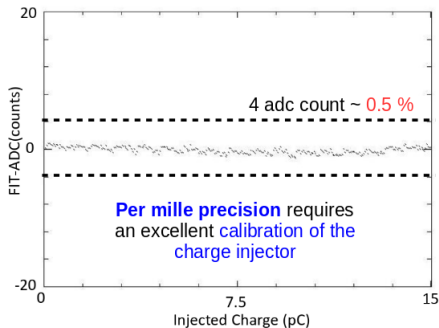
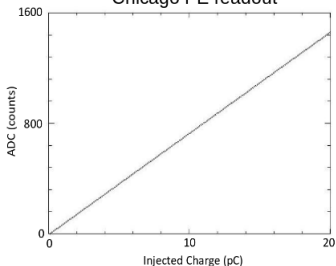
To: tang@edg.uchicago.edu <tang@edg.uchicago.edu> ✨, Kelby J Anderson <kelby@uchep.uchicago.edu> ✨,

Tags: **TileUpgrade**

Dear colleagues,
in the design of our Main Board, we have implemented your charge injection system that works well.
We would like to know its linearity.
Did you perform this study, and if yes, could you give us the results?

With our best regards,
Romeo and francois

From Valencia presentation :
Chicago FE readout



<https://indico.cern.ch/event/335721/session/0/contribution/7/material/slides/0.pdf>