

# Achievements and Perspectives of CMOS Pixel Sensors for HIGH-PRECISION Vertexing & Tracking Devices

M. Winter (Equipe PICSEL de l'IPHC-Strasbourg)

LLR-Palaiseau / 7 Décembre 2015

## Contents

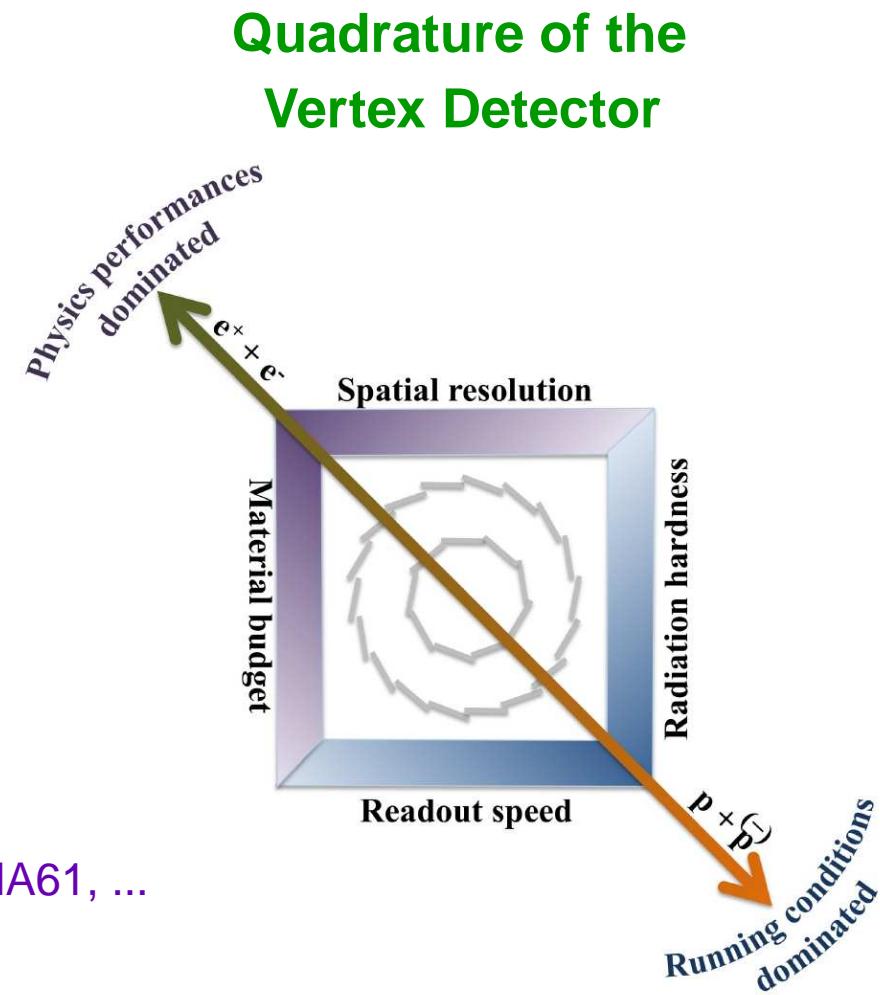
- *Primordial motivations & main features of CMOS sensors*
- *1st architecture developed - state of the art*
  - MIMOSA-26 (EUDET chip applications)  MIMOSA-28 (STAR-PXL)
- *Extension towards more demanding experiments*
  - ALICE-ITS & -MFT
  - CBM-MVD
  - ILC
- *Perspectives & forthcoming challenges*
  - read-out speed & rad. tolerance
  - architectures & emerging CMOS technologies
- *Conclusion*

SOURCES : Talks at CPIX-14 + VERTEX-14/15 + FEE-14 + TWEPP-13/14/15 + LHCC/ALICE

SLIDES : M.Deveaux, L.Greiner, Ch.Hu-Guo, M.Keil, M.Mager, L.Musa, F.Morel, D.Muenstermann, I.Peric, F.Reidt, W.Snoeys, ...

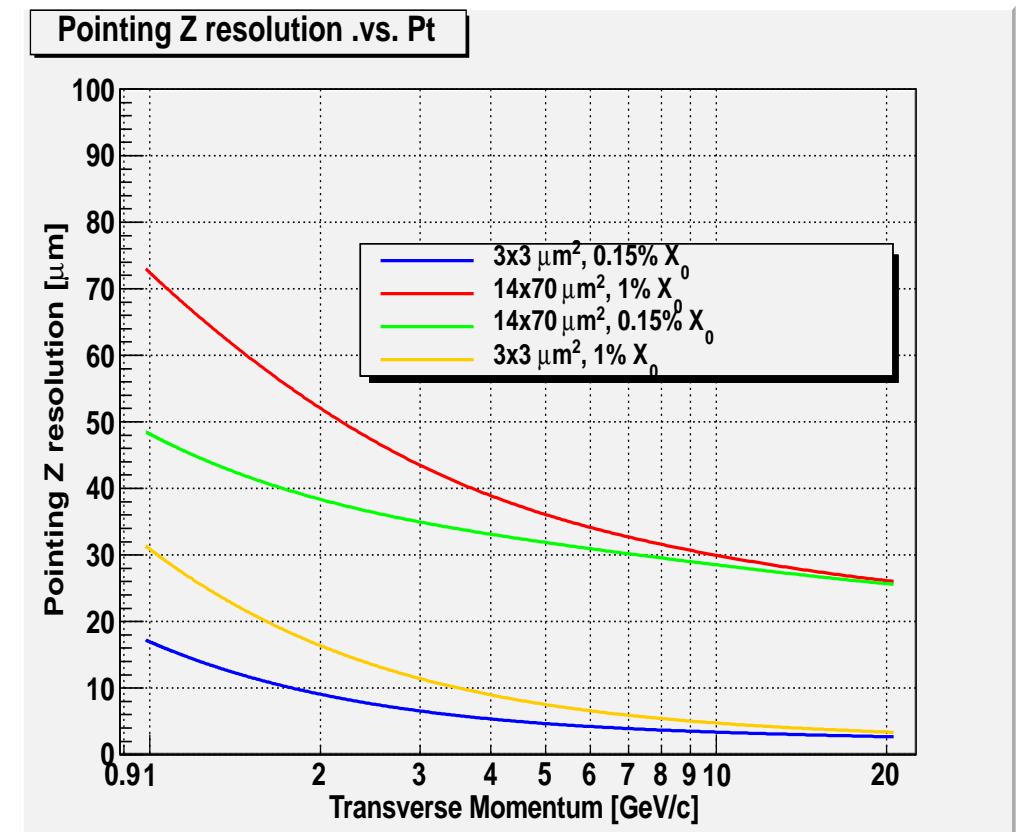
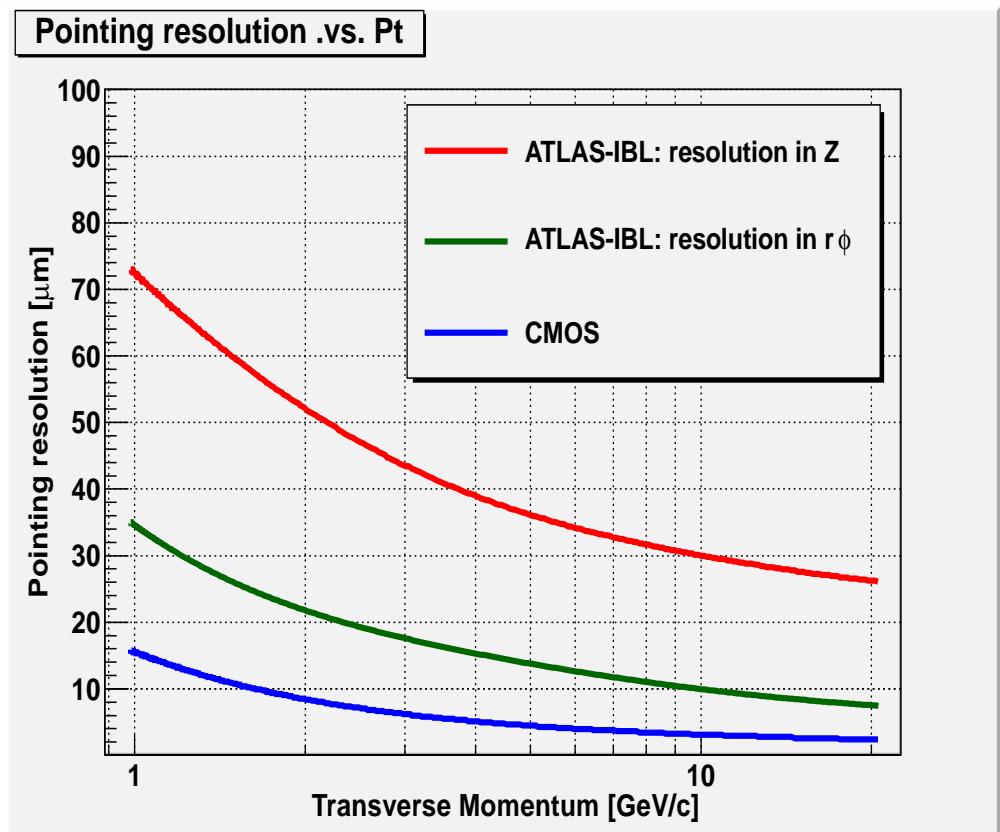
# Motivation for Developing CMOS Sensors

- CPS development triggered by need of very high granularity & low material budget
- Applications exhibit much milder running conditions than pp/LHC  
⇒ Relaxed speed & radiation tolerance specifications
- Increasing panel of existing, foreseen or potential application domains :
  - Heavy Ion Collisions : STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
  - $e^+e^-$  collisions : ILC, BES-3, ...
  - Non-collider experiments : FIRST, NA63, Mu3e, PANDA, ...
  - High precision beam telescopes adapted to medium/low energy electron beams :  
↪ few  $\mu m$  resolution achievable on DUT with EUDET-BT (DESY), **BTF-BT (Frascati)**, ...



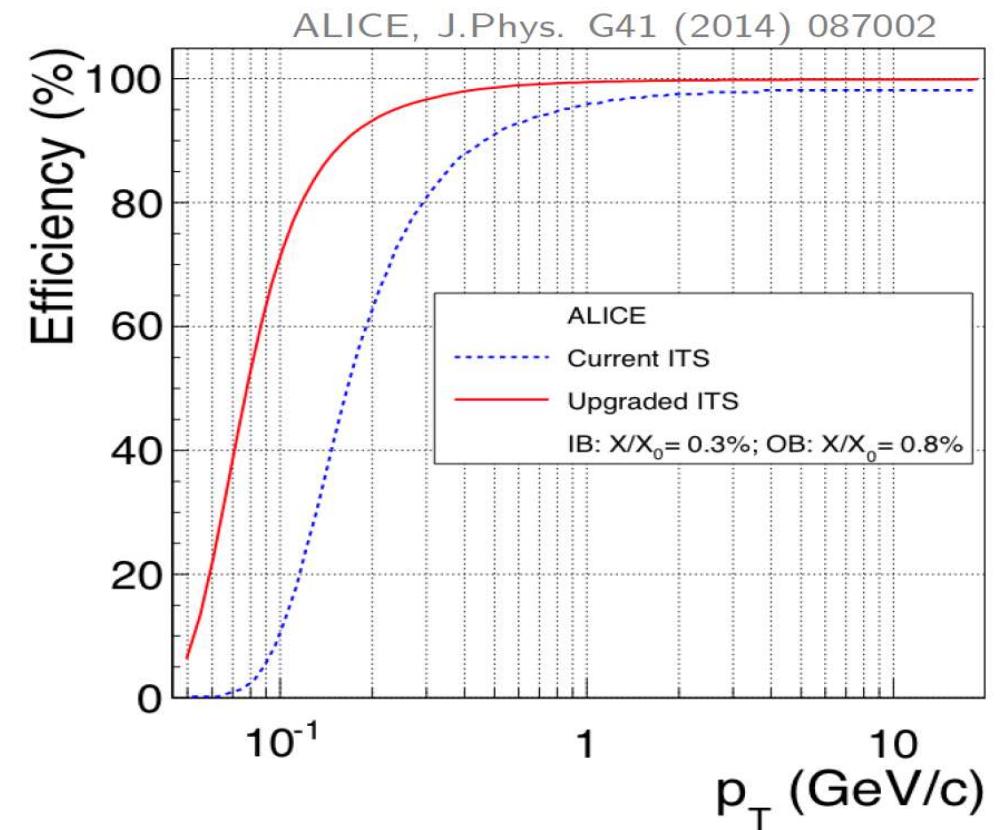
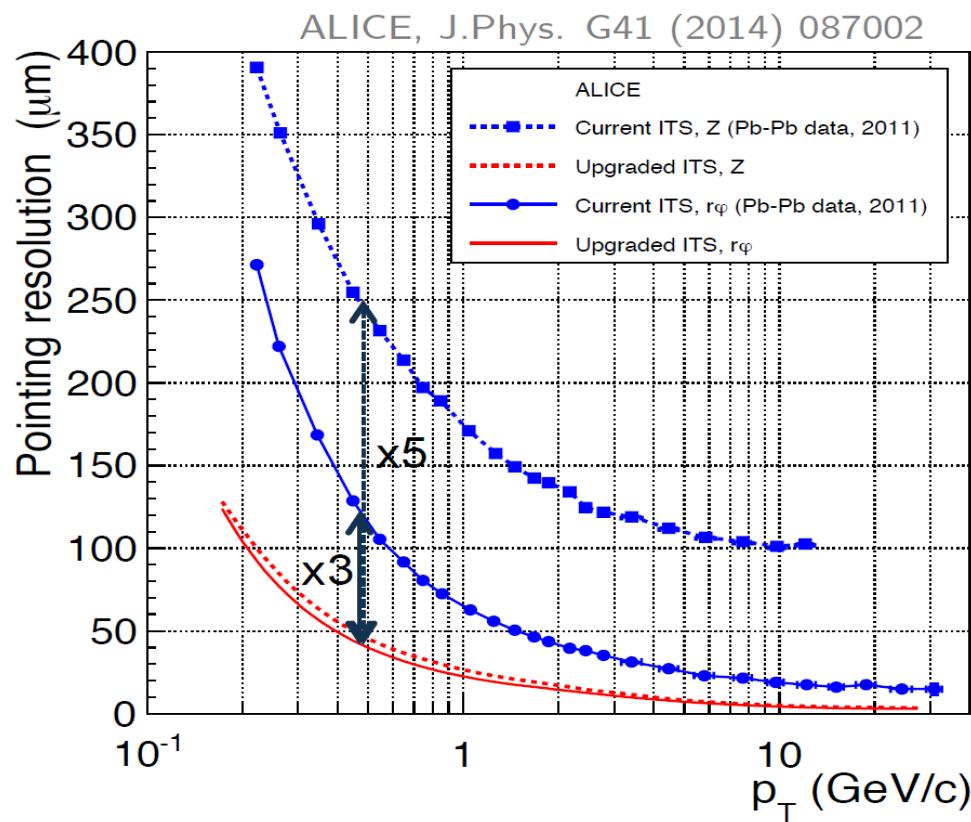
# Example of Application : ILC Vertex Detector

- Goal :  $\sigma_{sp} \lesssim 3 \mu\text{m}$  in both directions with  $\lesssim 0.15 \% X_0$  / layer
- Comparison:  $\sigma_{sp} = 3 \times 3 \mu\text{m}^2$  &  $0.15 \% X_0$  against  $14 \times 70 \mu\text{m}^2$  &  $1.0 \% X_0$



# Example of Application : Upgrade of ALICE-ITS

- ALICE Inner Tracking System (ITS) foreseen to be replaced during LS2/LHC
  - higher luminosity ( $\equiv$  collision rate), improved charm tagging
- Expected improvement in pointing resolution and tracking efficiency



# Long Term R&D

- *R&D activity of CPS initiated in 1999 for future subatomic physics experiments*
- *First contact for STAR PXL took place in Year 2000 during the workshop Vertex-2000*

**VERTEX 2000**  
9th International Workshop on Vertex Detectors  
Sleeping Bear Dunes  
National Lakeshore, Michigan, U.S.A.  
September 10-15, 2000

**MONOLITHIC ACTIVE PIXEL SENSORS FOR A LINEAR COLLIDER**  
(Marc Winter - IRES (Strasbourg))  
on behalf of IRES+LEPSI coll.

► Physics Motivations  
► Principle of Operation of M.A.P.S.  
► Characteristics of 1st M.A.P.S. prototype  
► Beam test Results (preliminary)  
► Outlook



**First Announcement**

**Submission of Proceedings**

**Referees**

**Registration**

**Workshop Program**

**Presentations**

**Picture**

**Comments**

**Accommodation**

**Travel**

**Attendee Information**

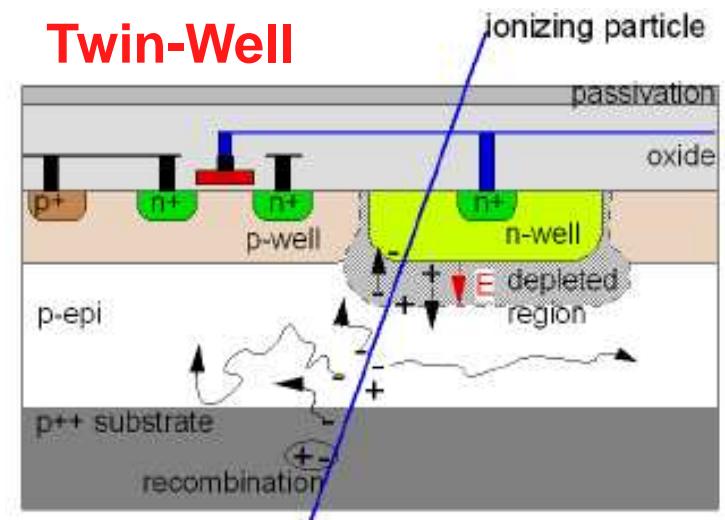
**Attendee Arrival Information**

# CMOS Pixel Sensors: Main Features

- Prominent features of CMOS pixel sensors :

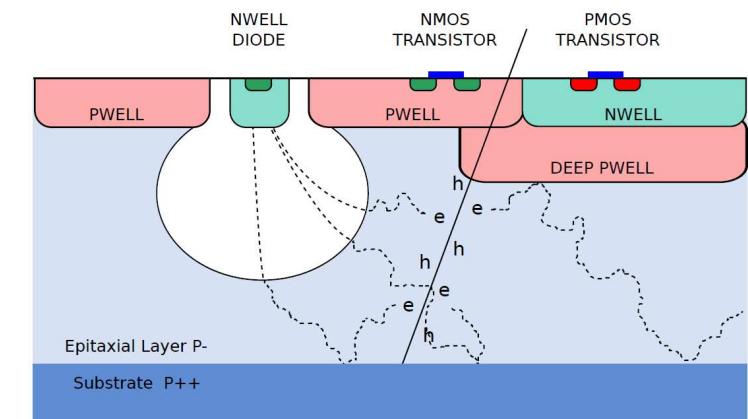
- high granularity  $\Rightarrow$  excellent (micronic) spatial resolution
- signal generated in (very) thin ( $15\text{-}40 \mu\text{m}$ ) epitaxial layer
  - ↪ resistivity may be  $\gg 1 \text{k}\Omega \cdot \text{cm}$
- signal processing  $\mu$ -circuits integrated on sensor substrate
  - $\Rightarrow$  impact on downstream electronics and syst. integration ( $\Rightarrow$  cost)

## Twin-Well



- CMOS pixel sensor technology has the highest potential :

- $\Rightarrow$  R&D largely consists in trying to exploit potential at best with accessible industrial processes
  - ↪ manufacturing param. not optimised for particle detection: wafer/EPI characteristics, feature size, N(ML), ...



## Quadruple-Well

- Read-out architectures :

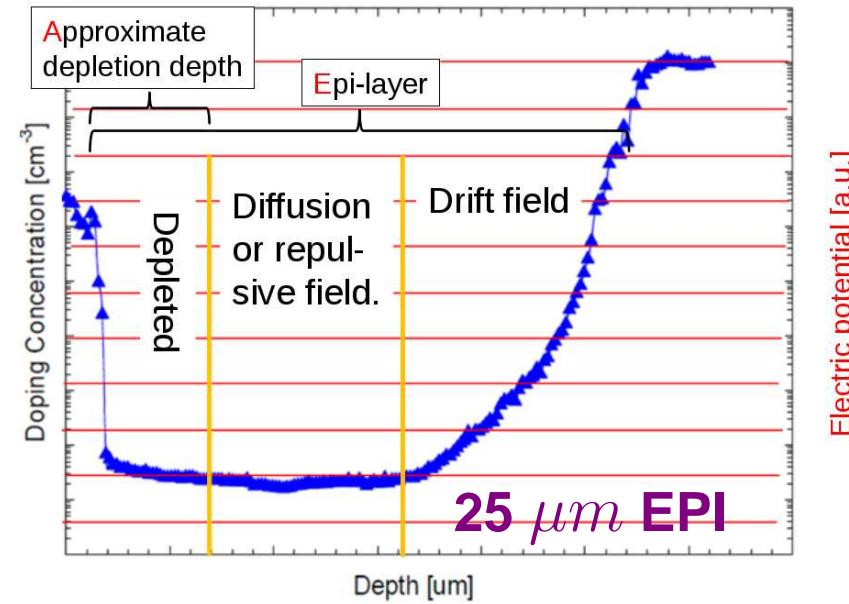
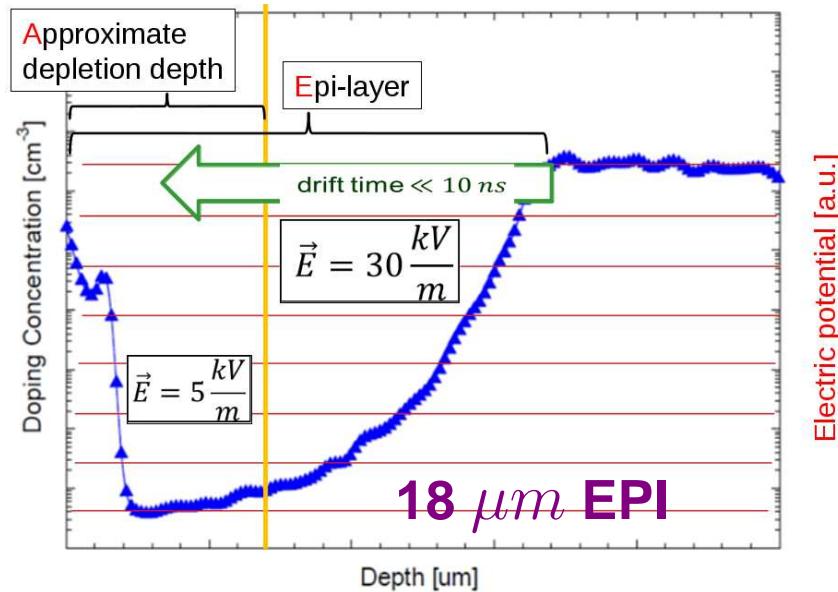
- 1st generation : rolling shutter (synchronous) with analog pixel output (end-of-column discri.)
- 2nd generation : rolling shutter (synchronous) with in-pixel discrimination
- 3rd generation : data driven (asynchronous) with in-pixel discrimination
- ...

# Role of the Epitaxial Layer

- Main influences :
  - $Q_{signal} \sim$  EPI thickness and doping profile
  - $\epsilon_{det}$  depends on depletion depth vs EPI thickness
  - NI radiation tolerance depends on depletion depth vs EPI thickness
  - Cluster multiplicity and  $\sigma_{sp}$  depend on pixel pitch / EPI thickness

## Case dependent optimisation mandatory :

- Deep depletion  $\Rightarrow$  higher SNR (seed pixel)  $\Rightarrow$  improved  $\epsilon_{det}$  but degraded spatial resolution ....
- Spatial resolution depends on Nb of bits encoding charge vs pixel pitch ...
- Density of in-pixel circuitry depends on CMOS process options : feature size, Nb(ML), twin/quadruple-well, ...



# Measured Spatial Resolution

- Several parameters govern the spatial resolution :

- pixel pitch
- epitaxial layer thickness and resistivity
- sensing node geometry & electrical properties
- signal encoding resolution

$$\Rightarrow \sigma_{sp} \text{ fct of pitch} \oplus \text{SNR} \oplus \text{charge sharing} \oplus \text{ADCu, ...}$$

- Impact of pixel pitch (analog output) :

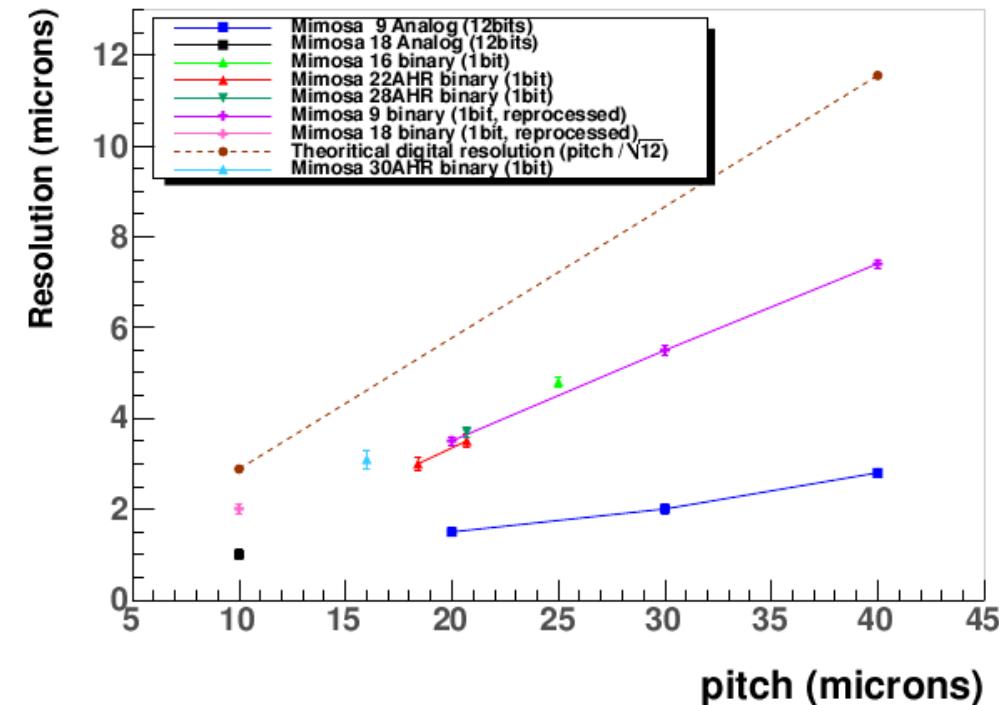
$$\sigma_{sp} \sim 1 \mu\text{m} \text{ (10 } \mu\text{m pitch)} \rightarrow \lesssim 3 \mu\text{m} \text{ (40 } \mu\text{m pitch)}$$

- Impact of charge encoding resolution :

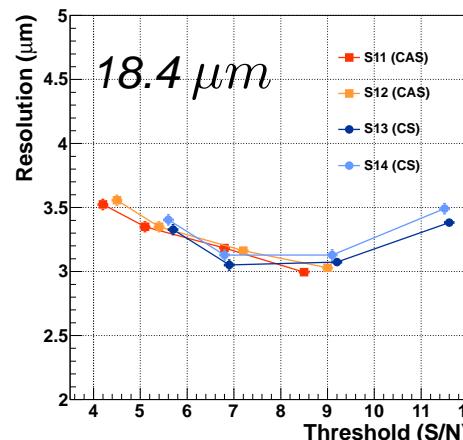
▷ ex. of 20  $\mu\text{m}$  pitch  $\Rightarrow \sigma_{sp}^{digi} = \text{pitch}/\sqrt{12} \sim 5.7 \mu\text{m}$

Nb of bits	12	3-4	1
Data	measured	reprocessed	measured
$\sigma_{sp}$	$\lesssim 1.5 \mu\text{m}$	$\lesssim 2 \mu\text{m}$	$\lesssim 3.5 \mu\text{m}$

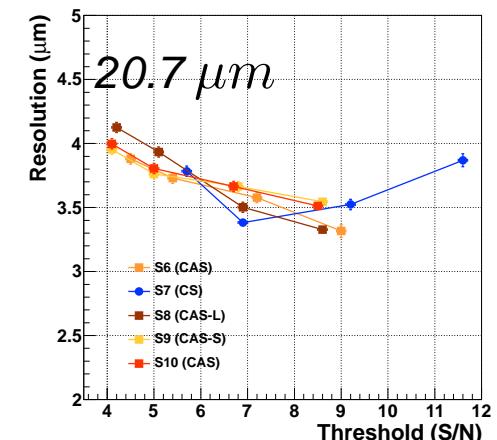
Mimosa resolution vs pitch



Resolution vs Threshold



Resolution vs Threshold

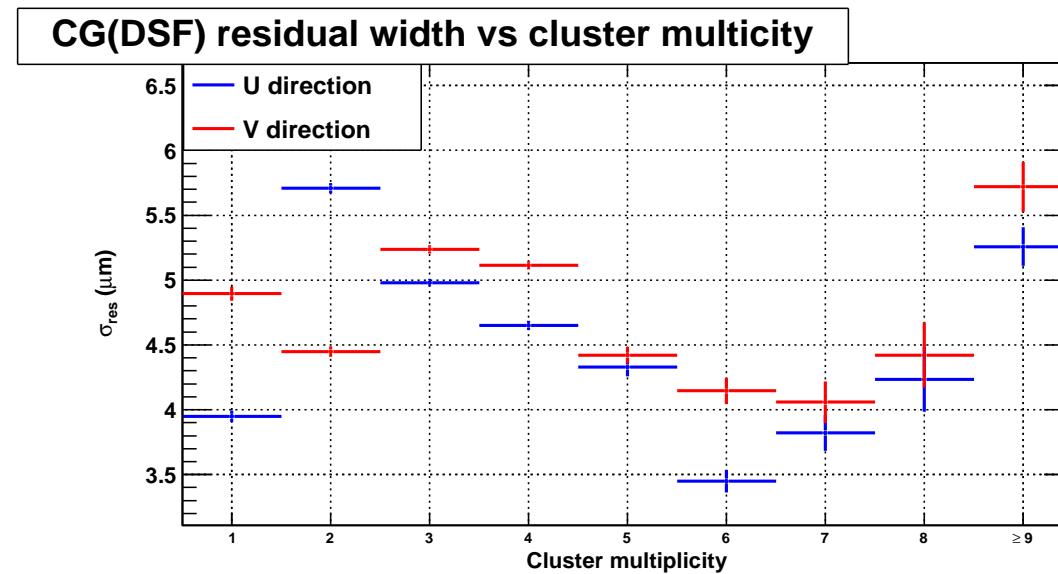
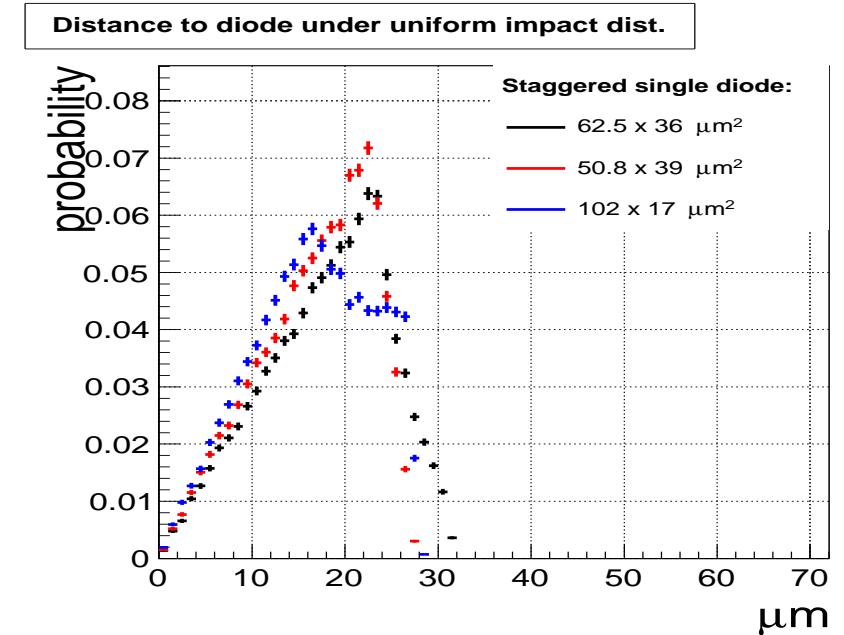
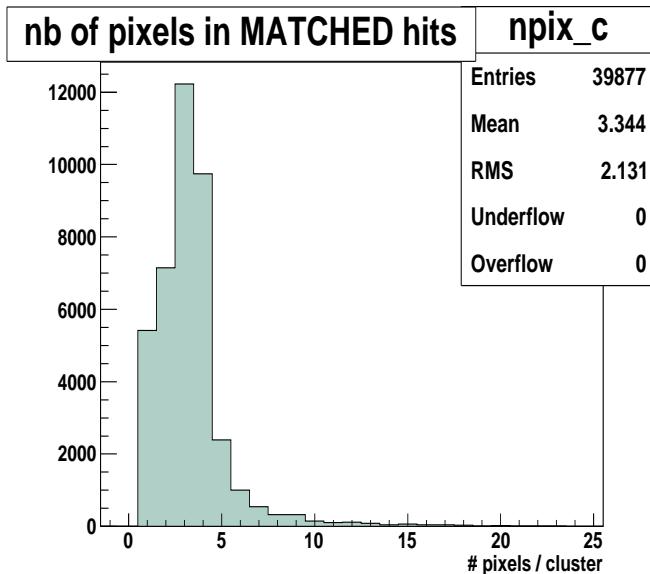


# Spatial resolution vs Cluster Dimensions

- Correlation between  $\sigma_{sp}$  & cluster hit multiplicity following from :

- \* pixel dimensions vs epitaxy characteristics  
(thickness, resistivity, doping profile)
- \* sensing node pattern (density, staggering, geometry)
- \* depletion voltage
- \* ...

- $9 \mu\text{m}^2$  diode : threshold at 5 mV



# Sensing Node & VFEE Optimisation

- General remarks on sensing diode :

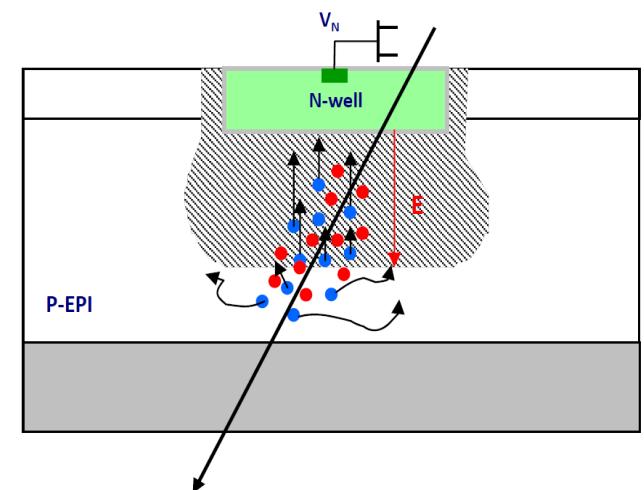
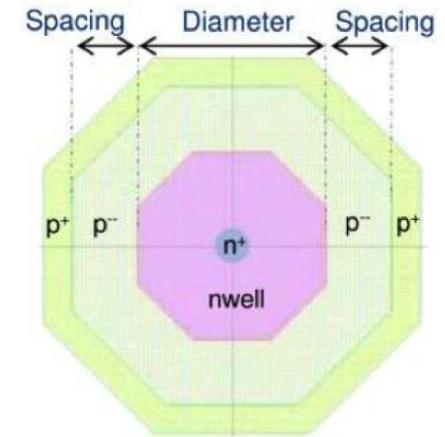
- should be small because :  $V_{signal} = Q_{coll}/C$  ; Noise  $\sim C$  ;  $G_{PA} \sim 1/C$
- BUT should not be too small since  $Q_{coll} \sim CCE$  (important against NI irradiation)

- General remarks on pre-amplifier connected to sensing diode :

- should offer high enough gain to mitigate downstream noise contributions
- should feature input transistor with minimal noise (incl. RTS)
- should be very close to sensing diode (minimise line C)

- General remarks on depletion voltage :

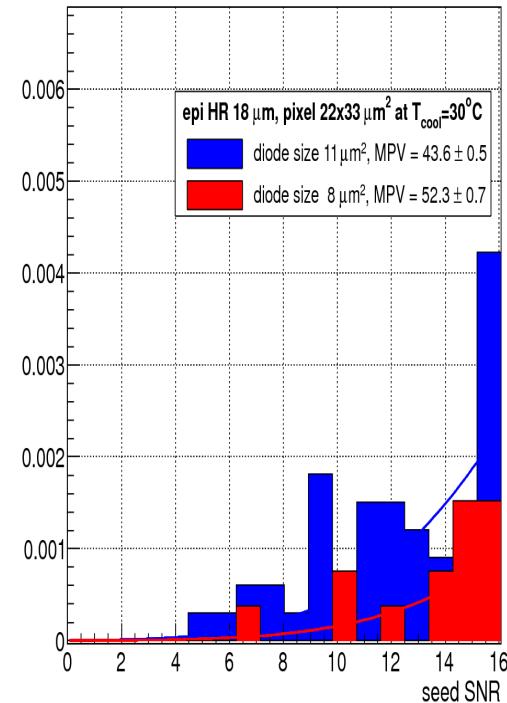
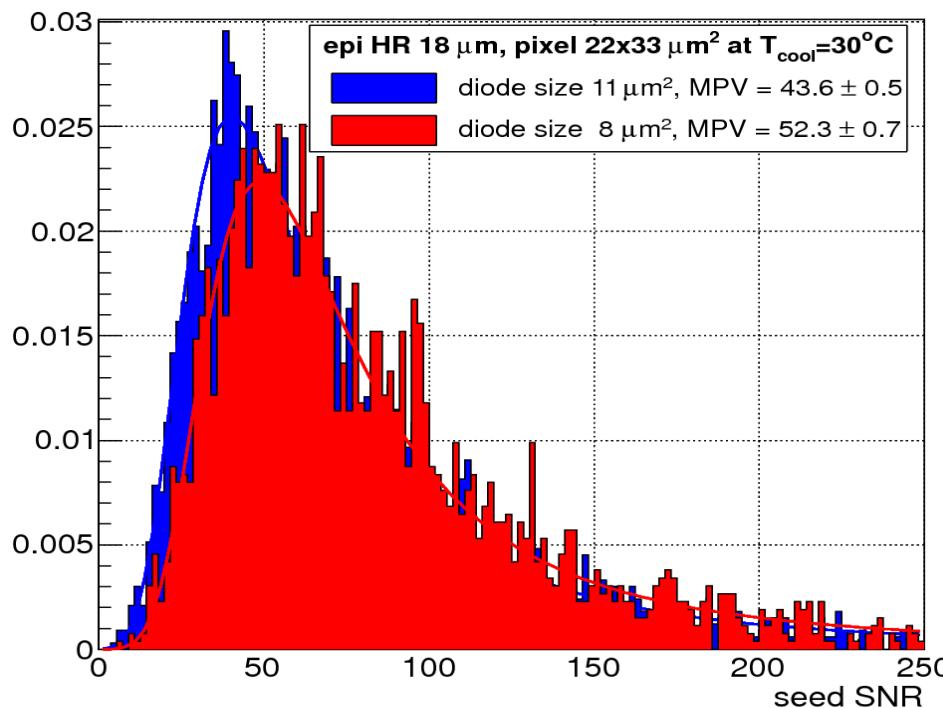
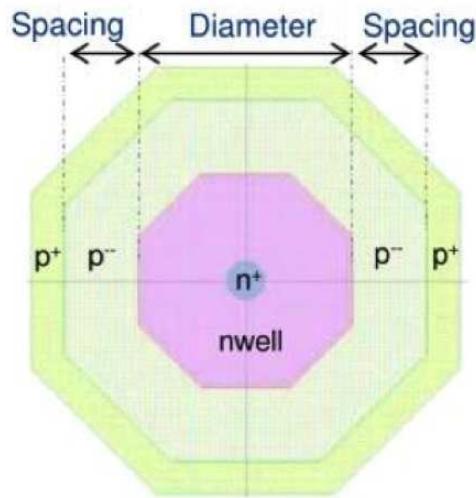
- apply highest possible voltage on sensing diode  
preserving charge sharing  $\mapsto \sigma_{sp}$
- alternative : backside/reverse biasing



⇒ Multiparametric trade-off to be found,  
based on exploratory prototypes rather than on simulations

# Charge Sensing Element $\mapsto$ Optimal SNR

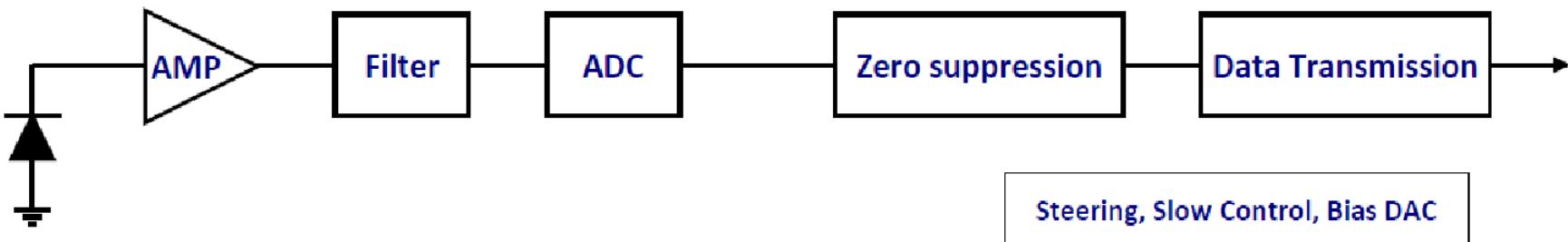
- Influence of sensing diode area



- Benefit from reducing the sensing diode area

- sensing diode cross-section varied from  $10.9 \mu\text{m}^2$  to  $8 \mu\text{m}^2$  underneath  $10.9 \mu\text{m}^2$  large footprint
  - suppresses low SNR tail  $\mapsto$  enhances detection efficiency (and mitigates effect of fake rate)

# Main Components of the Signal Processing Chain



- **Typical components of read-out chain :**

- **AMP** : In-pixel low noise pre-amplifier
- **Filter** : In-pixel filter
- **ADC** : Analog-to-Digital Conversion : 1-bit  $\equiv$  discriminator
  - ↳ may be implemented at column or pixel level
- **Zero suppression** : Only hit pixel information is retained and transferred
  - ↳ implemented at sensor periphery (usual) or inside pixel array
- **Data transmission** : O(Gbits/s) link implemented on sensor periphery

- **Read-Out alternatives :**

- **Synchronous** : rolling shutter architecture
- **Asynchronous** : data driven architecture

- **Rolling shutter : best approach for twin-well processes**

- ↳ trade-off between performance, design complexity, pixel dimensions, power, ...
  - ↳ MIMOSA-26 (EUDET), MIMOSA-28 (STAR), ...

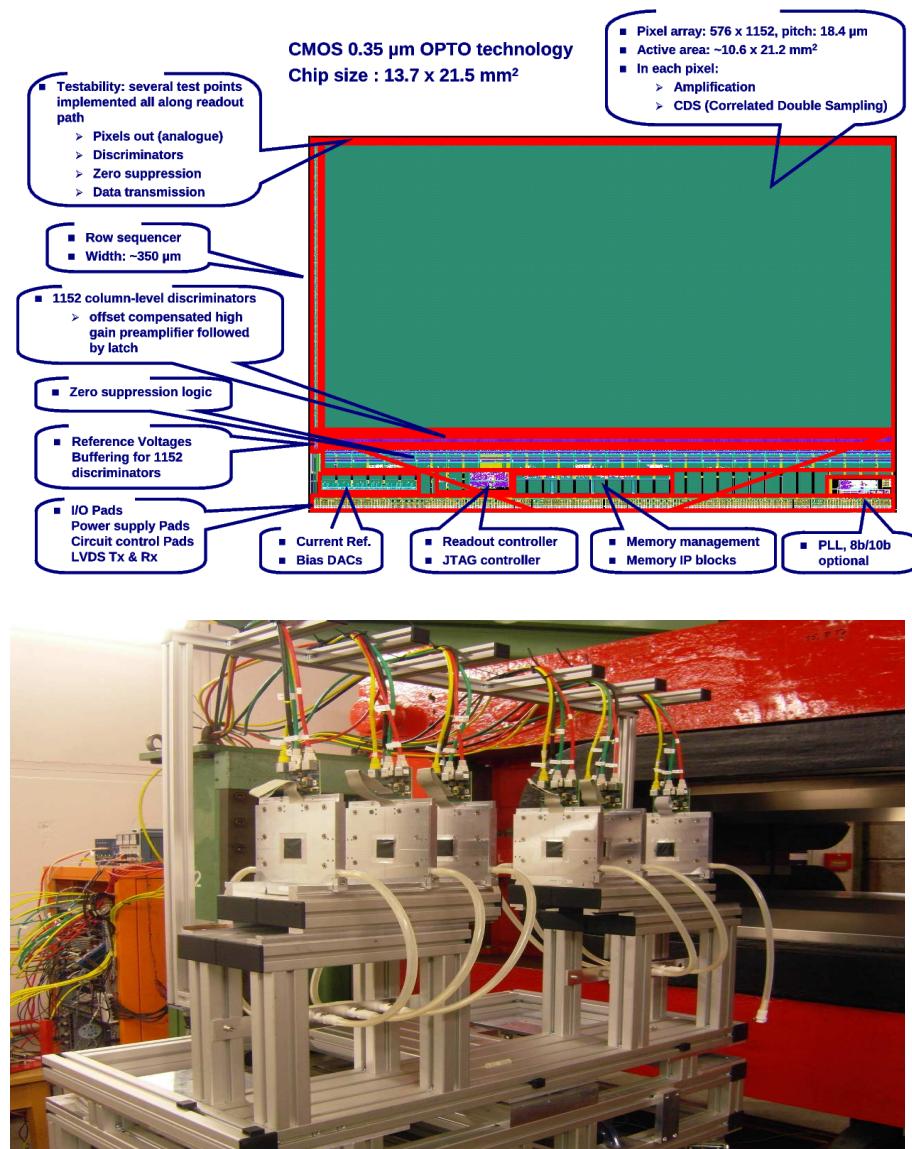
**STATE OF THE ART**

**RUNNING INSTRUMENTS  
EQUIPPED WITH CPS**

# CMOS Pixel Sensors: Established Architecture

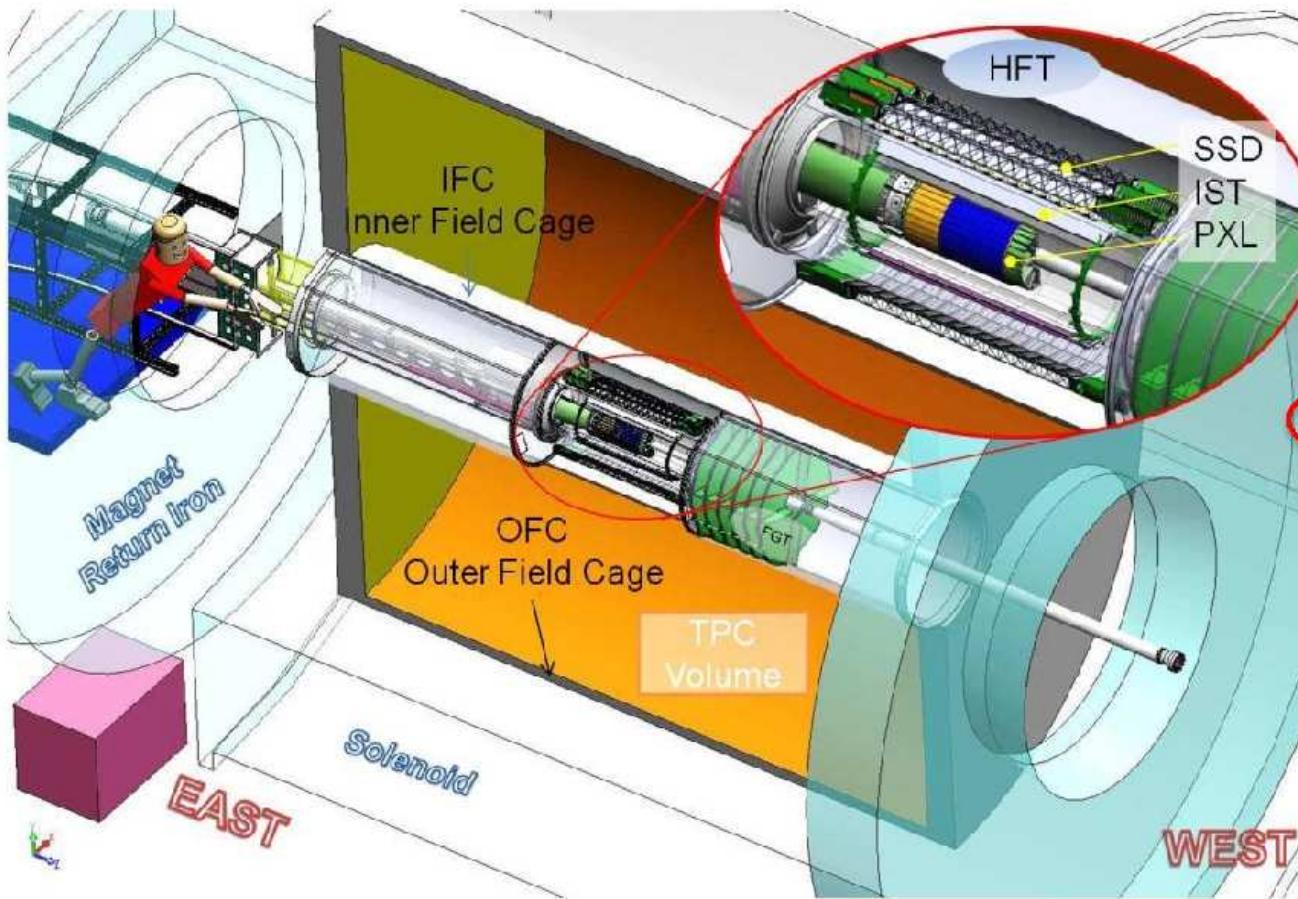
- Main characteristics of MIMOSA-26 sensor equipping EUDET BT :

- 0.35  $\mu\text{m}$  process with high-resistivity epitaxial layer (coll. with IRFU/Saclay)
- column // architecture with in-pixel amplification (cDS) and end-of-column discrimination, followed by  $\emptyset$
- binary charge encoding
- active area: 1152 columns of 576 pixels ( $21.2 \times 10.6 \text{ mm}^2$ )
- pitch: 18.4  $\mu\text{m}$   $\rightarrow$   $\sim 0.7$  million pixels
  - charge sharing  $\Rightarrow$   $\sigma_{sp} \sim 3\text{-}3.5 \mu\text{m}$
- $t_{r.o.} \lesssim 100 \mu\text{s}$  ( $\sim 10^4$  frames/s)
  - $\hookrightarrow$  suited to  $> 10^6$  part./ $\text{cm}^2/\text{s}$
- JTAG programmable
- rolling shutter architecture
  - $\Rightarrow$  full sensitive area dissipation  $\cong 1$  row
  - $\triangleright$   $\sim 250 \text{ mW/cm}^2$  power consumption (fct of  $N_{col}$ )
- thinned to 50  $\mu\text{m}$  (yield  $\sim 90\%$ )



- Various applications : VD demonstrators, NA63, NA61, FIRST, oncotherapy, dosimetry, ...

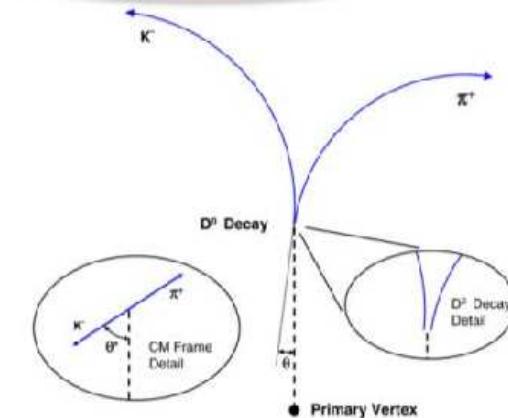
# PXL in STAR Inner Detector Upgrades



TPC – Time Projection Chamber  
(main tracking detector in STAR)

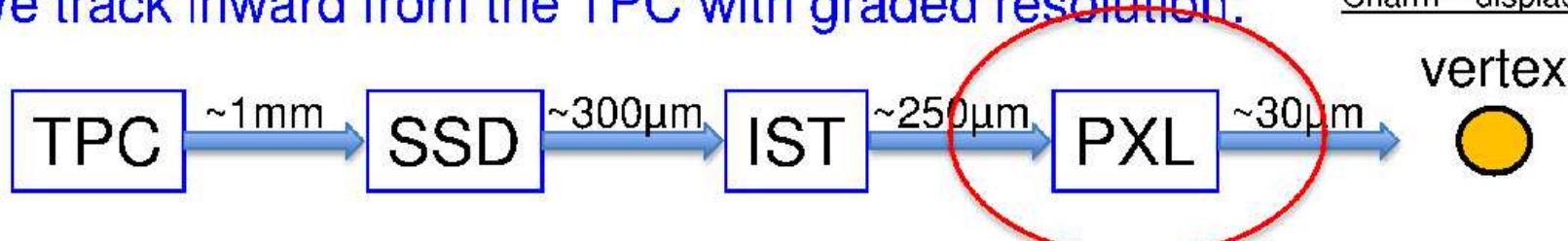
HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
  - $r = 22 \text{ cm}$
- IST – Inner Silicon Tracker
  - $r = 14 \text{ cm}$
- PXL – Pixel Detector
  - $r = 2.8, 8 \text{ cm}$



Direct topological reconstruction of  
Charm – displaced vertices

We track inward from the TPC with graded resolution:

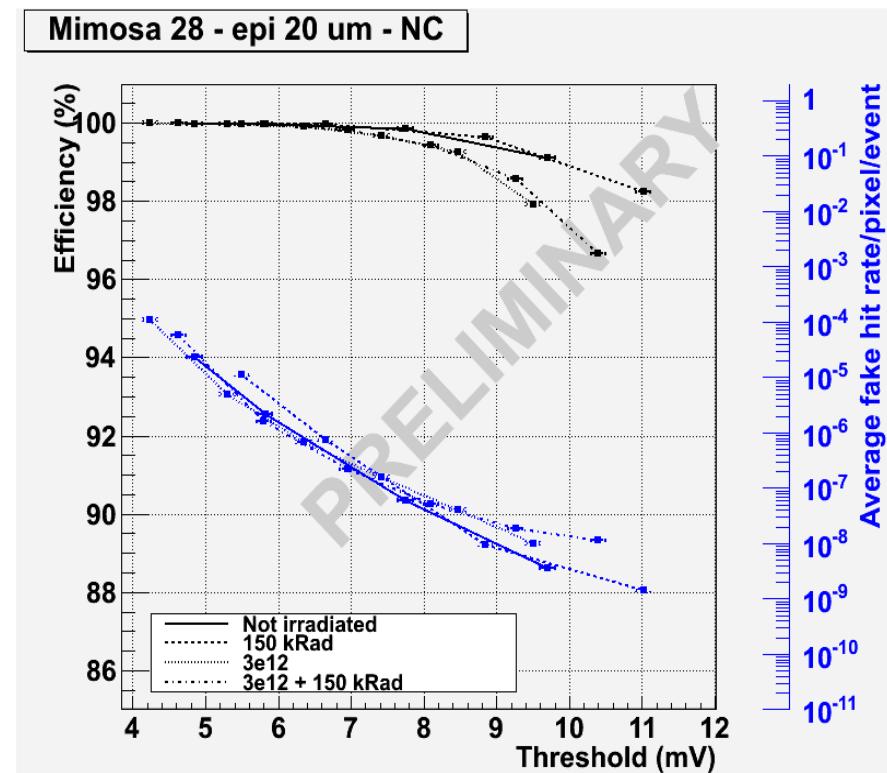
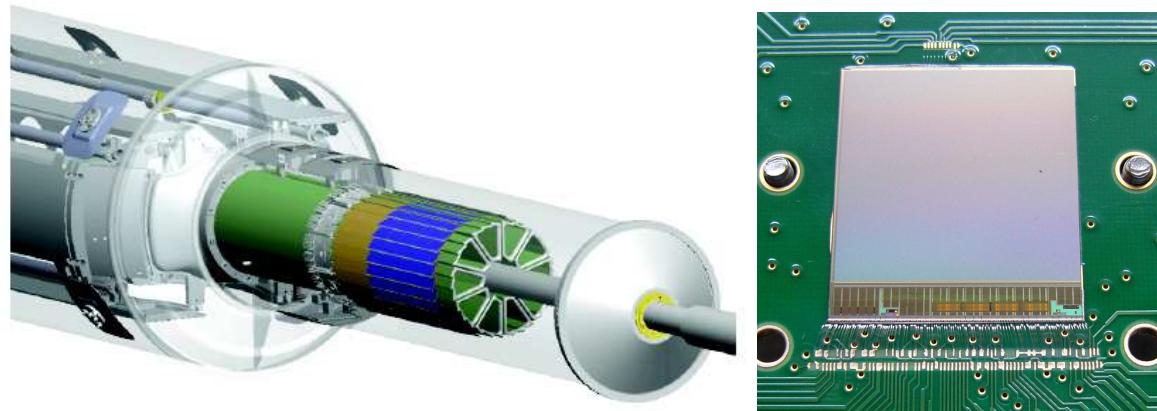


L. Greiner  
(CPIX-14)

# State-of-the-Art: MIMOSA-28 for the STAR-PXL

- Main characteristics of ULTIMATE ( $\equiv$  MIMOSA-28):

- 0.35  $\mu m$  process with high-resistivity epitaxial layer
- column // architecture with in-pixel cDS & amplification
- end-of-column discrimination & binary charge encoding
- on-chip zero-suppression
- active area: 960 columns of 928 pixels ( $19.9 \times 19.2 \text{ mm}^2$ )**
- pitch:  $20.7 \mu m \rightarrow \sim 0.9 \text{ million pixels}$** 
  - charge sharing  $\Rightarrow \sigma_{sp} \gtrsim 3.5 \mu m$
- JTAG programmable
- $t_{r.o.} \lesssim 200 \mu s (\sim 5 \times 10^3 \text{ frames/s}) \Rightarrow$  suited to  $> 10^6 \text{ part./cm}^2/\text{s}$
- 2 outputs at 160 MHz
- $\lesssim 150 \text{ mW/cm}^2$  power consumption

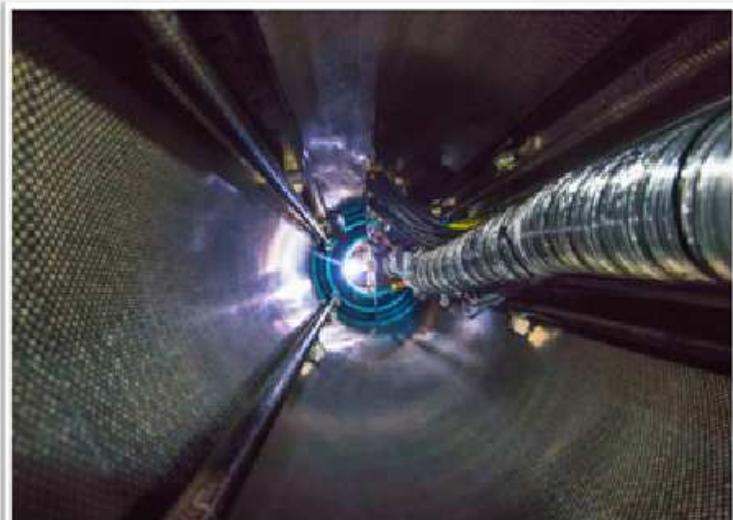


▷▷▷ Sensors FULLY evaluated/validated : (50  $\mu m$  thin)

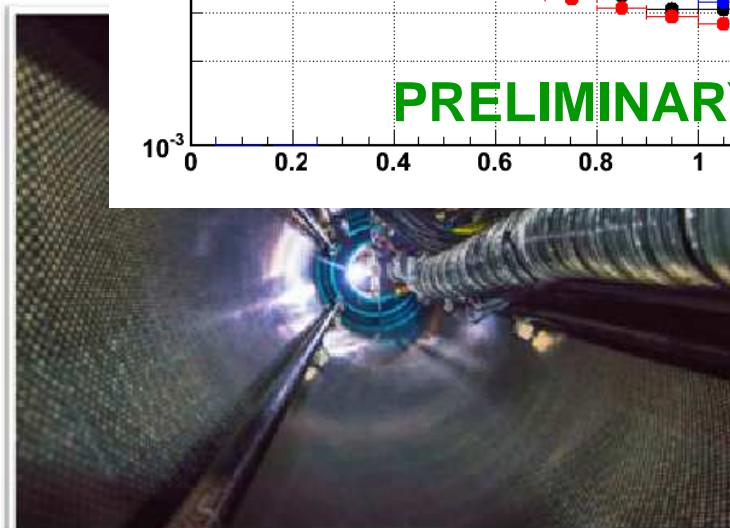
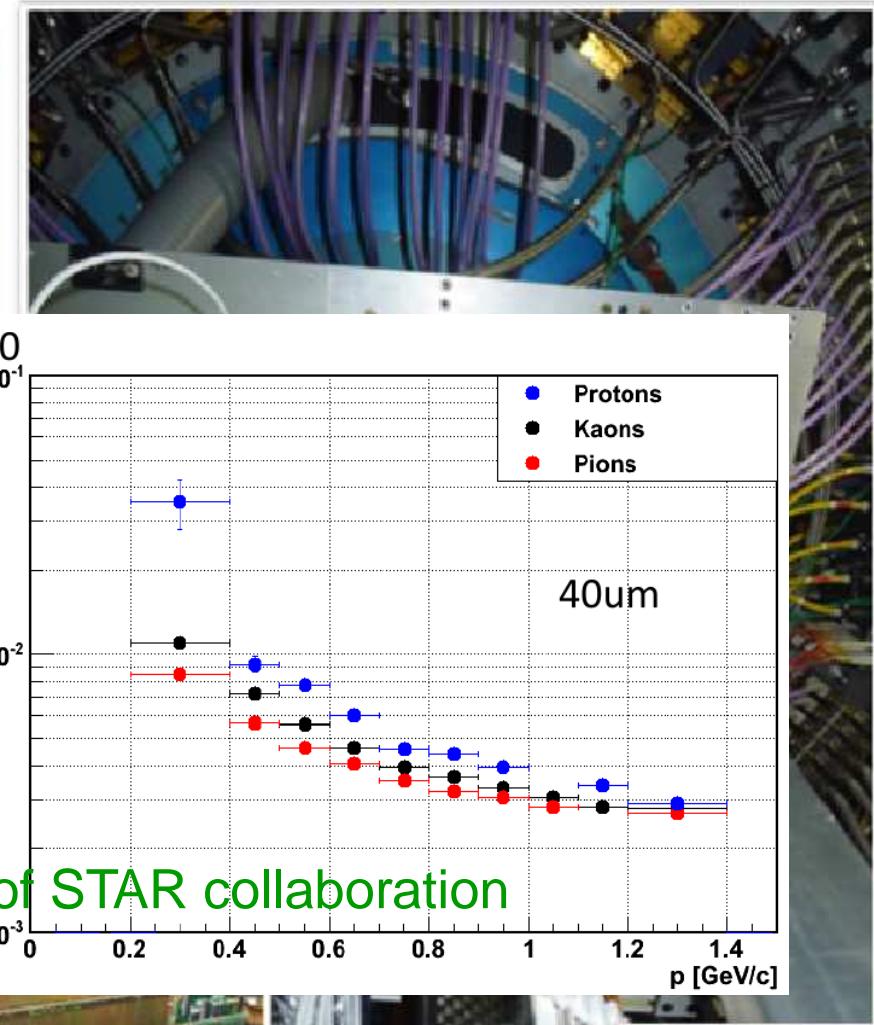
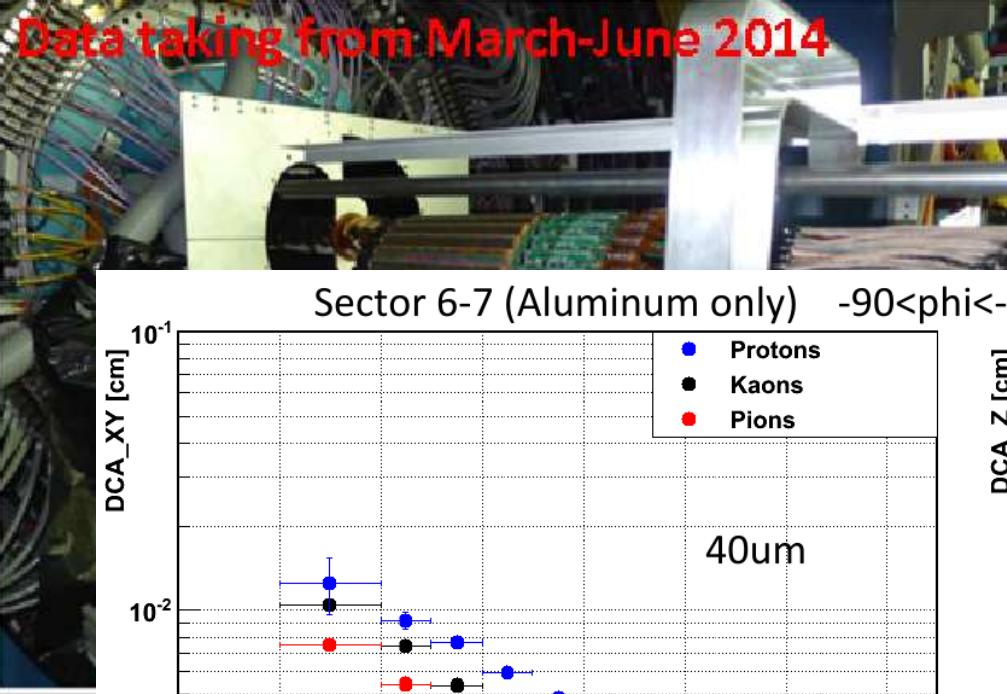
- $N \lesssim 15 \text{ e}^- \text{ ENC}$  at 30-35°C
- $\epsilon_{det}$ , fake &  $\sigma_{sp}$  as expected
- Rad. tol. validated ( $3 \cdot 10^{12} \text{n}_{eq}/\text{cm}^2$  & 150 kRad at 30°C)**
- All specifications were met  $\Rightarrow$  2 detectors of 40 ladders constructed

▷▷▷ Physics data taking since March 2014  $\mapsto$  measured  $\sigma_{ip}(p_T)$  match requirements

# State-of-the-Art : STAR-PXL

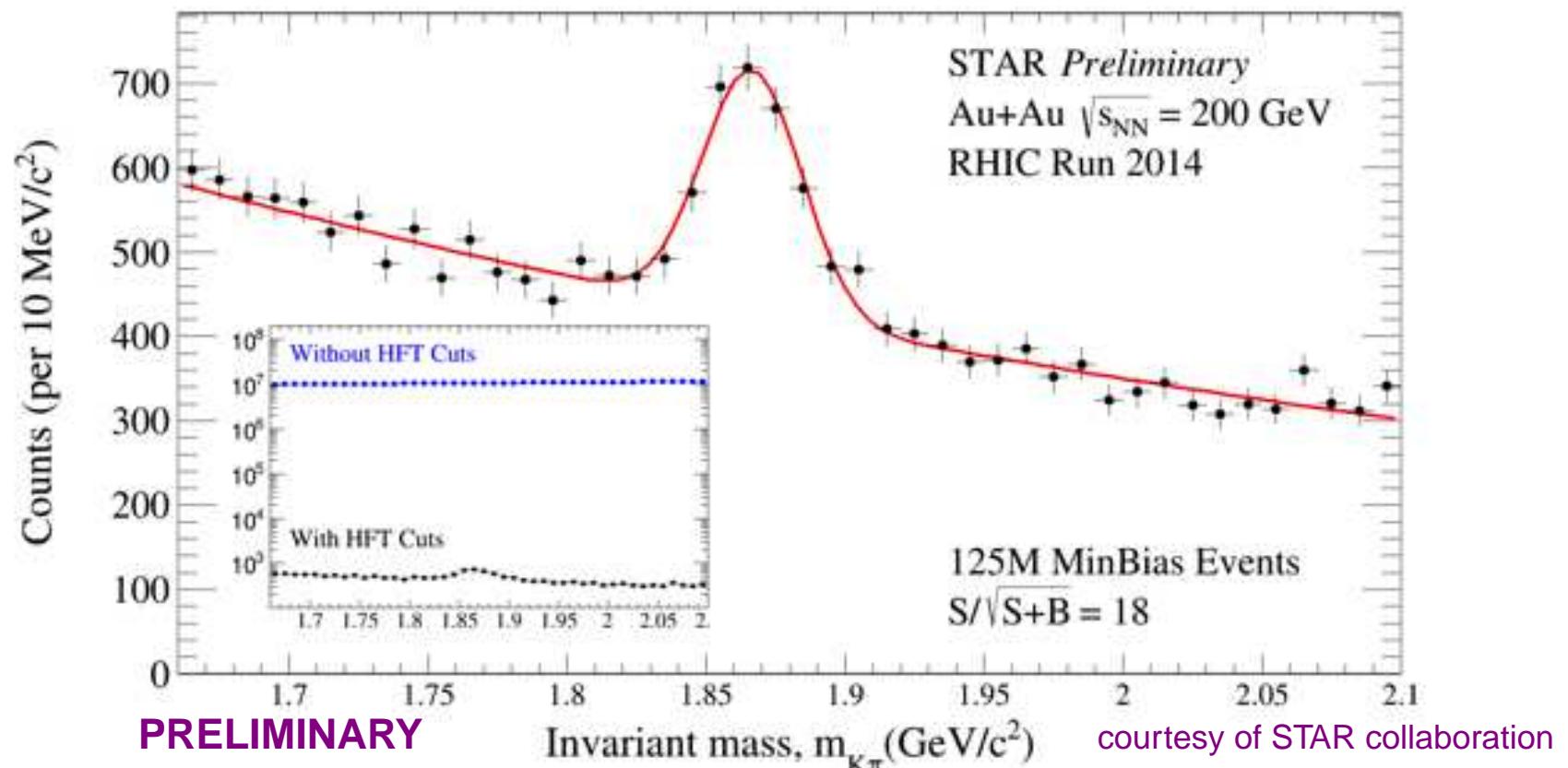
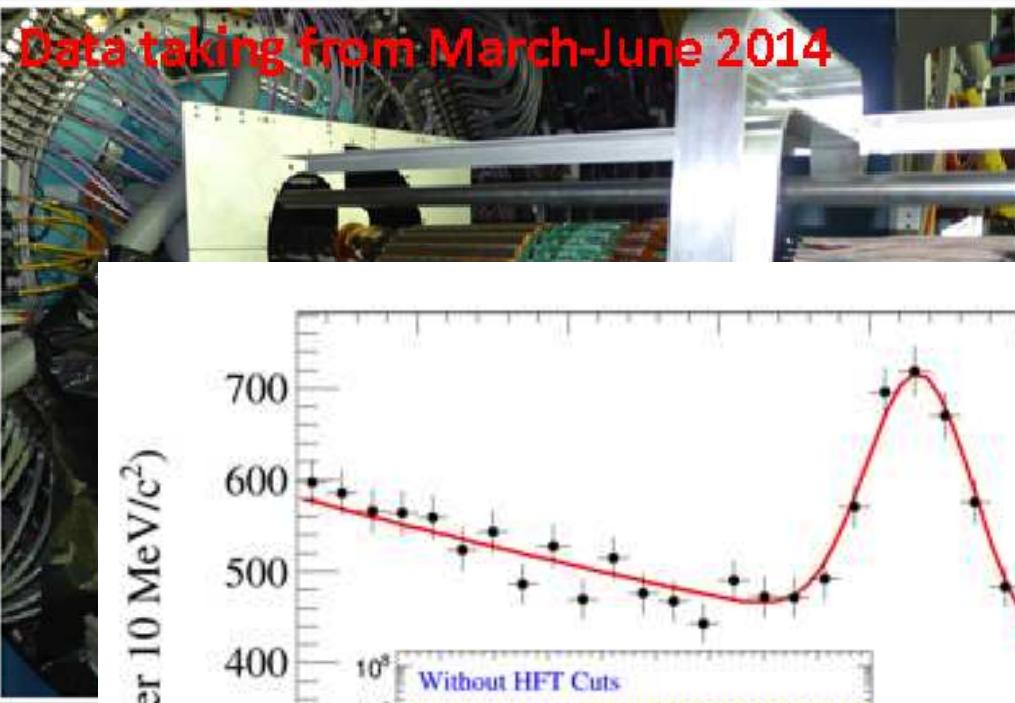


# State-of-the-Art : STAR-PXL



Validation of CPS for HEP (25/09/14 : DoE final approval, based on vertexing performance assessment)

# State-of-the-Art : STAR-PXL



Validation of CPS for HEP (25/09/14 : DoE final approval, based on vertexing performance assessment)

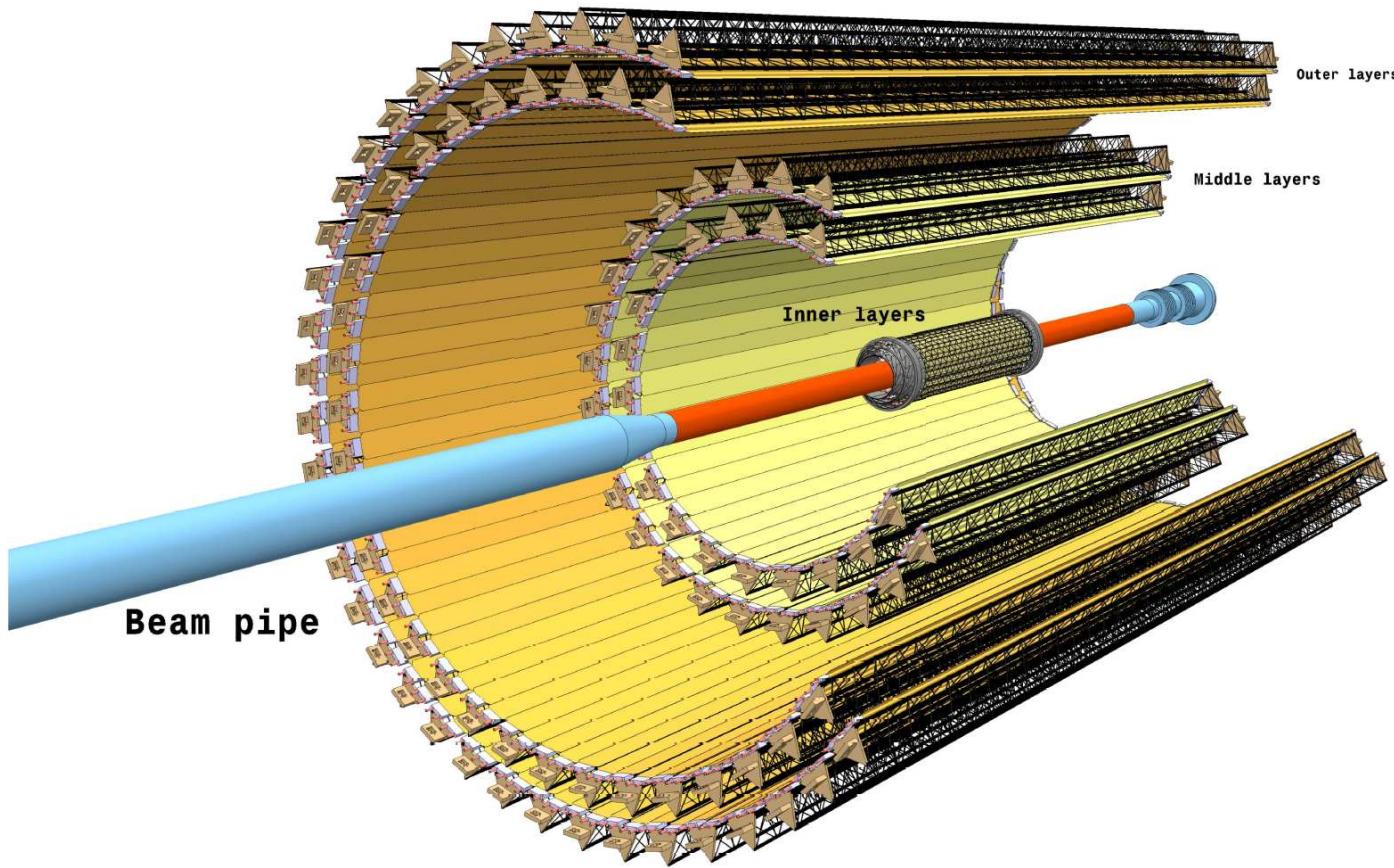
# **Next Generations of High Precision Tracking & Vertexing Sub-Systems**

# **Next Generations of High Precision Tracking & Vertexing Sub-Systems**

**call for FASTER and  
MORE RADIATION TOLERANT**

**CMOS Pixel Sensors (CPS)**

# Forthcoming Device : New ALICE Inner Tracking System



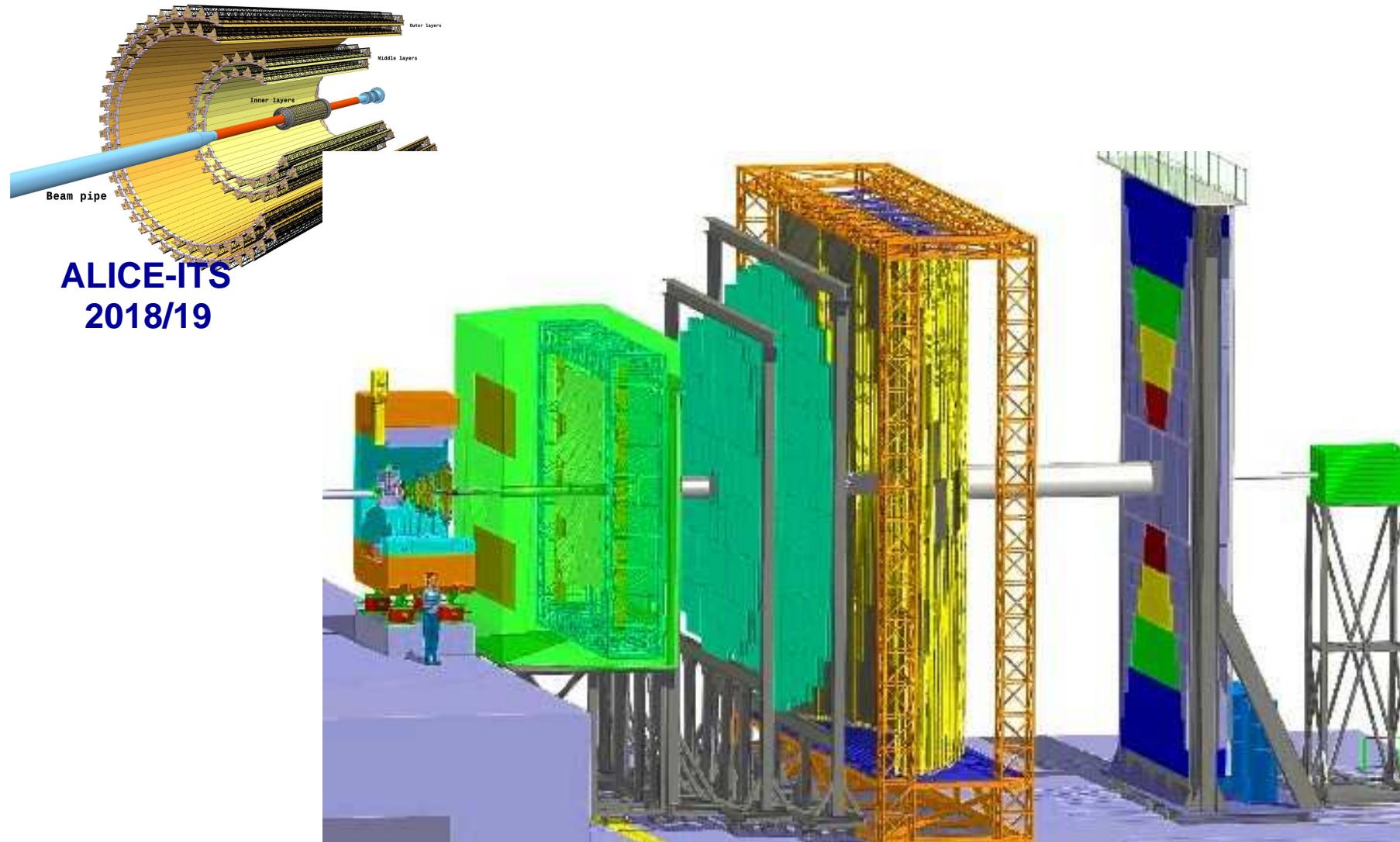
$$\sigma_{sp} \lesssim 5 \mu m$$

$$\simeq 0.3 \% X_0 / \text{layer}$$

## Upgrade of ALICE-ITS at LHC

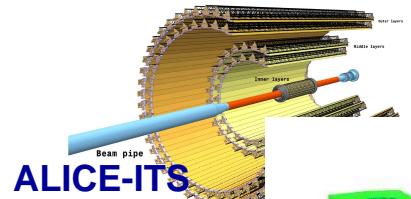
7 layers,  $> 10 \text{ m}^2$  active area with  $\gg 10^4 \text{ CPS}$

## Next Forthcoming Device : CBM Micro-Vertex Detector

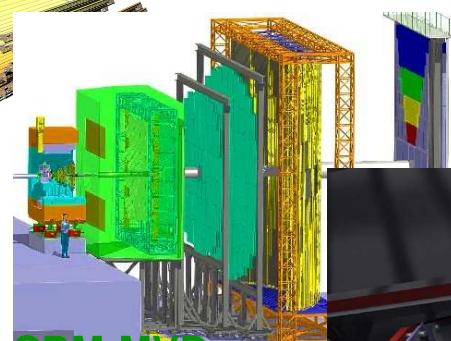


**CBM-MVD at FAIR/GSI :** 3 (2-sided) stations in vacuum at  $T < 0^\circ\text{C}$   
 $\mapsto \sigma_{sp} \lesssim 5 \mu\text{m}, \lesssim 0.5 \% X_0/\text{station}$

# Device under Study : ILC Vertex Detector

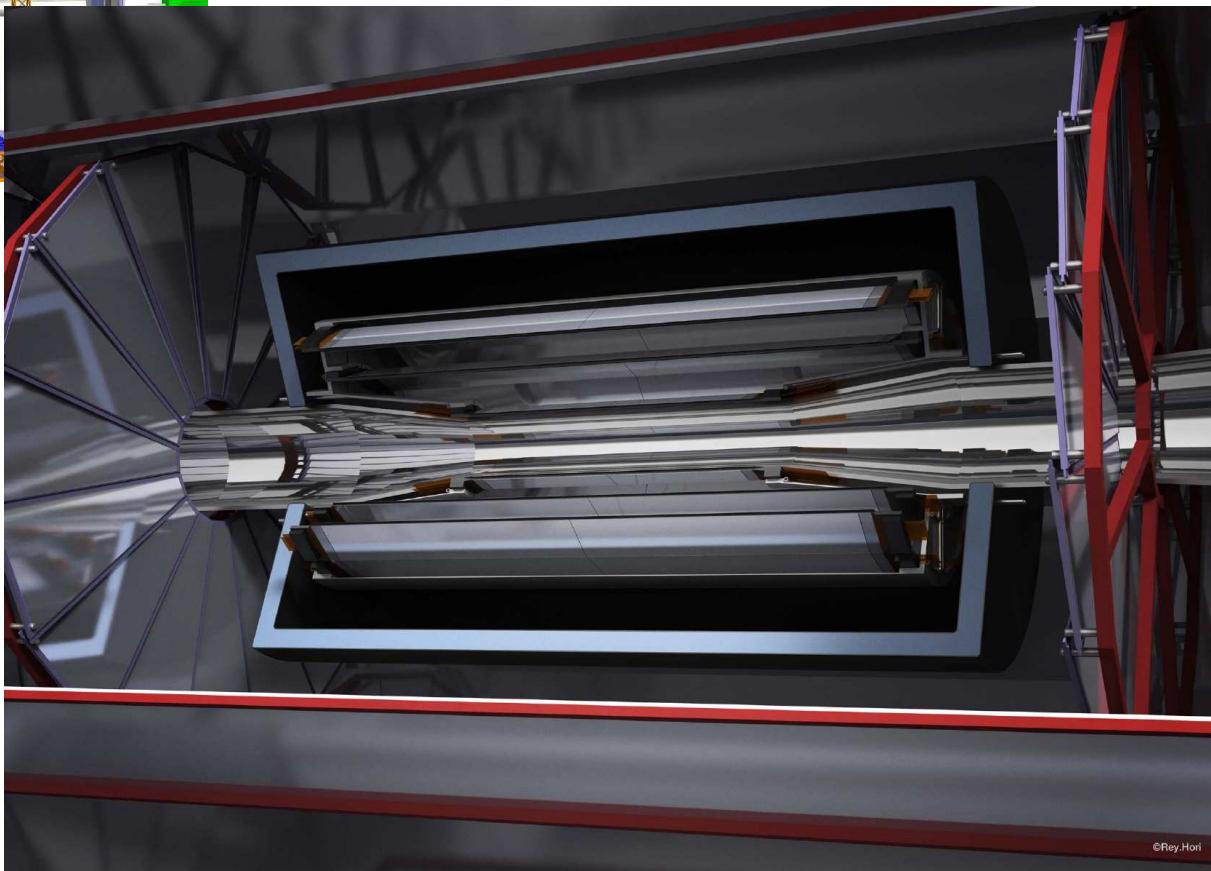


2018/19



> 2020

ILD-VXD  
(> 2025)

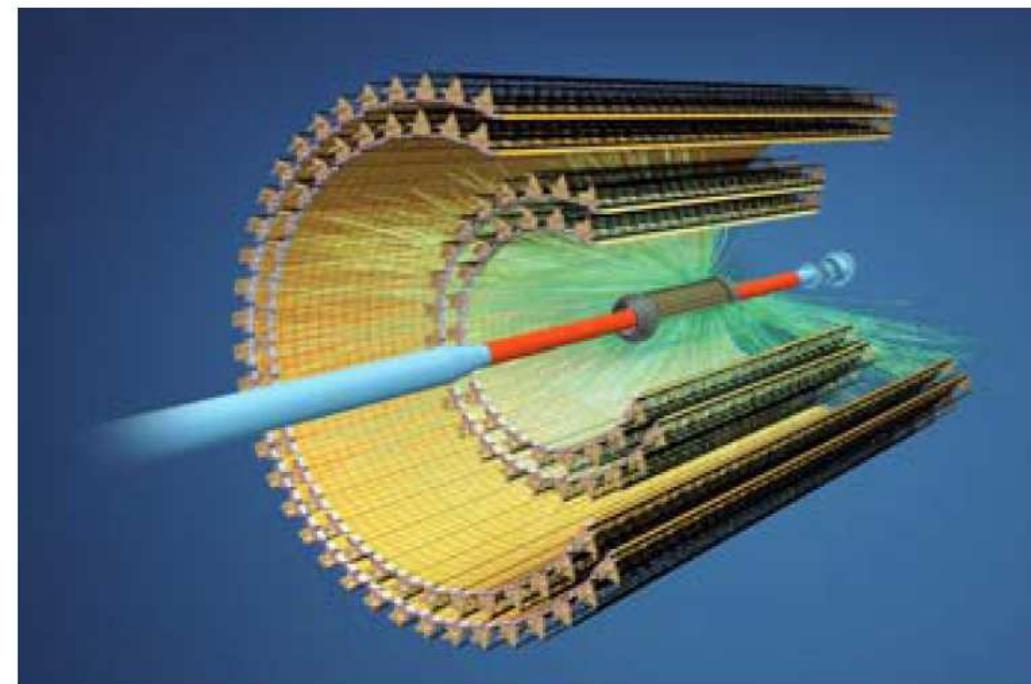


3 (2-sided) layers : CPS  $\equiv$  option  $\mapsto \sigma_{sp} \lesssim 3 \mu m, \lesssim 0.3 \% X_0/\text{layer}$

# Next Challenge : ALICE-ITS Upgrade

- Upgrade of ITS entirely based on CPS :

- Present geometry: 6 layers  
HPS x 2 / Si-drift x 2 / Si-strips x 2
- Future geometry : 7 layers    →    →    →  
all with CPS ( $\sim 25-30 \cdot 10^3$  chips)  
⇒ 1st large tracker ( $10 \text{ m}^2$ ) using CPS
- ITS-TDR approved March 2014 :  
Pub. in J.Phys. G41 (2014) 087002



- Requirements for ITS inner and outer barrels compared to specifications of STAR-PXL chip :

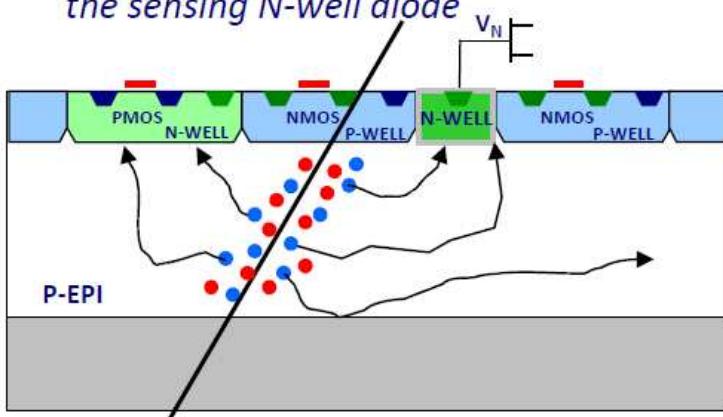
	$\sigma_{sp}$	$t_{r.o.}$	Dose	Fluency	$T_{op}$	Power	Active area
STAR-PXL	$< 4 \mu\text{m}$	$< 200 \mu\text{s}$	150 kRad	$3 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2$	30-35°C	$160 \text{ mW/cm}^2$	$0.15 \text{ m}^2$
ITS-in	$\lesssim 5 \mu\text{m}$	$\lesssim 30 \mu\text{s}$	<b>2.7 MRad</b>	$1.7 \cdot 10^{13} \text{ n}_{eq}/\text{cm}^2$	30°C	$< 300 \text{ mW/cm}^2$	$0.17 \text{ m}^2$
ITS-out	$\lesssim 10 \mu\text{m}$	$\lesssim 30 \mu\text{s}$	15 kRad	$4 \cdot 10^{11} \text{ n}_{eq}/\text{cm}^2$	30°C	$< 100 \text{ mW/cm}^2$	$\sim 10 \text{ m}^2$

⇒ **0.35  $\mu\text{m}$  CMOS process (STAR-PXL) marginally suited to read-out speed & radiation tol.**

# CMOS Process Transition : STAR-PXL $\mapsto$ ALICE-ITS

## ■ Twin well process: 0.6-0.35 $\mu\text{m}$

- ↳ Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode

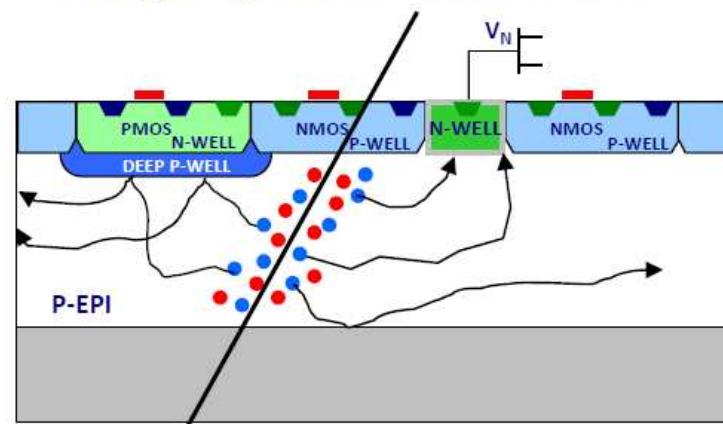


- ↳ Limits choice of readout architecture strategy
- ↳ Already demonstrate excellent performances
  - STAR PXL detector: MIMOSA28 are designed in this AMS-0.35  $\mu\text{m}$  process
    - ✓  $\varepsilon_{\text{eff}} > 99.5\%$ ,  $\sigma < 4 \mu\text{m}$
  - 1st CPS based VX detector at a collider experiment

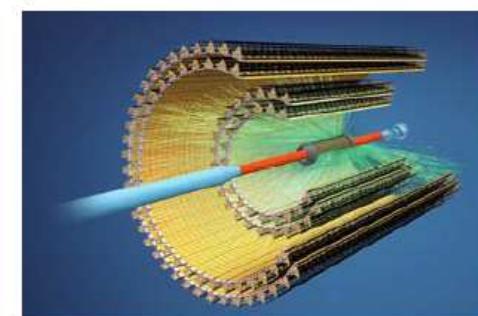


## ■ Quadruple well process (deep P-well): 0.18 $\mu\text{m}$

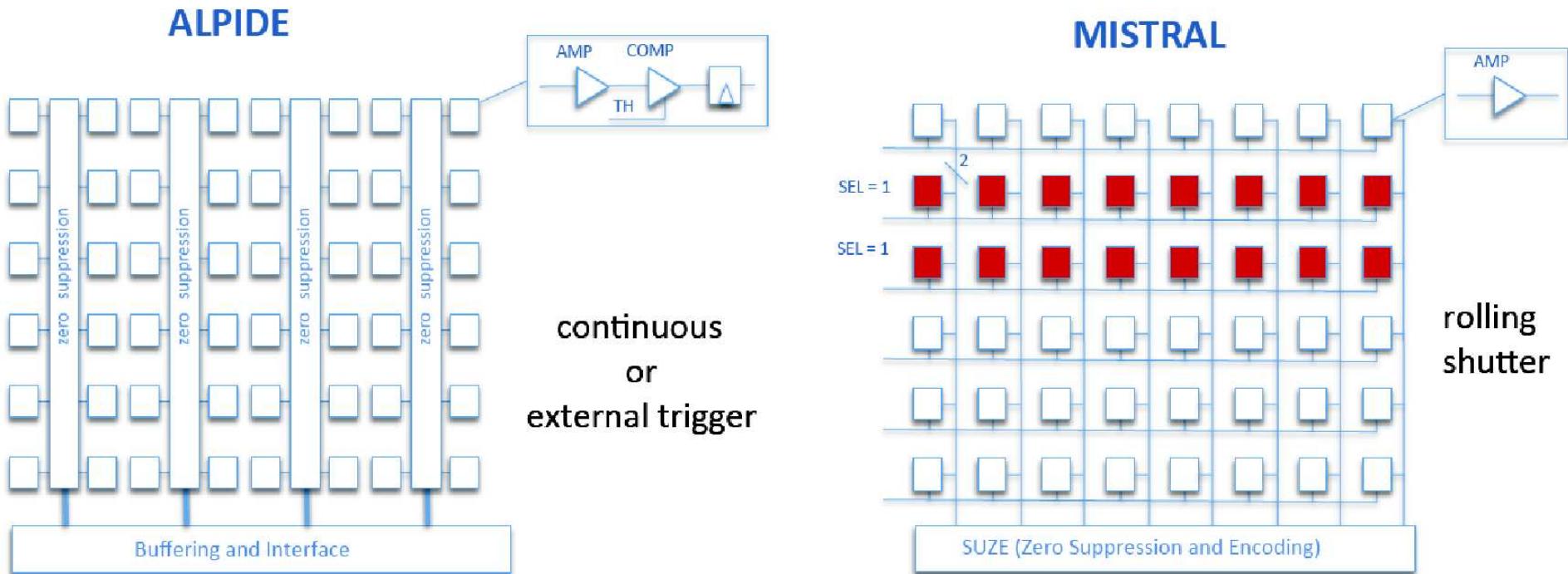
- ↳ N-well used to host PMOS transistors is shielded by deep P-well
- ↳ Both types of transistors can be used



- ↳ Widens choice of readout architecture strategies
  - Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18  $\mu\text{m}$  process (quadruple well)
    - Synchronous Readout R&D:
      - ✓ proven architecture = safety
    - Asynchronous Readout R&D: challenging



# ITS Pixel Sensor : Two Architectures



<b>Pixel dimensions</b>	$27\mu m \times 29\mu m$
<b>Event time resolution</b>	$4\mu s$
<b>Power consumption</b>	$< 50mW/cm^2$
<b>In insensitive area</b>	$\sim 1mm \times 30mm$

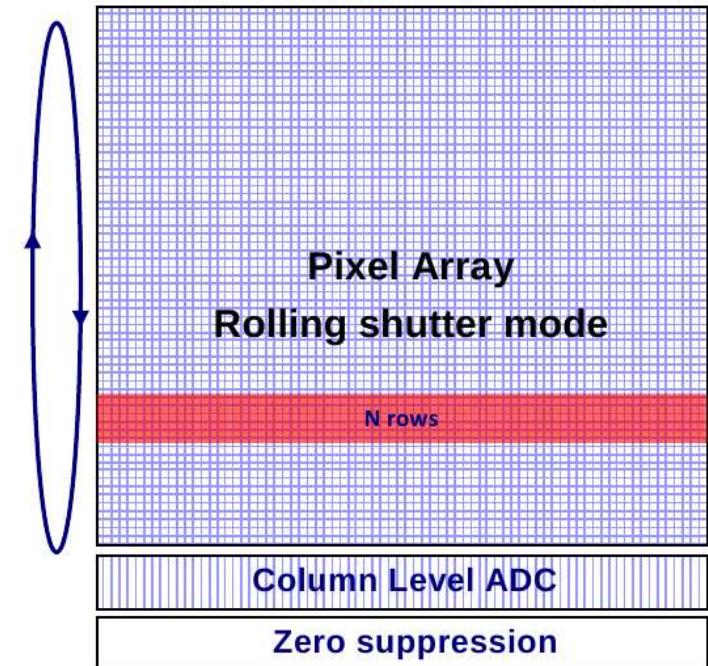
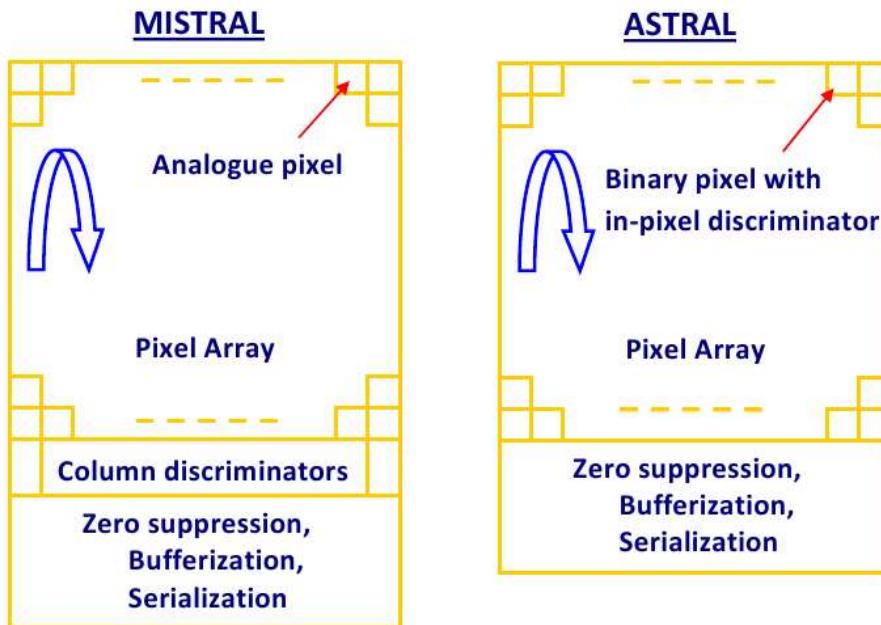
<b>Pixel dimensions</b>	$36\mu m \times 65\mu m$
<b>Event time resolution</b>	$20\mu s$
<b>Power consumption</b>	$\lesssim 90mW/cm^2$
<b>In insensitive area</b>	$1.5mm \times 30mm$

- Both chips have identical dim. (15mm x 30 mm) as well as physical and electrical interfaces:
  - \* position of interface pads
  - \* electrical signaling
  - \* steering, read-out, ... protocoles

# Synchronous Read-Out Architecture : Rolling Shutter Mode

## ■ Design addresses 3 issues:

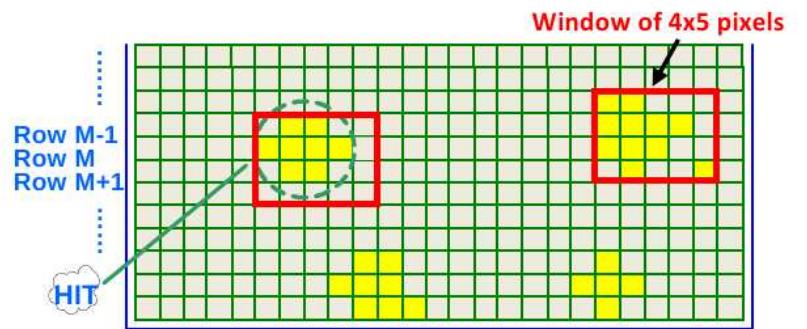
- ↳ Increasing S/N at pixel-level
- ↳ A to D Conversion:
  - at column-level (**MISTRAL**)
  - at pixel-level (**ASTRAL**)
- ↳ Zero suppression (**SUZE**) at chip edge level



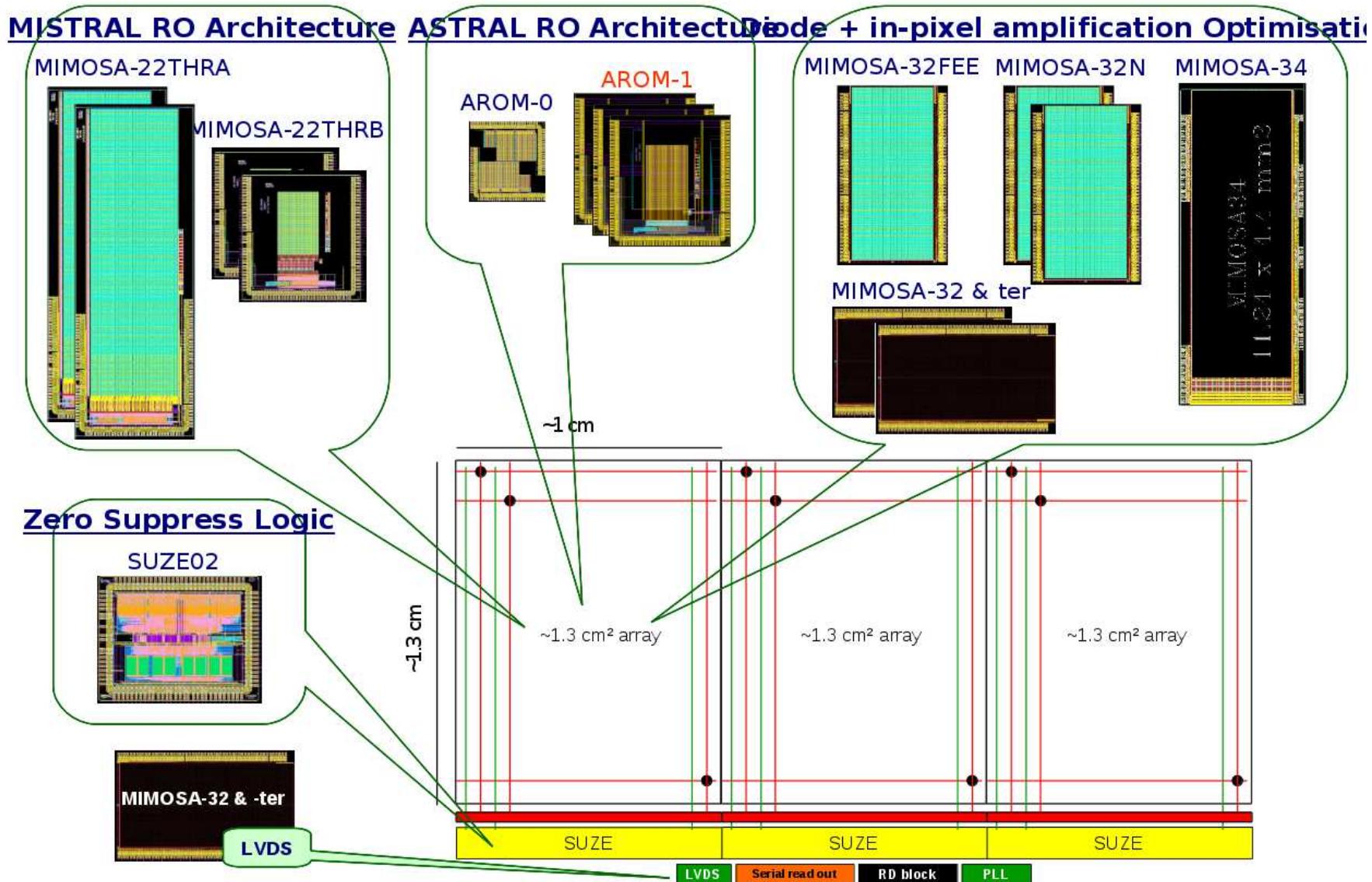
## ■ Power vs speed:

- ↳ Power: only the selected rows ( $N=1, 2, \dots$ ) to be read out
- ↳ Speed:  $N$  rows of pixels are read out in //
  - Integration time = frame readout time

$$t_{\text{int}} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}$$



# Sensor Development Organisation



# Main Features of the Final Prototypes

- Full scale sensor building block :

- \* complete (fast) read-out chain  $\simeq$  ULTIMATE
- \* pixel area ( $\sim 1 \text{ cm}^2$ )  $\simeq$  area of final building block
- \* same nb of pixels (160,000) than complete final tracker chip
- \* fabricated with  $18 \mu\text{m}$  thick high-resistivity EPI
- \* BUT : pixels are small ( $22 \times 32.5 \mu\text{m}^2$ ) and  
sparsification circuitry is oversized (power !)
- \* **Tested at DESY (few GeV e<sup>-</sup>) in June'15**  
**and CERN-SPS (120 GeV "pions") in Oct. '15**

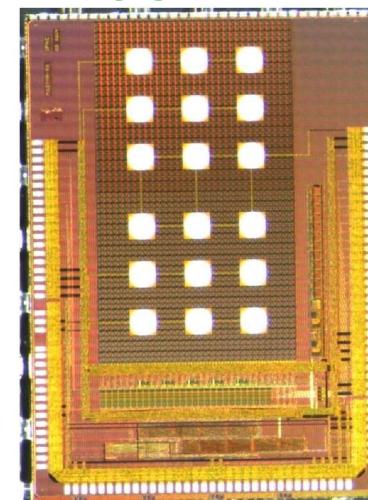
FSBB-M0bis



- Large-pixel prototype without sparsification :

- \* 2 slightly different large pixels :
  - $36.0 \mu\text{m} \times 62.5 \mu\text{m}$
  - $39.0 \mu\text{m} \times 50.8 \mu\text{m}$
- \* pads over pixels (3 ML used for in-pixel circuitry)
- \* fabricated with  $18 \mu\text{m}$  thick high-resistivity EPI
- \* BUT : only  $\lesssim 10 \text{ mm}^2$ , 4,000 pixels, no sparsification
- \* **Tested in Frascati (450 MeV e<sup>-</sup>) in March & May'15**

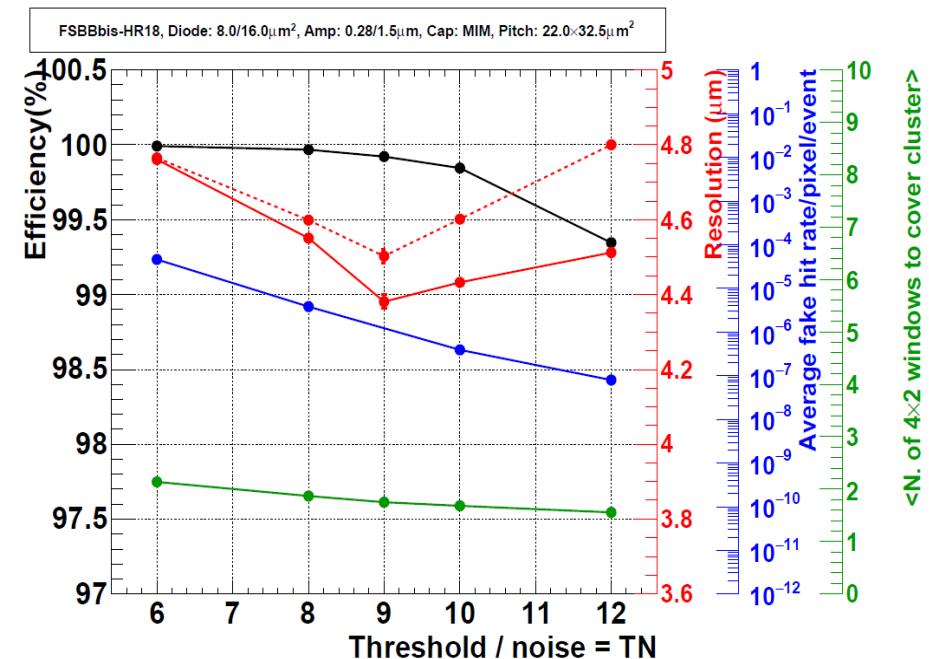
MIMOSA-22THRb



# Detection Performances of the Final Prototypes

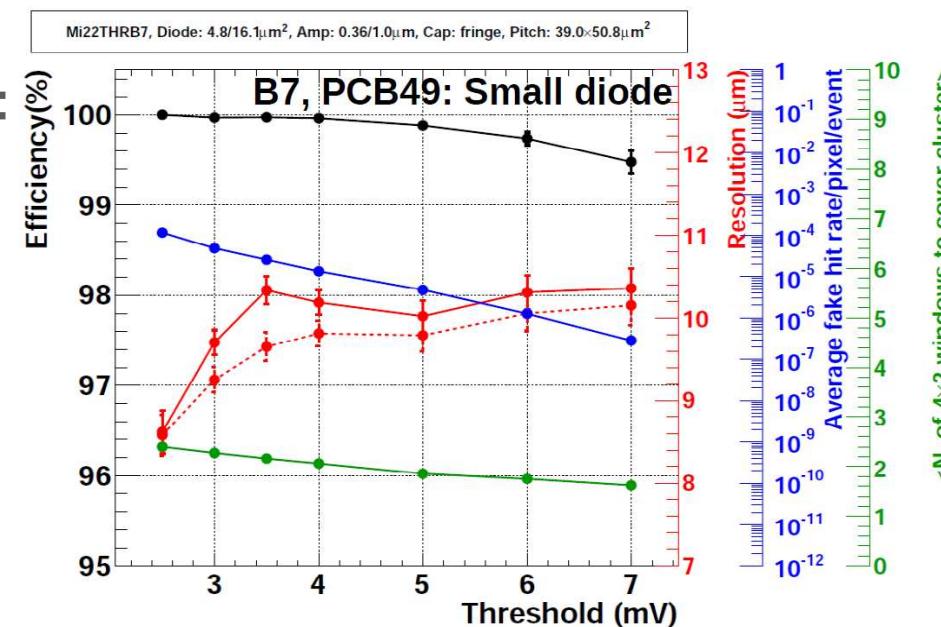
- **Full scale sensor building block :**

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- \* pixel area ( $\sim 1 \text{ cm}^2$ )  $\simeq$  area of final building block
- \* same nb of pixels (160,000) than complete final tracker chip
- \* fabricated with 18  $\mu\text{m}$  thick high-resistivity EPI
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- \* **Tested at DESY (few GeV e<sup>-</sup>) in June'15**  
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- **Large-pixel prototype without sparsification :**

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- \* BUT : only  $\lesssim 10 \text{ mm}^2$ , 4,000 pixels, no sparsification
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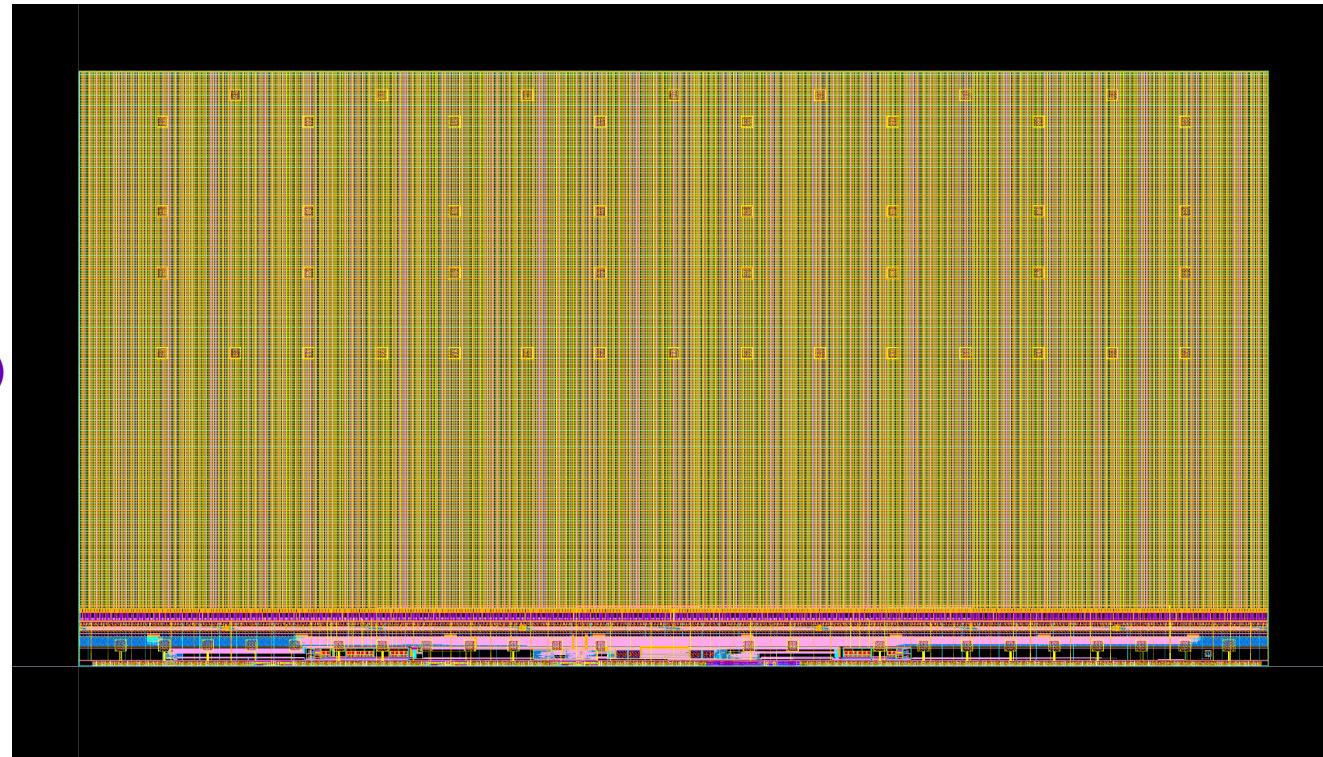


# Final Sensor : MISTRAL-O

- Combination of 4 FSBBs with MIMOSA-22THRb7 pixels

- Main characteristics :

- \* chip dimensions : 15 mm x 30 mm
- \* Sensitive area = 13.50 mm x 29.95 mm
  - 1.5 mm wide side band  
(evolving towards  $\sim 1$  mm)
- \* 832 columns of 208 pixels ( $1.6 \cdot 10^5$  pixels)
- \* pixel dimensions :  $36 \mu m \times 65 \mu m$
- \* in-pixel pre-amp & clamping (fringe capa)
- \* end-of-column signal discrimination
- \* discriminators' output sparsification
- \* fully programmable control circuitry
- \* pads over pixel array
  - \* possibility to mask noisy pixels

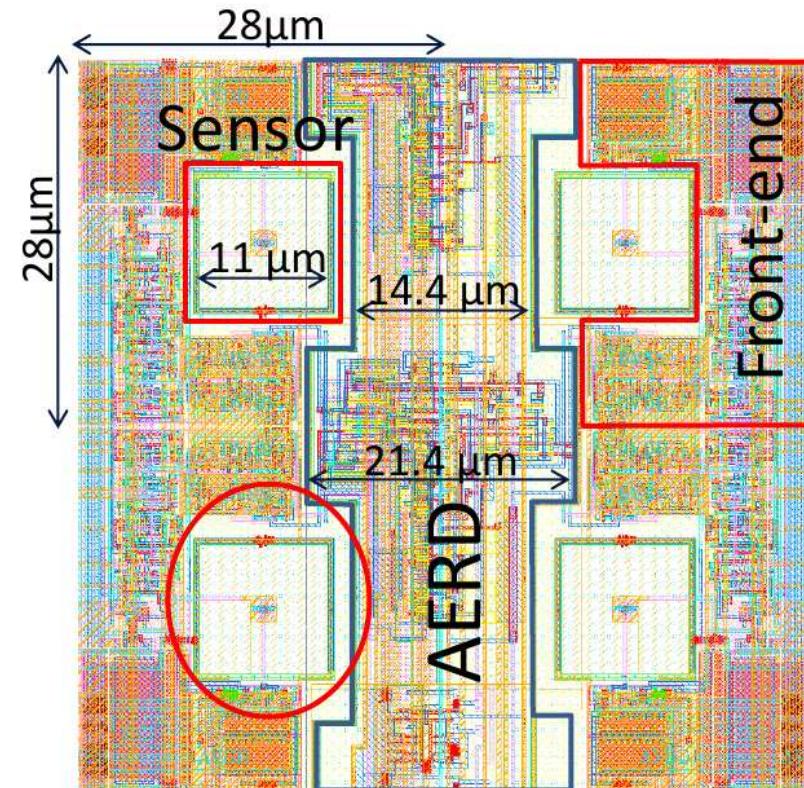
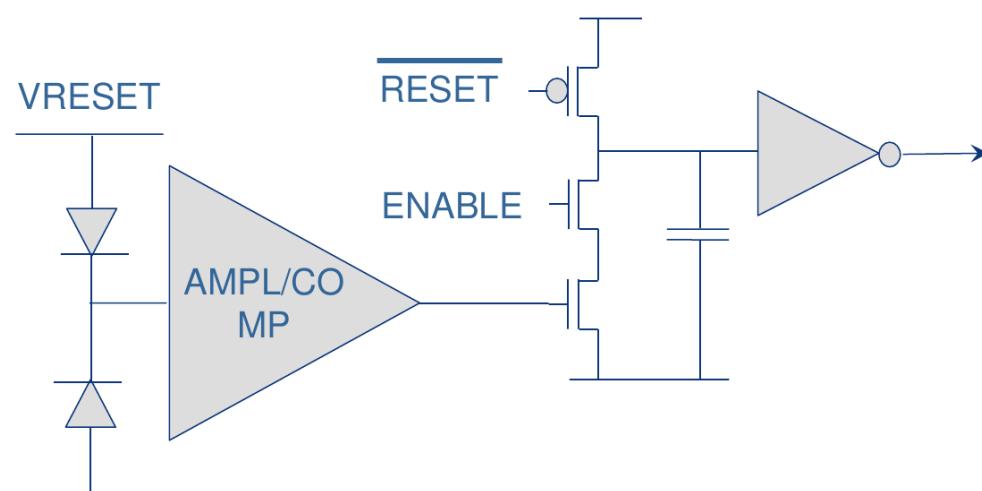


- Typical performances : (based on FSBB and MIMOSA-22THRb7 beam tests)

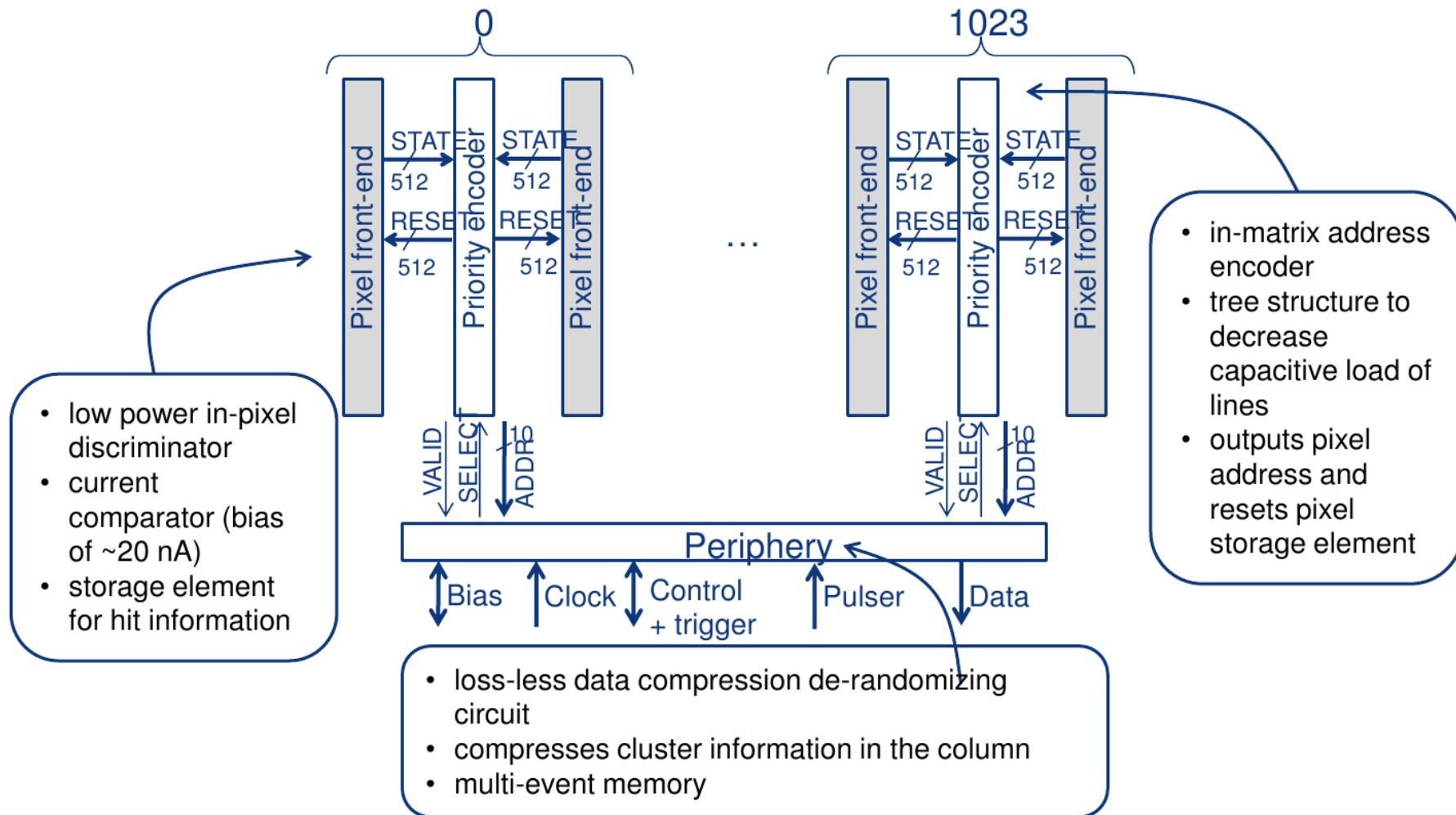
- \* read-out time  $\sim 20 \mu s$
- \* spatial resolution  $\sim 10 \mu m$
- \* power density  $\lesssim 90 \text{ mW/cm}^2$
- \* radiation tolerance  $> 1.5 \cdot 10^{12} n_{eq}/\text{cm}^2$  and 150 kRad at  $T > 30^\circ\text{C}$

# Asynchronous Read-Out Architecture : ALPIDE (Alice Pixel DEtector)

- Design concept similar to hybrid pixel read-out architecture exploiting availability of TJsc CIS quadruple well process : pixel hosts N- & P-MOS transistors
- Each pixel features a continuously power active
  - low power consuming analogue front end ( $P < 50 \text{ nW/pixel}$ ) based on a single stage amplifier with shaping / current comparator
    - amplification gain  $\sim 100$
    - shaping time  $\sim \text{few } \mu\text{s}$
  - Data driven read-out of the pixel matrix  
 $\Rightarrow$  only zero-suppressed data are transferred to periphery



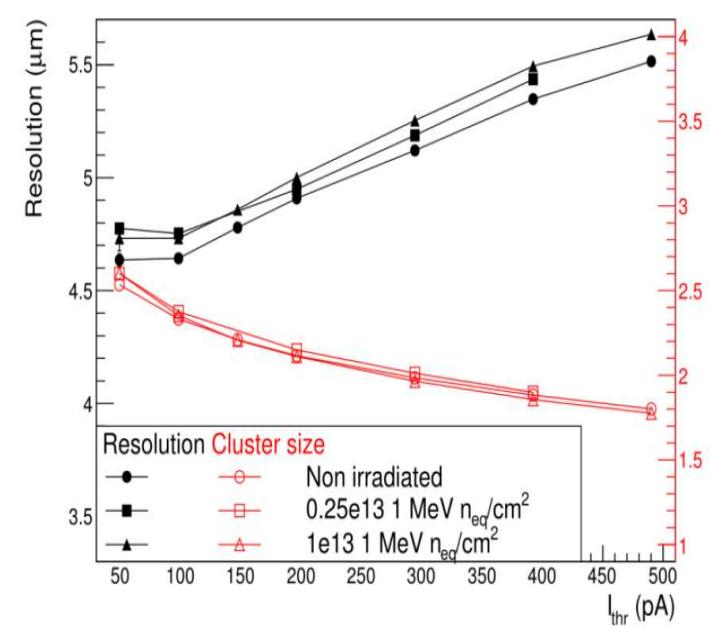
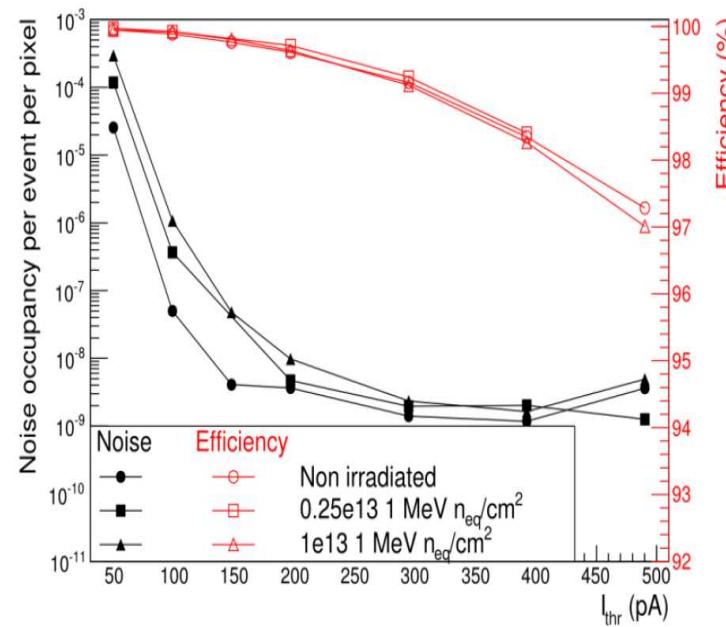
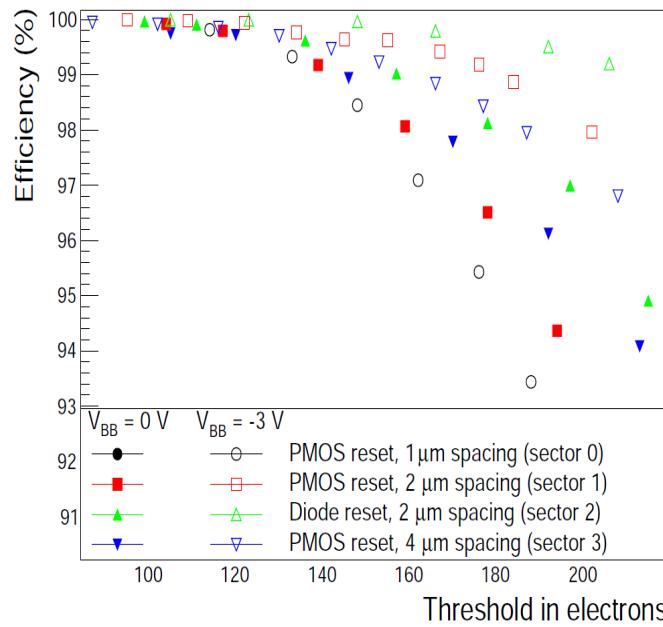
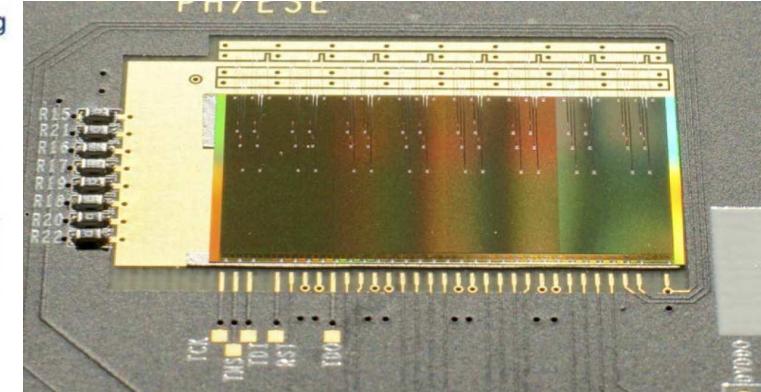
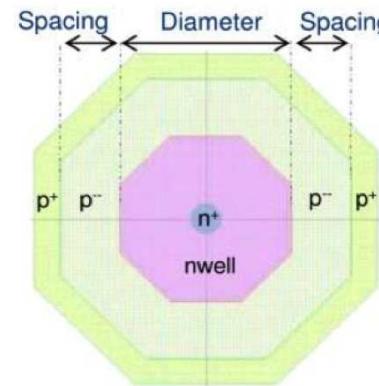
# Asynchronous Read-Out Architecture : ALPIDE



# ALPIDE Detection Performance Assessment

- ALPIDE-1 beam tests (5–7 GeV pions) :

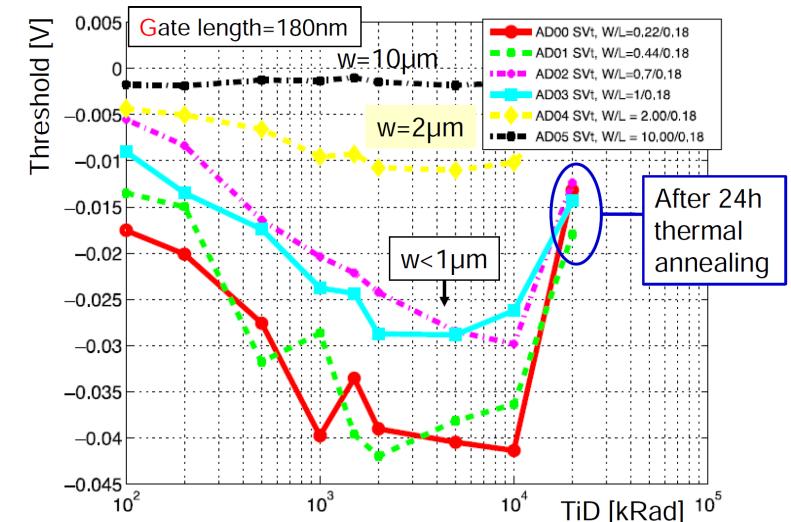
- Final sensor dimensions :  $15 \text{ mm} \times 30 \text{ mm}$
- About 0.5 M pixels of  $28 \mu\text{m} \times 28 \mu\text{m}$
- 4 different sensing node geometries
- Possibility of reverse biasing the substrate  
    ↳ default : - 3 V
- Possibility to mask pixels (fake rate mitigation)  
    ↳ default :  $\lesssim O(10^{-3})$  masked pixels



# Tolerance to Ionising Radiation

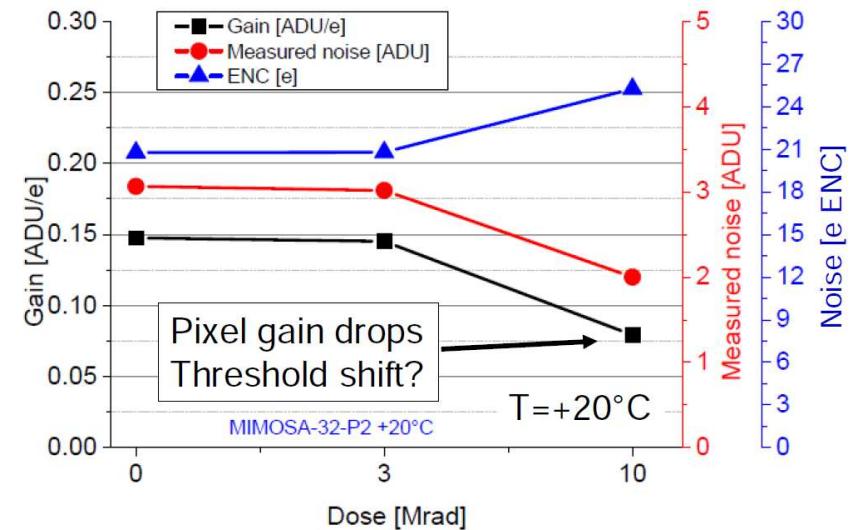
- Studies of  $0.18 \mu\text{m}$  transistors exposed to  $\text{TID} \geq 10 \text{ Mrad}$

- measurements performed ( $+20^\circ\text{C}$ ) :
  - leakage current & threshold shift
- increase of leakage current remains small
- threshold shifts remain small if  $W \gtrsim 2 \mu\text{m}$  and are recoverable with thermal annealing



- Studies of sensing node in  $0.18 \mu\text{m}$  process at  $+20^\circ\text{C}$  :

- Pixel gain drops  $> 5 \text{ Mrad}$  (threshold shift ?)
  - but SNR seems acceptable up to 10 Mrad
- Well known remedies seem efficient up to  $\gtrsim 10 \text{ Mrad}$  :
  - short integration time, low temperature, ELT with guard rings
- Potential conflict : space available in high resolution pixels



# Tolerance to Non-Ionising Radiation

- Main parametres governing the tolerance to NI radiation :

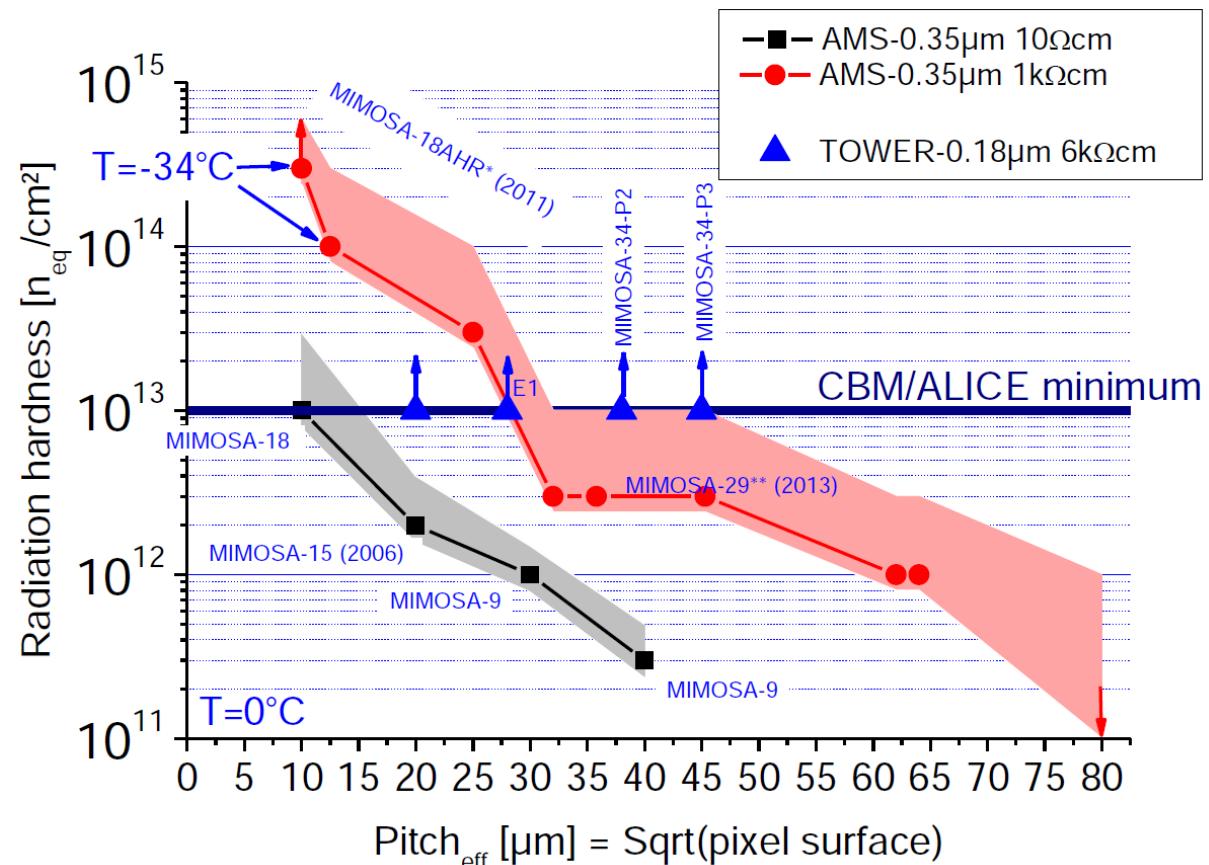
- epitaxial layer : thickness and resistivity
- sensing node : density, geometry, capacitance, depletion voltage
- operating temperature
- read-out integration time

- Most measurements performed with chips manufactured in two CMOS processes :

- $0.35 \mu\text{m}$  with low & high resistivity epitaxy
- $0.18 \mu\text{m}$  with high & resistivity epitaxy  
(mainly  $18 \text{ & } 20 \mu\text{m}$  thick)

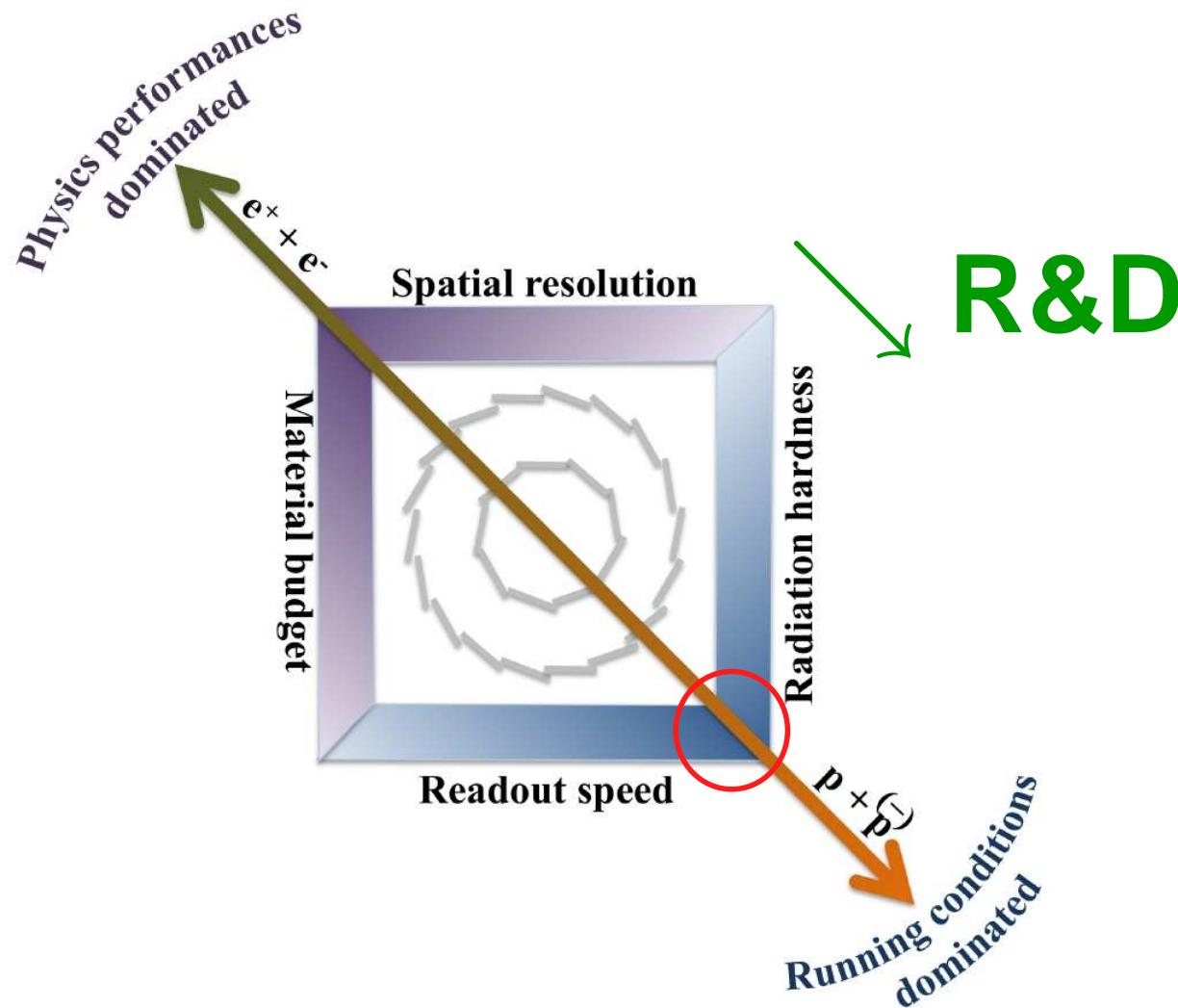
- Clear improvement with  $0.18 \mu\text{m}$  process w.r.t.  $0.35 \mu\text{m}$  process

- ALICE-ITS requirement seems fulfilled :  $2.7 \text{ MRad} \text{ & } 1.7 \cdot 10^{13} n_{eq}/\text{cm}^2$  at  $T = +30^\circ\text{C}$
  - Fluences in excess of  $10^{14} n_{eq}/\text{cm}^2$  seem within reach
- ⇒ requires global optimisation of design & running parametres



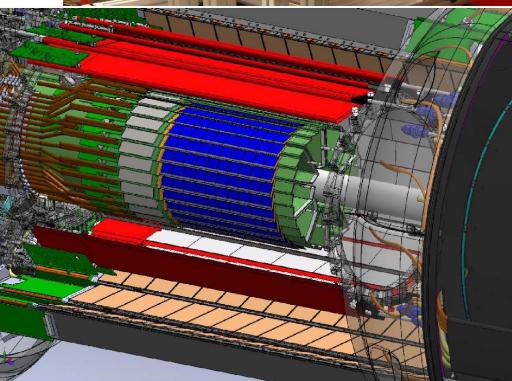
# Forthcoming Challenges

*How to reach the bottom right corner of the "Quadrature" ?*



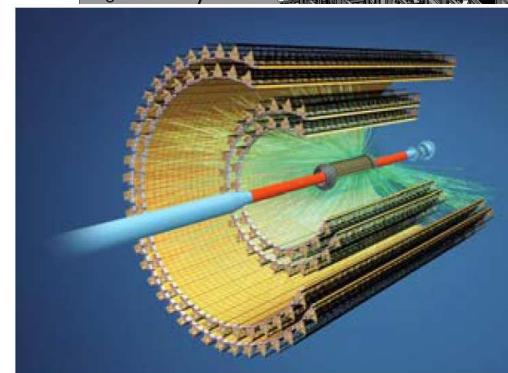
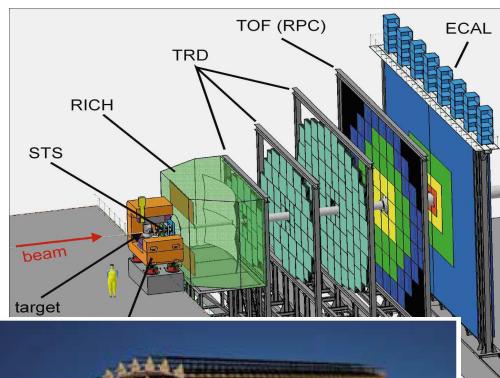
# Improving Speed and Radiation Tolerance

$O(10^2)$   $\mu s$

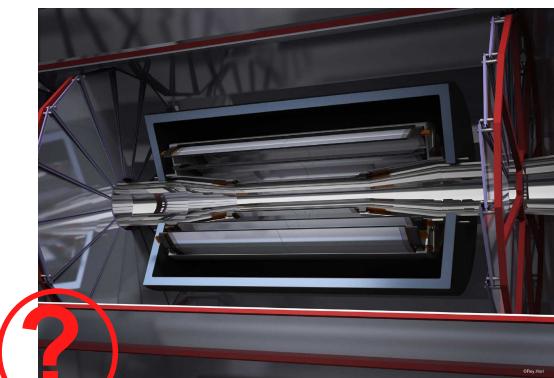


*How to improve speed & radiation tolerance  
while preserving 3-5  $\mu m$  precision &  $< 0.1\% X_0$  ?*

$O(10)$   $\mu s$



$O(1)$   $\mu s$



**EUDET/STAR**

2010/14



**ALICE/CBM**

2015/2019



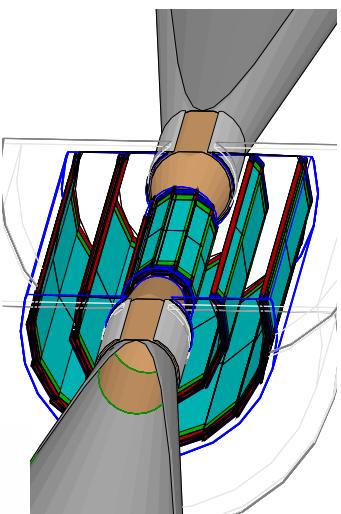
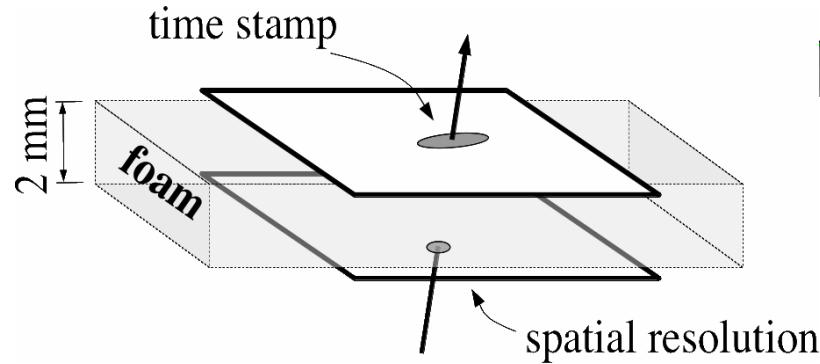
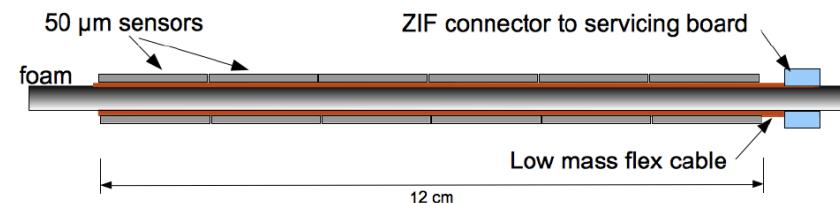
**?X?/ILC**

$\gtrsim 2020$

# Extrapolation to (ILC) Vertex Detectors

- VERTEX DETECTOR CONCEPT :

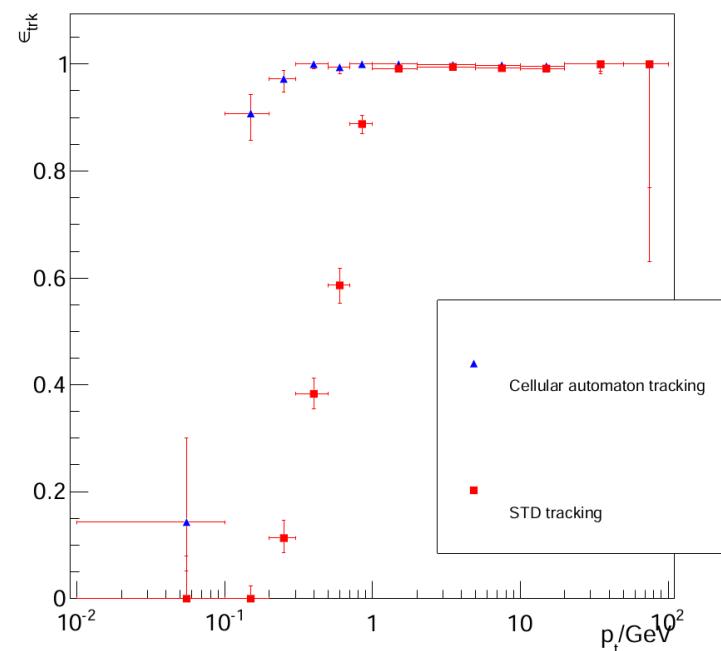
- \* Cylindrical geometry based on 3 concentric 2-sided layers
- \* Layers equipped with 3-4 different CMOS Pixel Sensors (CPS)



- CPS FOR DOUBLE-SIDED VXD LADDERS ACHIEVABLE

WITH PRESENT KNOWLEDGE :

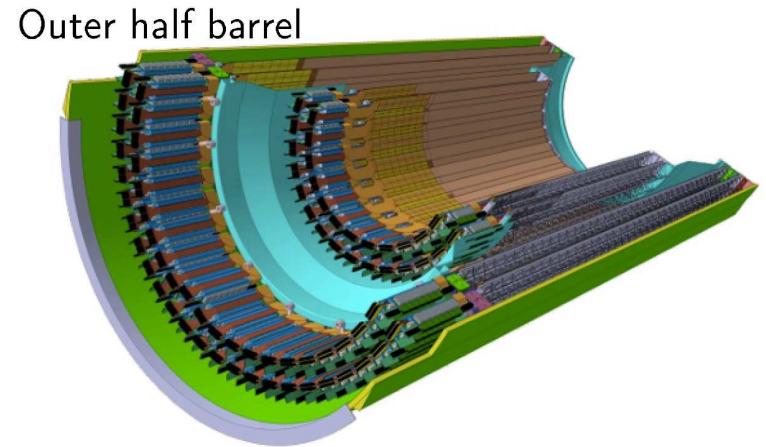
- \* L0 pixels:  $17 \times 17 \mu\text{m}^2 \Rightarrow < 3 \mu\text{m}$  &  $64\text{--}32 \mu\text{s}$
- \* L1 pixels:  $17 \times 102 \mu\text{m}^2 \Rightarrow \lesssim 5 \mu\text{m}$  &  $5\text{--}2/1 \mu\text{s}$
- \* L3–L6 pixels:  $25 \times 51 \mu\text{m}^2 \Rightarrow \sim 3.5 \mu\text{m}$  &  $40 \mu\text{s}$   
combined with  $27 \times 29 \mu\text{m}^2 \Rightarrow \lesssim 5 \mu\text{m}$  &  $4 \mu\text{s}$



# Extrapolation to ILC Trackers

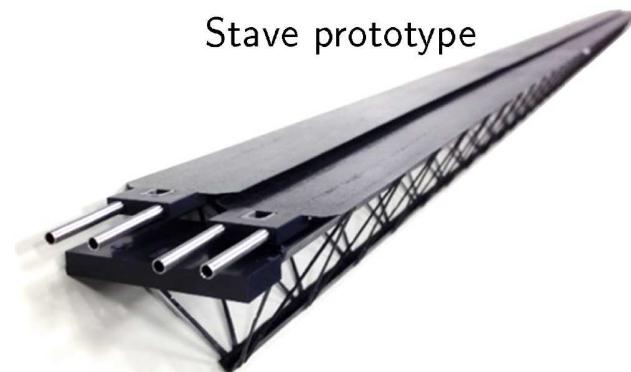
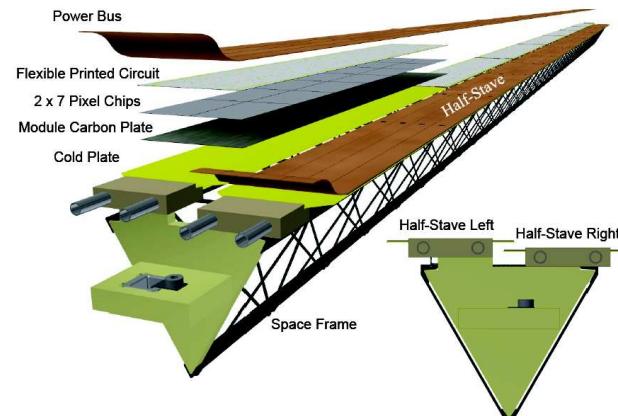
- ALICE-ITS CONCEPT :

- \* Cylindrical geometry based on 7 concentric single-sided layers
- \* Outer Barrel (4 layers;  $10 \text{ m}^2$ ) serves as a tracker
- \* All layers equipped with CMOS Pixel Sensors (CPS)
- \* Baseline sensor (ALPIDE) :  $5 \mu\text{m}$  &  $4 \mu\text{s}$   
(not yet validated on detector ladder)
- \* Outer Barrel material budget  $\lesssim 1\% X_0/\text{layer}$
- \* Stave length up to  $\sim 1.5 \text{ m}$

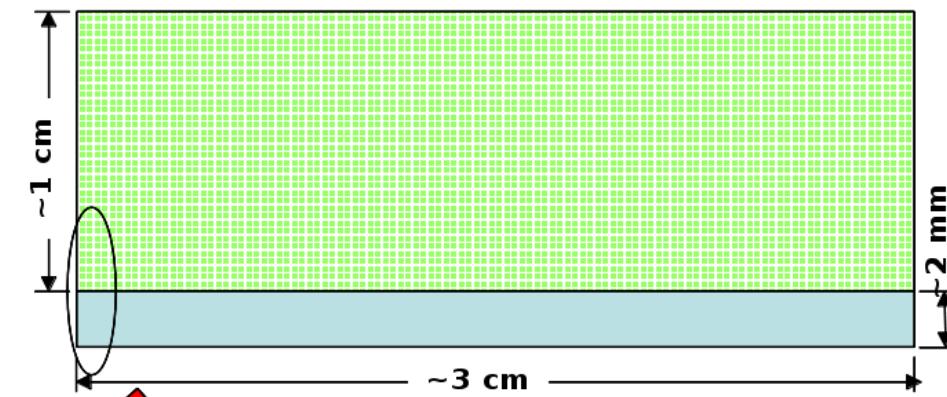


- CPS FOR DOUBLE-SIDED TRACKER LAYERS ACHIEVABLE WITH PRESENT KNOWLEDGE :

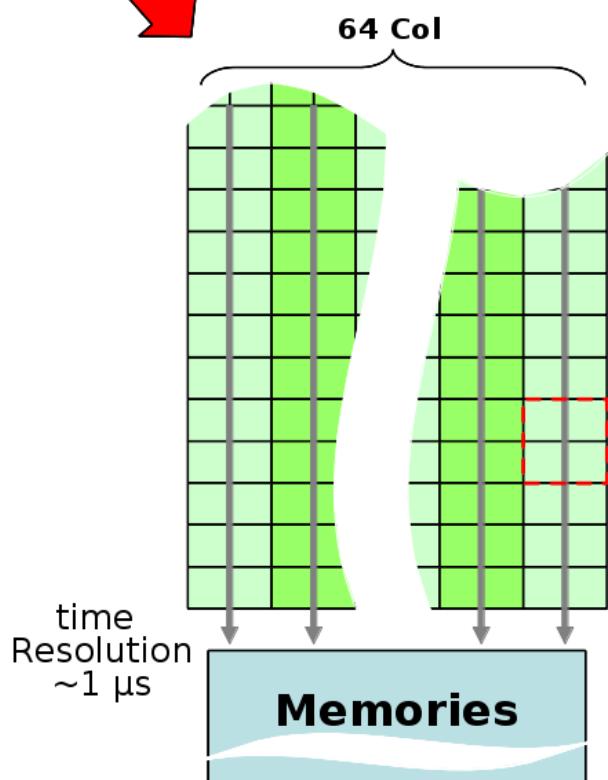
- \* transposing the ITS concept to an ILC exp.  
allows for  $5 \mu\text{m}$  resolution  
and  $4 \mu\text{s}$  read-out time
- \* alternative : use ITS sensor ( $5 \mu\text{m}$  &  $4 \mu\text{s}$ )  
on one ladder side and a faster  
(time stamping) version based on  
elongated pixels on the other side :  
 $\sim 1 \mu\text{s}$  seems achievable (tbc)



# Noria Based CPS Architecture for (ILC) Single Bunch Identification



- Pixel dimensions  $\sim 20 \times 20 \mu\text{m}^2$ 
  - ↳  $\sigma_{\text{sp}} \sim 3 \mu\text{m}$
- In-pixel amplification-shaping
  - ↳ integration time  $< 1 \mu\text{s}$
- In-pixel digitisation
- Organised in N sub-matrices of  $64 \times 512$  pixels



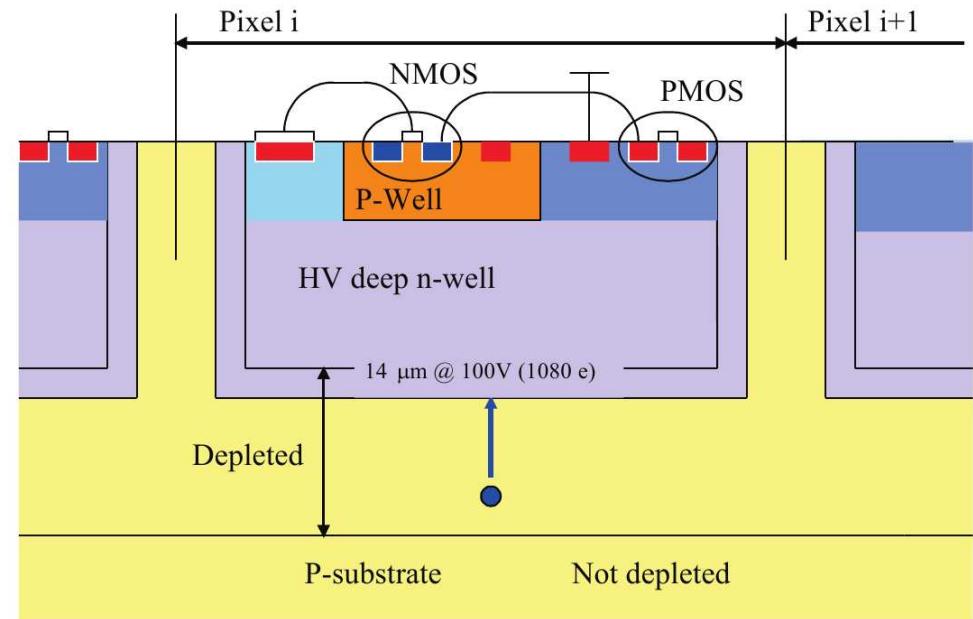
- Data-driven pixel readout in every pair of columns
  - ↳ Asynchronous readout
- Time stamp at the bottom of pixel array within  $\mu\text{s}$
- Hit pixel clusters of each column pair are stored into memories (possibly after cluster selection)
  - ↳ Cluster format  $2 \times 2$  pixels
  - ↳ Column address
  - ↳ Row address
  - ↳ Time stamp (structure)
- Data readout in a few ms after end of train

**Still only a concept, not yet a design**

# Further Perspectives of Performance Improvement

- **Expected added value of HV-CMOS :**

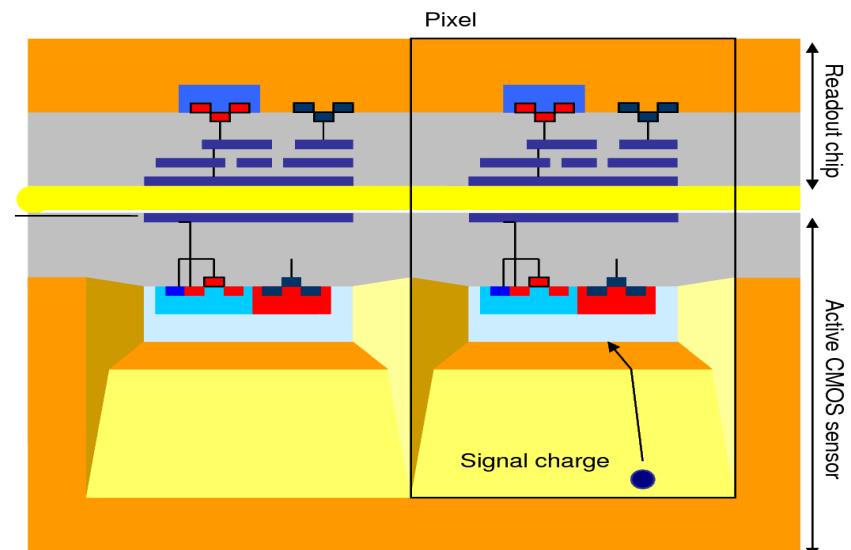
- Benefits from extended sensitive volume depletion :
    - faster charge collection
    - higher radiation tolerance
  - Not bound to CMOS processes using epitaxial wafers  
⇒ easier access to VDSM (< 100 nm) processes  
⇒ higher in-pixel micro-circuit density



- **Questions :**
  - minimal pixel dimensions vs  $\sigma_{sp} \lesssim 3 \mu\text{m}$  ?
  - uniformity of large pixel array, yield ?

- **Attractive possible evolution : 2-tier chips**

- signal sensing & processing functionnalities distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous :
    - 1 optimal for sensing, 1 optimal for signal processing
  - benefit : small pixel → resolution, fast response,  
data compression, robustness ?
  - challenge : interconnection technology (reliability, cost, ...)



# CONCLUSION

- CPS have demonstrated that they can provide the spatial resolution and material budget required for numerous applications
- CPS are suited for vertex detectors ( $\ll 1 \text{ m}^2$ )
  - attractive features for tracking devices ( $\gg 1 \text{ m}^2$ ), incl. cost (!)
- Forthcoming & Upcoming challenges :
  - Large active area : ALICE-ITS  $\equiv 10 \text{ m}^2$  to cover with 20-30,000 sensors
  - Radiation tolerance :  $\gtrsim 10 \text{ MRad}$  &  $\gtrsim 10^{14} \text{ n}_{eq}/\text{cm}^2$  (e.g. CBM expt at FAIR/GSI)
  - Read-out speed :  $\lesssim 1 \mu\text{s}$  (e.g. ILC vertex detector & tracker)
- Perspectives :
  - HV-CPS but exposed to challenges if small pixels and very low power consumption are required
    - VDSM processes ?
  - 2-tier sensors  $\equiv$  (sensing + ampli)  $\oplus$  (sparsification + data transfer)
    - combining 2 CMOS processes at pixel level
      - still an R&D ...