OMEGA ROC ASICs for SiPMs

Salleh AHMAD, Sylvie BLIN, Stéphane CALLIER, Frederic DULUCQ, Julien FLEURY, Christophe de LA TAILLE,Gisèle MARTIN-CHASSARD, Ludovic RAUX Nathalie SEGUIN-MOREAU, Damien THIENPONT, Jeanne TONGBONG

OMEGA microelectronics group
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr
& WEEROC SAS
http://weeroc.com

Organization for Micro-Electronics desiGn and Applications

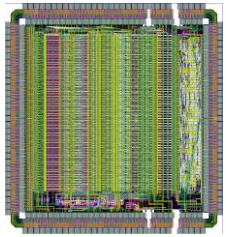
OMEGA ROC chips

- Use of Silicon Germanium 0.35 µm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for calorimetry
- Very high level of integration : System on Chip (SoC)

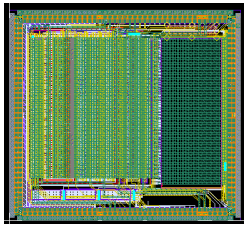
Chip	detector	ch	DR (C)
MAROC	PMT	64	-2f-50p
SPIROC	SiPM	36	+10f-200p
SKIROC	Si	64	+0.3f-10p
HARDROC	RPC	64	-2f-10p
PARISROC	PM	16	-5f-50p
SPACIROC	PMT	64	-5f-15p
MICROROC	µMegas	64	-0.2f-0.5p
PETIROC	SiPM	32	50fC-300pC

http://omega.in2p3.fr

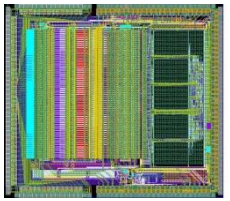
MAROC3



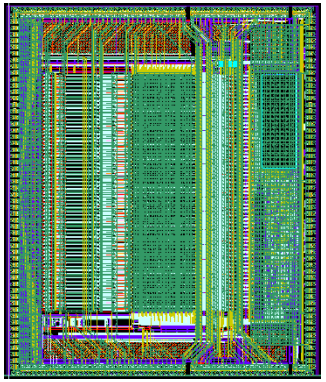
HARDROC2



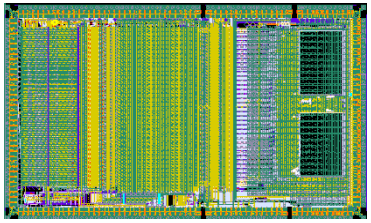
MICROROC1



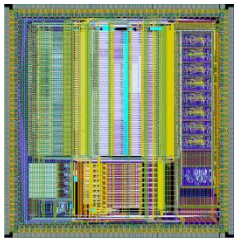
SKIROC2



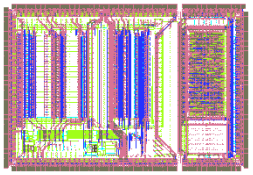
SPIROC2



SPACIROC

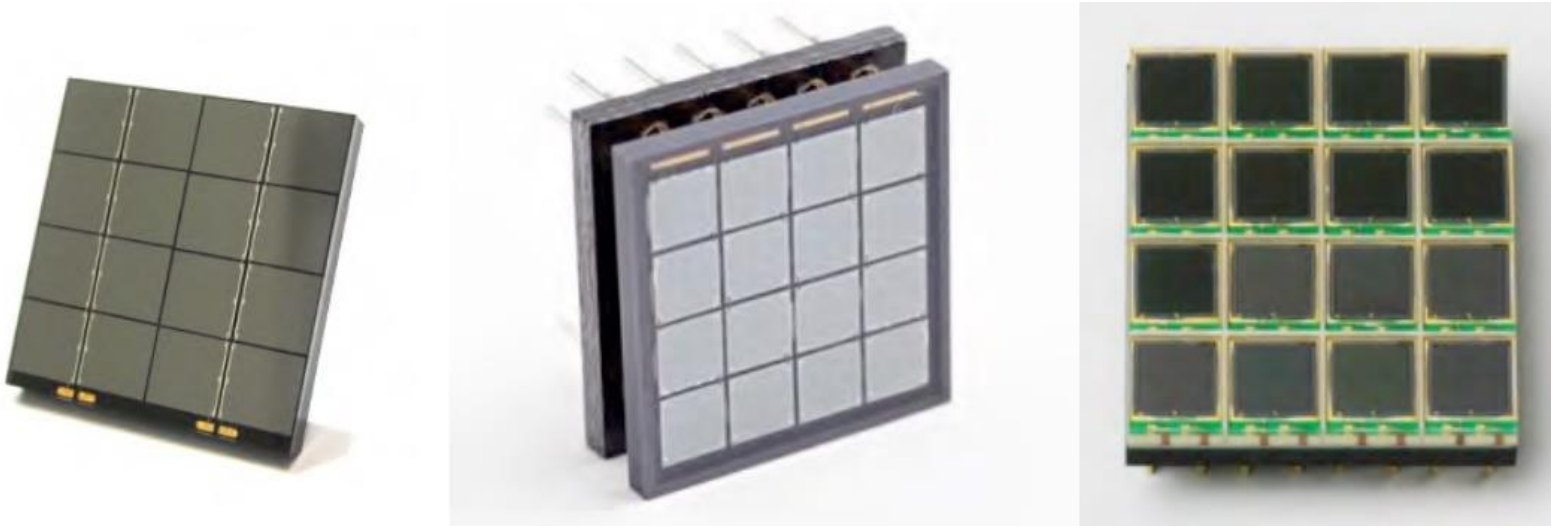


PARISROC2



Silicon-Photomultipliers Readout

- SPIROC
- EASIROC/CITIROC
- PETIROC
- TRIROC



CdLT SiPM ROC chips

SiPM from SPIROC to TRIROC

- FLC_SiPM designed and produced to equip the Analog H-Cal physics prototype for the ILC in 2005 (1 cubic meter, 38 layers, 2cm steel plates, 8000 tiles with SiPM)
  - 1st ASIC to readout SiPM
- SPIROC developed in November 2007 to equip the CALICE AHCAL and ECAL EUDET technological prototypes
- Variants of SPIROC: EASIROC designed in September 2009, CITIROC in 2013
  - EASIROC/CITIROC : "light" analog version of SPIROC for SiPM users who don't need the ILC specific digital core

➢ **Several thousands produced**

- Others applications using SPIROC/EASIROC/CITIROC chips for SiPM readout
  - Astrophysics: PEBS experiment (Aachen University), CTA
  - Medical imaging (Roma, Pisa, INMC Orsay, Valencia, etc.)
  - Nuclear physics: E40 experiment (KEK)
  - Volcanology: MuRay muon radiography of geological structures (INFN Napoli)

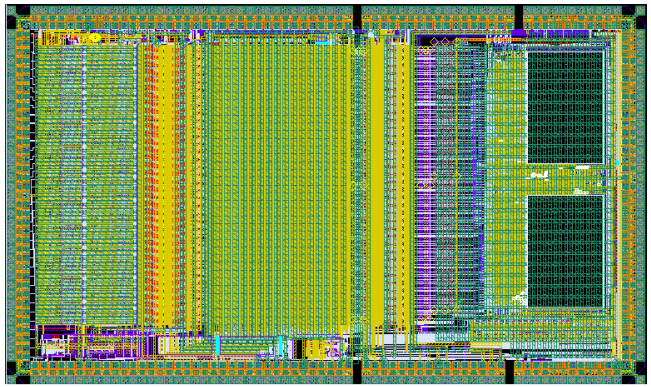
- Dedicated chips for fast timing and high timing resolution applications
  - PETIROC (November 2013)
  - TRIROC (March 2014) "FP7" project

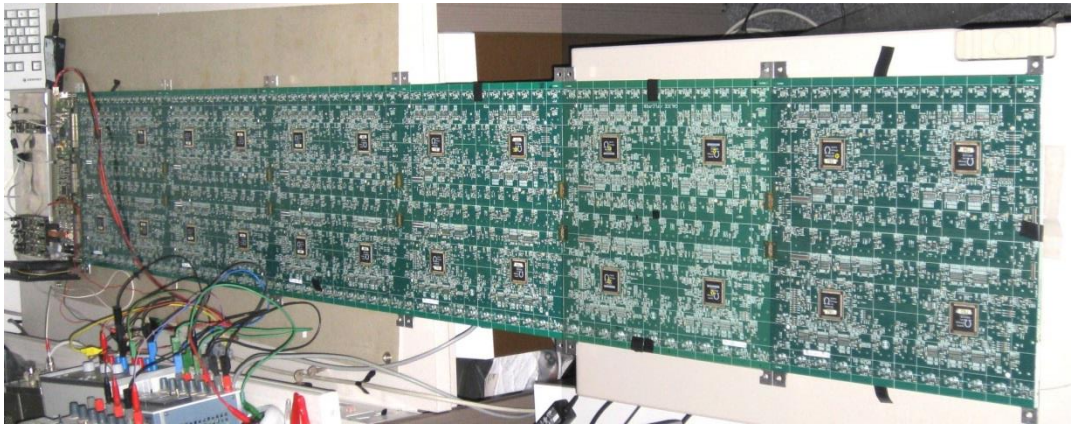
SPIROC for SiPM readout

- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Developed to read out the analog hadronic calorimeter for CALICE (ILC)
  - DESY collaboration (EUDET project)
  - Chip embedded in detector : low power !

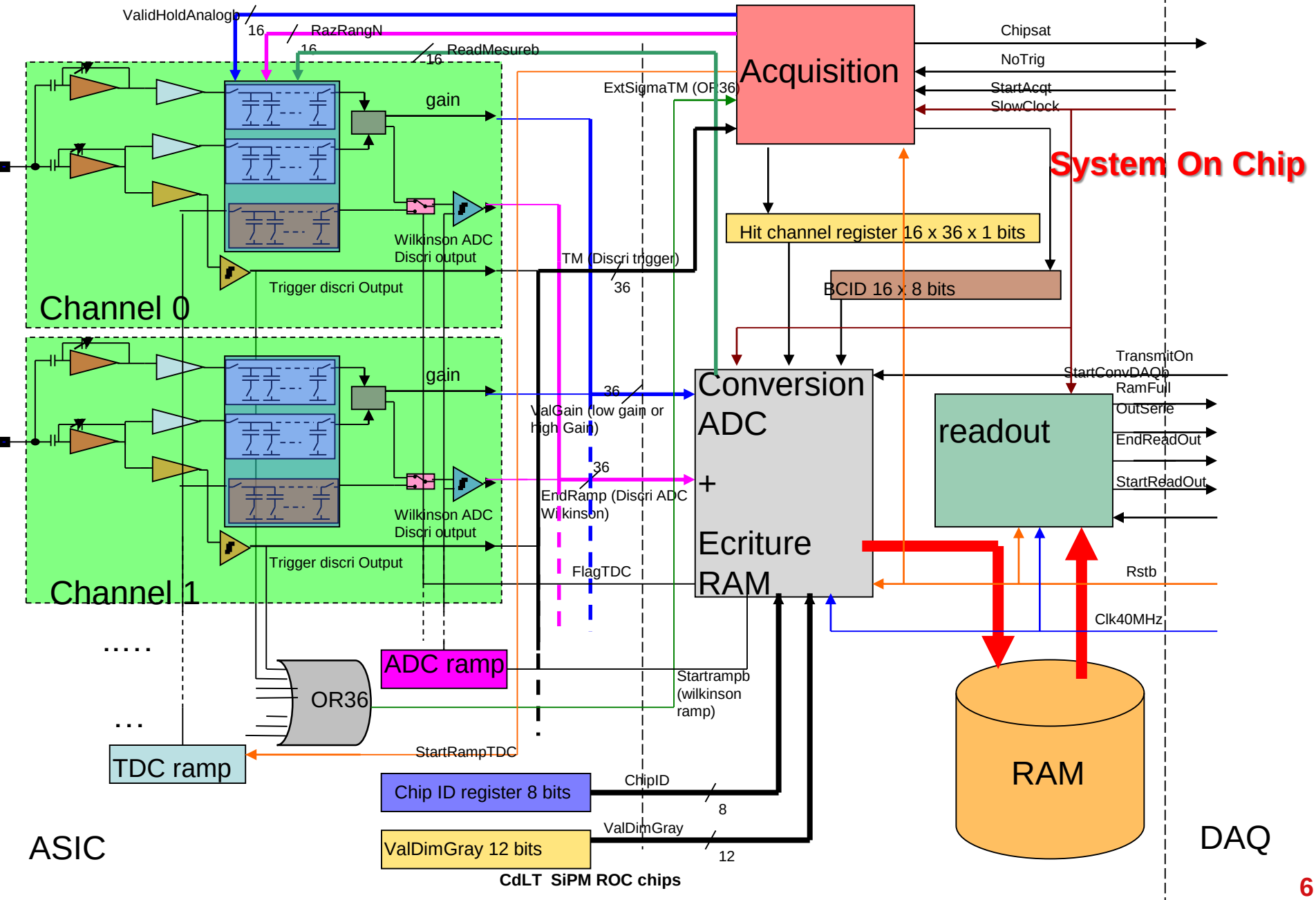
(0.36m)² Tiles + SiPM + SPIROC (144ch)

- 36 channels autotrigger 15bit readout
  - Energy measurement : 15 bits in 2 gains
  - Autotrigger down to ½ p.e.
  - Time measurement to ~1ns
  - Power dissipation : 25µW/ch (power pulsed)

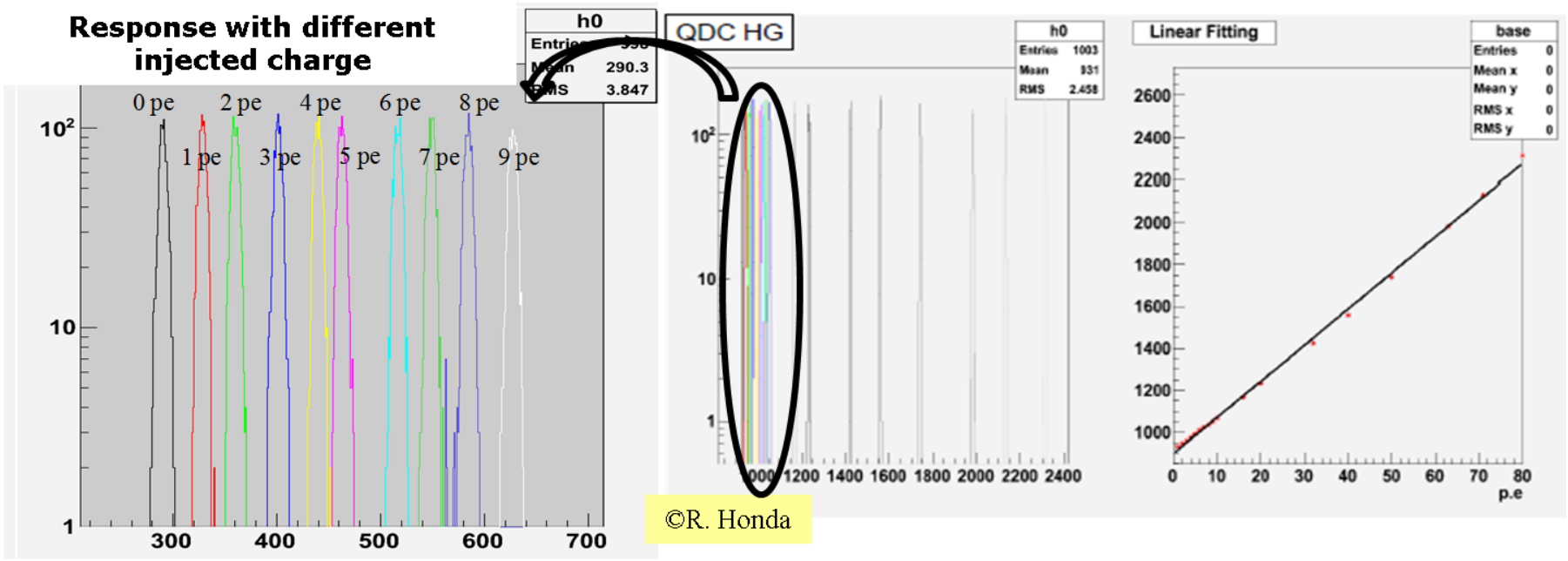




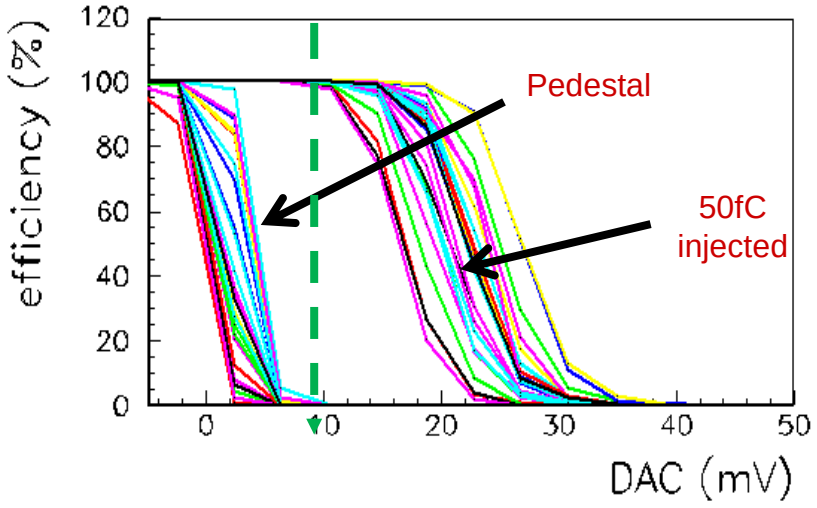
SPIROC : System On Chip

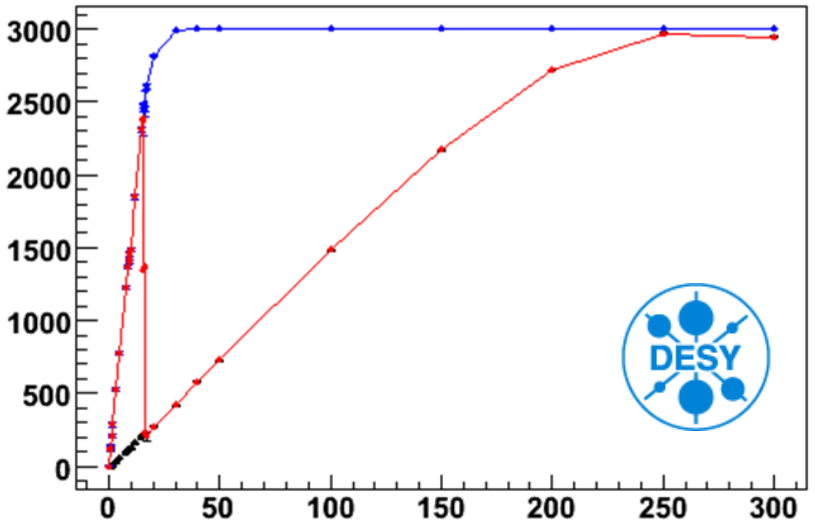


SPIROC performance



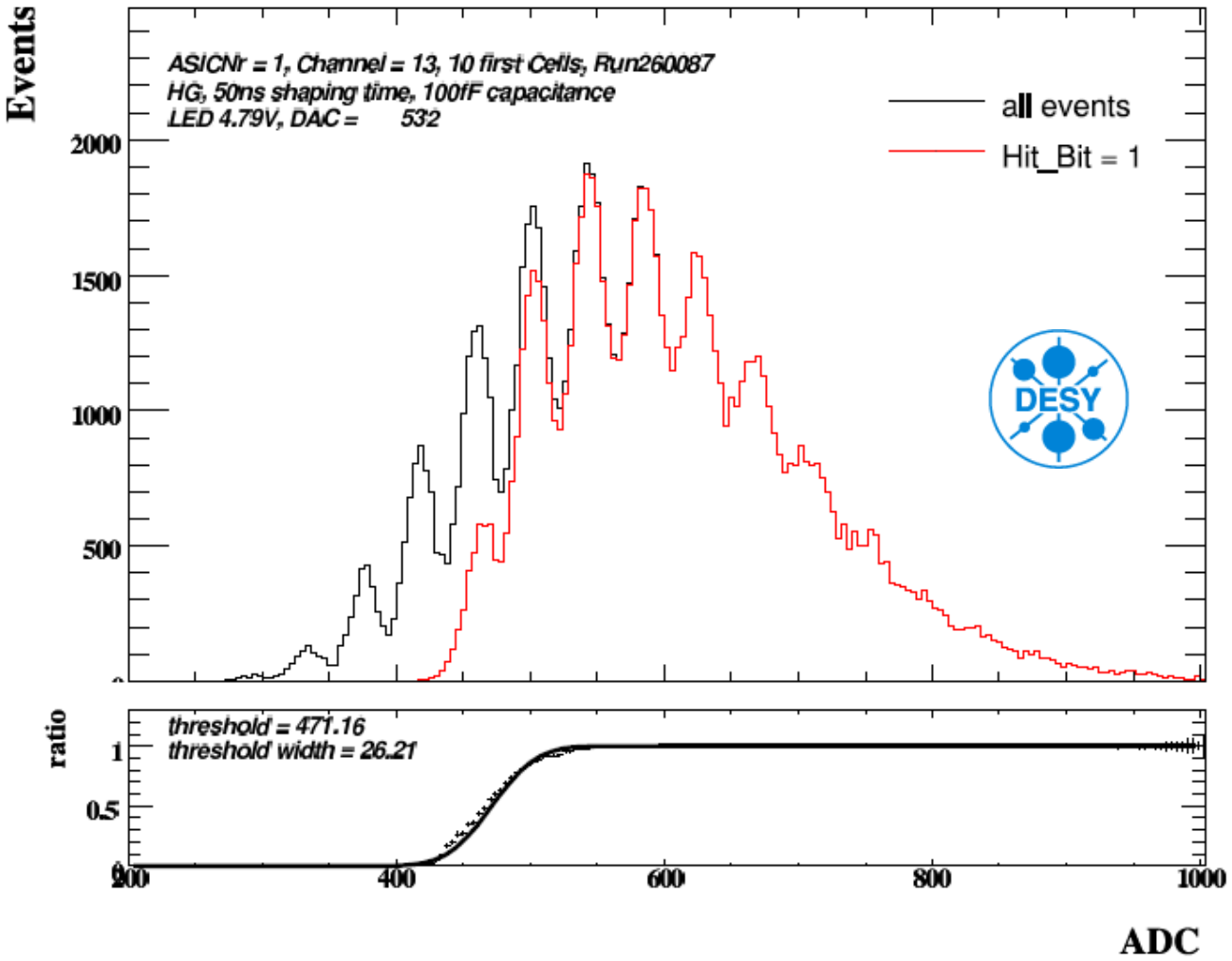
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



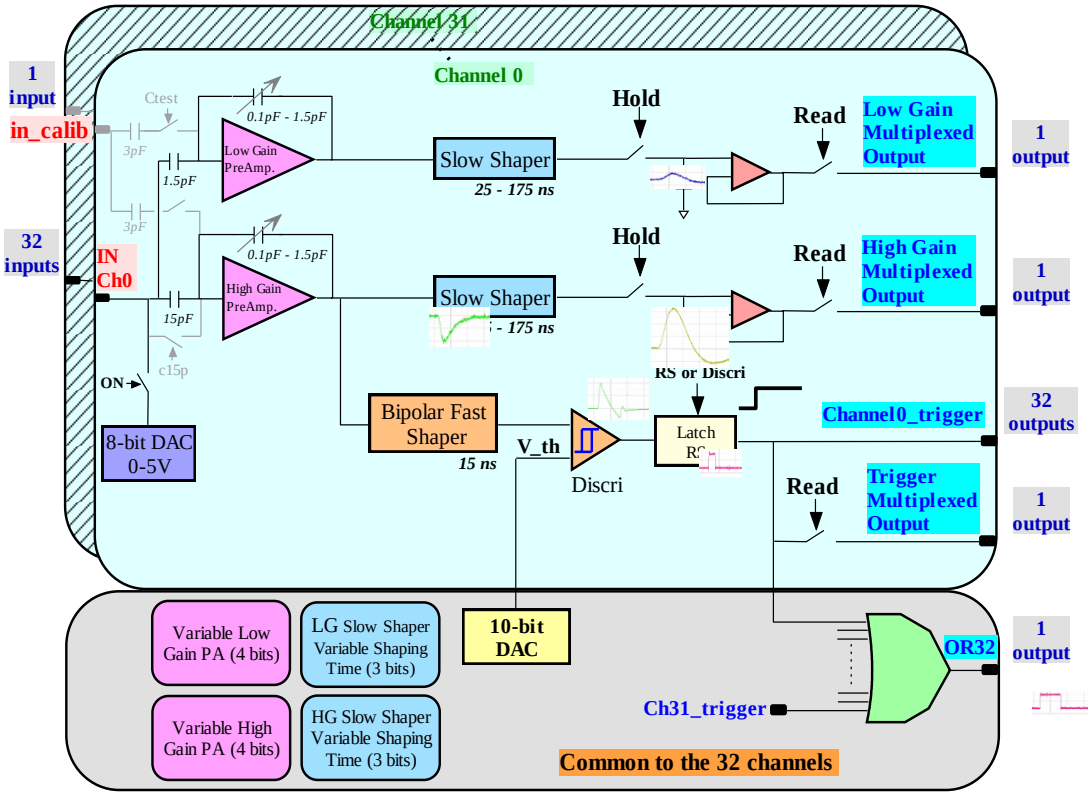


SPIROC2 performance

SiPM SPECTRUM with Autotrigger

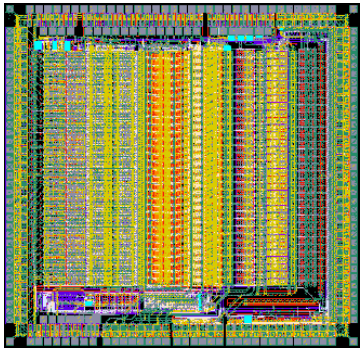


Variant : EASIROC/CITIROC



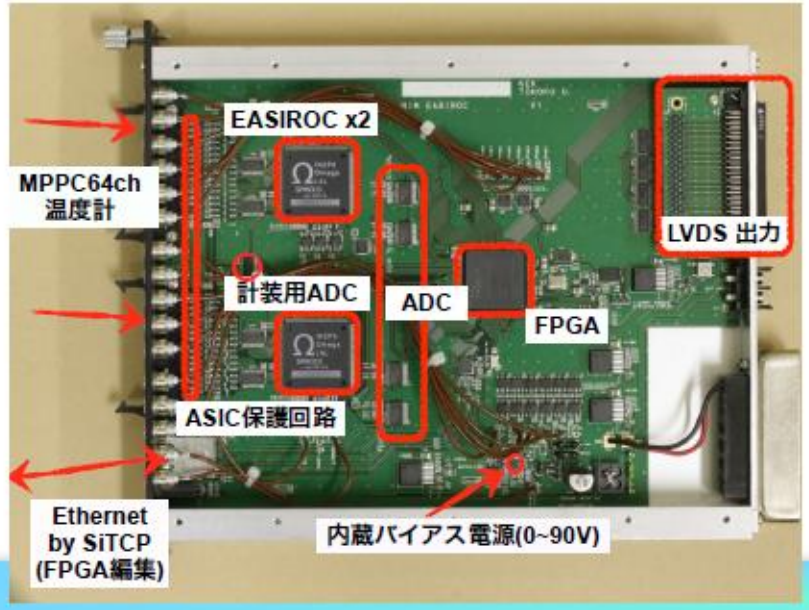
- 32-channel front-end readout (analogue part of SPIROC)
  - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Low power : 4.84 mW/channel, 155 mW/chip

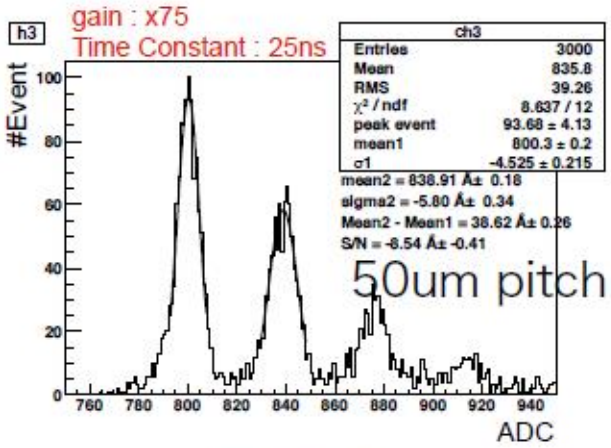
SipMed, IMNC, LAL, OMEGA



Easiroc module

- two EASIROC's + on board ADC
- 32x2 channel
- Vb = V0~-4.5V 8bit
- TCP/IP connection

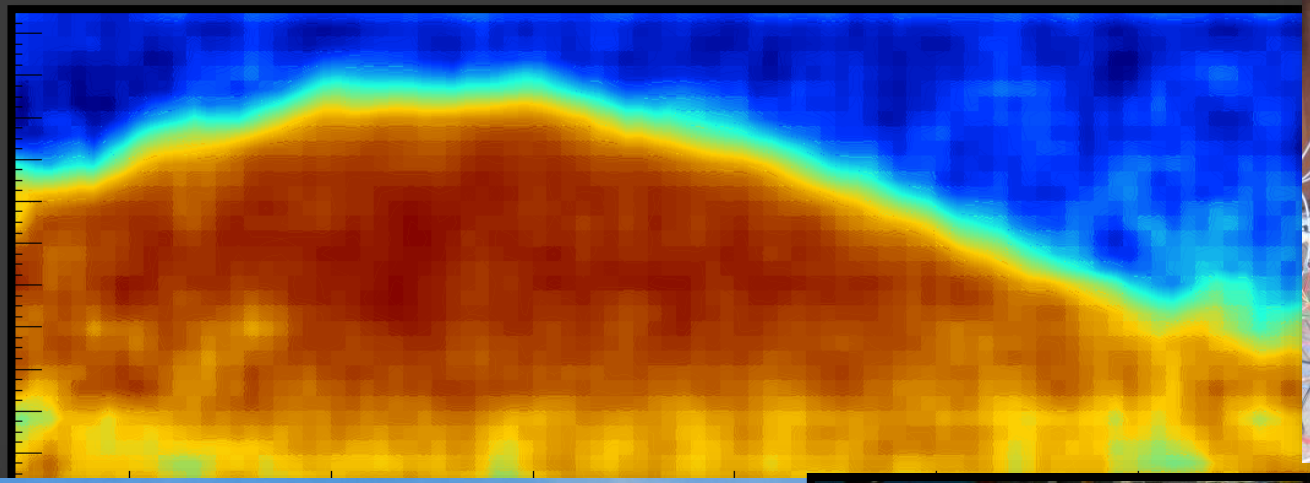


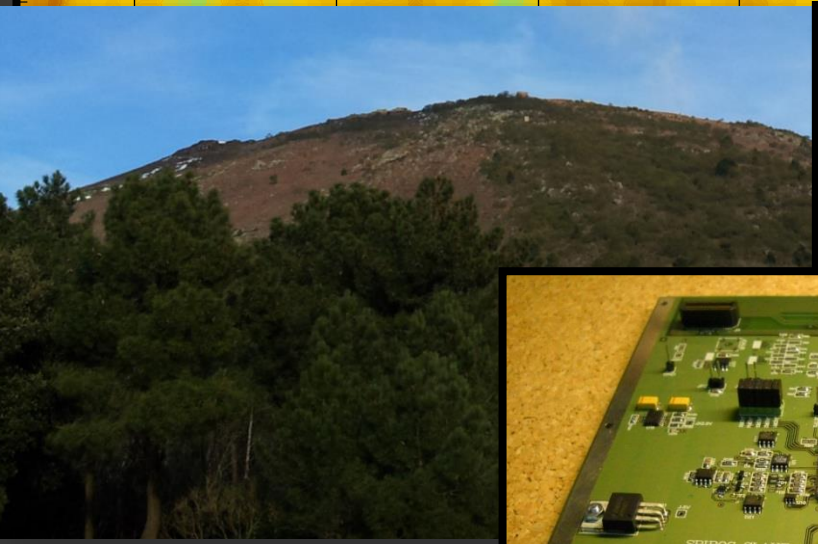


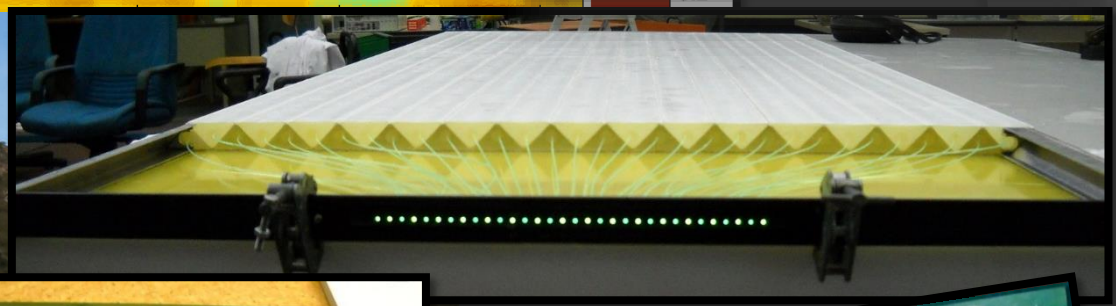
LED

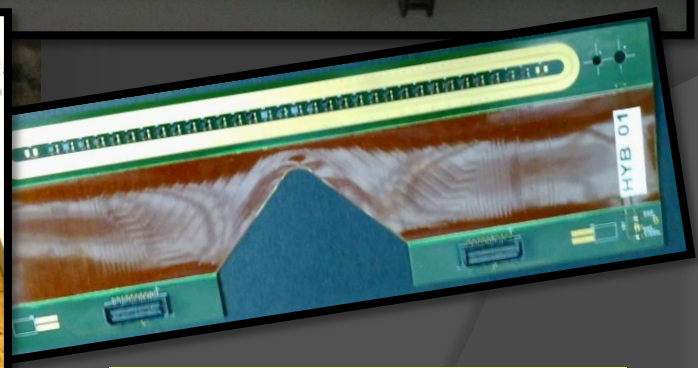
Ishijima

The “Shadow” of the Vesuvius









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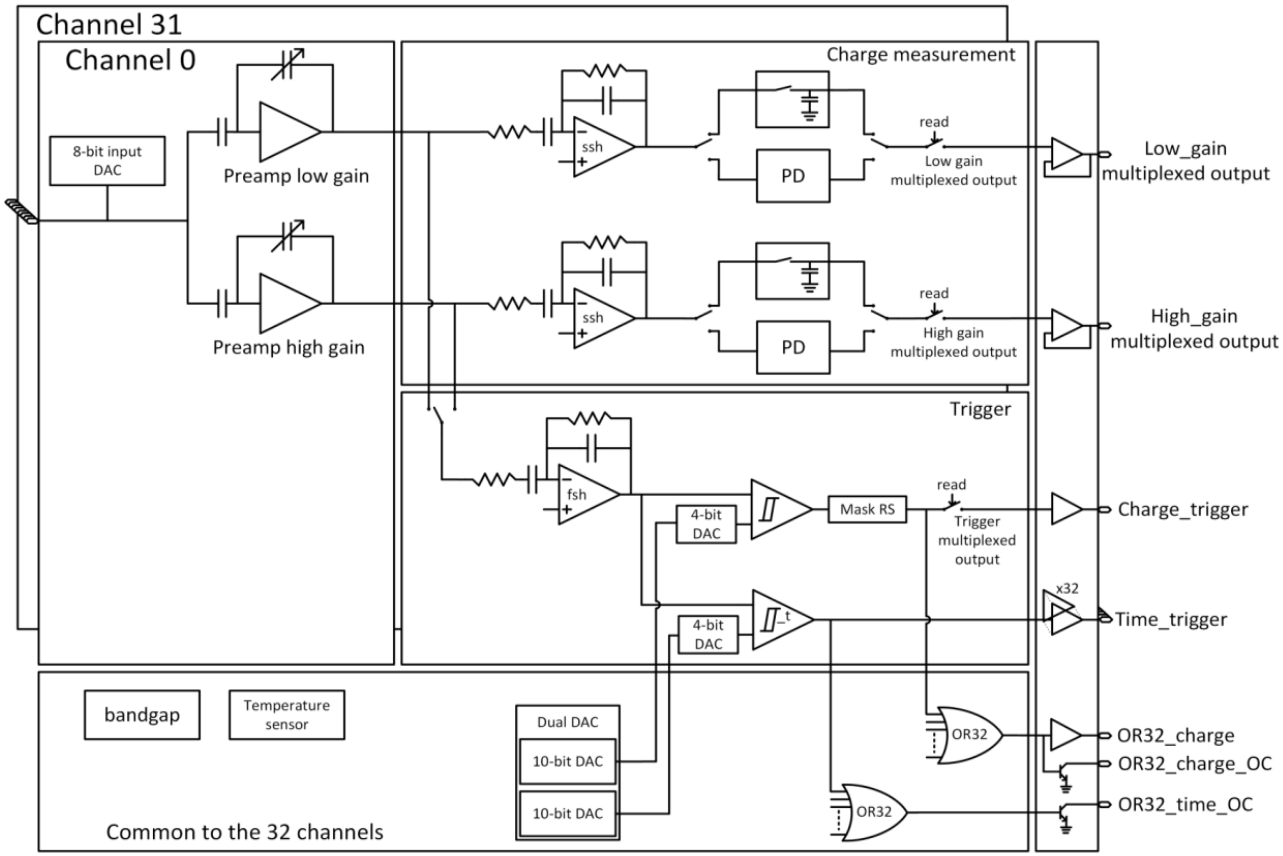
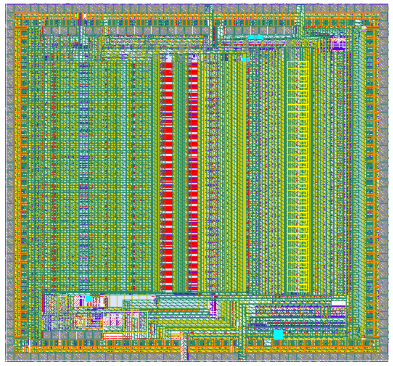
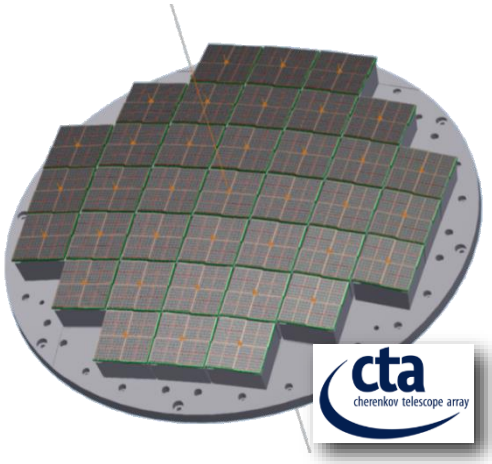
- Evolution of EASIROC 32 ch SiPM readout
  - 32 channels, positive input, 5V input DAC HV adjustment
  - 32 trigger outputs & High Gain / Low gain multiplexed charge output
  - Peak detector and two trigger level (timing & energy)
  - Gain adjustment per channel (6 bits)





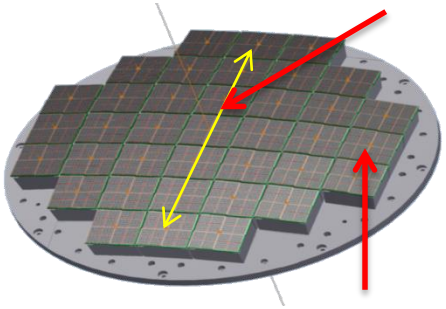


CdLT SiPM ROC chips

PDM Electronics

FOV = 9.6°

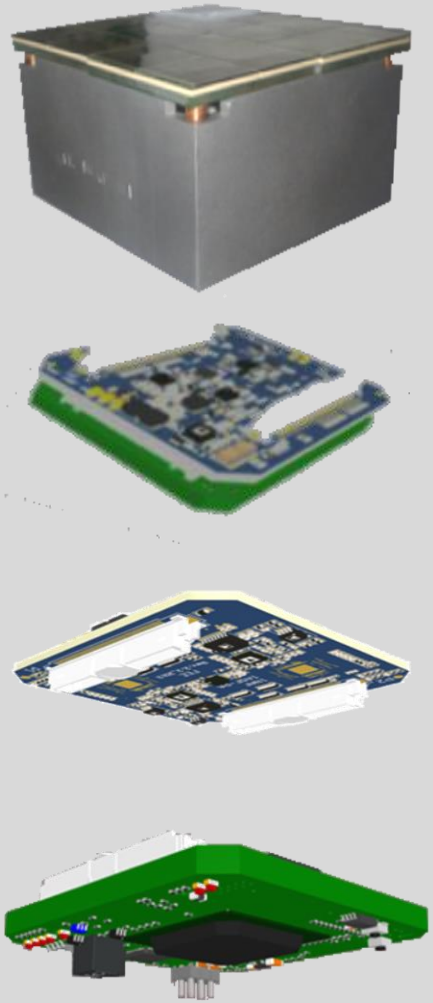
Ø = 350mm

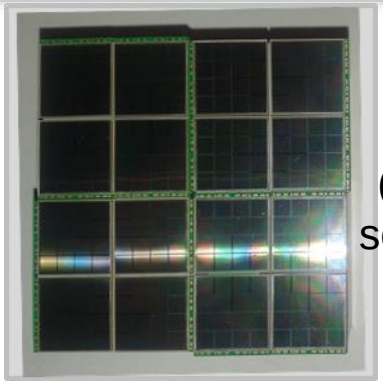


Photon Detection Module (PDM)

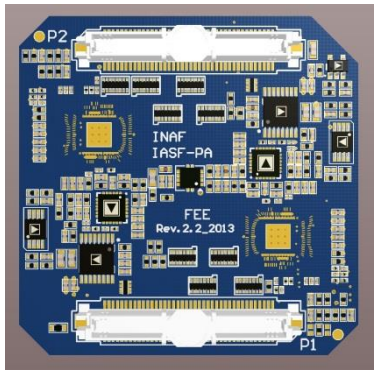
Pixel = 0.17° → 6.2 x 6.2 mm

ASSEMBLING





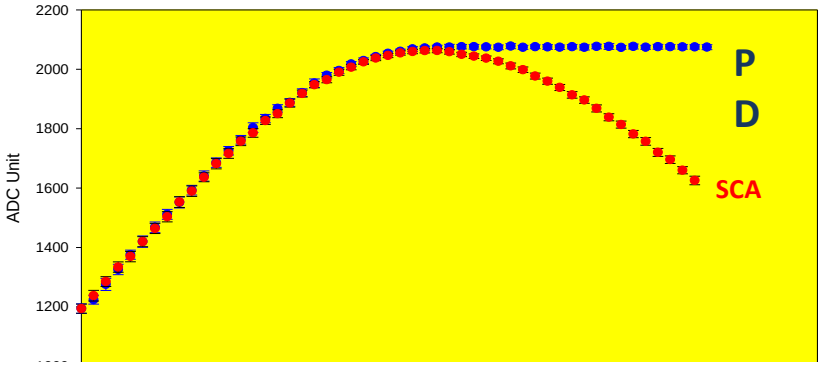
SiPM board
(9 +1 temperature
sensors embedded



Front-End board
(2 CITIROC
ASIC)

PDM FPGA Board
(XILINX ARTIX 7)

CITIROC: Peak detector



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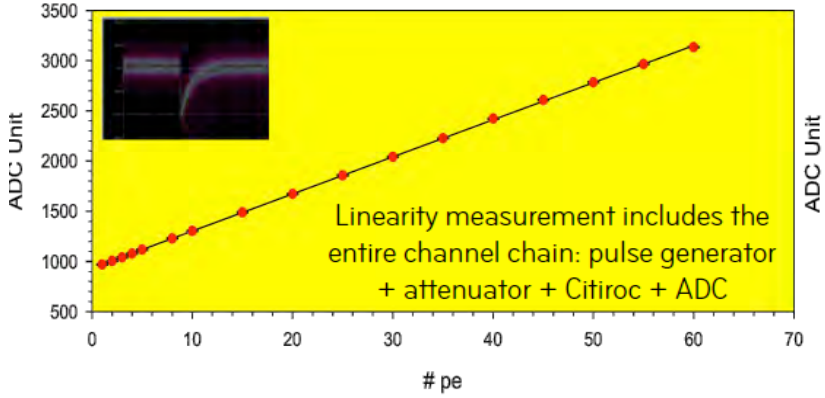
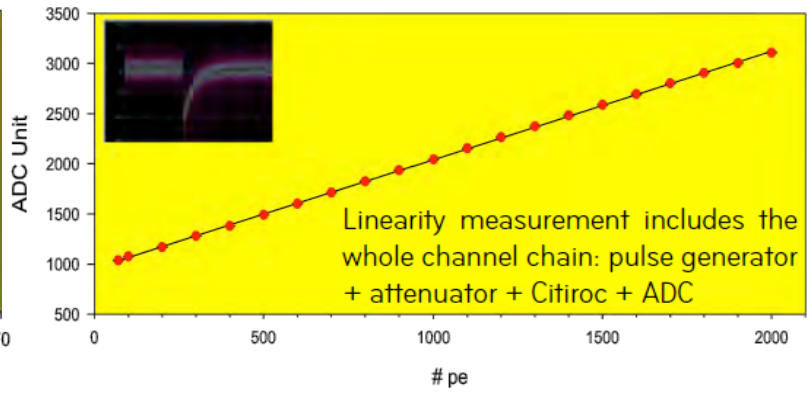
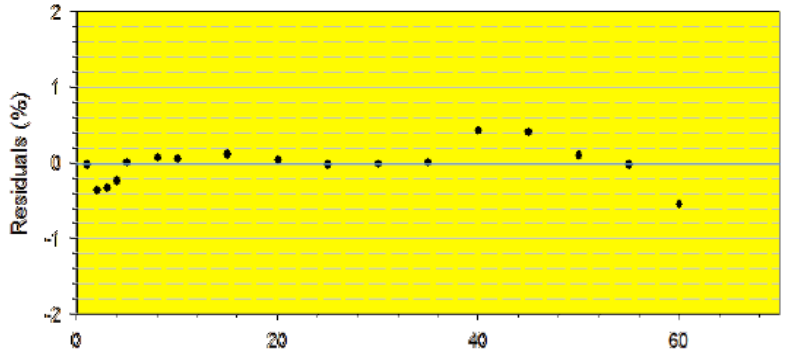
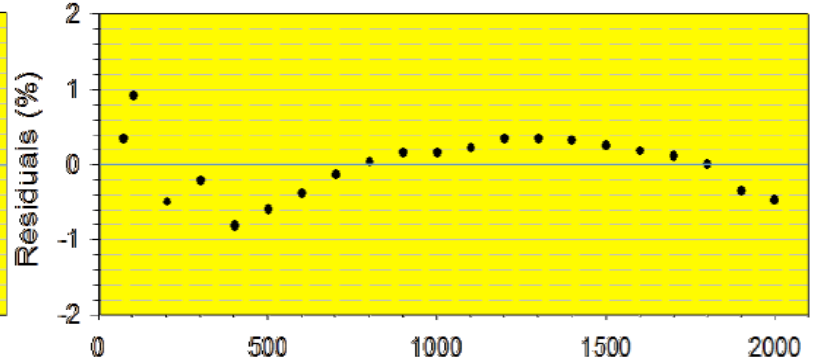


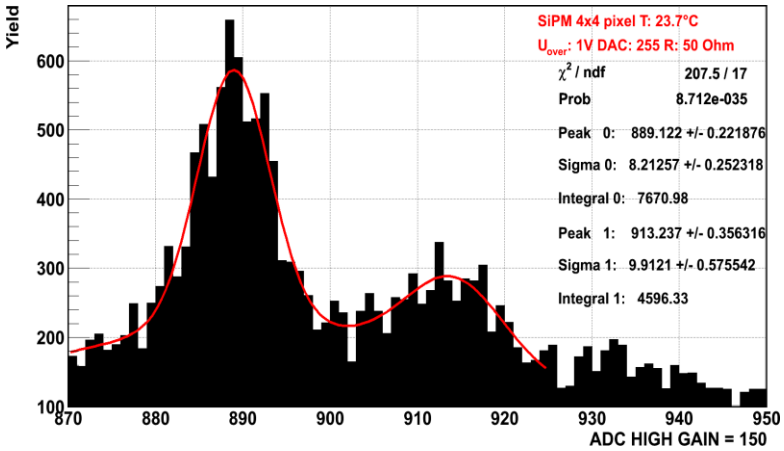


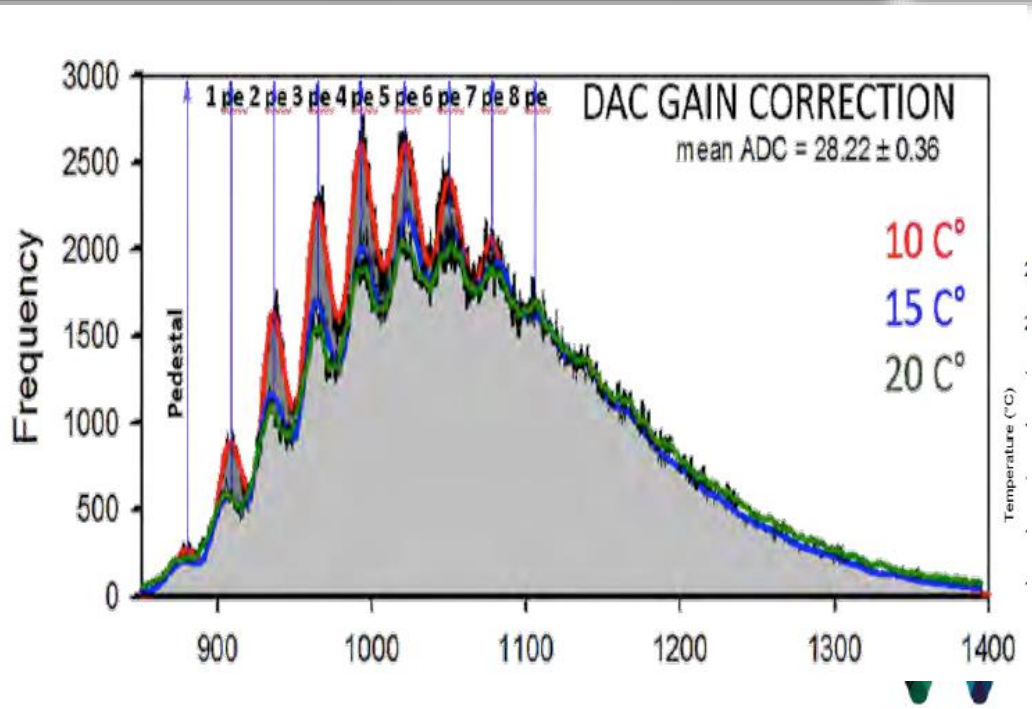




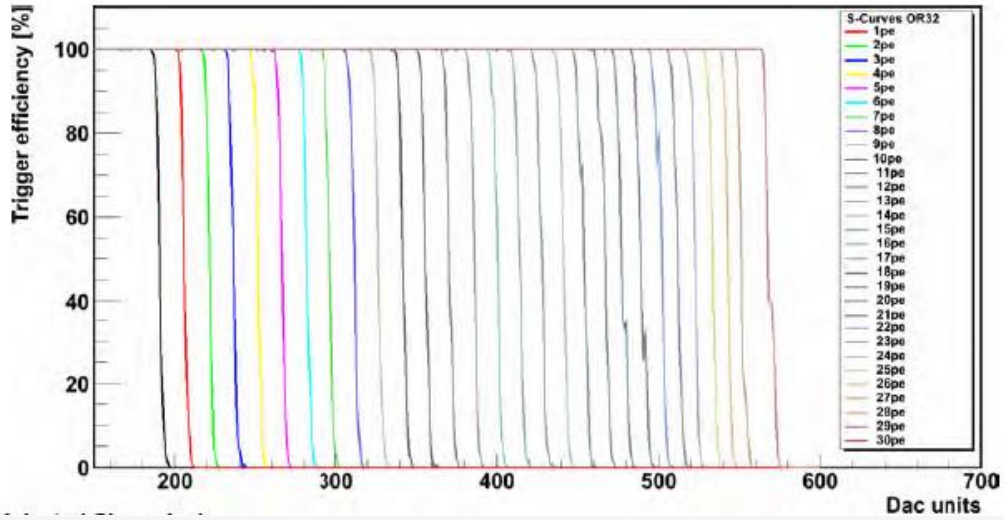
CITIROC: Trigger Linearity

Gain premplifier =4*25fF ≈ 150 nom.
Shaping Time = 50ns
Steps of 1,2,3,4,5,6,7,8,9,10 pe





SiPM 4 pixel High Gain =150
Shaping Time = 50ns
delay time = 38 x 2.5 ns
Temp = 23.7 °C U_{over} = 1V
Resistance = 50 Ohm
Threshold = 922 DAC ~50% of 1 plateau



SiGe GHz Front End

- R&D of 10GHz GBWP preamps for applications where fast timing or high timing resolution is needed (Time Of Flight PET MRI, preclinical, particle physics…)
- 3 architectures in 0.35µm SiGe technology integrated and tested

1 pe-=160fC

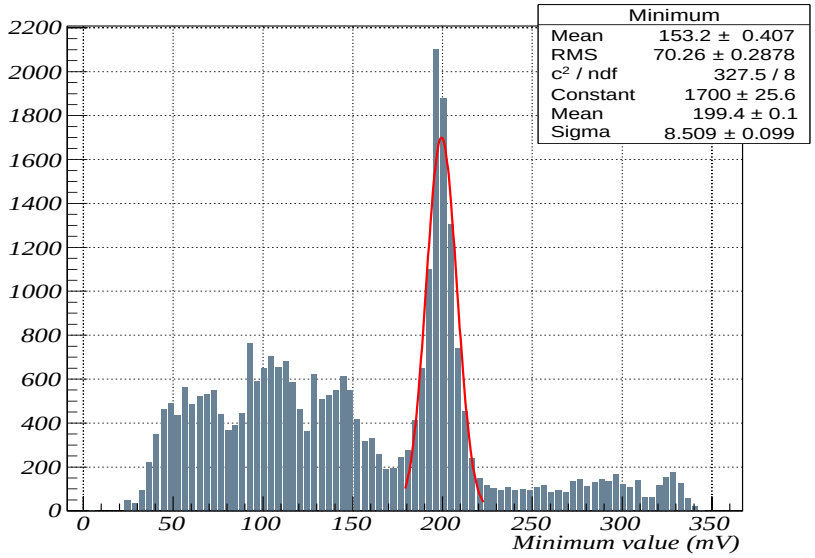
Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/p**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injecti**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

⇒ **Design of PETIROC1: 16 channels with RF amplifier**

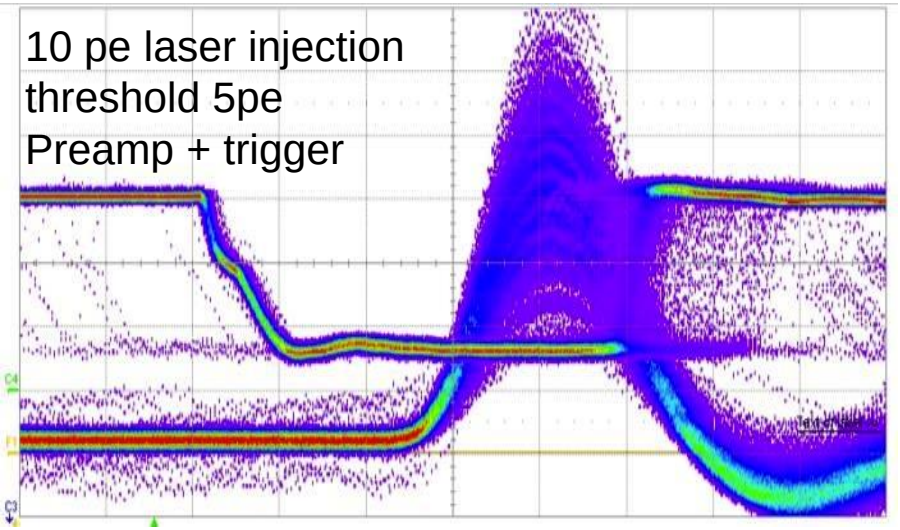
⇒ **PETIROC2 32ch TRIROC 64 ch**

PETIROC1: Triggers on first pe

- Tests on EPTIROC1 (analog version of PETIROC2)
- 1x1mm SiPM Hamamatsu
- Laser for low light injection
  - 405nm, Jitter : 28 ps FWMH
- Petiroc can trigger on first photoelectron
- Petiroc is low noise : single photon identification



2 ns/div



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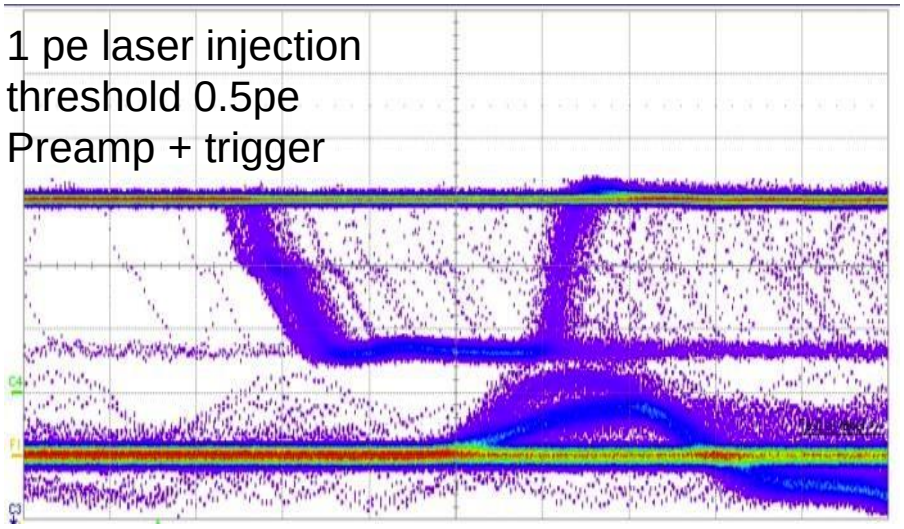
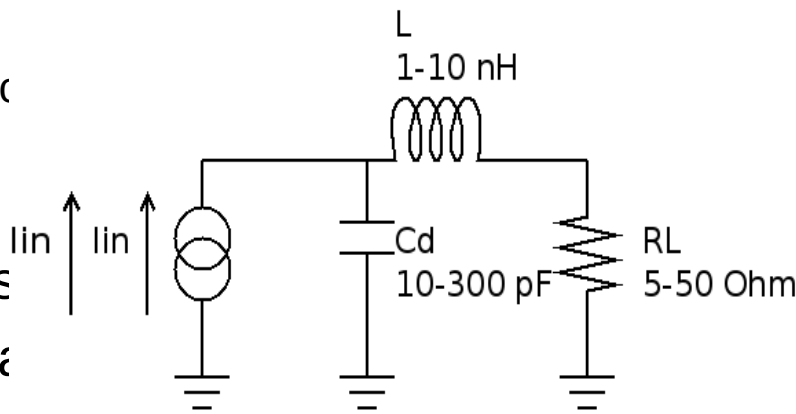
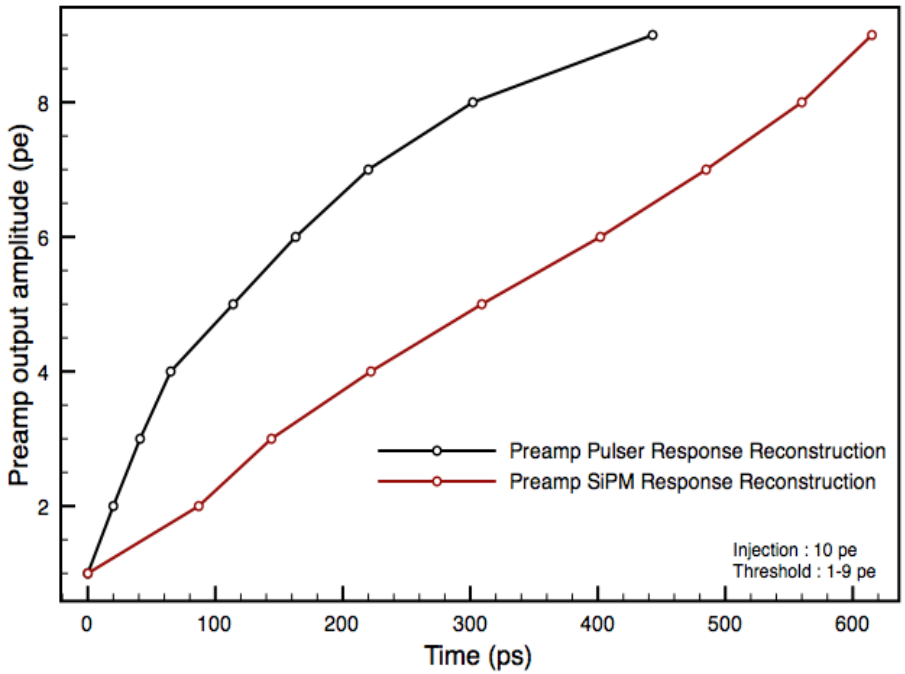


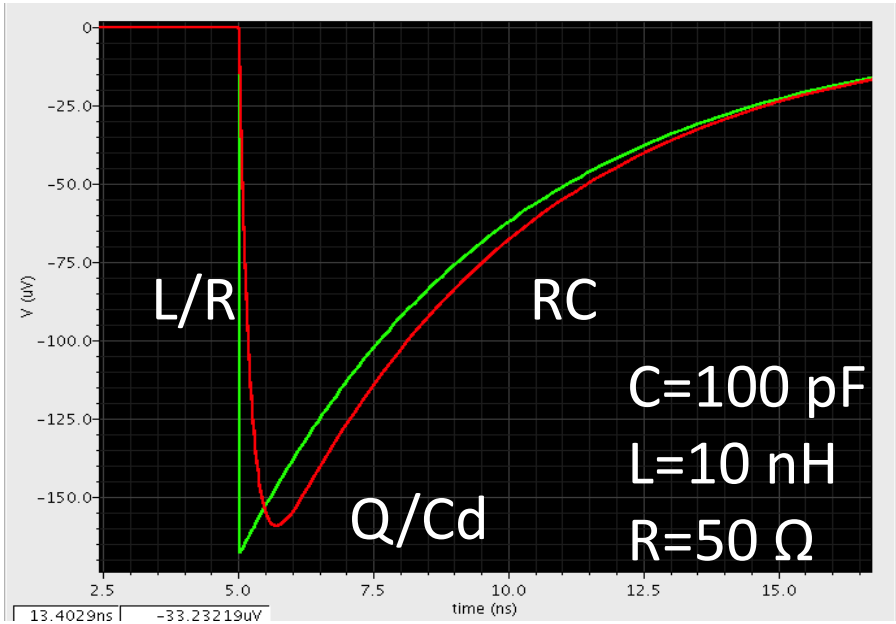
2 ns/div

Petiroc : bandwidth issues

- Pulser vs SiPM comparison
- SiPM is significantly slower than Petiroc
  - Pulser with 100pF injection capacitance, 10pe injec
  - SiPM illuminated with laser pulse, 10pe measured
  - Threshold from 1pe to 9pe
- Petiroc bandwidth meas. : 877MHz with puls
- With SiPm: limitation due to the stray inducta

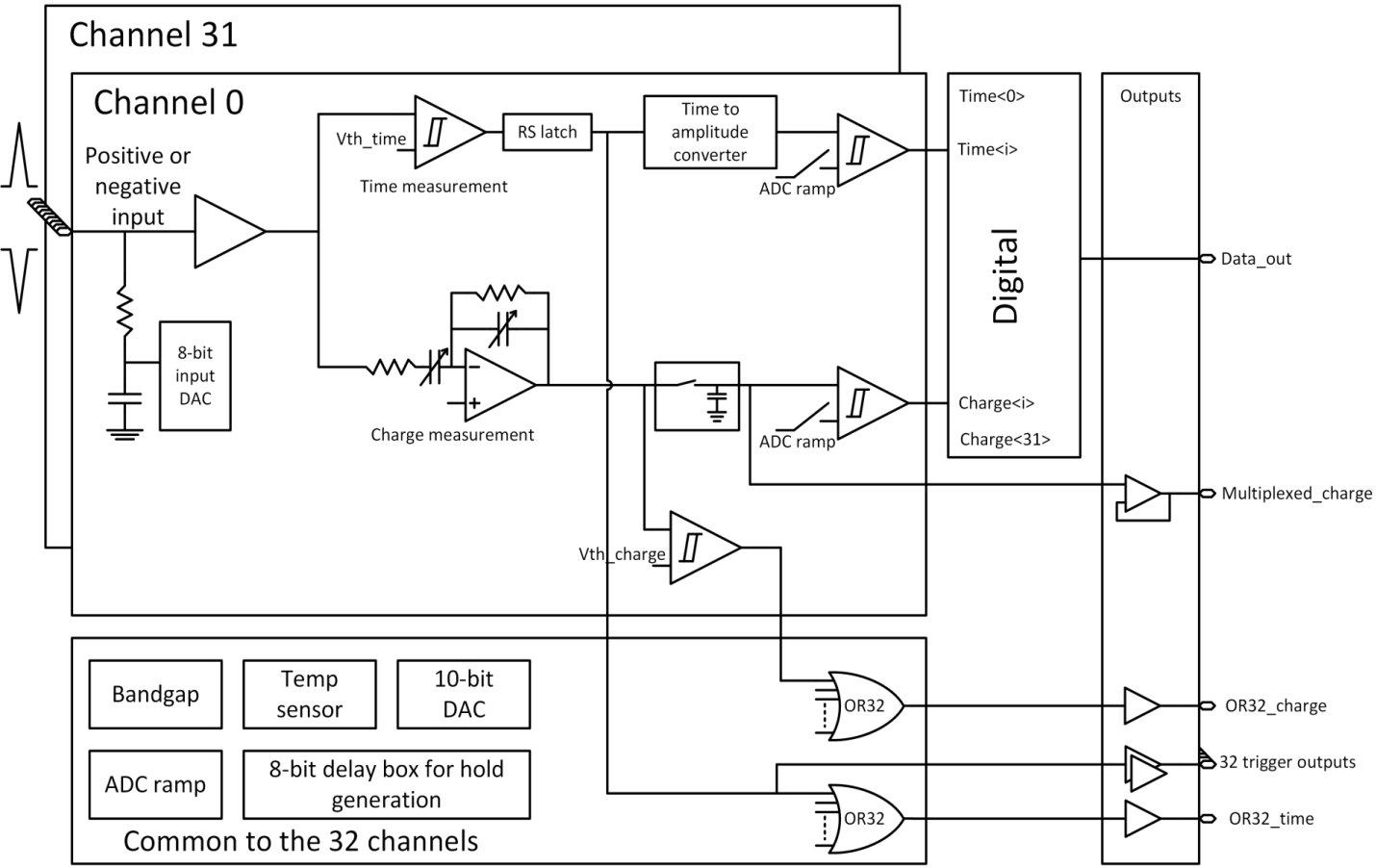


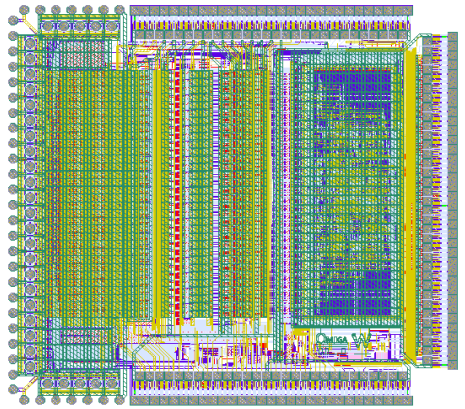




PETIROC2

- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 50 ps TDC
- Dual threshold : first photons and energy

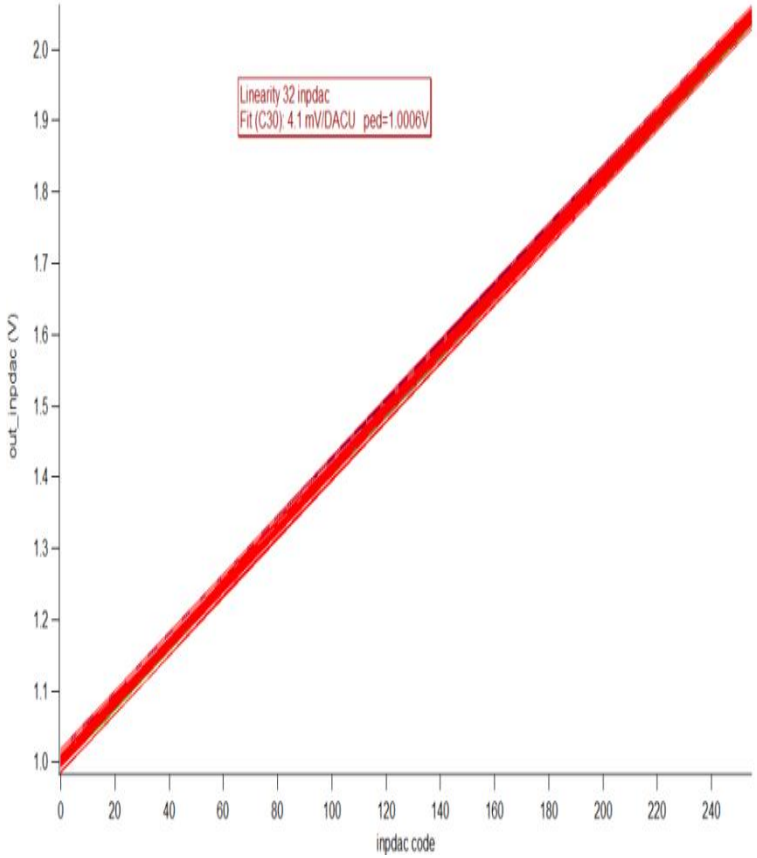




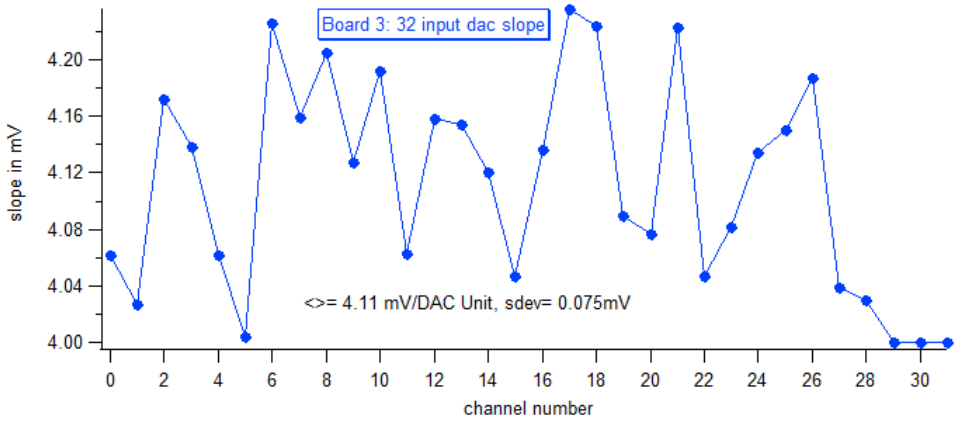
CdLT SiPM ROC chips

PETIROC2: Input DAC uniformity

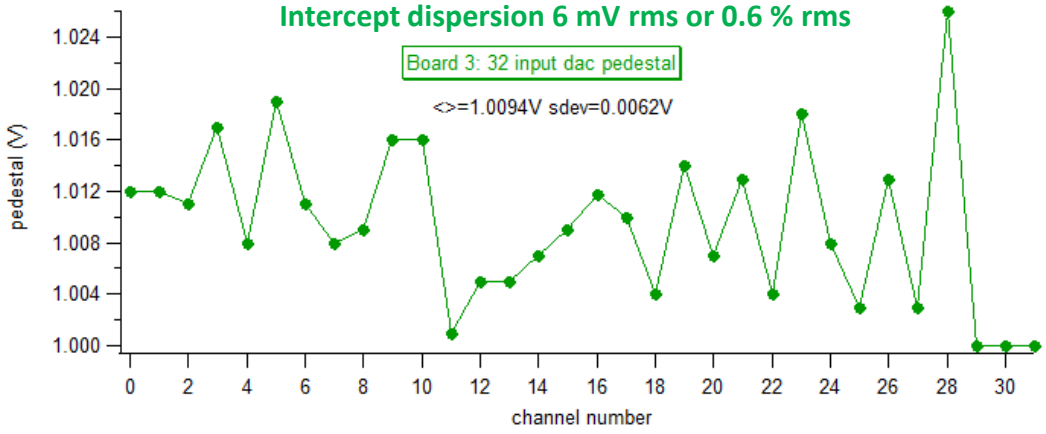
- Linearity and dispersion of the 32 8-bit input DAC



Slope dispersion 75 uV rms or 2% rms

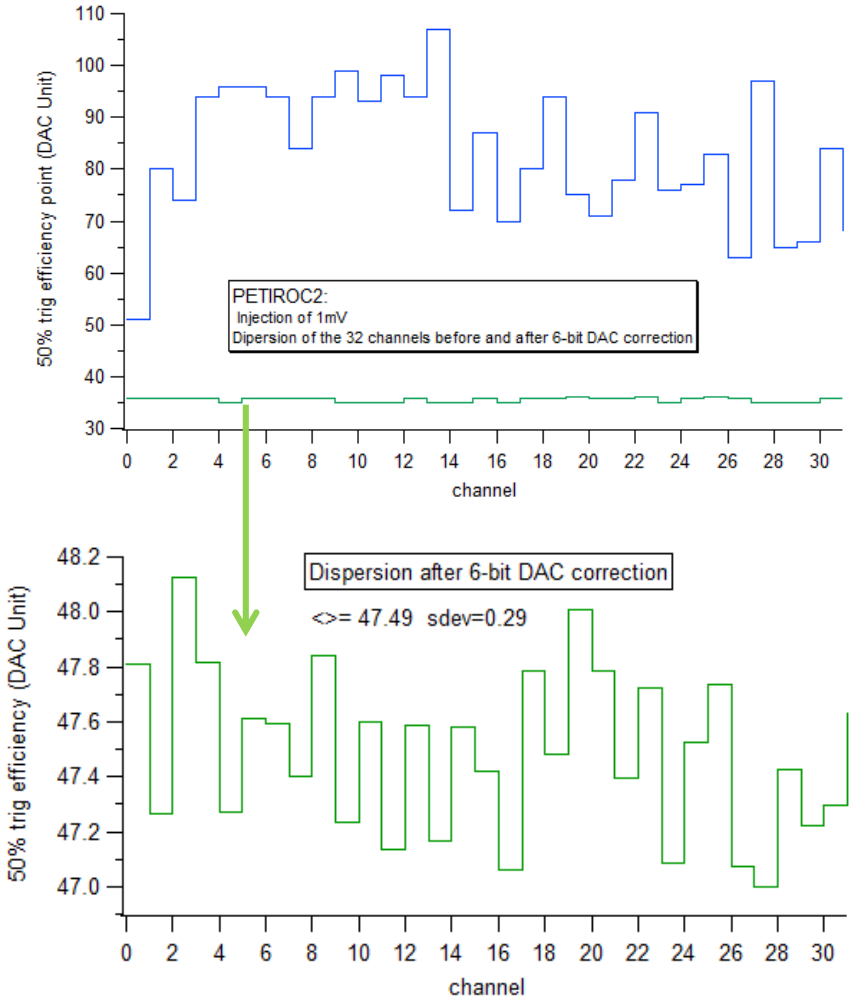


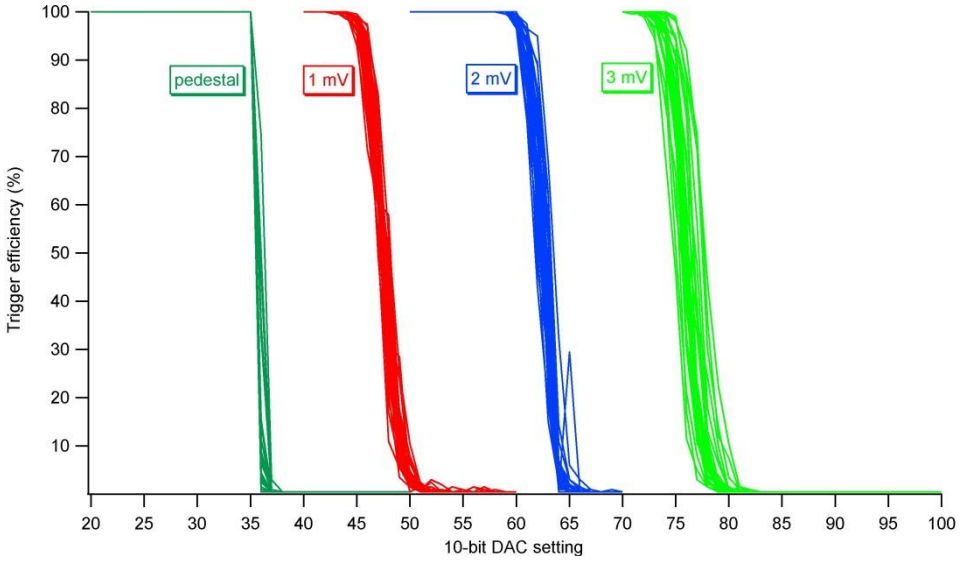
Intercept dispersion 6 mV rms or 0.6 % rms

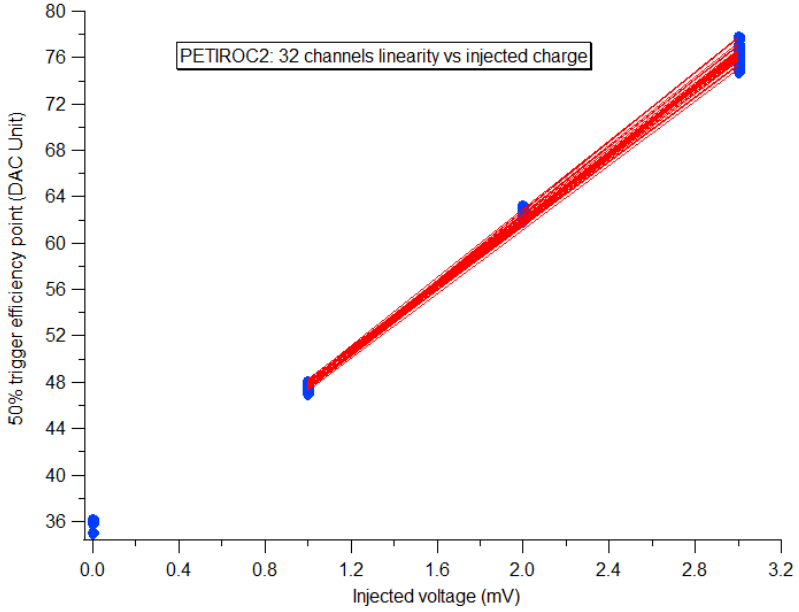


PETIROC2: « S-curves »

- Trigger efficiency measurements:

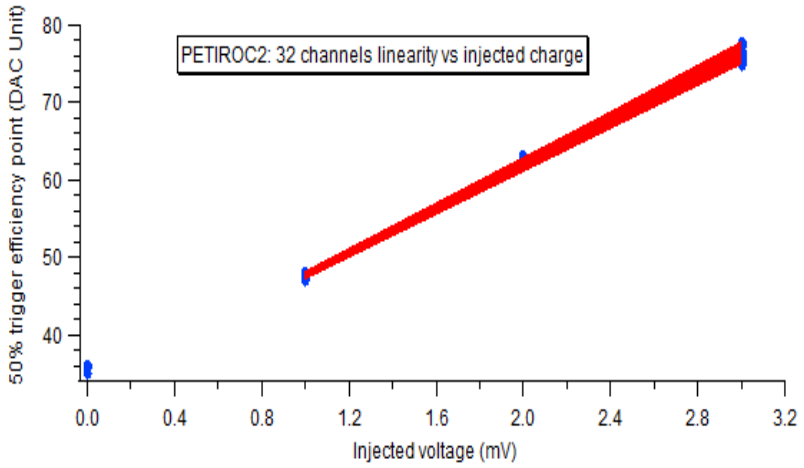


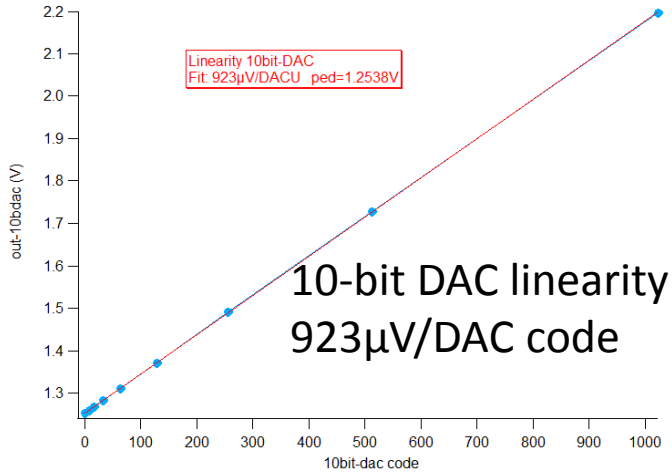




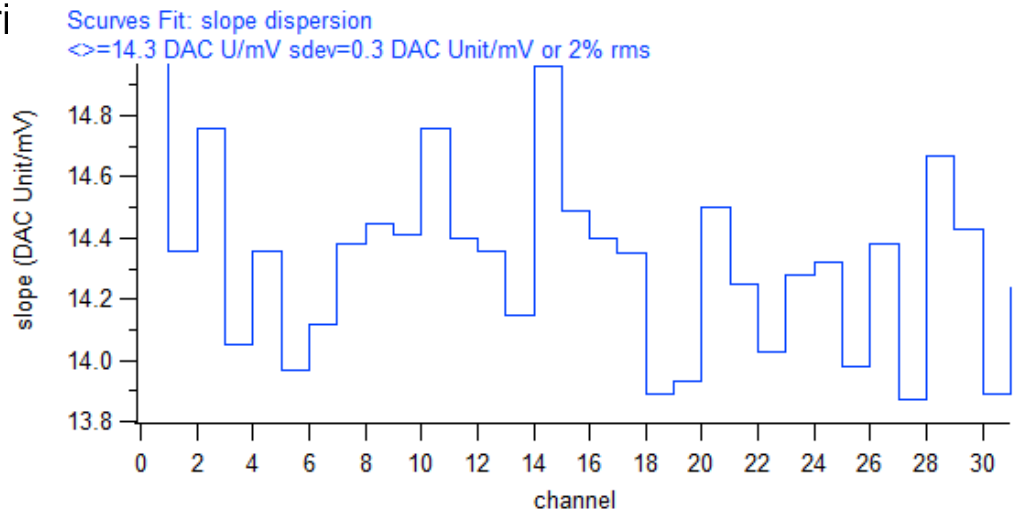
PETIROC2: efficiency uniformity

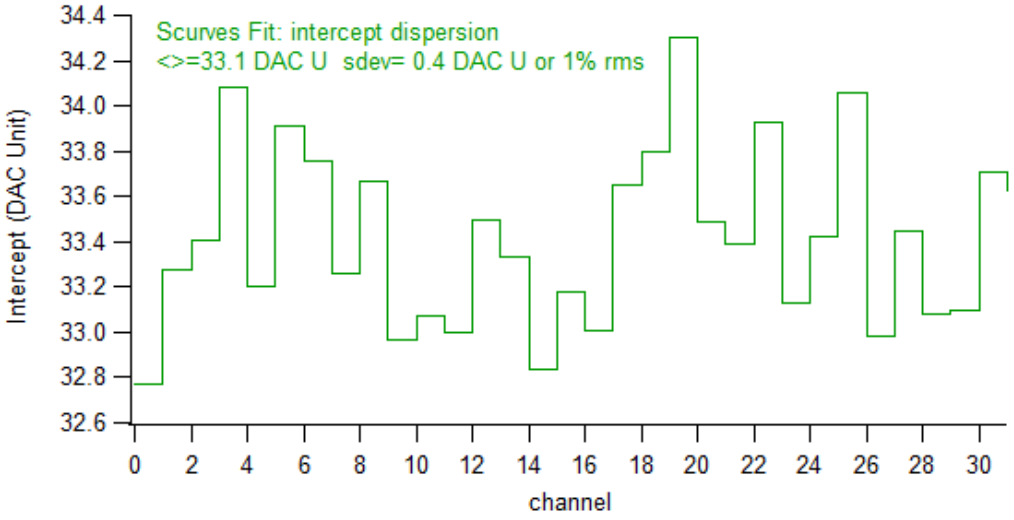
- Trigger efficiency measurements: Lineari
- One 10-bit DAC Unit= 923 µV





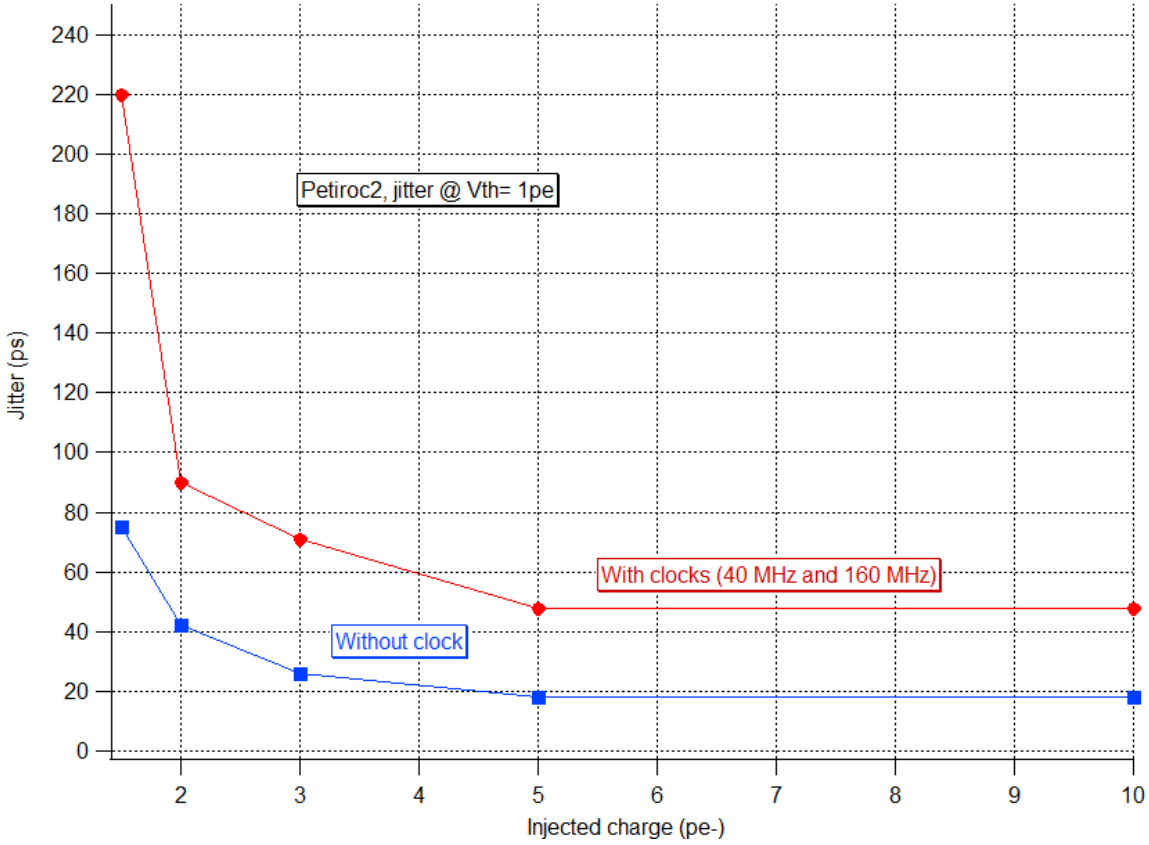
10-bit DAC linearity
923µV/DAC code



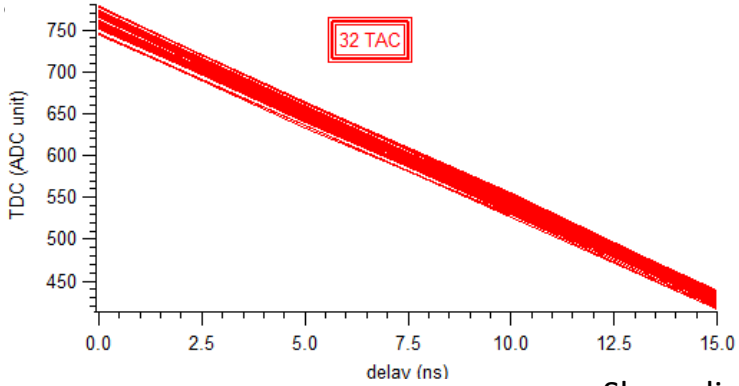


PETIROC2: Time measurement

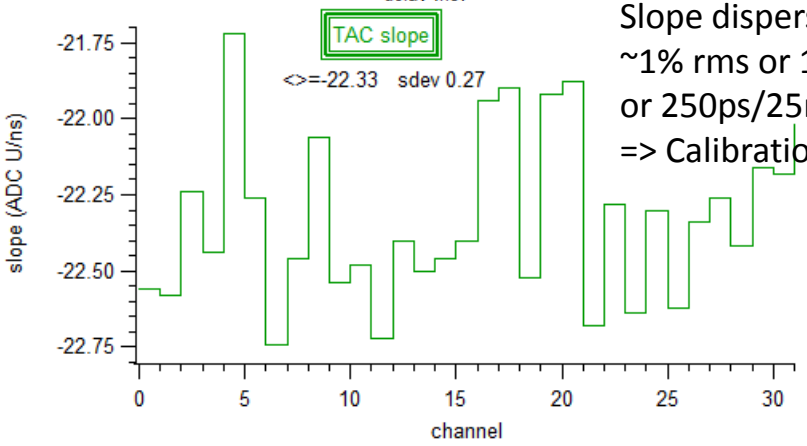
- Jitter vs threshold & injection
- Jitter improves with signal
- Clock couplings (understood)
- Jitter below 20ps



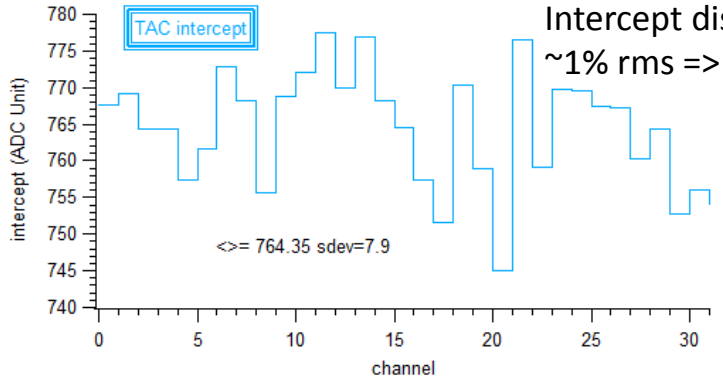
PETIROC2: TAC measurement



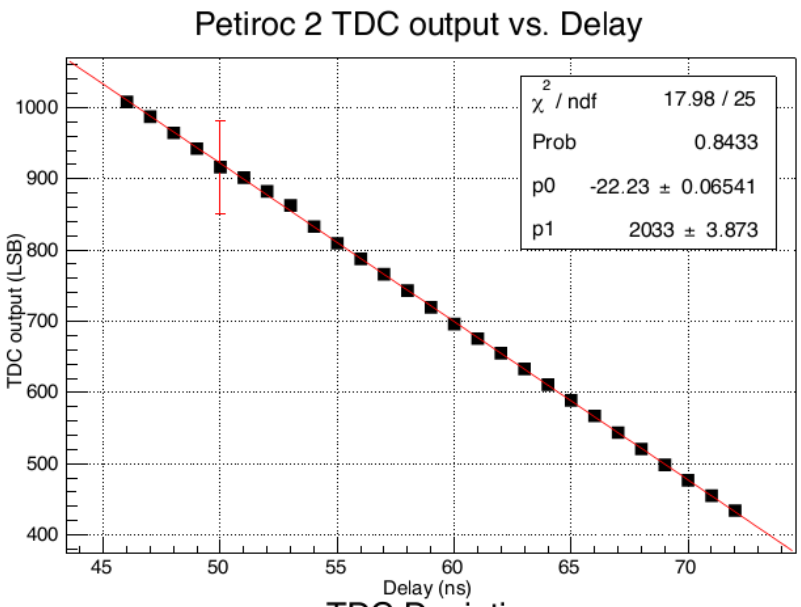
weeroc

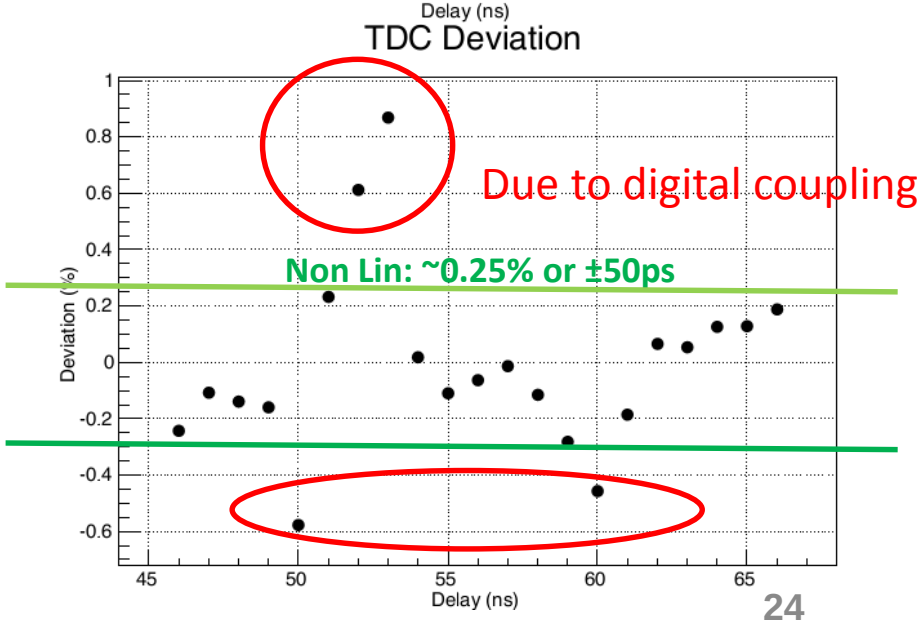


Slope dispersion:
~1% rms or 10ps/1ns
or 250ps/25ns
=> Calibration



Intercept dispersion:
~1% rms => Calibration

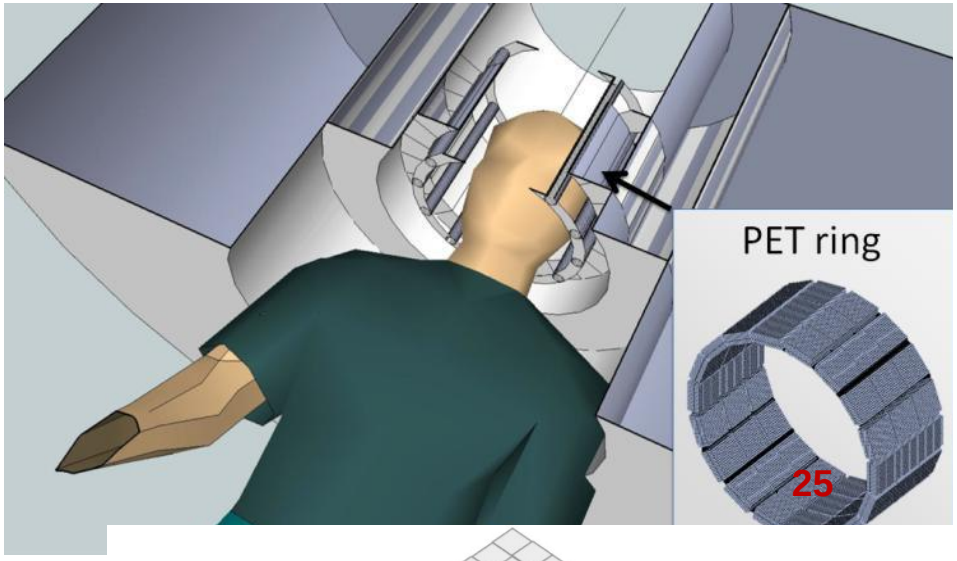


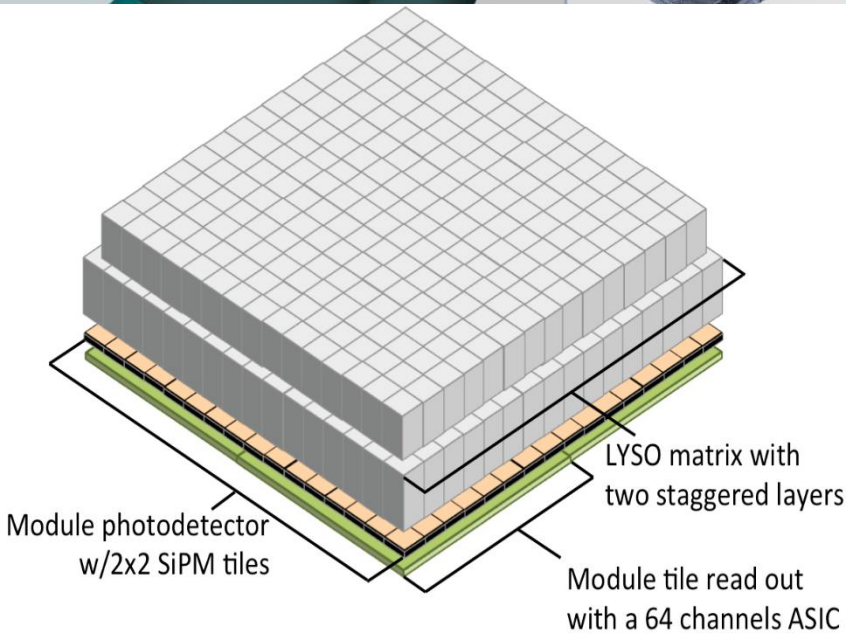


The TRIMAGE european project

- Cost effective tri-modality (PET – MR – EEG) imaging tools

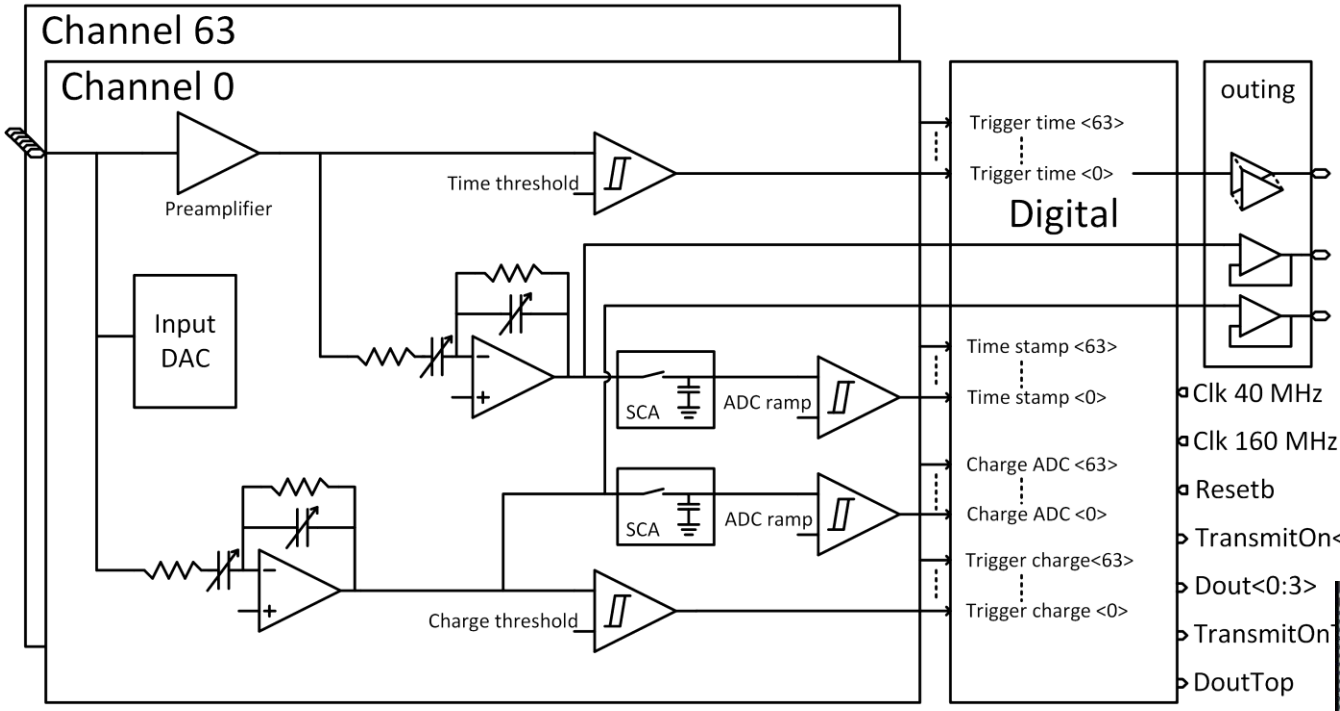
Project Partners	Role in the project
University of Pisa (UNIPI)	Coordinator & PET system development
Technological Educational Institute of Athens (TEIA)	Dissemination & Monte Carlo simulations
Forschungszentrum Juelich GmbH (FZJ)	Coil design & PET/MR/EEG integration
JARA BRAIN, RWTH (JRB)	Clinical application
Technische Universitat Munich (TUM)	Image quantification & clinical application
University of Zurich (PUK)	Patient recruitment & clinical data analysis
Istituto Nazionale di Fisica Nucleare (INFN)	PET system development & characterization
AdvanSiD (ASD)	SiPMs and chip-scale package development
Weeroc (WRC)	PET modules production & testing
Raytest GmbH (RAY)	Mechanical parts design & market strategy
RS2D (RS2D)	Design, assembly, test 1.5T MRI

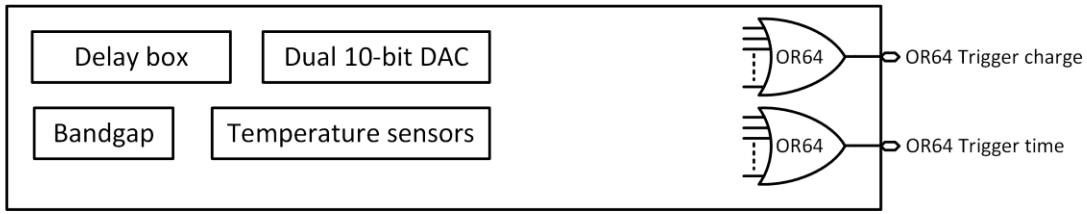


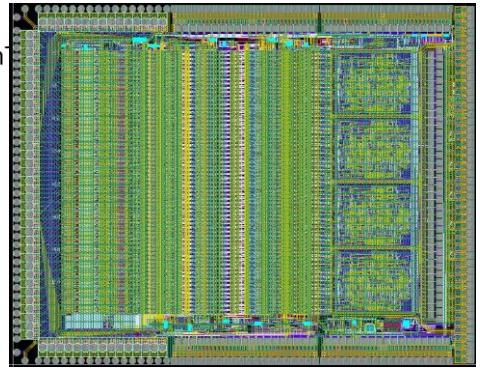


TRIROC

- 64-channel SiPM readout : positive & negative polarity inputs
- 8-bit Input DAC for SiPM HV tuning
- Time Stamp and ADC charge outputs







CdLT SiPM ROC chips

Technology transfer

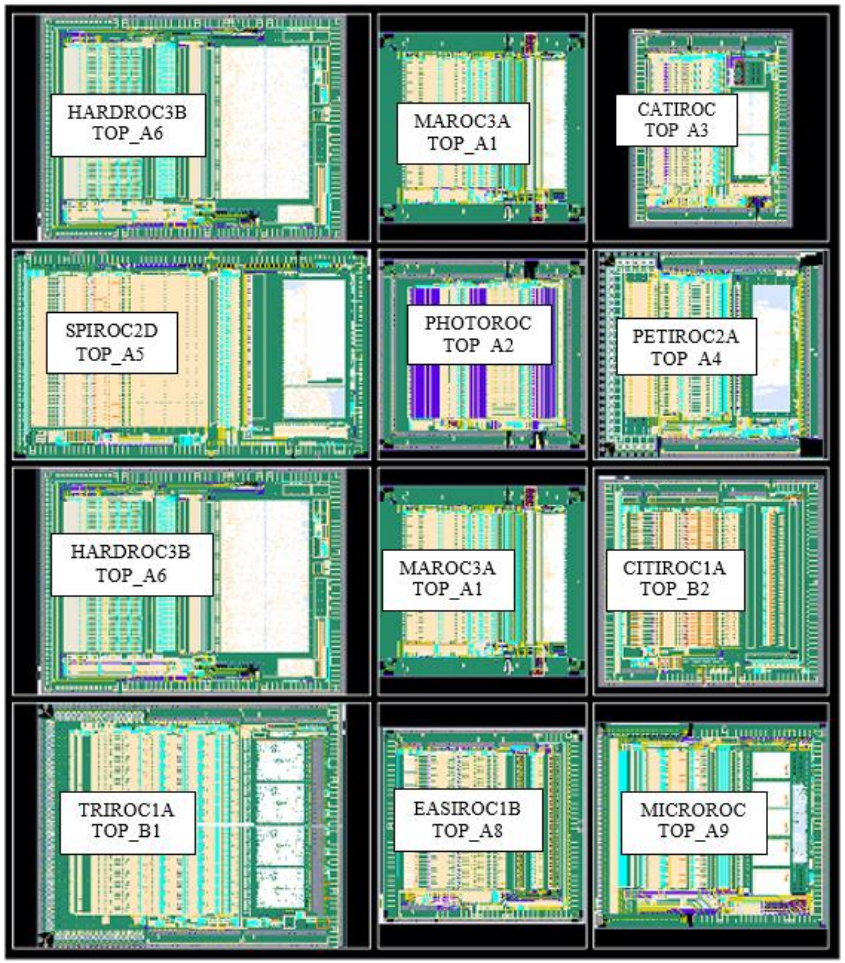
- Several chips transfered to other academic users
- Non-profit « academic price » (100€/chip). Free for IN2P3 ! (10 pieces)
- Industry transfer via startup « WEEROC »

chip	year	IN2P3 users	external users
MAROC3	2010	**LAL**, APC, CSNSM	NEVIS, KEK, CERN, Roma, Seoul, Pisa, Bari, Genève, Mocow, Valencia, Kolkata, Durham, Bruxelles, München, Jülich, Valparaiso, Lisboa, Bristol, Frascatti, Budapest, Catania, Glasgow, Coimbra, Grenoble
HARDROC2B	2010	**IPNL**, LPCCF	
SPIROC2B	2010		**DESY (D)**, TOHOKU (JP), Bergen (N)
SKIROC2	2010	LAL, **LLR**	IHEP
SPACIROC1	2010	**APC**, LAL	
EASIROC	2010	**IMNC**, LAL, LLR,	Palermo, FNAL, KEK, München, Dijon, CERN, Roma, Aachen, Toulouse, Lyon, Seoul, Bari, Tokyo, Pusan, Kyushu, Osaka
PARISROC2	2010	**IPNO**, LAPP, LLR, APC	IHEP
CITIROC	2013		**INAF**, CERN, JLAB, Rio, Berne, Mendoza, Aachen
PETIROC2	2013	**IPNL**, LPCCF	KEK, Tohoku

Summary

- Large family available
  - SPIROC et al. : large dynamic range, internal digitization
  - PETIROC et al. : GHz bandwidth, high speed discriminators
- Used by many external groups
  - DESY, KEK, INFN, CERN, FNAL…
- Large production available

- NB : variant SKIROC for Si
  - Used for CALICE and CMS
  - Will be moved to 65 or 130 nm



SUMMARY

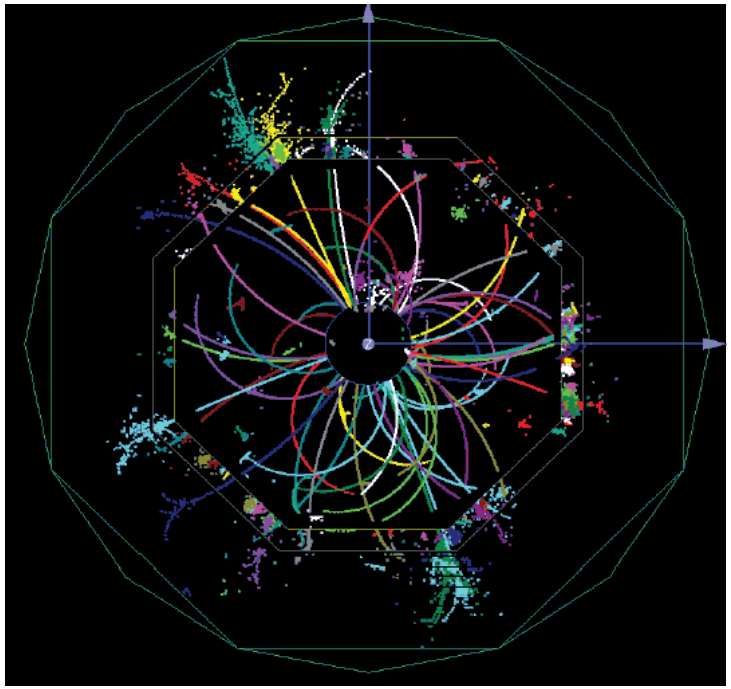
http://omega.in2p3.fr/ http://www.weeroc.com/

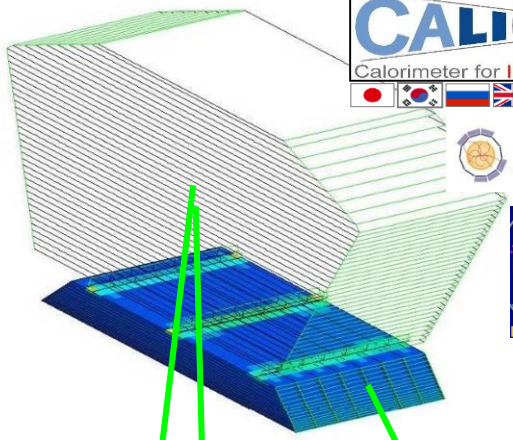
Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	50 fC - 100 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

Backup slides .

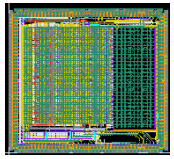
CALICE = « imaging calorimetry »

- Calorimeter readout: auto-trigger, analog storage, digitization and token-ring readout…
- power pulsing : <1 % duty cycle
- Optimized commonalities within EUDET/AIDA

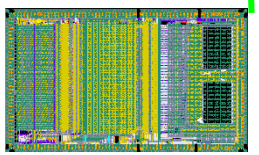




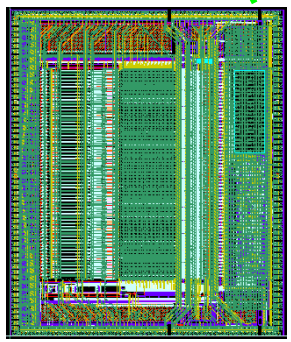
HARDROC2
SDHCAL RPC
64 ch 16 mm^2



SPIROC2
AHCAL SiPM
36 ch 30 mm^2



SKIROC2
ECAL Si
64 ch. 70 mm^2

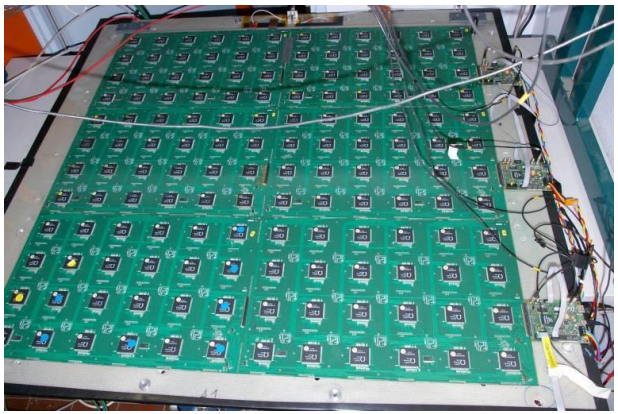


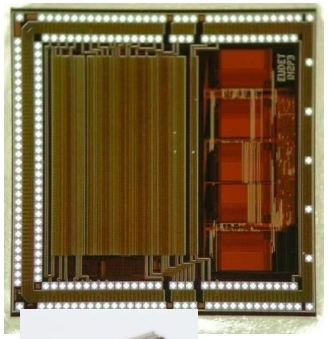
FLC_PHY3 (2003)

HARDROC2 for RPC readout

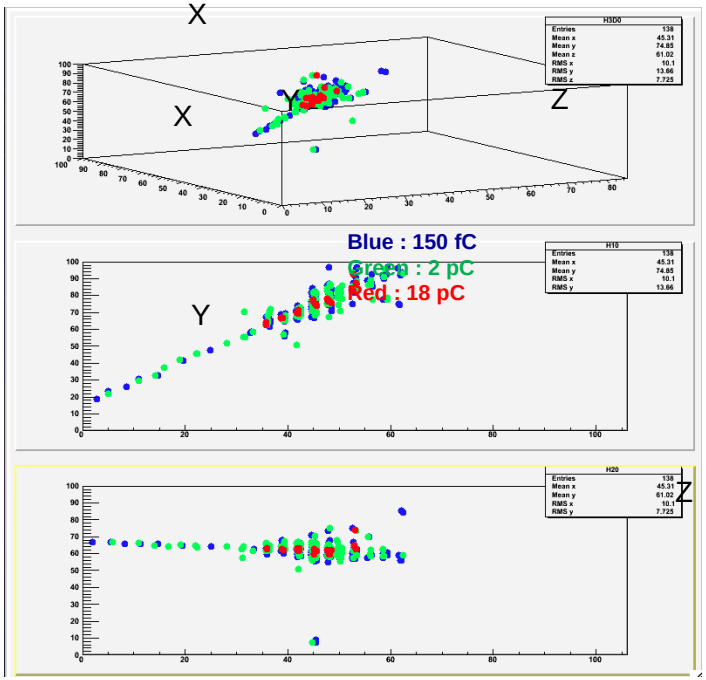
- **HARDROC2: 64 channels (RPC DHCAL)**
  - preamp + shaper+ 3 discris (semi digital readout)
  - Auto trigger on 10fC up to 20 pC
  - 5 0.5 Kbytes memories to store 127 events
  - Full power pulsing => 7.5 µW/ch
  - Fully integrated ILC sequential readout
  - 10 000 chips produced to equip 400 000 ch
  - SDHCAL technological proto with 40 layers (5760 HR2 chips
    - Successful TB in 2012 : 40 layers with Power Pulsing mode

Cosmic hadronic shower





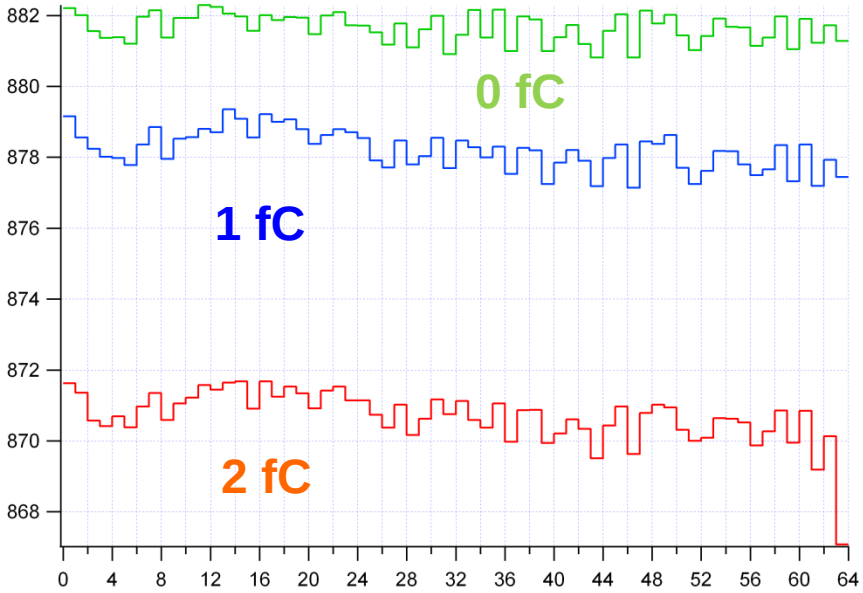

CdLT SiPM ROC chips



Variant: MICROROC

MICROROC: 64 channels for µMegas (DHCAL ILC)

- ❑ Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- ❑ Noise: **0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- ❑ Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- ❑ **HV sparks protection**
- ❑ 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m2 in TB



@LAPP Annecy

1m2 equipped with 144 MICROROC

SKIROC : SiECAL chip

- 64 ch Si readout chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits
  - Time measurement 1 ns