Wojciech.Dulinski@iphc.cnrs.fr

Post-processing steps for monolithic (CMOS) sensors: possible added-on value

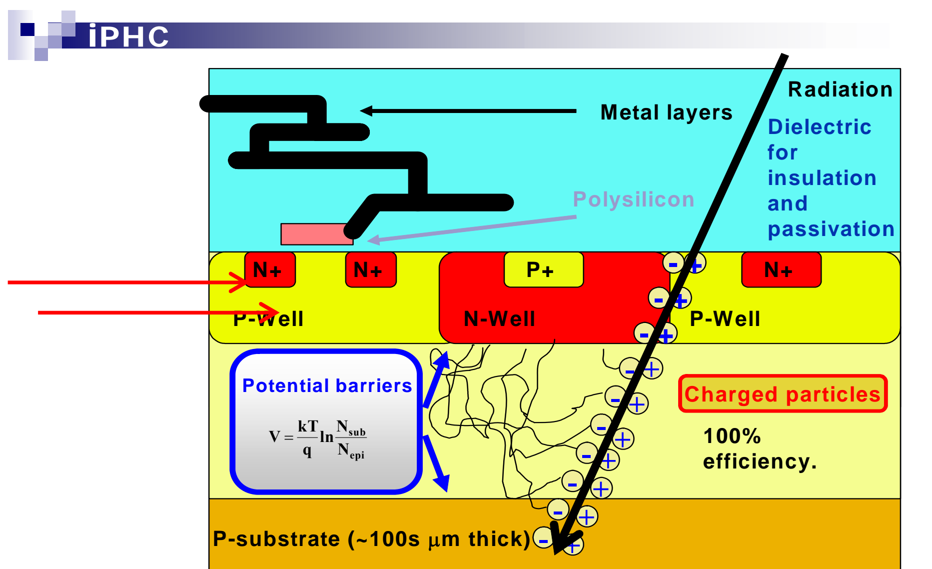
Wojciech Dulinski, IPHC Strasbourg, France

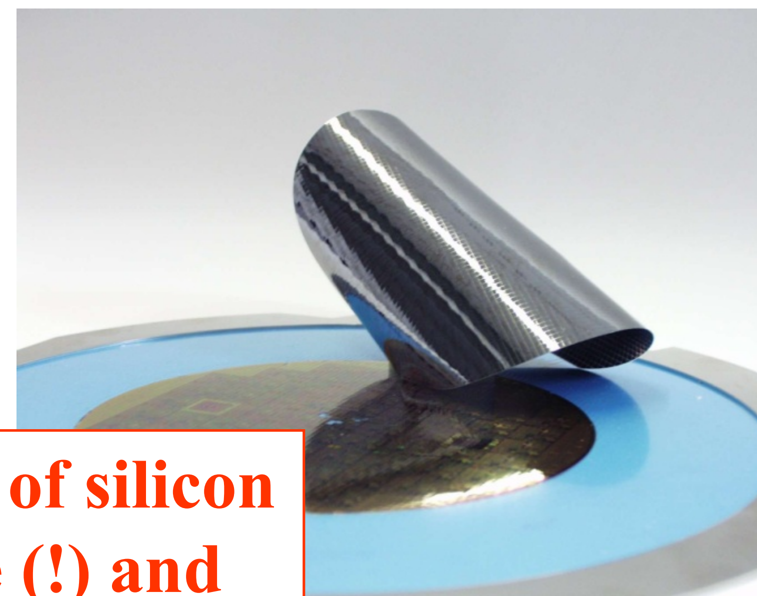
Outline

- Process evolution for monolithic radiation sensors
- Thinning and dicing
- Embedding in plastics
- Processing for back-illumination
- 3D Integration
- Conclusions and prospects

Wojciech.Dulinski@iphc.cnrs.fr

Monolithic Active Pixel Sensor: effective use of a thin epitaxial layer (10 – 20 µm) for MIP tracking

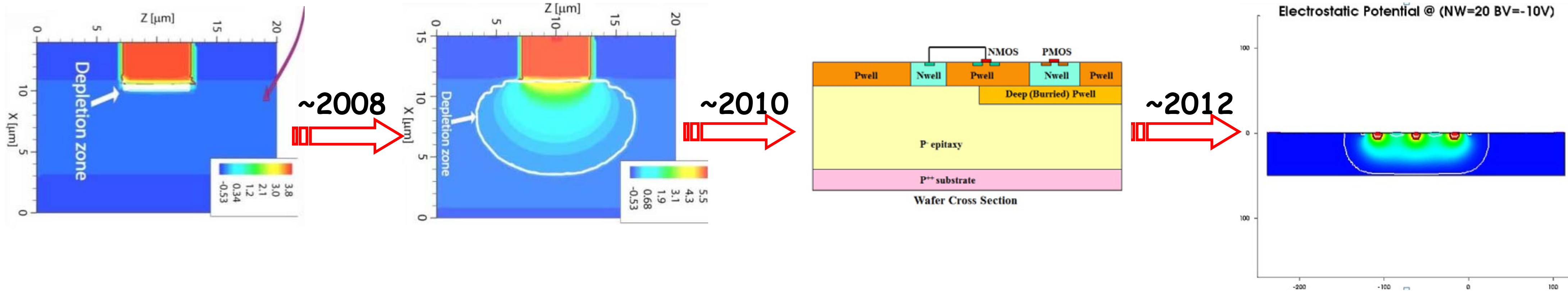




May be extremely thin (~25 µm of silicon in total, ~0.027 % X_0), flexible (!) and still fully efficient for MIP tracking!

Wojciech.Dulinski@iphc.cnrs.fr

Monolithic Active Pixel Sensor process evolution: towards complete CMOS and thick, fully depleted substrate



Non-depleted, thick epi substrate: ~10^{12} n/cm²

- AMS 0.6
- AMS 0.35

Semi-depleted, HR epi substrate >10^{13} n/cm²

- XFAB 0.6
- AMS 0.35

Quadruple-well CMOS: both type of transistors admitted in the pixel array

- TOWER 0.18

Fully depleted, thick substrate >10^{14} n/cm² ?

- ESPROS 0.15
- TOWER 0.18 (Appendix1)

New applications? Soft X-rays Imaging for example…

Wojciech.Dulinski@iphc.cnrs.fr

Thinning and dicing, to profit from low material budget

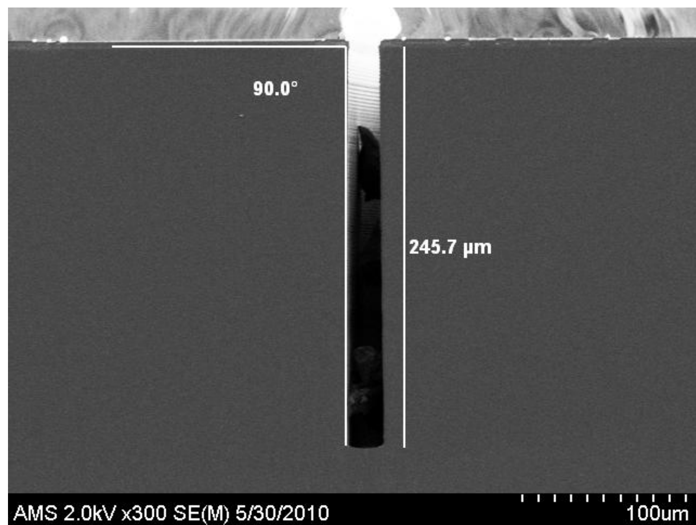
Sensor thinning down to ~50 µm by mechanical grinding starts to be a standard process, available through many companies. Our partners: Aptek Industries Inc. (California) and ROCWOOD Wafer Reclaim (France). The first is able to process individual chips.

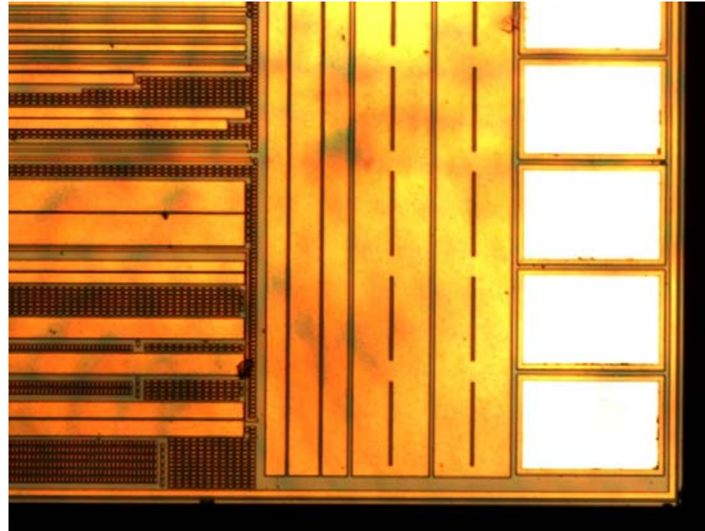
Precision: ± 5 µm for thickness, few tens of µm for x-y dimensions (standard sewing channel of 100 µm)

Wojciech.Dulinski@iphc.cnrs.fr

For better mechanical precision → trench dicing, to minimize dead space in case of buttable assembling

Trench Dicing is a standard AMS module for 0.35 OPTO process. Deep Reactive Ion Etching (DRIE) is used to create trenches (width 15 µm, attached to the seal ring).
The die separation is done after fabrication by a thinning step. Dicing precision ~1 µm.



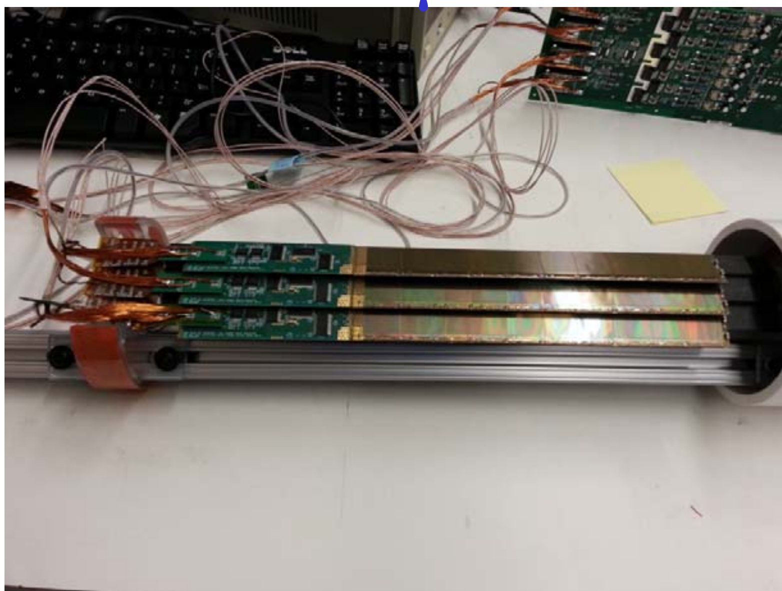


DRI diced Mimosa 28 (STAR Ultimate-2) sensor

Wojciech.Dulinski@iphc.cnrs.fr

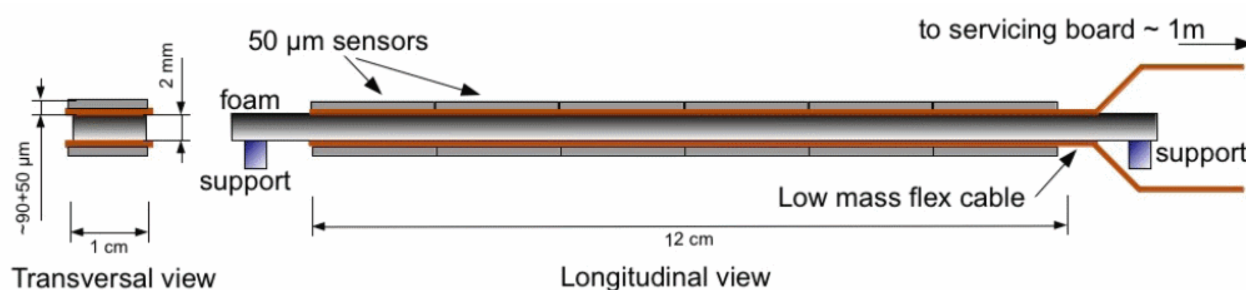
Thin sensor packaging: to keep low material budget

Reminder: 100 µm of Si is equivalent of 0.1% of X_0



STAR Microvertex module

- 10 Mimosa28 (2x2 cm^2) sensors/ladder
- Kapton flex PCB (double sided, Cu or Al) carbon fiber support
- Estimated 0.37 % X_0/layer



PLUME (IPHC, Strasbourg): double-sided ladder (ILC compatible)

- 2x6 Mimosa26 sensors thinned down to 50 µm
- Standard double-side kapton PCB: Cu conductor (20 µm/layer)
- SiC foam (8%) for spacer between layers
- Estimated 0.6 % X_0/two sensor layers

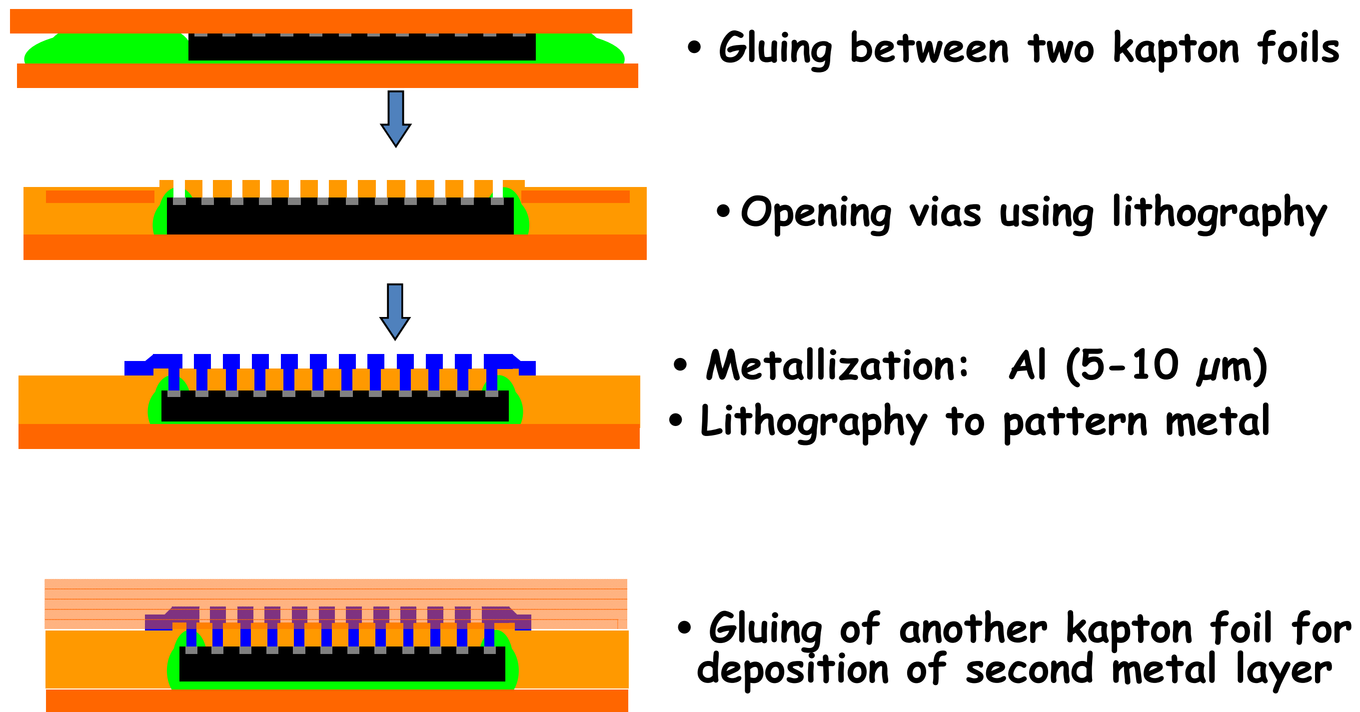
Can it be better?

Wojciech.Dulinski@iphc.cnrs.fr

Novel approach for ultra thin sensor packaging:

use of a "standard" flex PCB process for chip embedding in plastic foils

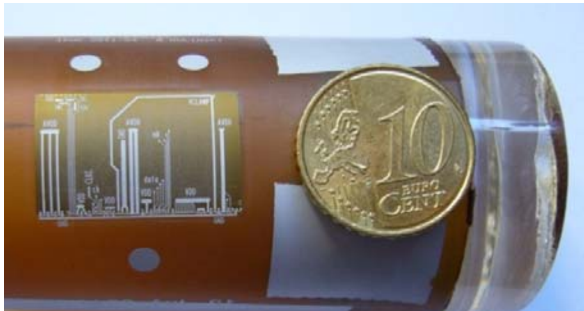
The goal: < 0.1 % of X_0 per sensor layer (large area ladder, all included)



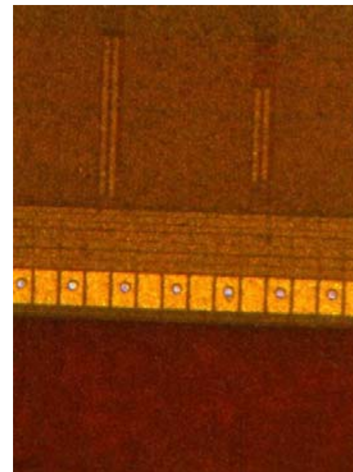
No wire bonding, excellent mechanical chip protection

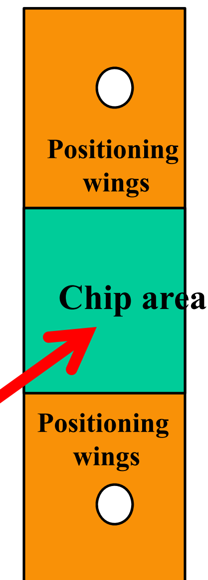
Wojciech.Dulinski@iphc.cnrs.fr

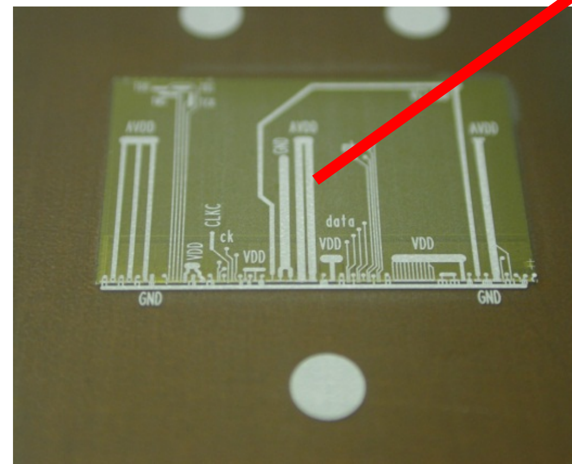
Redistribution layer : make the connection between silicon world and PCB world (from 50 µm vias to 200 µm vias). Here on top of M-26 (EUDET) CMOS pixel sensor, thinned down to 50 µm



Solid state flexible sensor wrapped over cylindrical shape (R=20 mm)





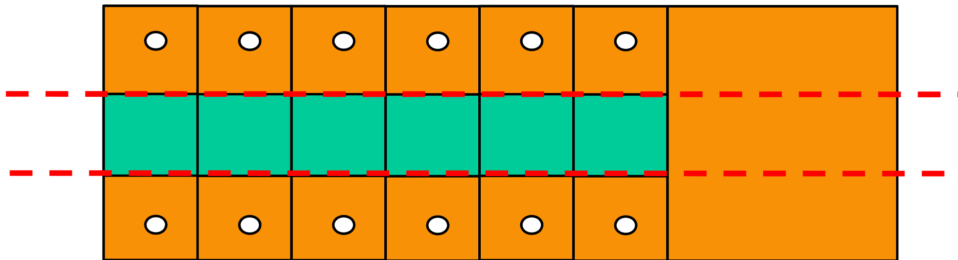


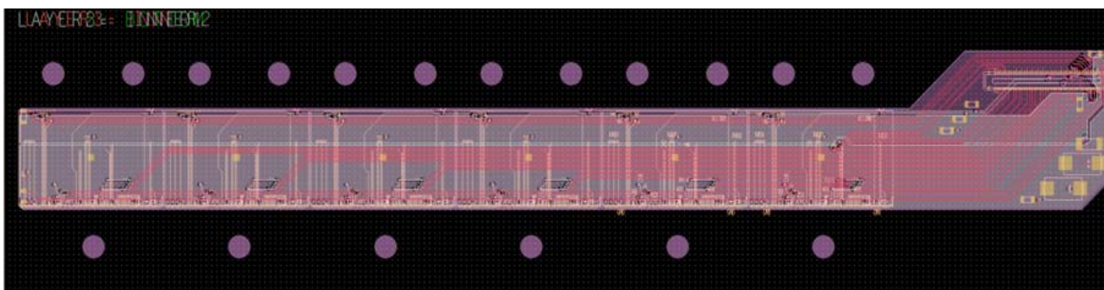
Laser flex cutting keeping positioning wings.

50um accuracy

Wojciech.Dulinski@iphc.cnrs.fr

Multi chip embedding principle





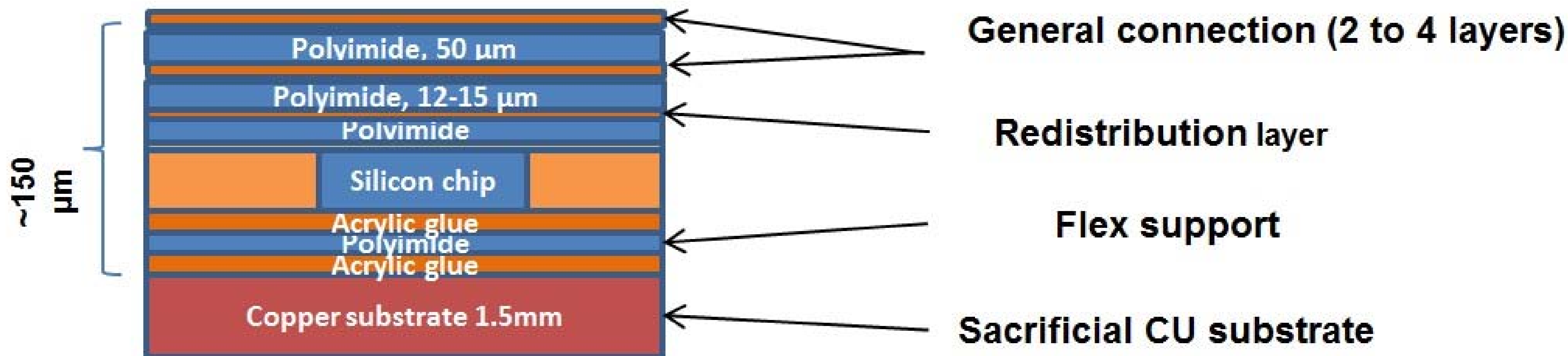
1. Redistribution layer is made on single chips

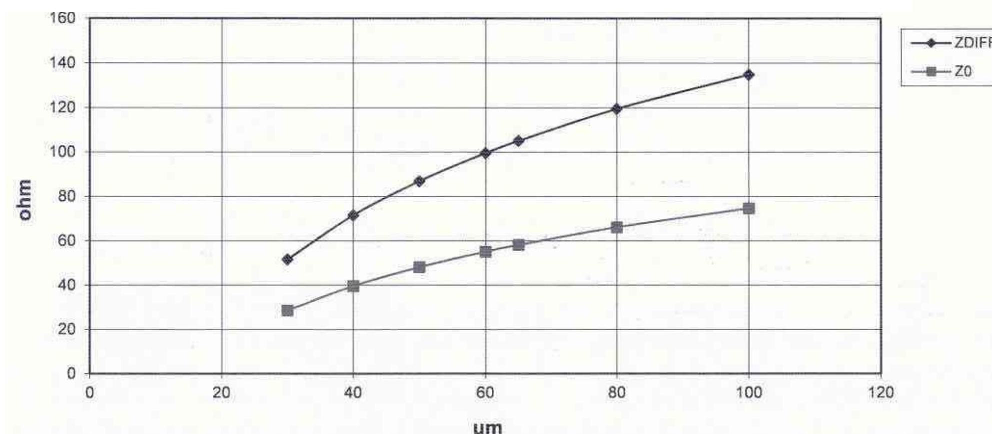
2. Individual chips with redistribution layer mechanically aligned and fixed by attachment to another polyamide layer

3. General connection are made on the full module (ladder) by adding more polyamide/metal layers

Wojciech.Dulinski@iphc.cnrs.fr

Stack formation (during processing, before copper substrate dissolution)

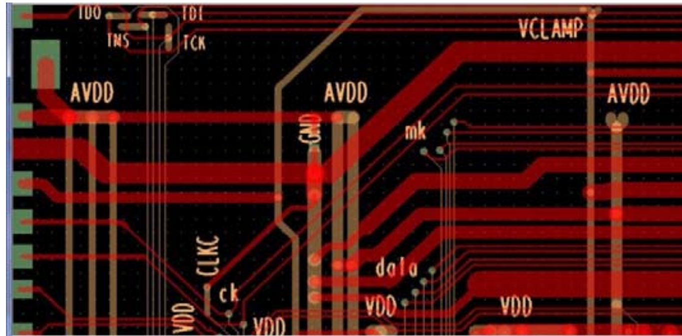




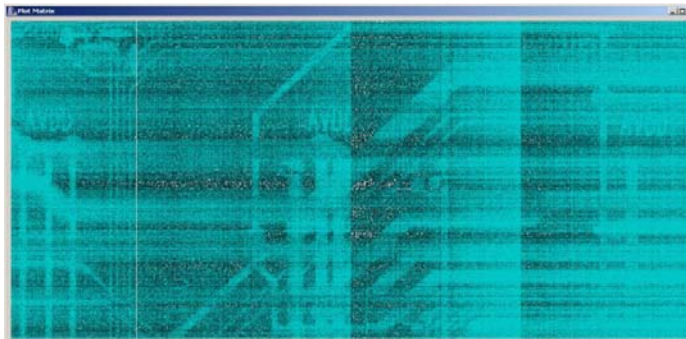
Impedance of readout lines (last metal, 100 µm width, 100 µm gap) as a function of kapton thickness: 100 Ω for 60 µm thick kapton (last layer)

Wojciech.Dulinski@iphc.cnrs.fr

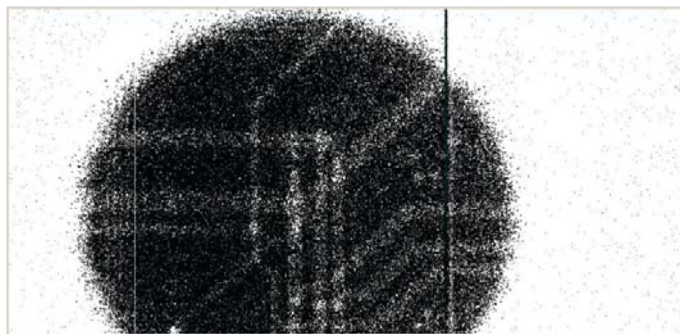
Imaging results with our first embedded sensor: single Mimosa 26 chip, two interconnecting metal layers



Lithography details of interconnecting metal (two layers of ~10 µm thick Al) deposited on top of the pixel sensor



"Shadow" of metal measured by pixel sensor in visible light



Auto-radiography of metal measured by pixel sensor using 5.9 keV X-rays (^{55}Fe)

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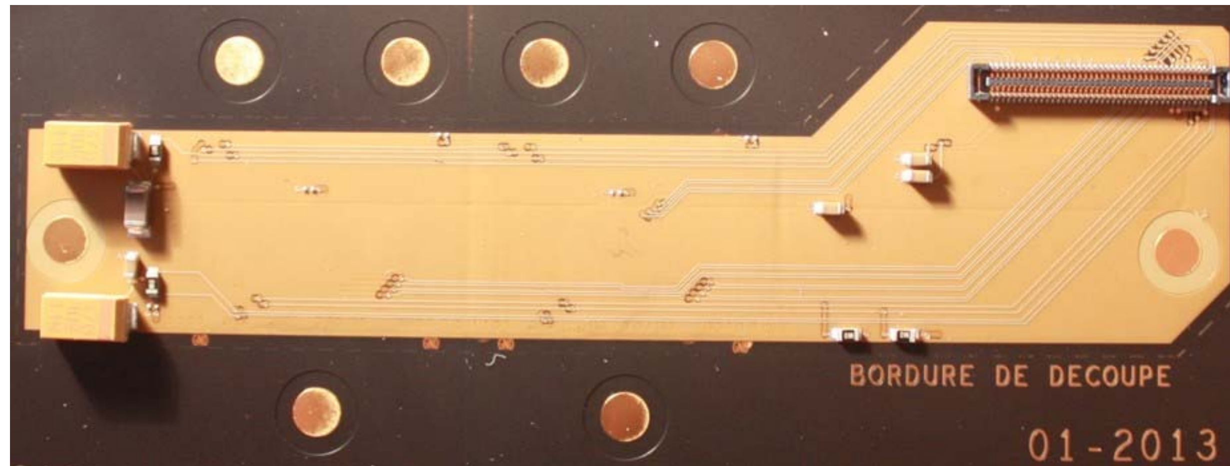
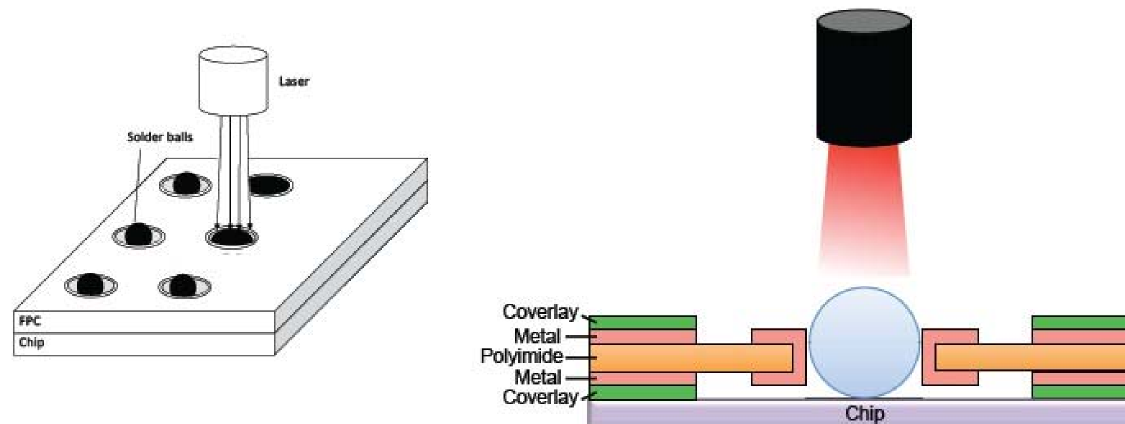
Second step: two-M26 chip ladder (4 kapton/aluminum layers)



Another approach exists: laser ball bonding (ALICE ITS upgrade)



Wojciech.Dulinski@iphc.cnrs.fr

Back illumination: optimization of entrance window. Why it is crucial for some applications? Example of soft X-rays…

Typical thickness of front-side entrance window is ~10 µm (Al/SiO_2 multilayer sandwich, transistor wells)

	8kev	5keV	3keV	1keV
100 µm	78%	100%	100%	100%
50 µm	53%	94%	100%	100%
10 µm	14%	44%	90%	97%
1 µm	1.5%	5.5%	20%	31 %
0.1 µm	0.15%	0.6%	2.2%	3.6%

X-rays absorption in silicon

Wojciech.Dulinski@iphc.cnrs.fr

"Standard" back-side processing: several critical steps

Particle track
P^+well N^+well P^+well
depletion
P^- epitaxial layer
Sensitive thickness (~10 µm)
Potential minimum
Low resistivity P^{++} substrate

support
passivation and interconnection layers
Pwell and Nwell - electronics layer
P^- epitaxial layer
electric field profiler and surface passivation
wire bounding interconnection
periphery electronics
Nwell
Pwell
pixel array area
10-15 µm

1. **Attaching of support wafer from the front side**
2. **Material removal from the original wafer, down to the epi layer (<20 µm thick)**
3. **Back-side contact implantation (ion doping)**
4. **Implant activation at low temperature (local heating by laser beam scan)**
5. **Back-side opening of bonding pads**

Step 3 and 4 are the most important: must optimize the dead layer thickness and maintain the low leakage current

Mimosa5 prototype (2x2 cm^2, 2003) thinned-down to the epitaxy layer (14µm)

Wojciech.Dulinski@iphc.cnrs.fr

Back-side processing industrial offer

- **"Big" companies like ATMEL → I2V (Grenoble): optimized for their products, difficult access.**

- **"Small companies" like TRACIT = SOITEC (Grenoble) for thinning, IBS (Gréasque, France) for backplane implantation. Uncertain quality…**

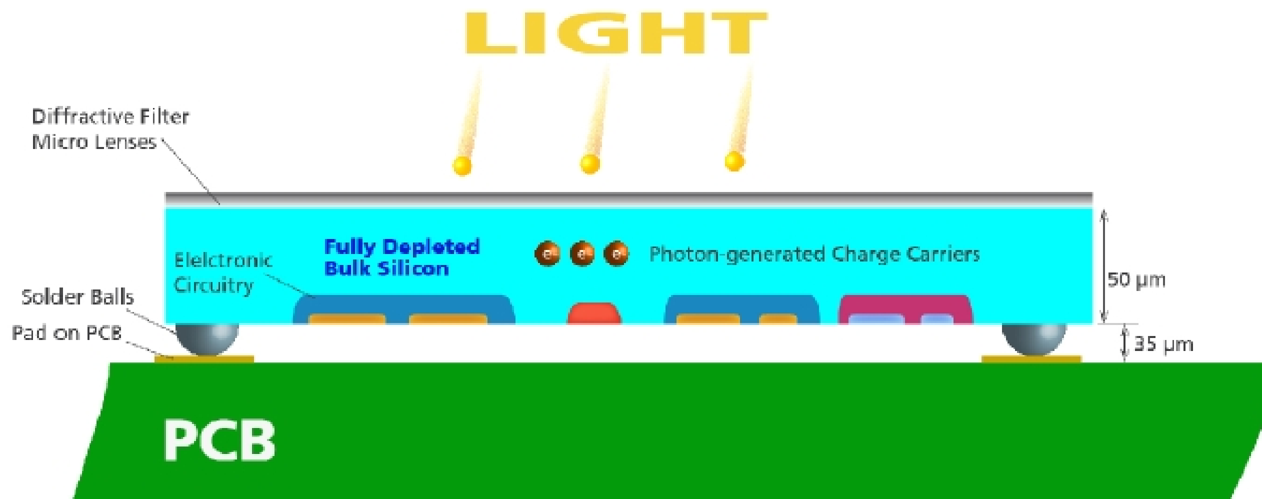
- **National Technology Development Labs like IMEC or JPL: cost issue, framework. May provide top parameters: see "Delta doping process" at Appendix 2**

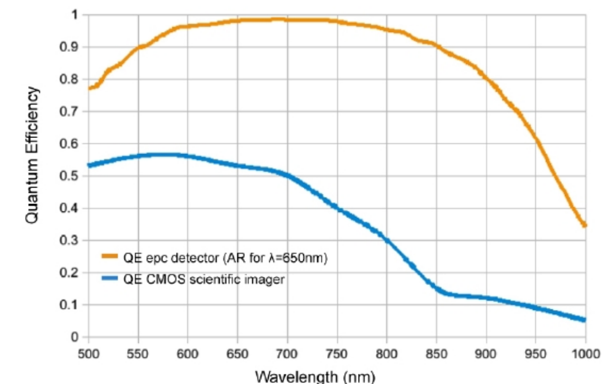
- **Substantial process simplification if thick (>50 µm), fully depleted wafer…**

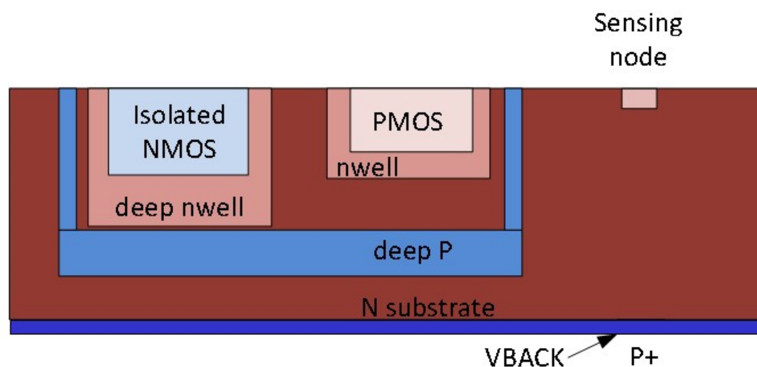
Wojciech.Dulinski@iphc.cnrs.fr

Full depletion + backside illumination industrial offer: ESPROS CMOS (+CCD) process (150 nm)

Detector grade, n-type, fully depleted 50 µm thick bulk silicon
+ deep p-implant to separate transistor level + backside processing
No restrictions for use of both PMOS and NMOS in pixels







ESPROS wafer cross-section

First results of our design at ESPROS available, second iteration started…

Competition is coming: Sensor Creation Inc.
Fully Depleted, Backside Illuminated, 200 µm thick, 15 µm pitch VGA Resolution CMOS Imager (Appendix 3)

3D-Interconnection of (heterogeneous) CMOS wafers

Second tentative, after the one proposed ~5 years ago (also at FEE) (Tezzaron/Chartered+XFAB .6 µm)

May increase substantially monolithic sensors performance and flexibility, even if limited to two tiers only.

Possible use in the future: monolithic, vertically integrated pixel detectors for future vertex detectors and novel solutions for X-ray imaging (synchrotron radiation sources) . "Good" combination may be:
First tier: fully depleted MAPS (DMAPS) - sensor plus analog electronics using "imager" process. At present, 130 – 180 nm process available, 65 nm coming soon?
Second tier: digital processing in very deep submicron CMOS. "Standard" 65nm?

Other example: back-illuminated, GM-APDs (SiPMs) arrays integrated with the readout circuitry (Appendix 4)

Wojciech.Dulinski@iphc.cnrs.fr

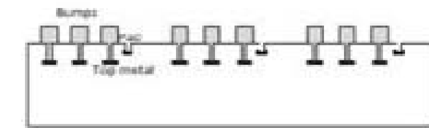
AIDA 3D package

(IPHC/IN2P3 and Bergamo-Pavia/INFN partnership)

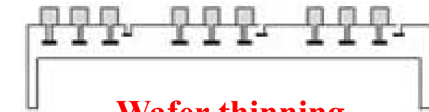
Integration of two generic (standard) CMOS wafers with a minimum pitch

Industrial partner: IMS Fraunhofer, Duisburg
Process: SLID (Appendix 5), chip-to-wafer,
10 µm interconnection pitch
Additional requirements: wafer thinning (<100 µm total stack)

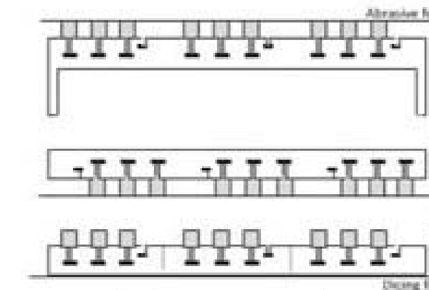
SLID based vertical integration is a "surface quality tolerant" process. The only requirements for the CMOS wafers (to keep processing simple) is the standard wafer planarization by the Foundry. It is also supposed to be potentially cheap (automatic).



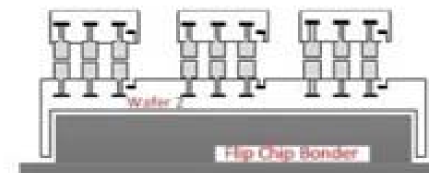
Electroplating

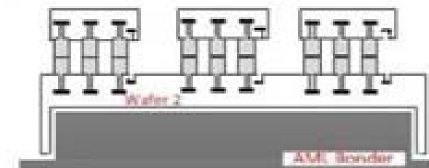


Wafer thinning



Chip preparation





Chip-to-wafer bonding

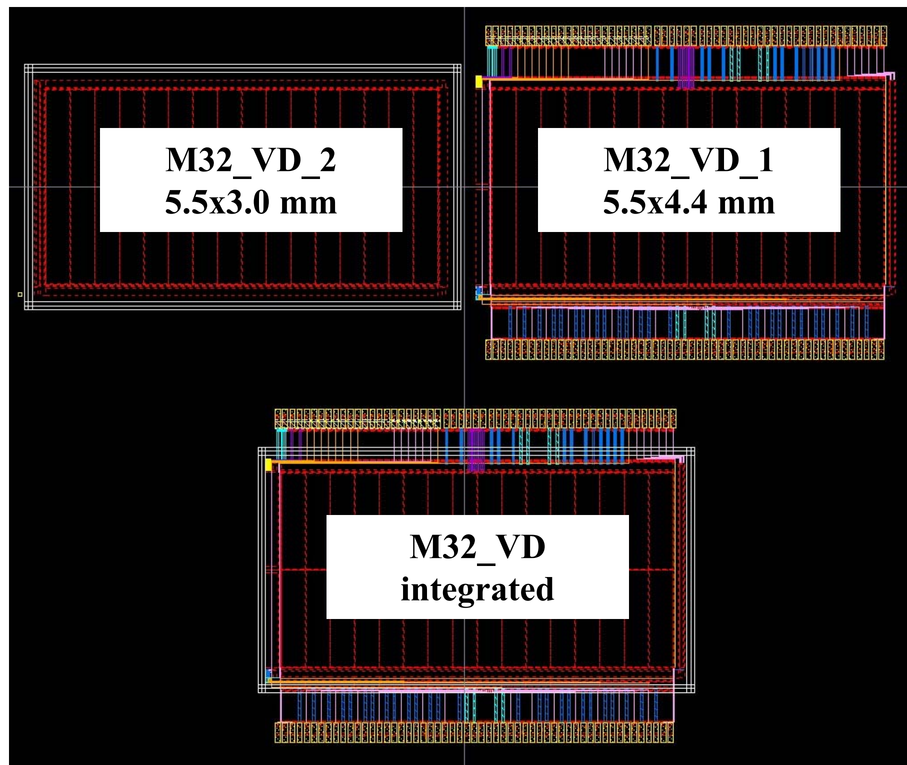
Intended IMS processing flow

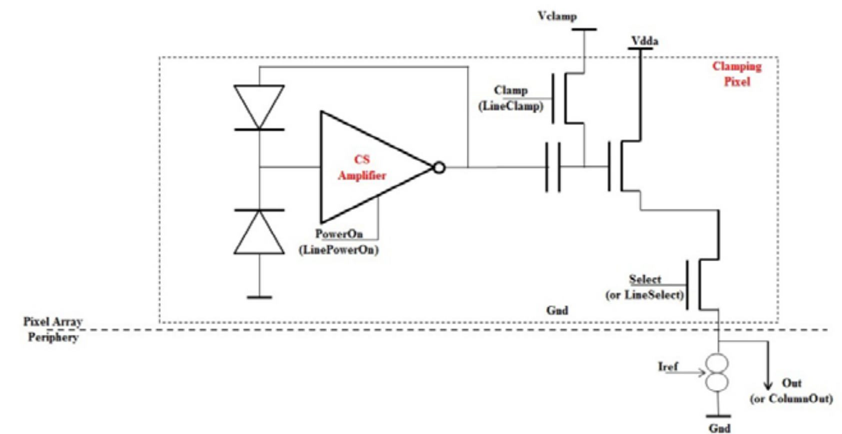
Wojciech.Dulinski@iphc.cnrs.fr

Mimosa32_VD: AIDA 3D integration test vehicles

Tower CIS, February 2014 submission: 6 Metals, MiM Capacitor, Quadruple Wells, HR epi, ARC

NMOS and PMOS based ampli structures



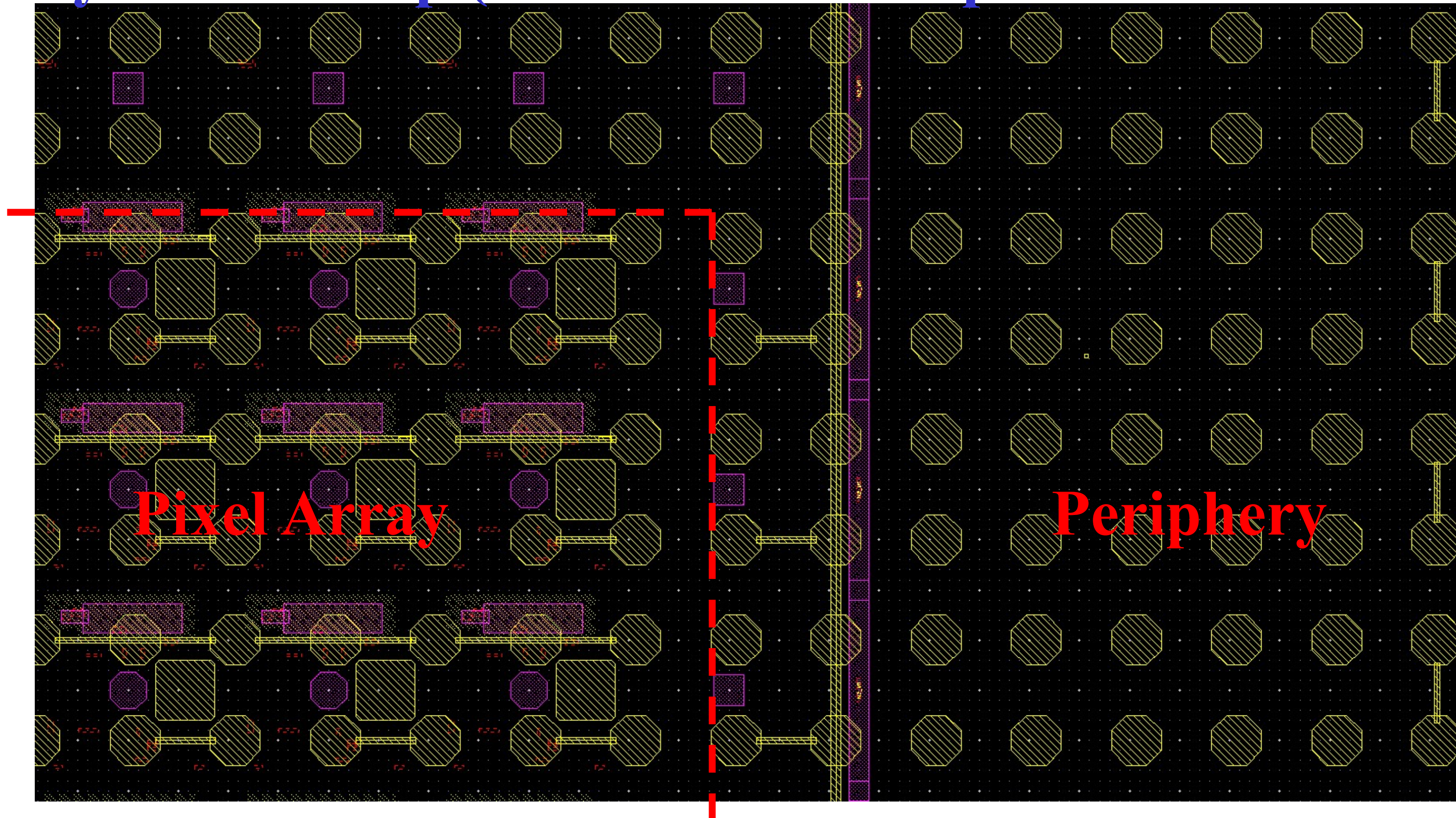


In-pixel circuit (20 µm pitch)

Wojciech.Dulinski@iphc.cnrs.fr

Specific structure to test 3D interconnection quality:

top metal “daisy chain” between tiers, 4 vias/pixel → 10 μm pitch, vicinity of MIM cap (standard DRC separation from bonding pads)

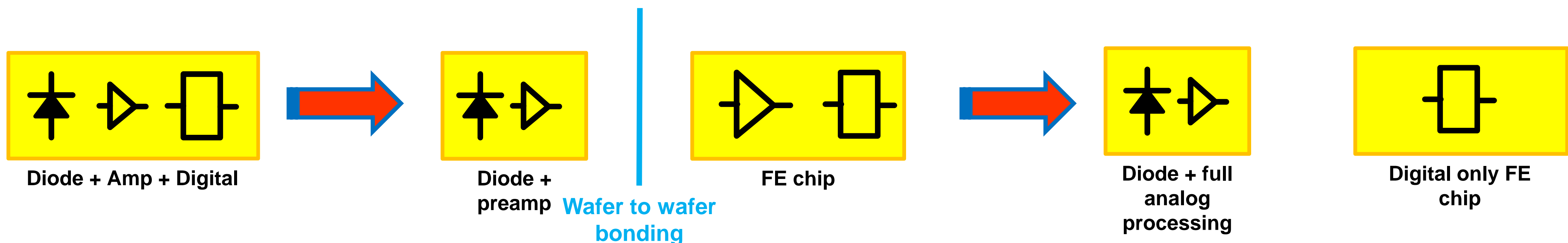


Wafers fabricated, processing at IMS started, results by the end of this year!

Wojciech.Dulinski@iphc.cnrs.fr

Conclusions

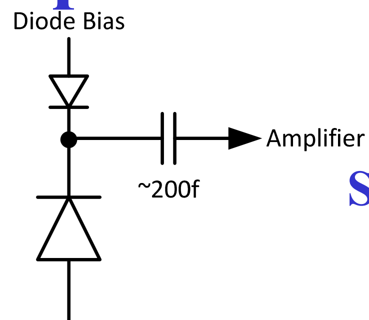
- To take full profit from monolithic sensors promises, several post-processing steps are (usually) required.
- Unfortunately, this post-processing is often more complicated and more expensive than CMOS wafers production…
- Keep it in mind from the beginning of the project, choose the best suited industrial offer which minimize the number of post-processing steps!
- Low-pitch, 3-D integration of just two heterogeneous wafers from different foundries may be a new interesting post-processing step, opening many applications. If demonstrated to be reliable and cost effective…



Possible evolution of CMOS sensors: from “standard” MAPS to “monolithic-hybrid”

Wojciech.Dulinski@iphc.cnrs.fr

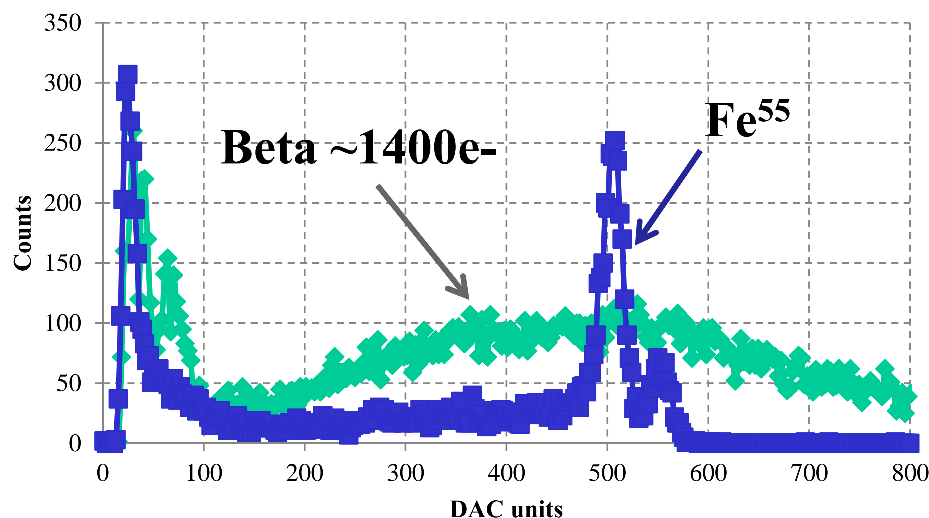
Appendix 1
PEGASUS (Strasbourg-Bonn) sensor: tentative of full substrate depletion using standard CMOS (TOWER CIS)



Solution based on AC-coupled diode (MIM cap)*

***T .Hemperek, Bonn**

- First results: ENC ~40 el, gain ~80 µV/e



- 1400 e^- -> substrate with 18um epi
- Single hit clusters

Wojciech.Dulinski@iphc.cnrs.fr

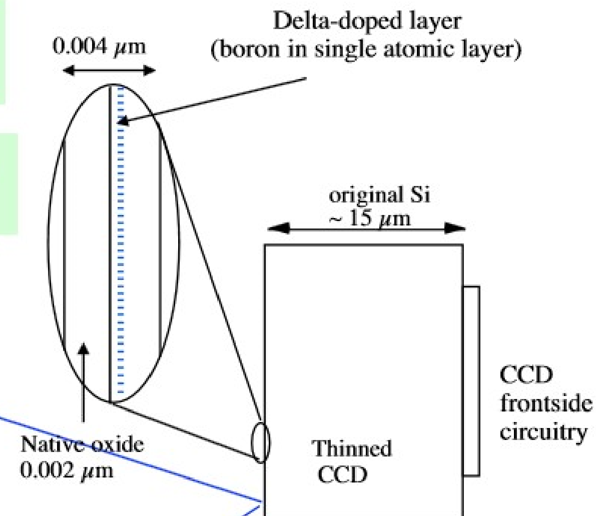
Appendix 2
Microdevices Laboratory (JPL) offer

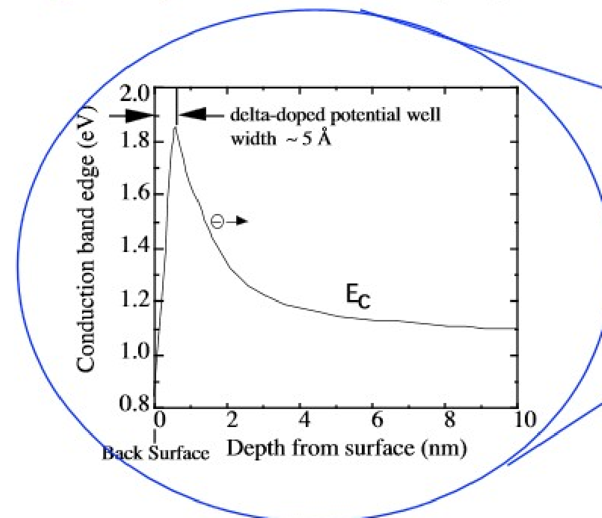
Delta doping technology as the ideal BI solution

Bandstructure engineering for optimum performance
Atomic layer control over device structure

Low temperature process, compatible with VLSI, fully fabricated devices (CCDs, CMOS, PIN arrays)

Hoenk et al., *Applied Physics Letters*, **61**: 1084 (1992)





Fully-processed devices are modified using Molecular Beam Epitaxy (MBE)

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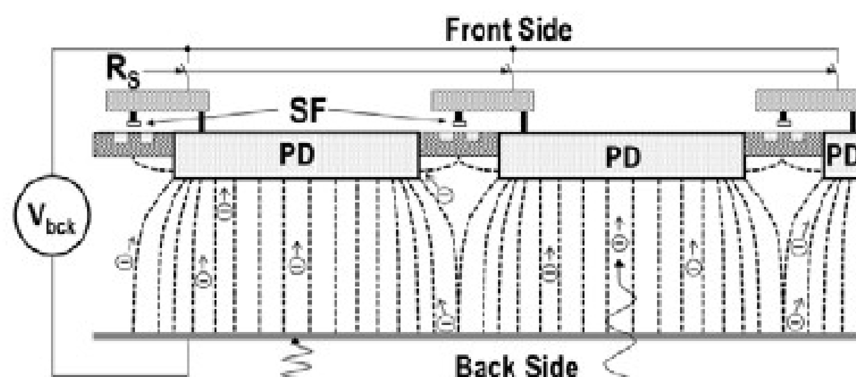
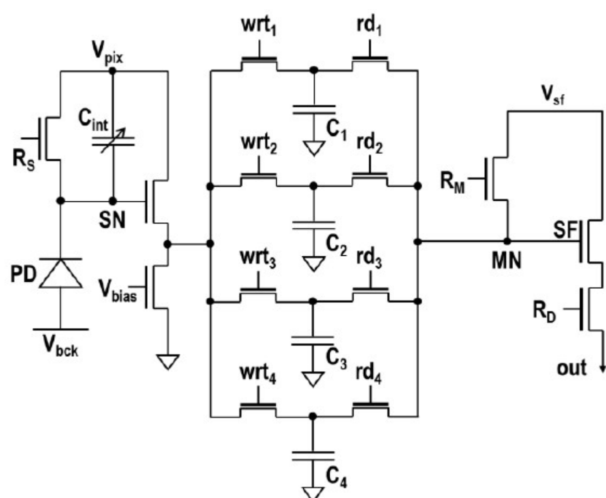
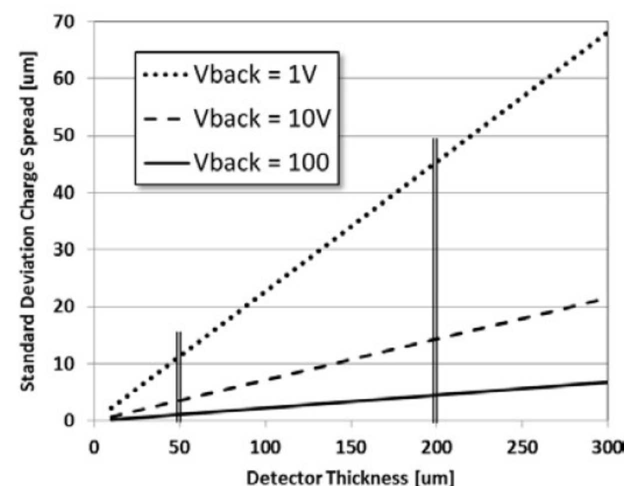
Appendix 3

Sensor Creation Inc. Fully Depleted, Backside Illuminated, 200 µm thick, 15 µm pitch VGA Resolution CMOS Imager



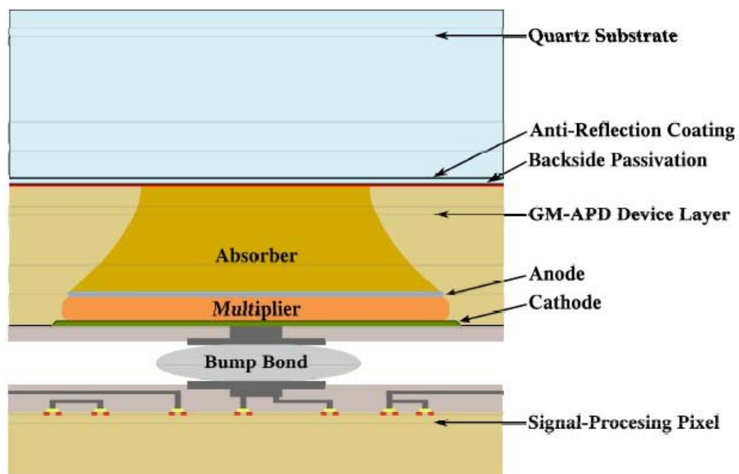


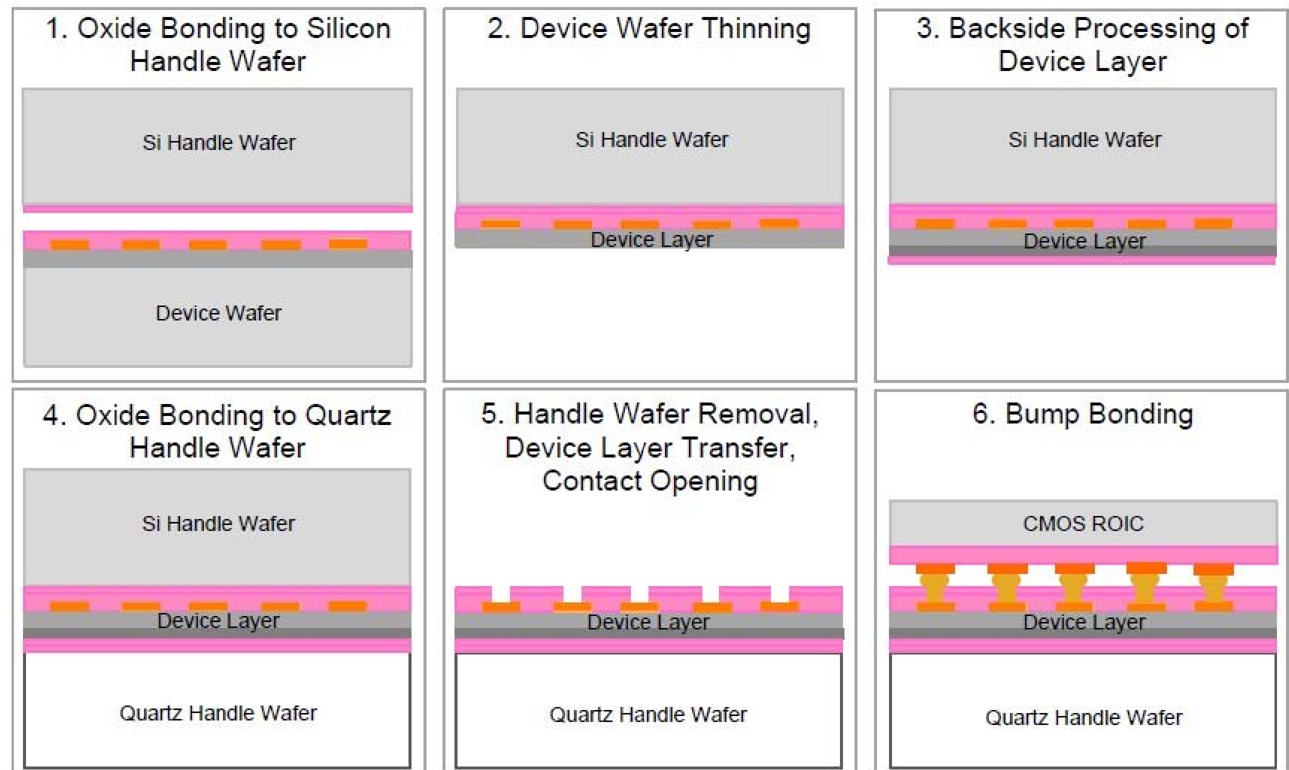


Wojciech.Dulinski@iphc.cnrs.fr

Appendix 4 (MIT)

“Back-illuminated silicon Geiger-mode avalanche photodiode arrays”





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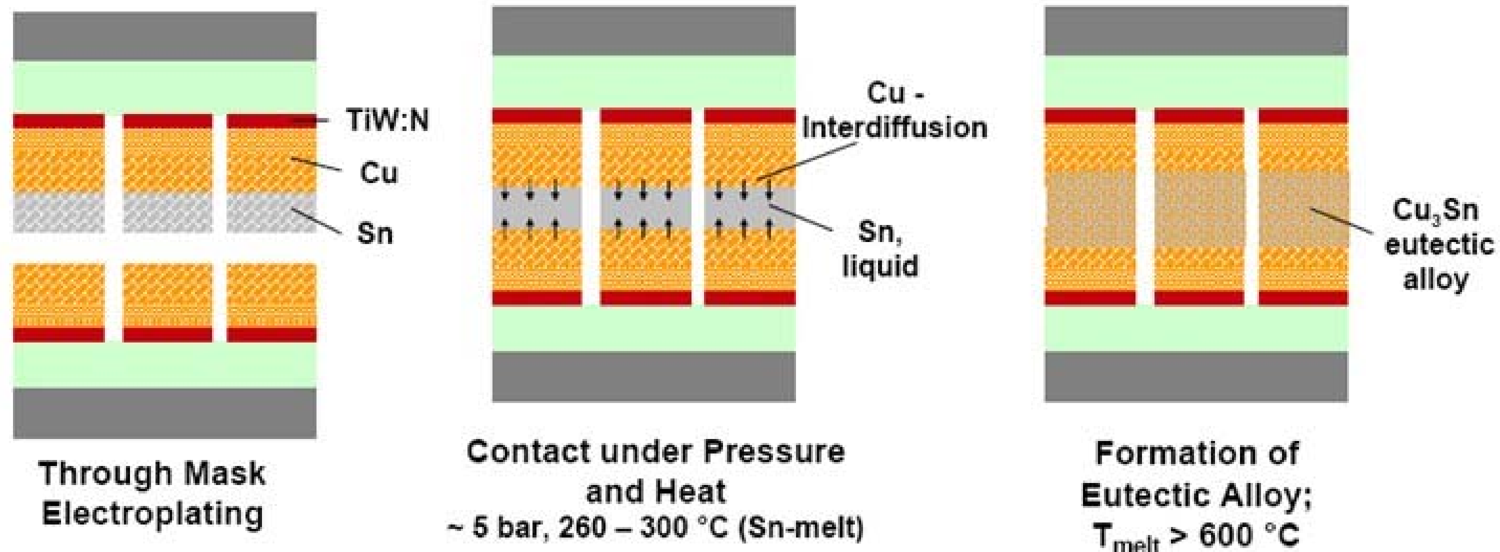
Appendix 5: 3D Integration using SLID process

Metallization SLID (Solid Liquid Interdiffusion)



- Alternative to bump bonding (less process steps "lower cost" (EMFT)).
- Small pitch possible (~ 20 µm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

***Credit to Anna Macchiola, MPI**