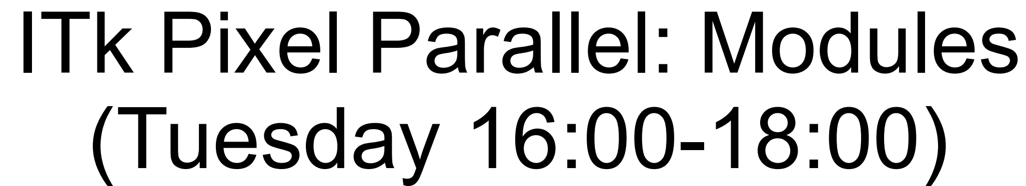
Impressions from the ITK week

LAPP ITK group meeting
02.03.2015

A. Rummler


ITk Pixel Parallel: Modules
(Tuesday 16:00-18:00)

lapp

RD53

Summary

- Several test chip fabricated at end of 2014 and now under test
- Report with design guidelines to radiation tolerance in preparation
- Progress on definition of I/O protocols. Will have a command and control protocol proposal for ITK week.
- Meeting with ATLAS and CMS sensor groups reached consensus that first bump-bondable prototype will have 50u x 50u bump pattern.
- 50u x 50u small test chip with “digital cores” in preparation for March/April submission
- Plan a first wafer-scale submission in 2016. This will cost 700K if it is an MLM run, to be shared among ATLAS and CMS. 12Mm x 12mm pixel matrix. If other projects are available could go for full run and get more area with the same cost. Would like to get feedback from sensor groups at April meeting.
- Next RD53 meeting will be April 23, 24 at CERN, during AUW.

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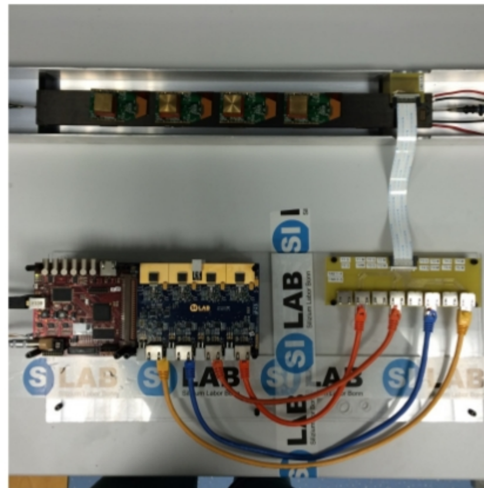
Serial Powering Test Stave Bonn and Göttingen

Serial power stave prototype

- Dummy modules (i.e. flex with resistive loads) loaded on one side of the stave
- Tested cooling, current distribution and electrical connectivity
  - Cooling done with a mix of water and ethanol works very well
  - One TAB not useable due to shorts or open lines
  - One TAB has one DO line open, can still readout two FEs



monitoring configuration

All ON | All OFF | Refresh readings

☑ turn off in reverse order ☑ no update during scan ☐ continuously refresh status

Item name	Status	Enabled?	Voltage (V)	Current (A)	Temp. (C)
SILAB25	DCS				
USB-regulators_209	OK	ALL OFF			
CH1	OK	OFF	0.003681	0.001196	19.0
CH2	OK	OFF	0.004353	0.001892	19.1
CH3	OK	OFF	0.003598	0.002487	19.0
CH4	OK	OFF	0.004982	0.002116	19.2

gonella@physik.uni-bonn.de

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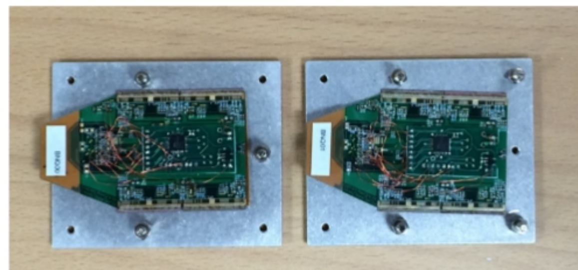
Quad flex modules

Quad modules for SP stave

universitätbonn

- Three quad modules available for stave prototype
  - BNQ00: digital module
  - BNQ01: pseudo quad, n-in-p sensor
  - BNQ02: pseudo quad, n-in-n sensor
- Two more modules are assembled this week

BNQ00 and BNQ01
pseudo flex and LBNL MUX PCB



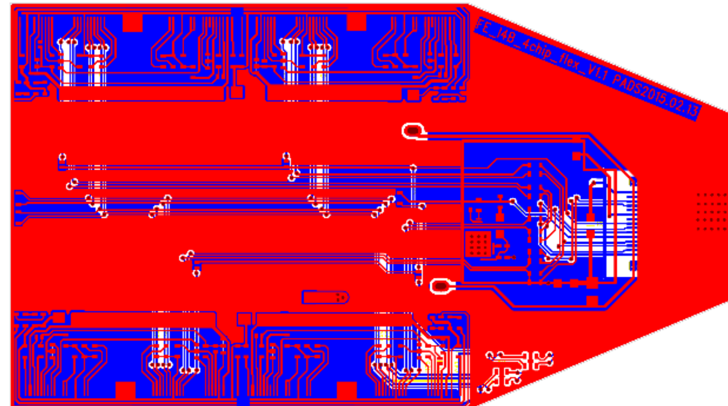
BNQ02
MUX-DCS flex

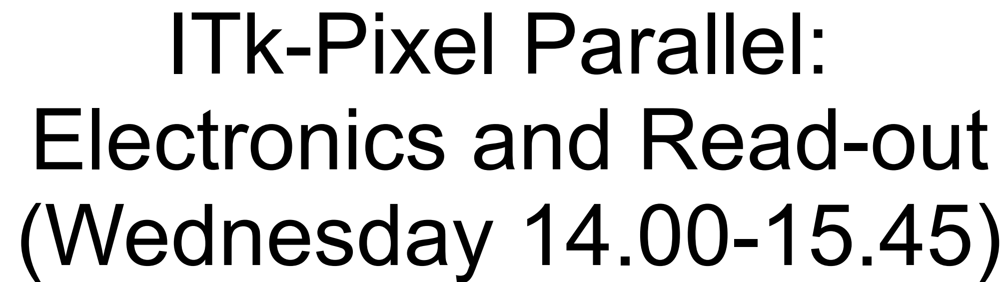
gonella@physik.uni-bonn.de

Flex modules in Siegen

Siegen Module Flex Activities

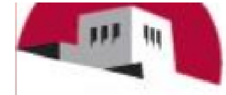
- Bonn Flex design of July 2013 converted into PADS format.
- Production of first X PCBs at QPrint as soon as possible.
  → Is there any interest in these flexes?
- Assembly will be done by hand in Siegen.
- Design changes are welcome (e.g. board outline extension for better handling).
- Is a flex support structure needed?




ITk-Pixel Parallel:
Electronics and Read-out
(Wednesday 14.00-15.45)

Stave flex

Summary



- The flex cables are a realistic cable which meet the current specifications.
  Irradiation Level requirement: $2x10^{16}$ neq/cm^2
  -tested to $3x10^{16}$ 800MeV p/cm^2, $2x10^{16}$ n/cm^2, 500 Mrad Gamma

  Length: Long enough to bring the signals out of the Pixel volume
  -We have produced 0.875m cables with impedance variation ~ 4% and have good results with two of these cables attached together.

  Bandwidth: 5 to 6 Gbit/sec,
  -We have good results on two cables at 5 Gbit/sec

  Signals: 100 ohm differential pair produced with differential pair microstrip with reference plane design

  X_0 [%]: the designs presented have a calculated radiation length 0.02-0.015%

Neil McFadden, UNM

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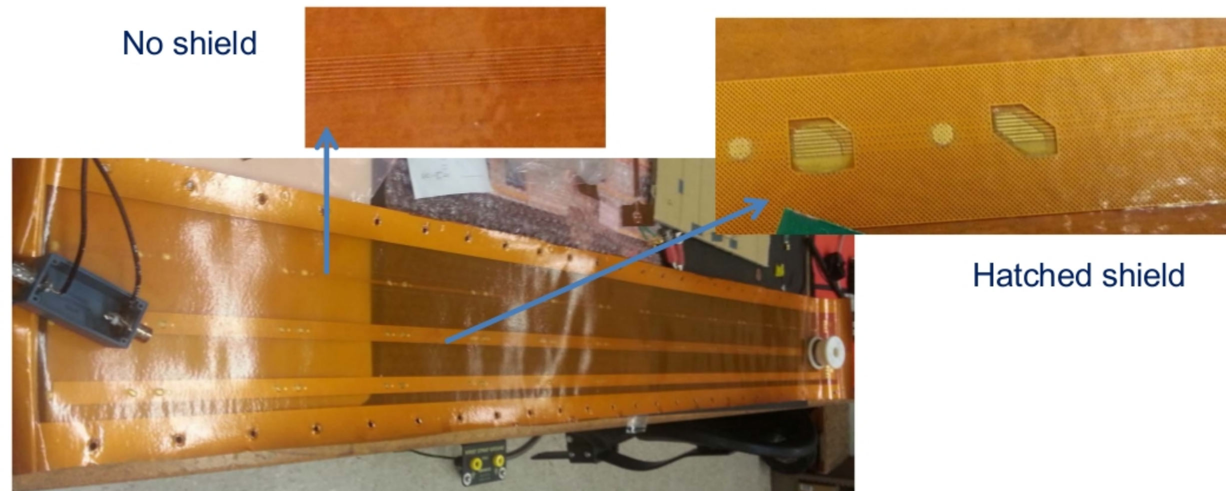
Stave flex Oxford

New Flex Tape

A new tape was made at Oxford for purposes of **strip** readout. It features wider trace pitch: 6 mill (150 um) track and gap. Length is 1.25 m.
This is clearly different from UNM cable: 225/500 um trace/gap with reduced GND width, 0.875 m long.
It also explores variations of the top-level shield: solid metal / hatch / no shield.



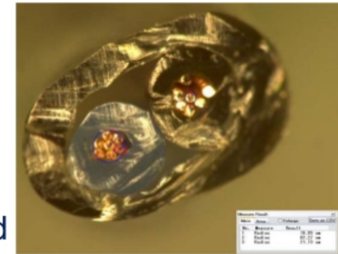
2015-02-25 Data transmission on TWP 11

Twinax

PEEK Cable

The new, pure-PEEK cable was delivered on Friday last week.
Measurement of dimensions:

Cable Type	R (single) [µm]	R (7x) [µm]	d (insul) [µm]	d (jacket) [µm]	Total R [µm]
As designed	25.1	63.5	165.1		482.6
PEEK-jacketed	32.1	88.6	194.2	188.3	



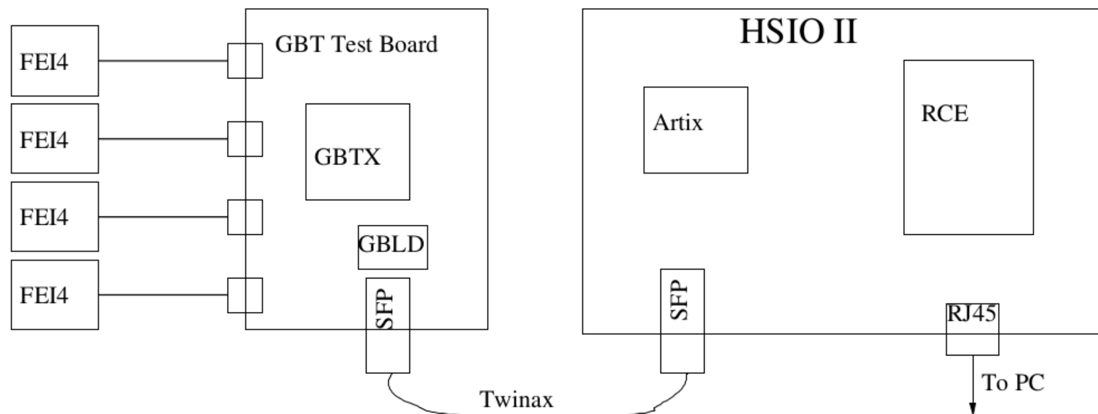
Will double-check the insulation thickness (somewhat lower than expected), then calculate X0.
Expect it to be similar to solid-core AWG 36 cable we tested earlier, i.e. < 0.01% at Z=0.

Cross-section with x200 magnification

Twinax and GBT test

GBT Tests

SLAC



- Use the HSIO II for readout (with the usual calibration software).
- Either use the CERN GBT test board or create a custom version of it to connect to FEI4 frontend chips.
- GBLD as driver either on test board or on SFP module (like Versatile Link).
- Already bought 20 GBTX chips from CERN (preproduction version).
- The number of FEs depends on the testboard capabilities (connectors, e-links). Probably some number between 4 and 16.
- The same setup can also be used with optical data transmission and for different readout/module studies.

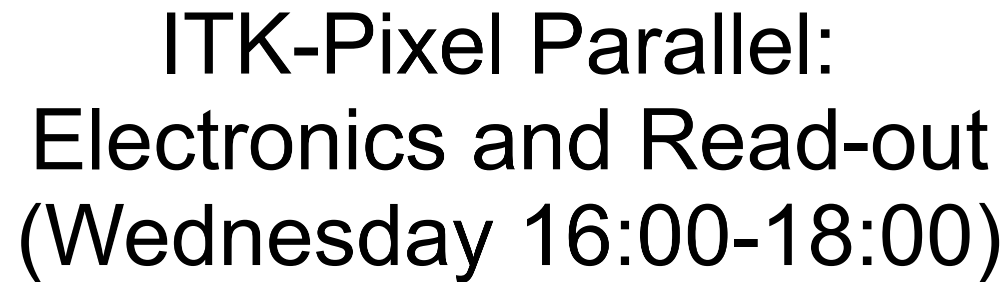
DCS/PSPP

Next Prototype planned (PSPPv2)

- Improved version of PSPP
- Same or similar components
- Smaller footprint
    - Only one shunt
    - Less IO pads
    - Maybe another ADC
- Bond-compatible if possible
- ETS May '15

- Further tests with the current chip are also planned

If you are interested in a sample of PSPPv2, please contact Susanne or me!
kersten@uni-wuppertal.de
puellen@uni-wuppertal.de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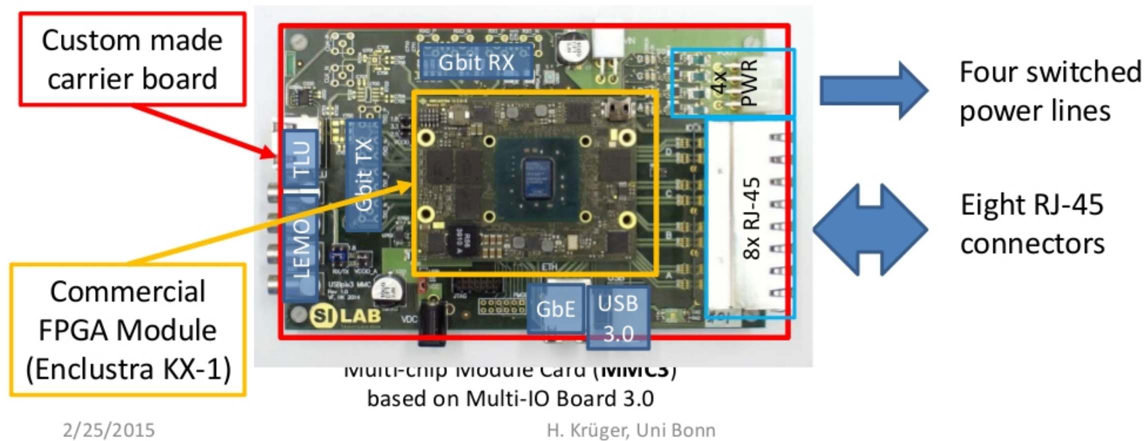
USBpix3

Alternative USBpix3 Hardware for Multi-chip Modules/Stave Tests

MIO3 card with **integrated multi chip support → MMC3**

- Same connectivity as MIO3 (including MGT for future RD53 chips)
- KEL connector replaced with eight RJ-45 connectors (optional ac-coupling)
- Additional four power channels (power switch + current sense/limit)
- Direct connection of up to 4, 8, or more FE-I4 modules (depending on CLK and CMD line sharing)



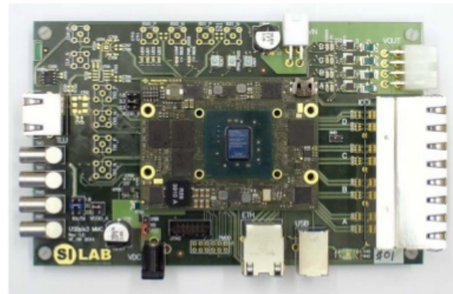
based on Multi-IO Board 3.0

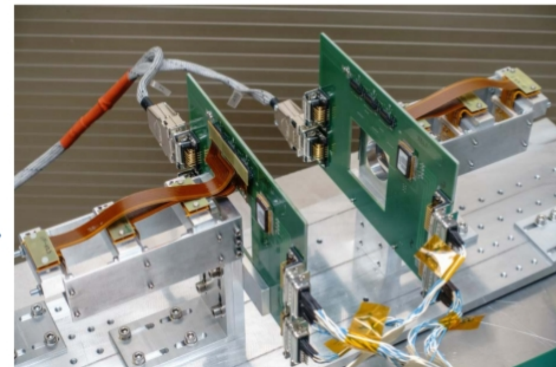
USBpix3

Max. bandwidth determined by computer port: 200 MB/s USB3 or 100 MB/s UDP (Ethernet)

MMC3 Use Cases

- Stave testing (LVDS lines can be ac-coupled to allow for serial powering)
  - Four Quad modules (16 FE chips)
    - Two RJ-45 connectors per module → CMD, CLK, 4x DATA, no multiplexing required
  - Eight Quad modules (32 FE chips)
    - One RJ-45 connectors per module → CMD, CLK, 1x DATA, with data multiplexing on module
- Combined Telescope and DUT R/O
  - Eight channels → for example six FE-I4 planes + two FE-I4 based DUT
  - Example: AIDA SBM FE-I4 telescope (under investigation)





2/25/2015 H. Krüger, Uni Bonn

USBpix3

HW Status & Component Availability

- **GPAC**: new production ready, 30 pcs. available immediately
- **MIO3 and MMC3**: prototype tested → production to be started

- **GPAC** (850€), **MIO3**, and **MMC3** (price tbd.) will be distributed by Bonn via CERN TID or invoice (contact Fabian)

Oral estimation: >~800€ for MMC3

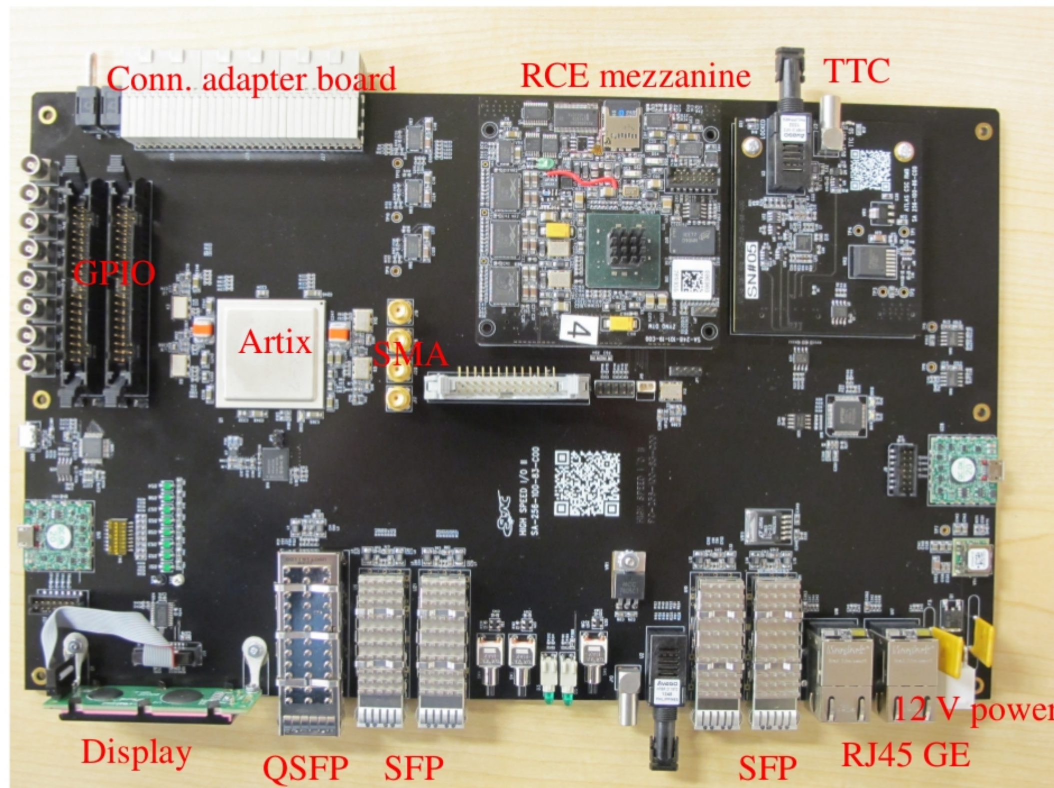
- New boards available ~Mar 2015

- Only very few **BIC** left
- No more FE-I4 adapter cards
- No more **MIO** boards

- Please contact Fabian or me to indicate your interest in
  - MIO3 boards
  - MMC3 boards
  - GPAC boards

LAPP has interest in 1-2 systems, will tell them

HSIO-II

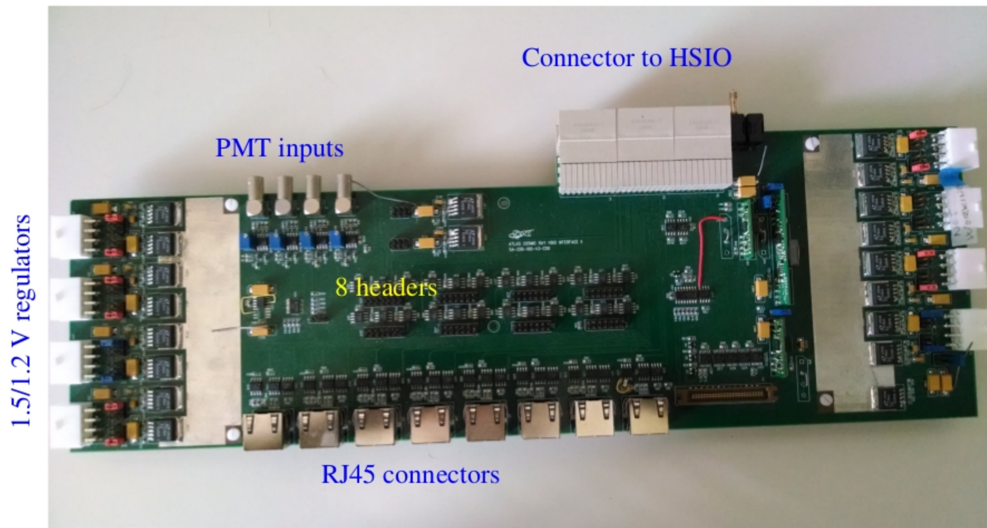


HSIO-II

Adapter boards

SLAC

- The HSIO II is compatible with the old adapter boards.
- We are currently revising the most common (“Cosmic”) adapter board.
- 18 RJ45 interfaces instead of the current 8 RJ45/8 headers.
- 4 PMT inputs for triggering.
- TLU interface.
- No more power connectors.



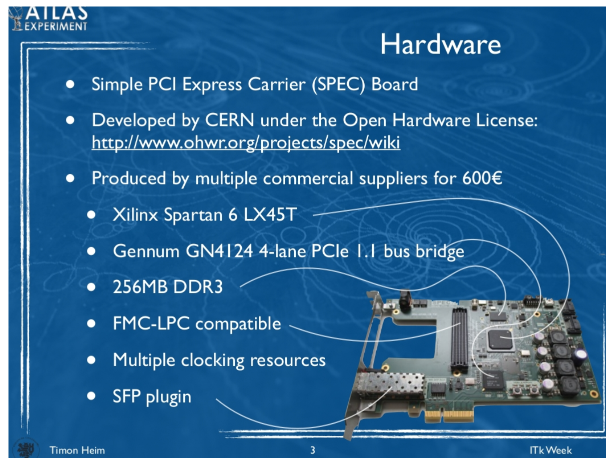
HSIO-II

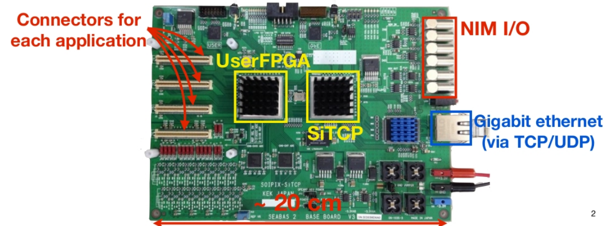
Hardware Availability

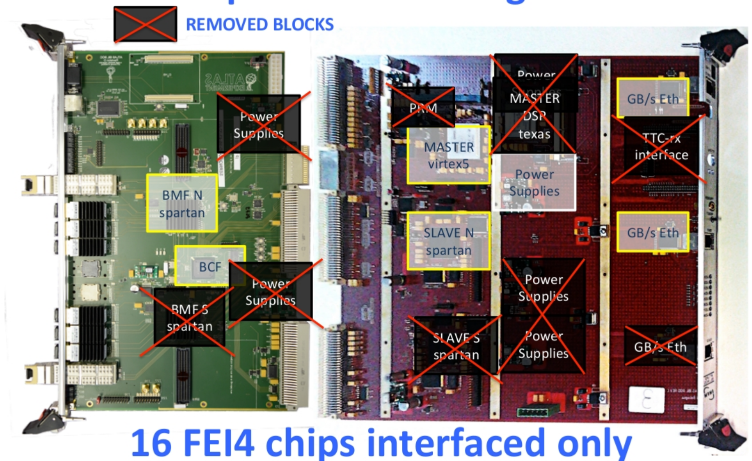
SLAC

- The hardware has settled enough that we are gathering cost info to release a call for shared production by the end of this week.
- The list of hardware on offer:
  1. The COB with DPM, DTM mezzanines, and SFP RTM. For more info check out `https://indico.cern.ch/event/359387` (RCE workshop at CERN).
  2. HSIO-II with RCE mezzanine.
  3. Pixel cosmic telescope interface.
  4. Strip stave test interface (unchanged previous design).
- Announcement will be made to the atlas-highlumi-RCE-development e-group.

…, YARR, SEABAS + another one to rule them all



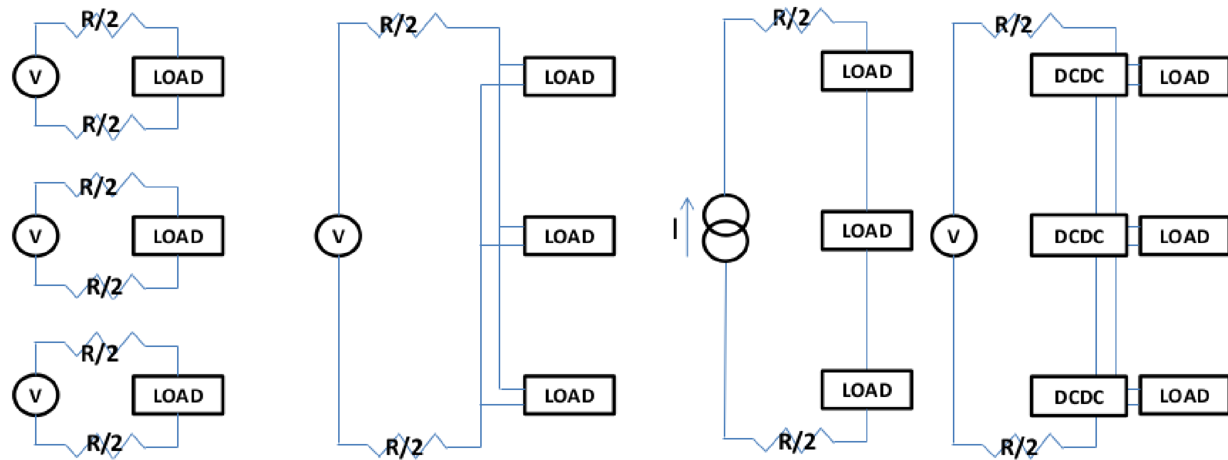




Misc

Strips powering schemes
No decision yet

Powering Schemes and Cables



Independent Powering | Parallel Powering | Serial Powering | DC-DC Powering

Losses in off-detector cabling of total resistance R for n loads drawing current I:

$P = nI^2R$ | $P = n^2I^2R$ | $P = I^2R$ | $P = n^2I^2R / r^2$

where ratio r = Vin/Vout

Serial Powering and DC-DC Point of Load conversion offer more efficient cable usage than Independent or Parallel Powering. *Total system efficiency will be lower as this depends upon the efficiencies of bulk supplies, DC-DC converters & shunts which are neglected here.*

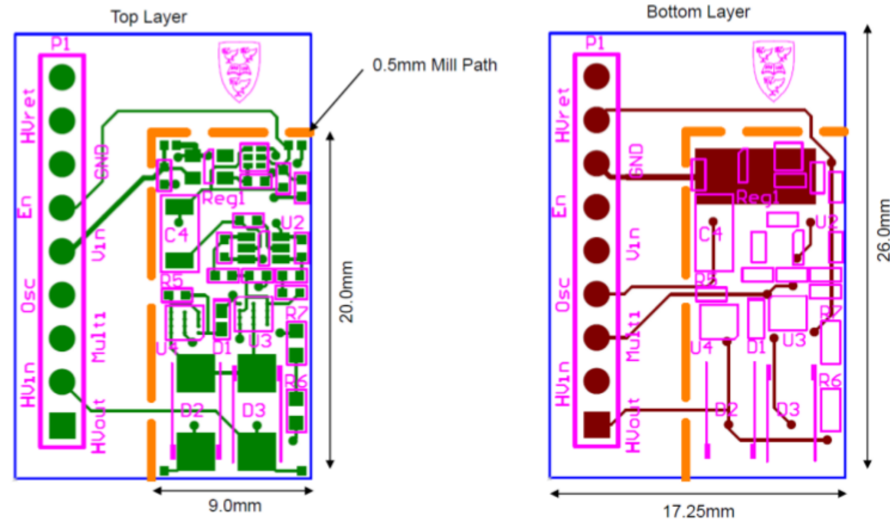
26/02/2015 Peter W Phillips, ITK Week, 02/15 2

Strips HV Switch/Monitoring

Stacked Circuit Development

ABC130 HV Switch Layout

- Circuit is 2 layer
  - HV separation adhered to, >1.0mm for 250V and >1.75mm for 500V
- Active switch circuit is 9 x 20mm, comes as 'snap-out' with tabs
  - Complete circuit dimensions are 17.25 x 26.0mm
- 0.1" 9-way header added for access to switch probe points etc.



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