Status report of the FATALIC project

Tile week upgrade session @ Cern

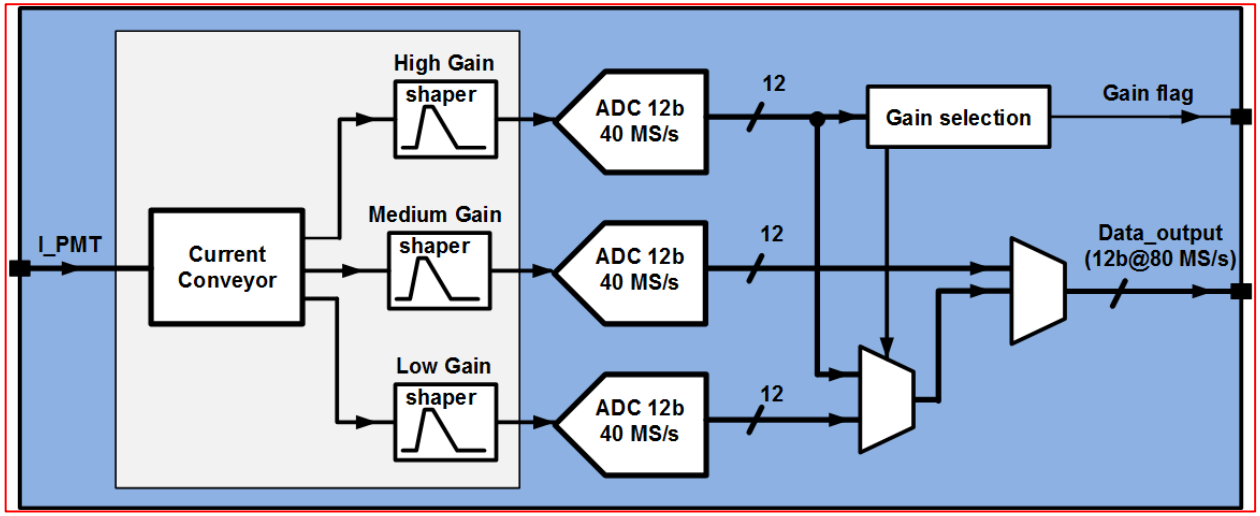
Laurent.Royer@clermont.in2p3.fr

Status report of the FATALIC project

- Status report of the test of FATALIC_4 chip
- Status report of the development and test of the main board prototype

The FATALIC chip

- FATALIC chip embedded in the "All-in-One" FE board

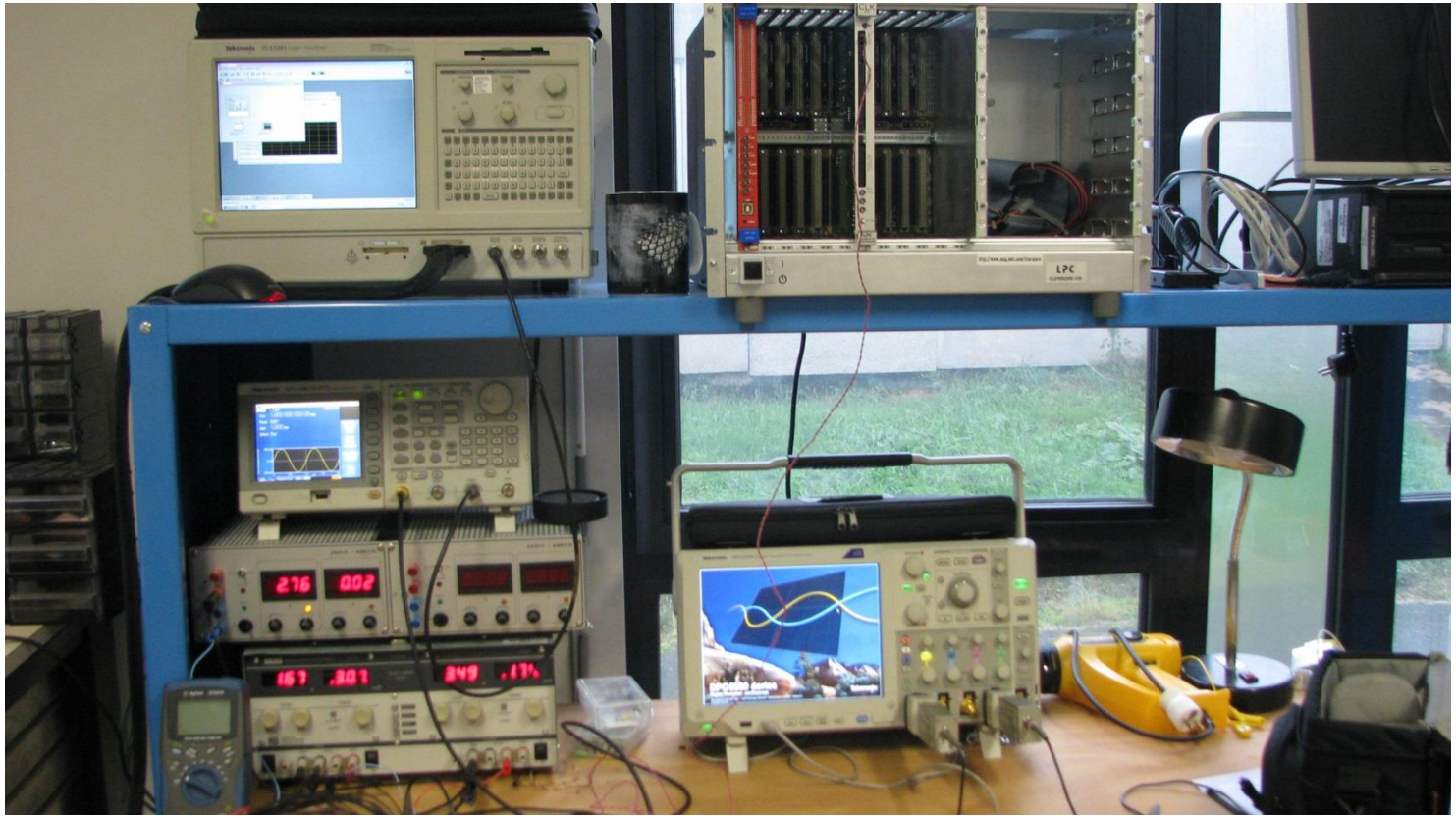


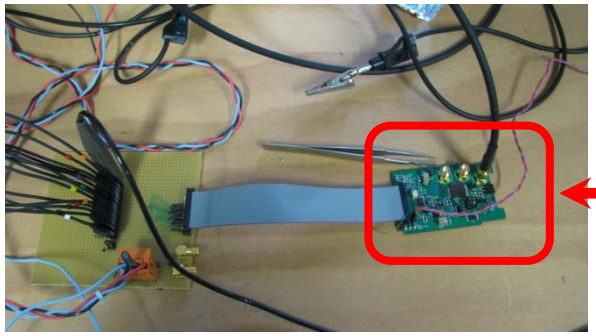
- Main characteristics of FATALIC:
  - A 3-gain PM-signal **analog processing** (current conveyor + 3 shapers)
  - 3 embedded **12-bit ADCs** (one per gain)
  - An **auto gain-selection**

    → either the **high-gain** data **or** the **low-gain** data are outputted (medium-gain data are always outputted)
  - A **12-bit data output bus** with the data of the 2-selected channels multiplexed

Extra items: independent analog core and ADC blocks implemented for test purpose

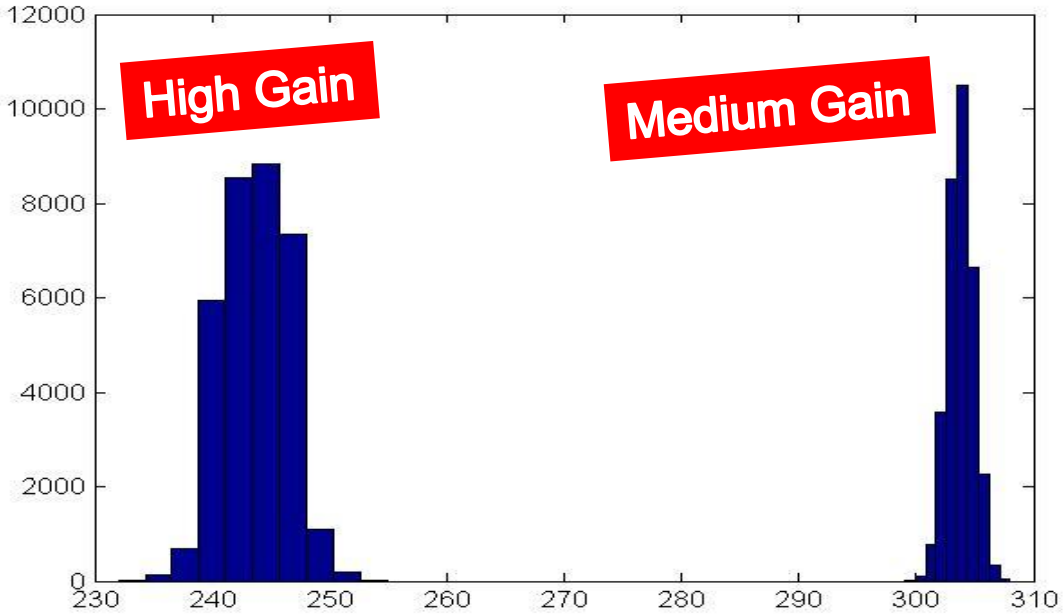
Test Bench of FATALIC





Device Under Test:
« All-in-One » with FATALIC

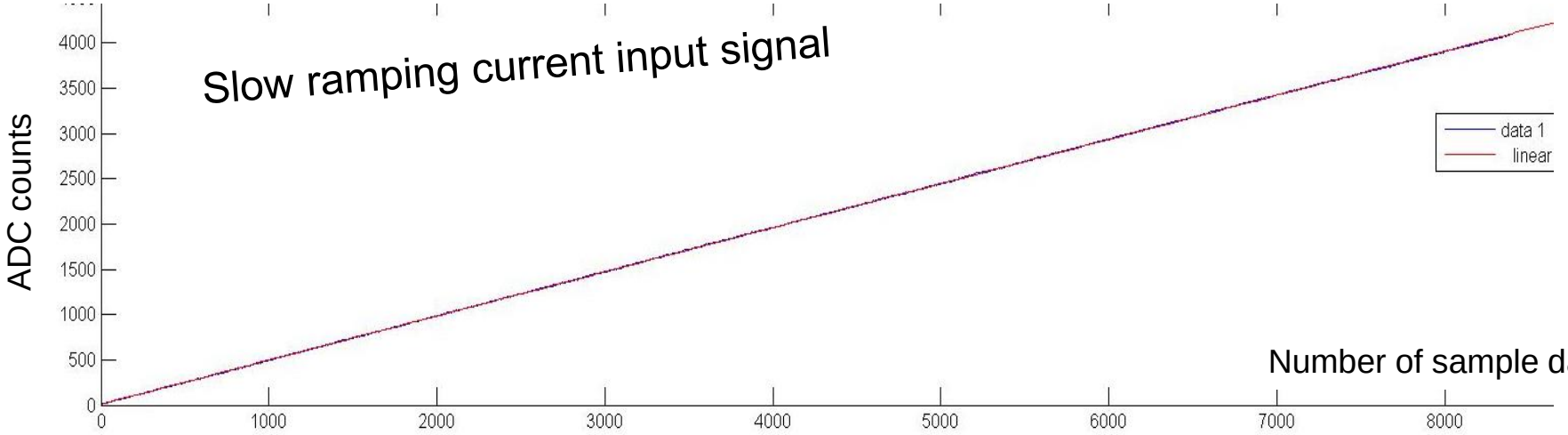
Measurement of the Noise

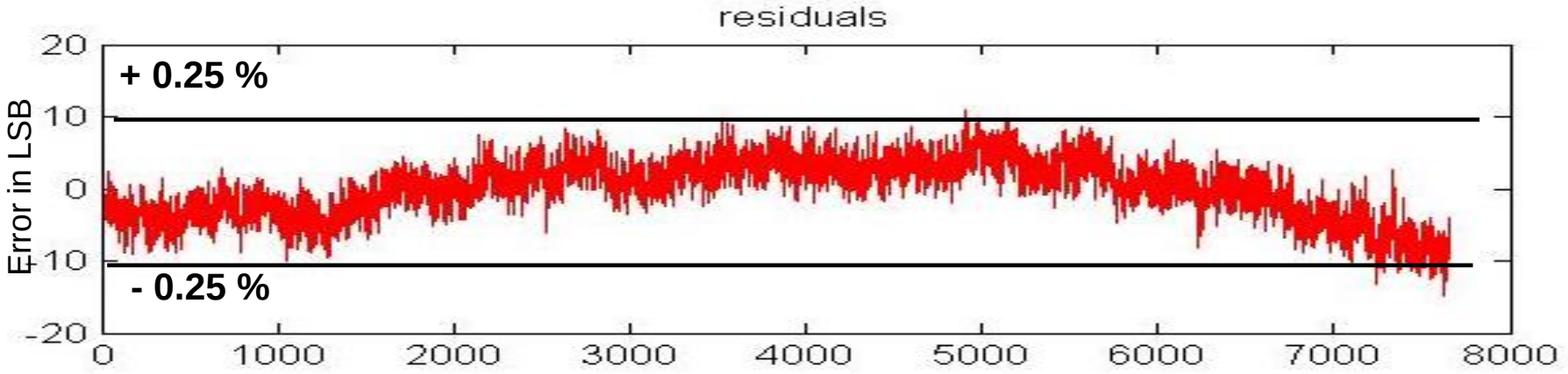


- Histograms of output code fluctuation (no input signal):
  - Medium Gain : Std Deviation = 1.23 LSB → 42 fC rms
  - High Gain : Std Deviation = 2.74 LSB → **9.4fC rms**

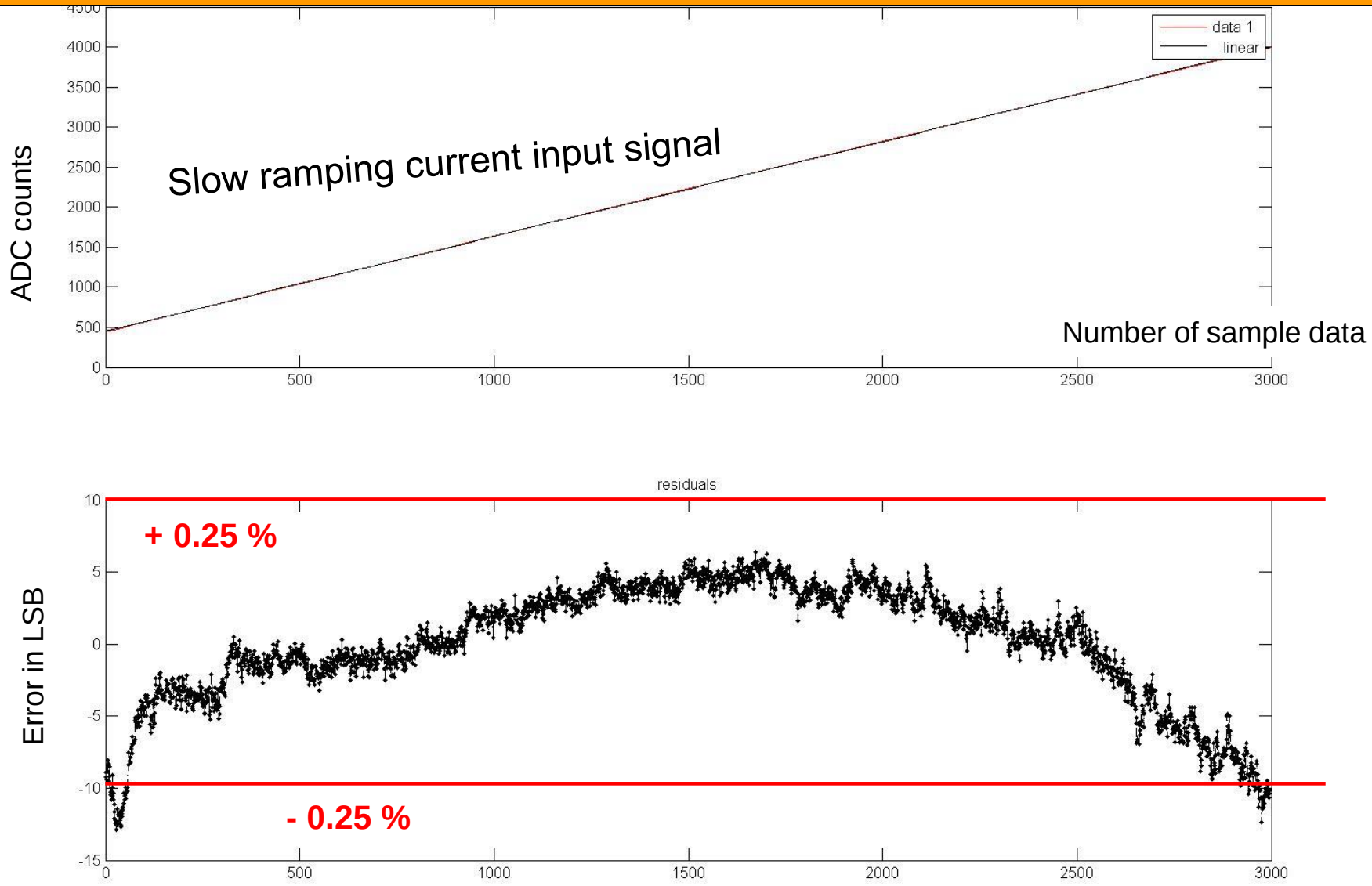
" Noise Requirement: the smallest signal of interest from the detector, expressed in terms of **equivalent input charge** delivered to the front end electronics, is **24 fC**. The intrinsic noise of the electronics, as measured through the digitization path, expressed in terms of equivalent input charge, shall not be greater than **12 fC rms** at pedestal. "

FATALIC: Linearity of the High-Gain channel

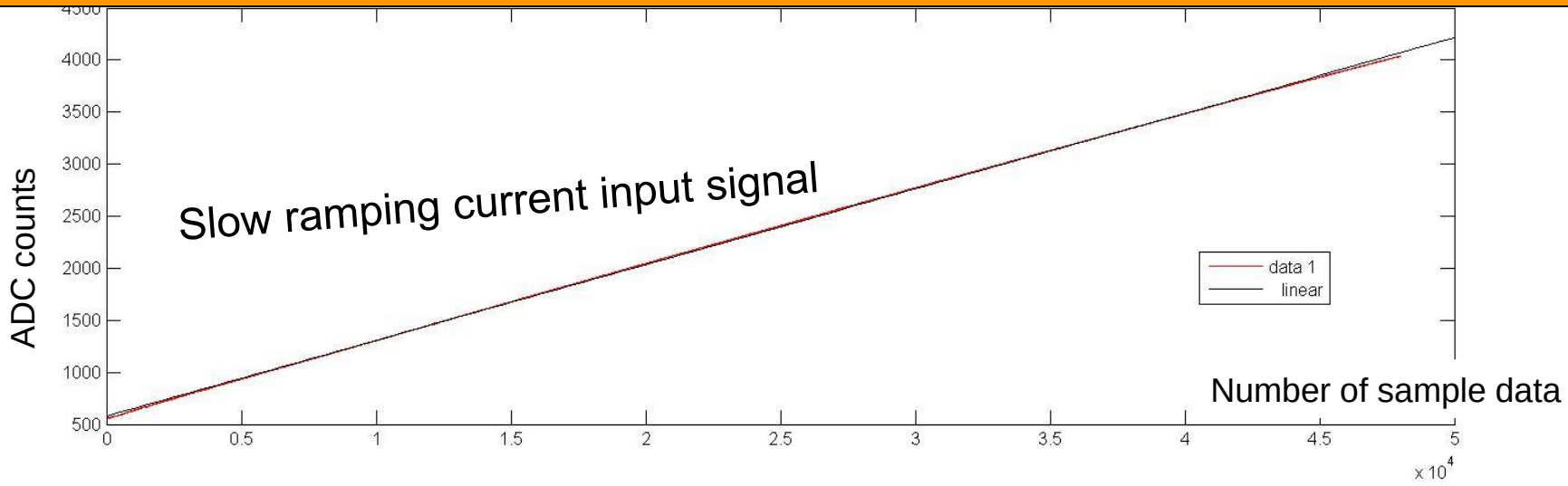


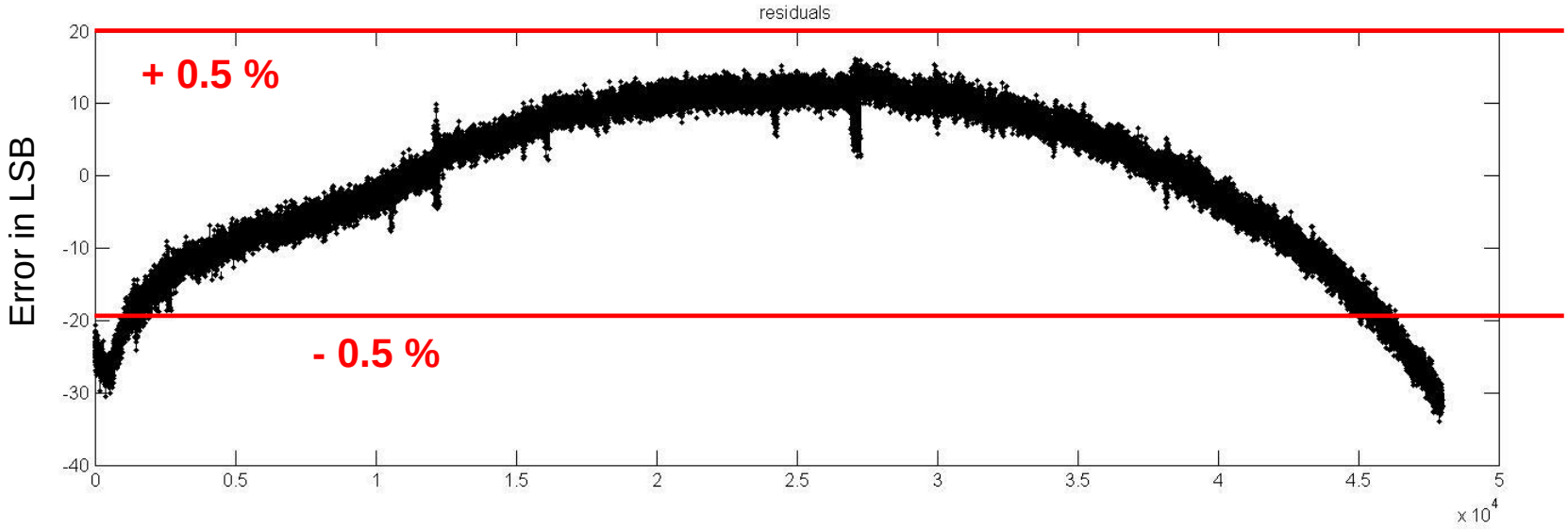


FATALIC: Linearity of the Medium-Gain channel



FATALIC: Linearity of the Low-Gain channel



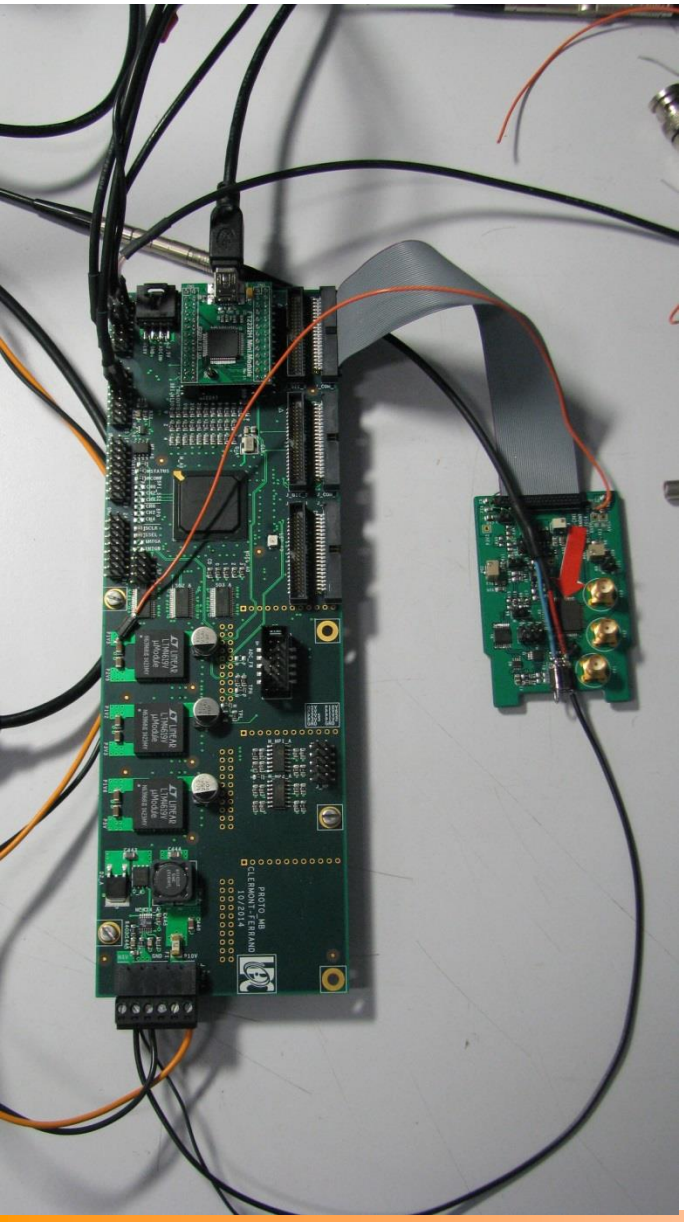


FATALIC: measured performance

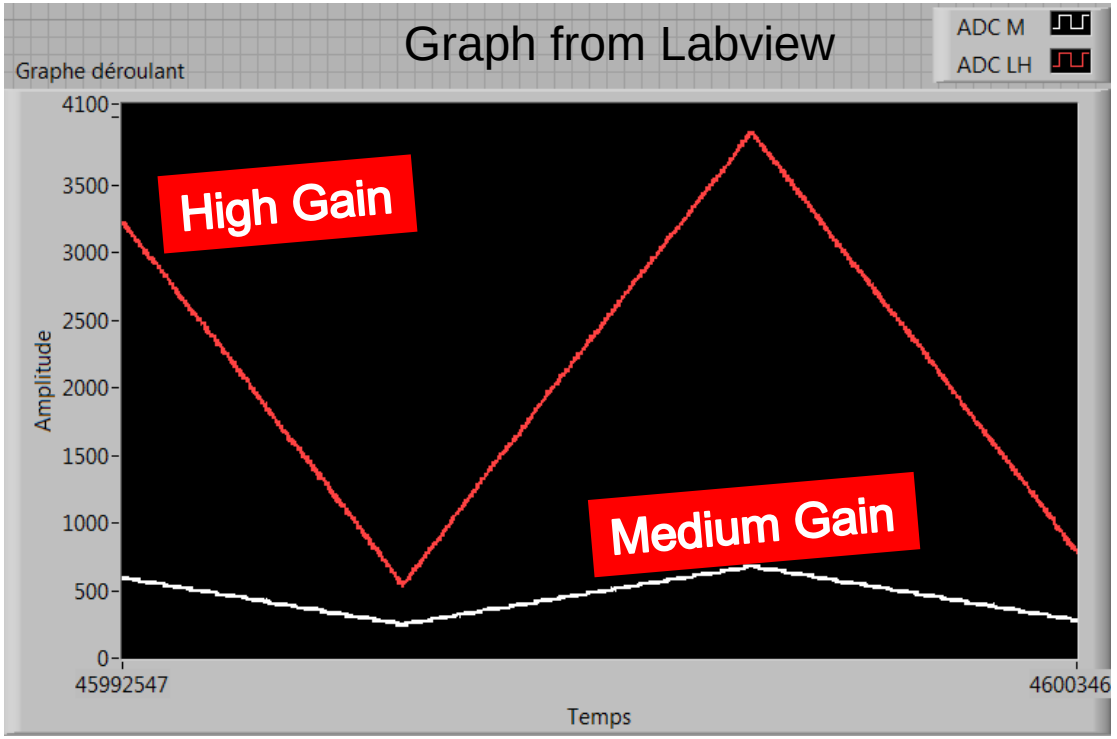
	High gain	Medium gain	Low gain
Power cons. (All-in-One)	208 mW @ 1.6V		
Dynamic range (pC)	To be measured	To be measured	To be measured
Noise (rms)	9.4 fC	42 fC	-
Non-Linearity	± 0.25 %	± 0.25 %	± 0.5 %

- ✓ Global functioning @ 40MHz with the All-in-One board (AinO)
- ✓ Power consumption
- ✓ Auto gain-selection
- ✓ Noise
- Dynamic range → to be checked
- ✓ Linearity → quality of measurement must be improved

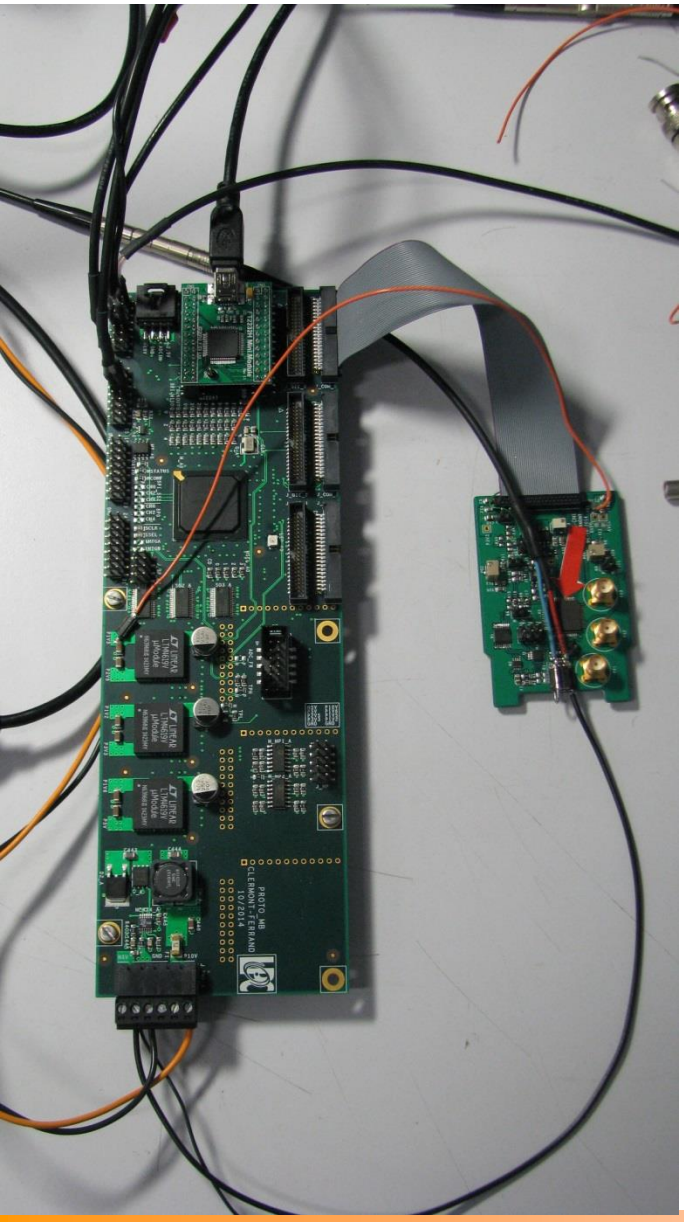
Status of the ¼ Main Board prototype (1/2)



- ✓ Data transfer: "All-in-One" → Main board → USB → Computer (Labview)
- ✓ Digital readout of the two relevant channels (auto switching from LG to HG)

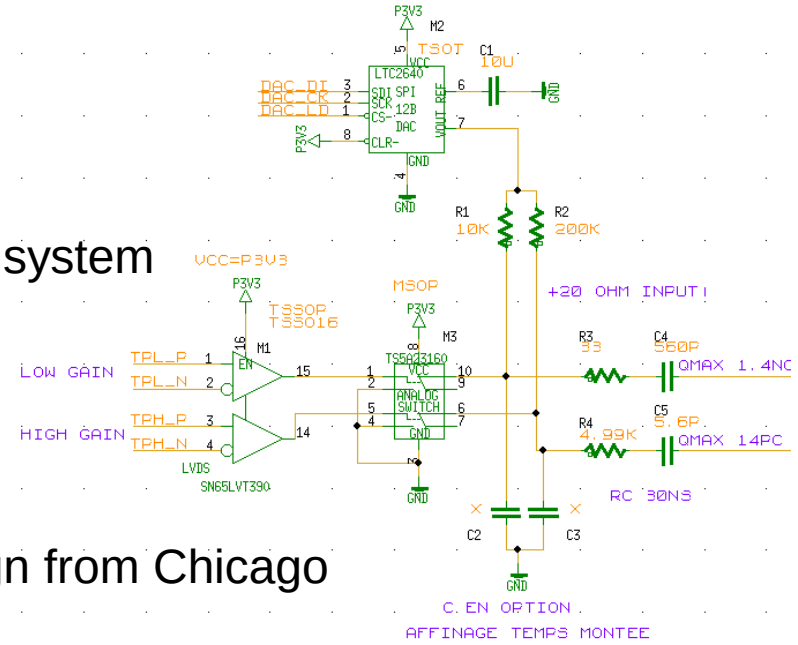


Status of the ¼ Main Board prototype (2/2)



- Calibration: control of the Injector from Computer (Labview) → USB → MB → to AinO
  - ✔ Set of the DAC value
  - ✔ Triggering of the switch
  - ✔ Synchronous triggering and data readout

Injector system



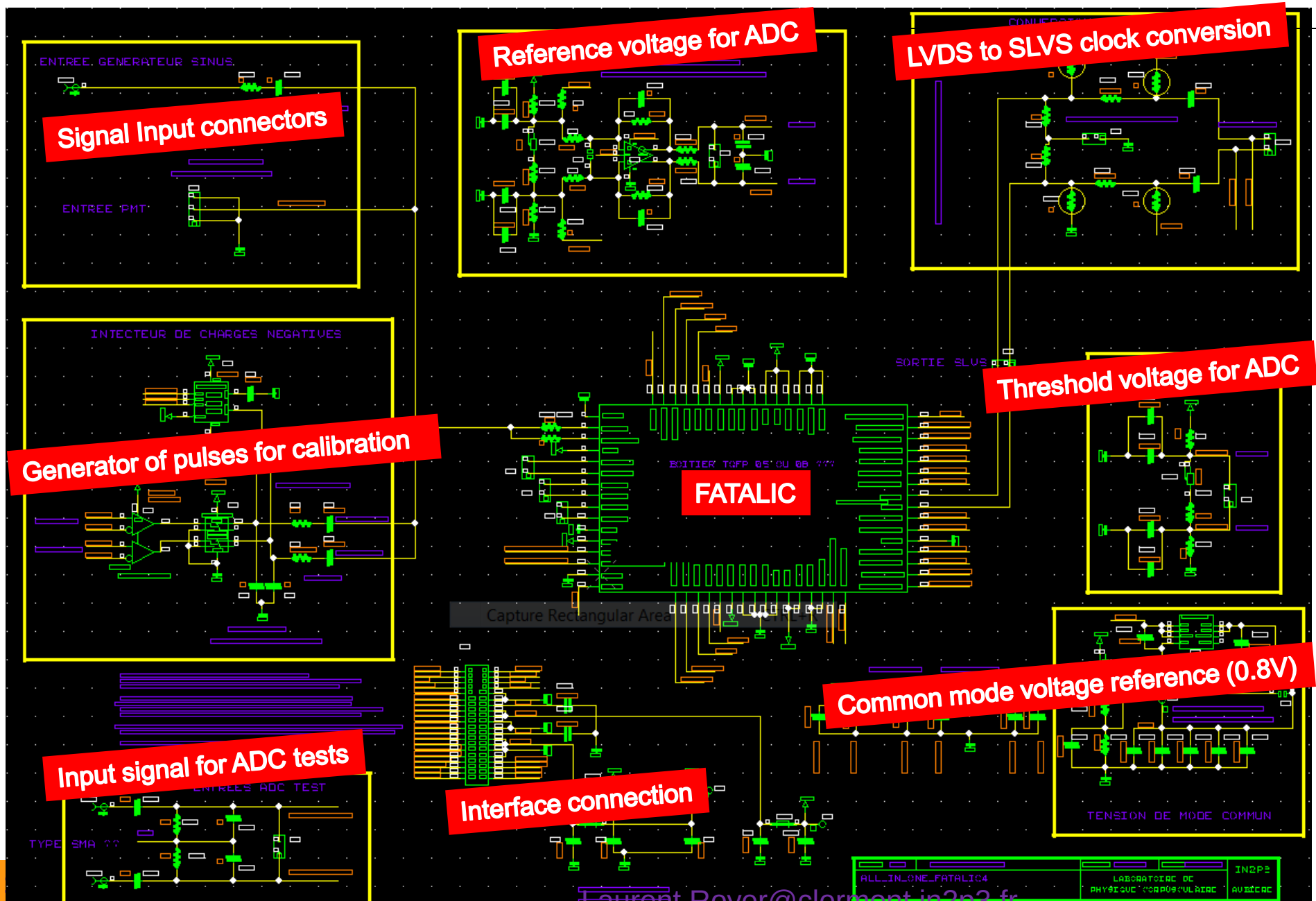
Design from Chicago

Next steps …

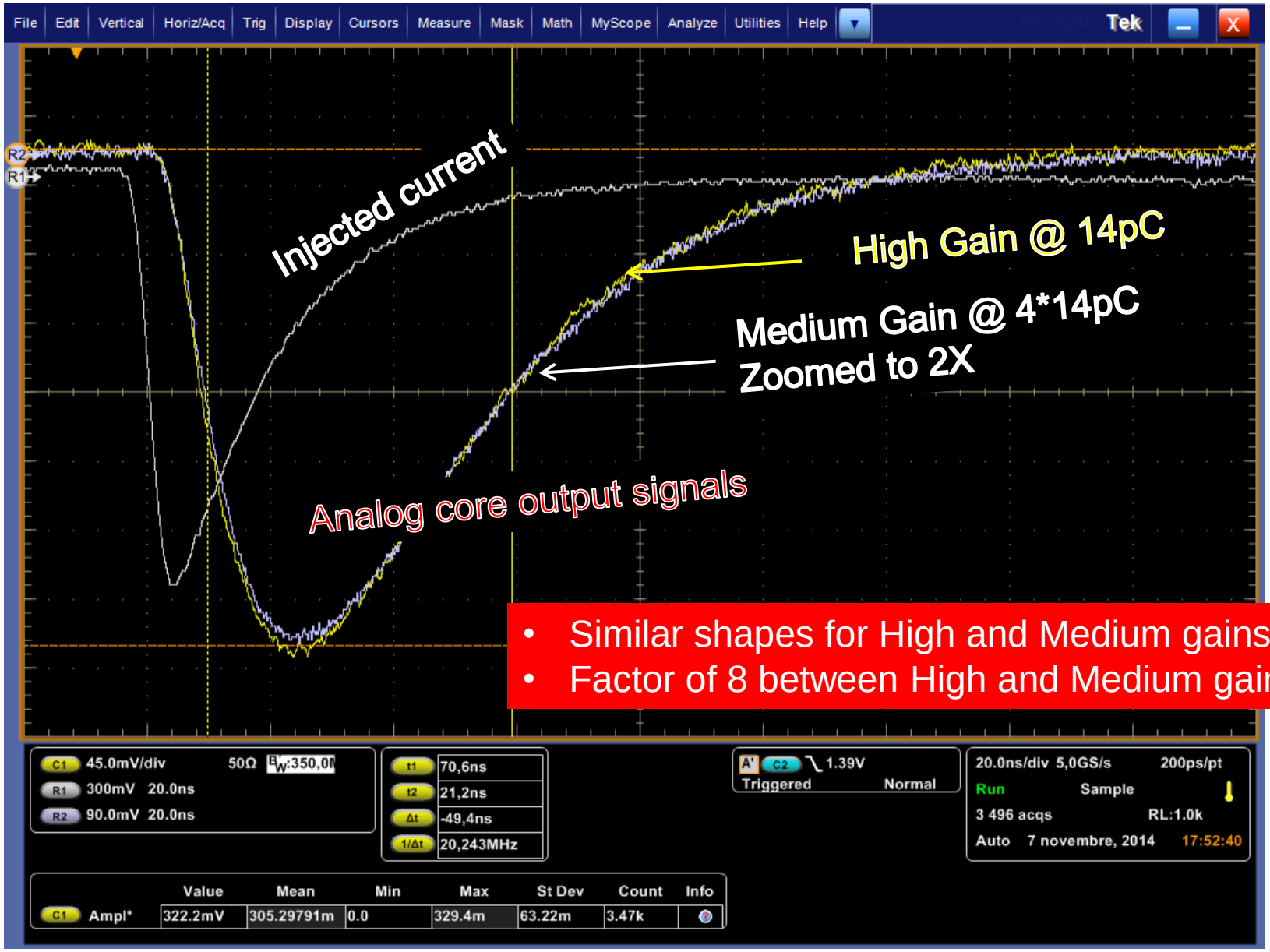
- The measurement of the linearity of FATALIC must be improved. The design of a new test board with a high-precision reference ADC is in progress. This reference ADC will help to calibrate the input signal.
- Measurements on All-in-One with the injector system will be carry out.
- In order to evaluate the behavior with pile-up, a test setup with a PMT block lighted with 3 LEDs will be ready at the end of February.
- The link between the Main Board and the Daughter Board @ ≥ 280Mbit/s will be tested thanks to a LPC's DAQ board in place of the DB.

Backup slides

FATALIC implemented on “All-in-One”

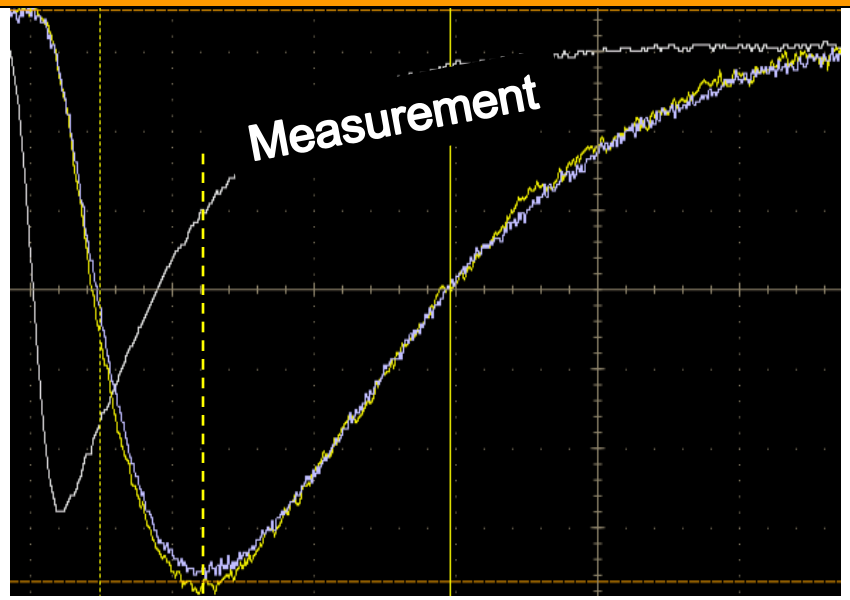


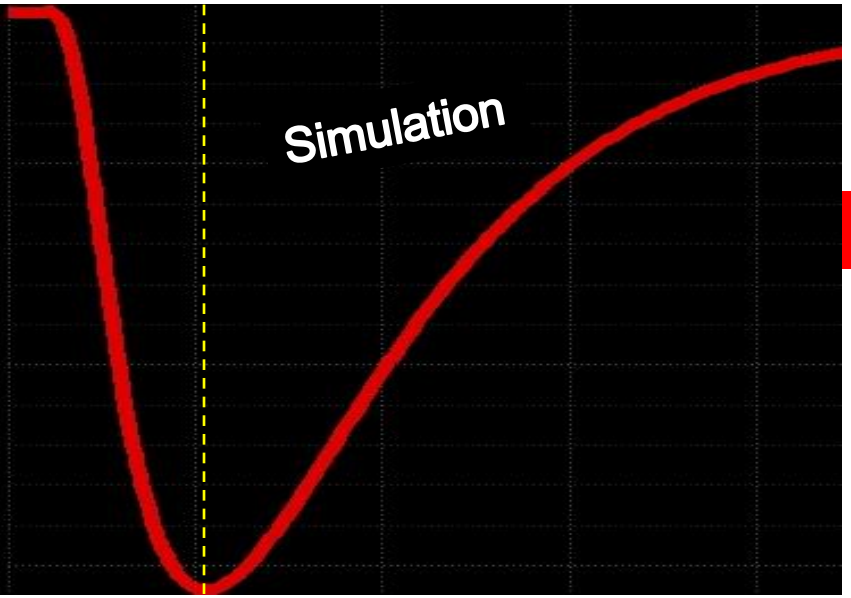
Analog Outputs



- Similar shapes for High and Medium gains
- Factor of 8 between High and Medium gains

Analog Outputs





Power cons. of Fatalic_4 (mA)		Peaking time (ns)		FWHM (ns)	
180	200 *	23*	≈ 25	43*	≈ 49

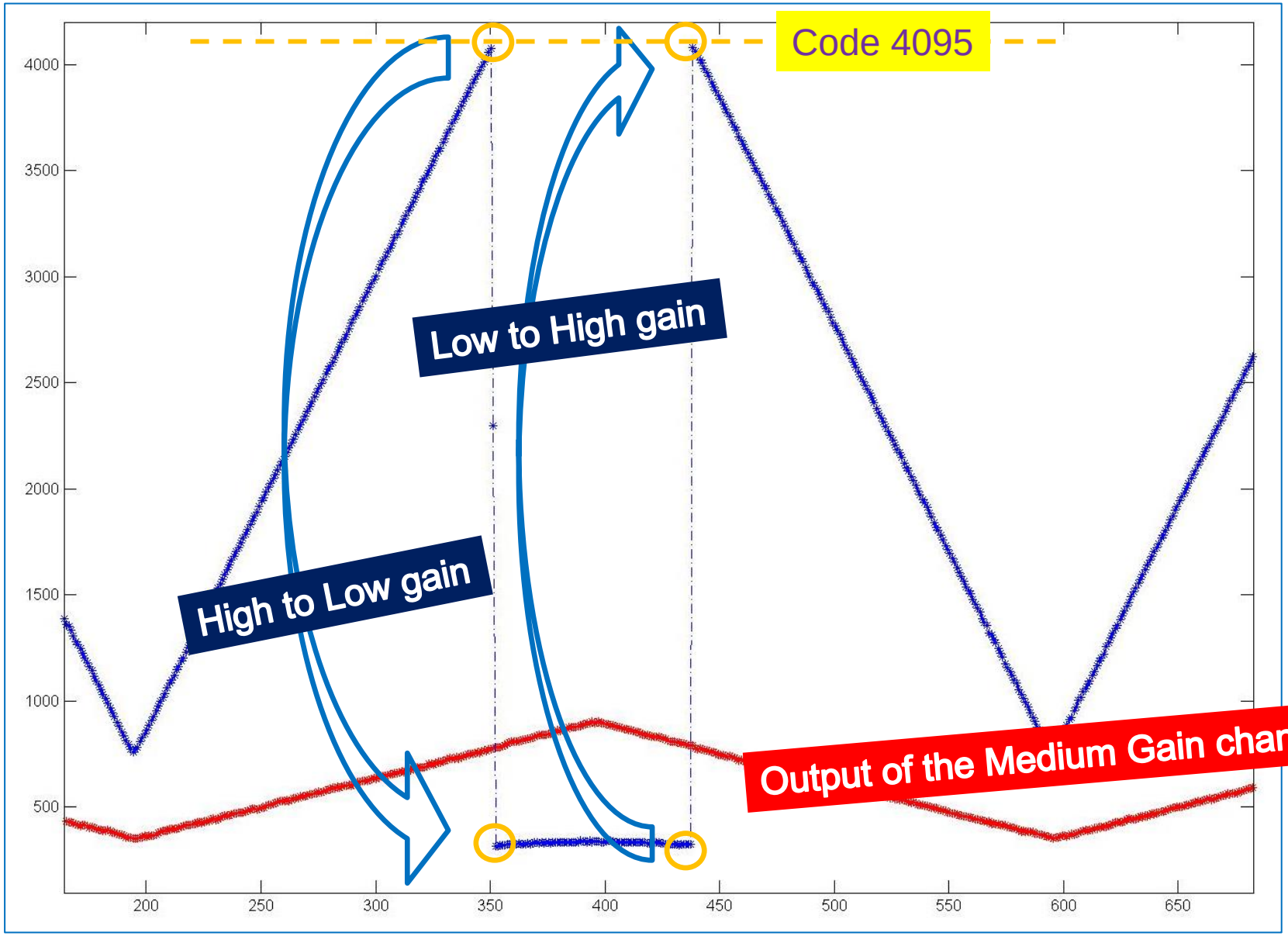
→ simulation

→ measurement

* Power consumption of the complete « all-in-one » board
* with a 4ns-rise-time and 36ns-falling-time current pulse

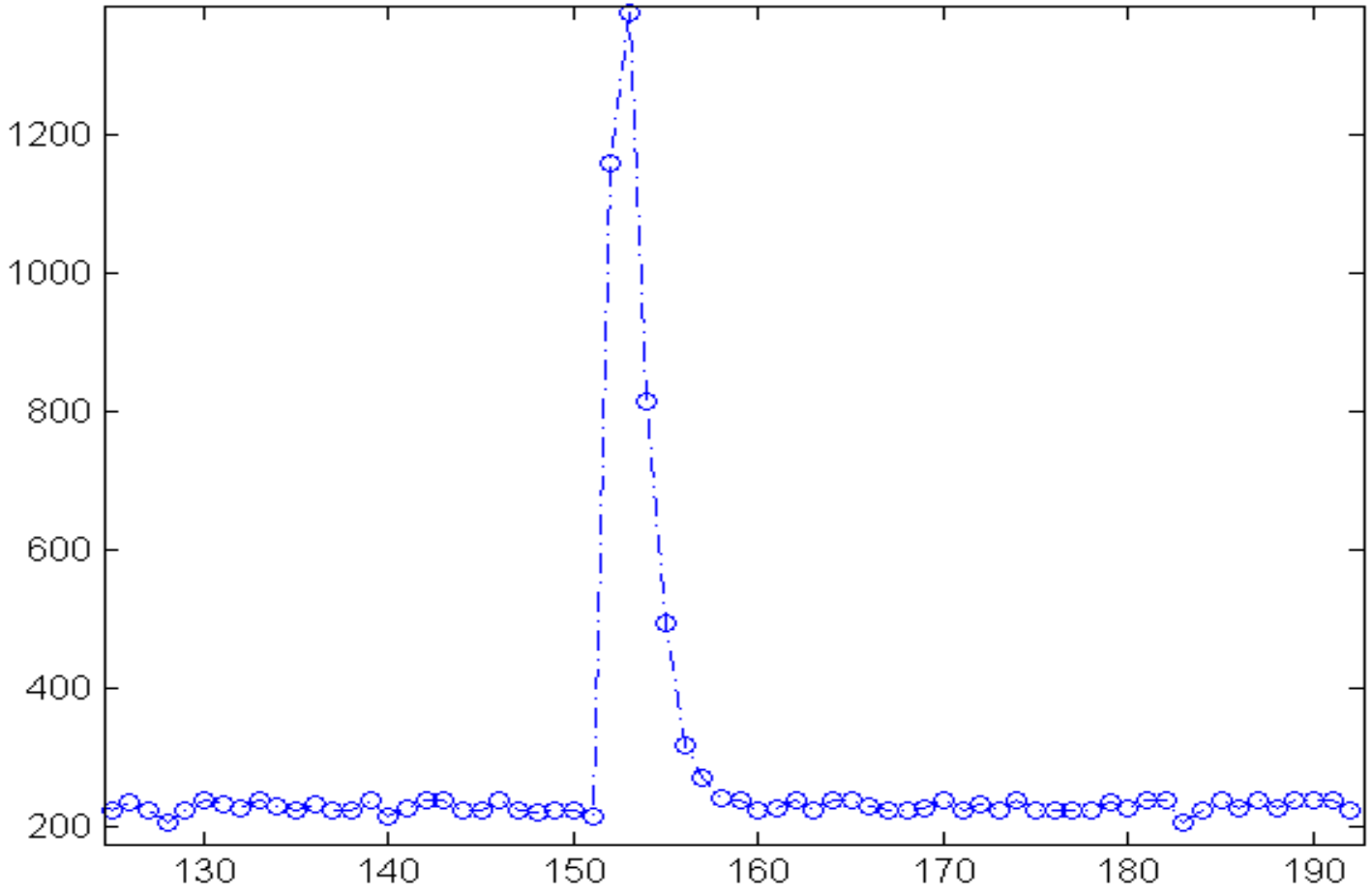
Similar shapes between test and simulation

Auto-Gain switching



PM-like input signal

Medium Gain:
"All-in-One" board response to a PM-like pulse signal



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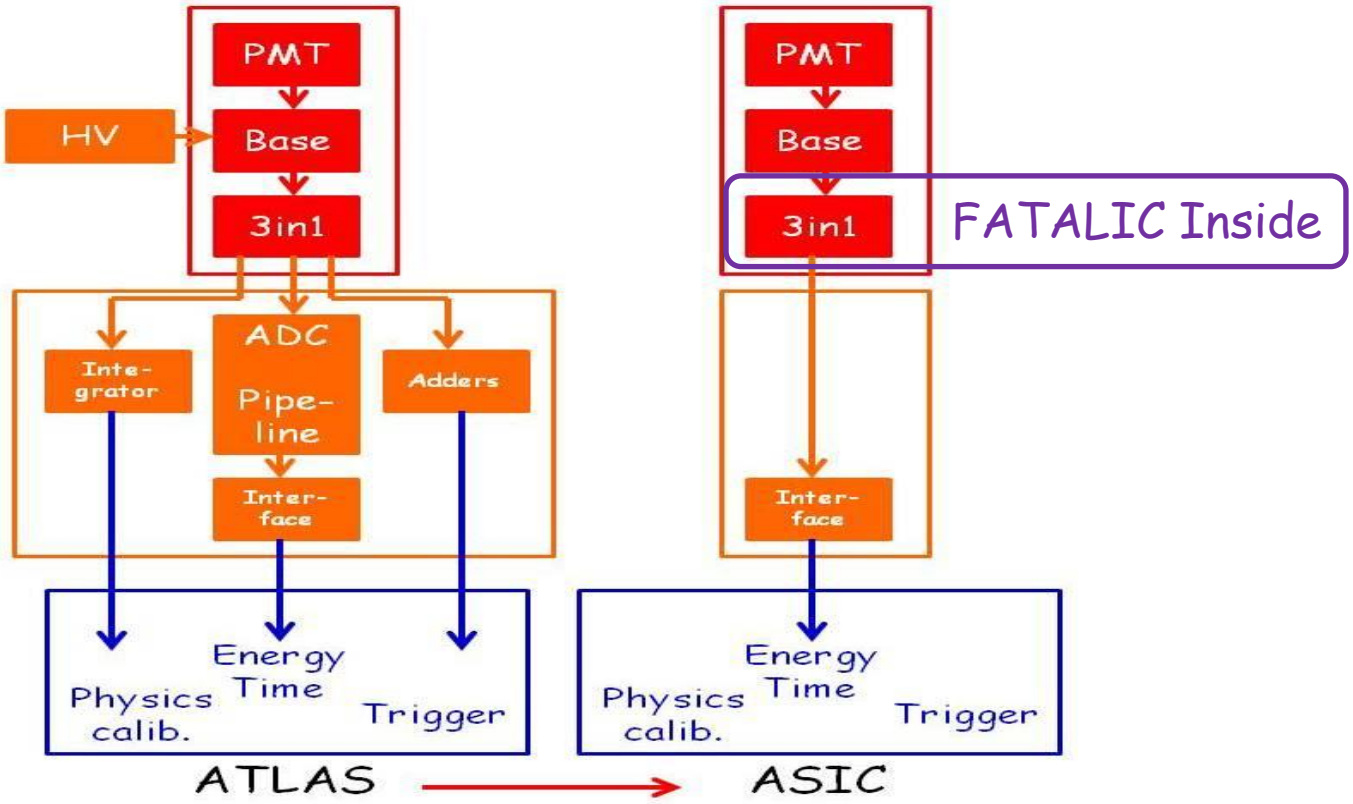
FATALIC project

A single link from Front End to the Back End electronics, with the maximum of functionalities implemented inside a custom-made ASIC (FATALIC) holding:

- A current conveyor to read the signal of the PMT
- 3 amplification channels to cover the large dynamic range up to 1200pC
- An optimized shaping (filtering)
- A 40-MSps 12-bit digitization for each channel



Performance of the analog core (simulation)

Noise Requirement: the smallest signal of interest from the detector, expressed in terms of **equivalent input charge** delivered to the front end electronics, is **24 fC**. The intrinsic noise of the electronics, as measured through the digitization path, expressed in terms of equivalent input charge, shall not be greater than **12 fC rms** at pedestal.

	Dynamic range	LSB	Noise (rms)	Linearity error	Peaking time fluctuaction
High Gain	up to 14 pC	3.4 fC	**0.05% →7 fC**	< ± 0.1%	< 1ns
Medium Gain	up to 140 pC	34 fC	0.05%		< 0.5ns
Low Gain	up to 1200 pC	300 fC	0.05%	< ± 1%	

☺ **Dynamic range extended from 800 pC to 1200 pC**

FATALIC_4: digitization