R&D for Si-W ECAL

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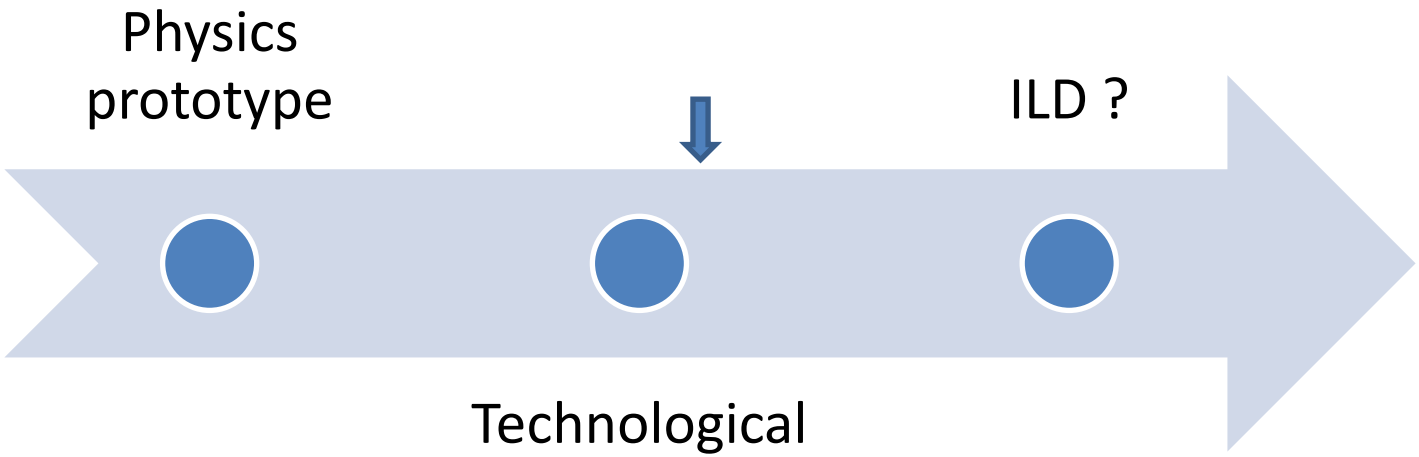
Time line



Proof of concept
- Linearity
- Resolution
- Sensors
- Very front-end

Feasibility of design options
- Compactness
- Granularity
- Front-end
- Demonstrators

Construction
- Integration
- Environement
- Services
- Industrialization
- Logistics

Technological prototype (2011) : Proof of feasibility

Engineering challenges :

→ embedded “system on chip” electronics,

→ extremely low power consumption typ. 25 µW/chn,

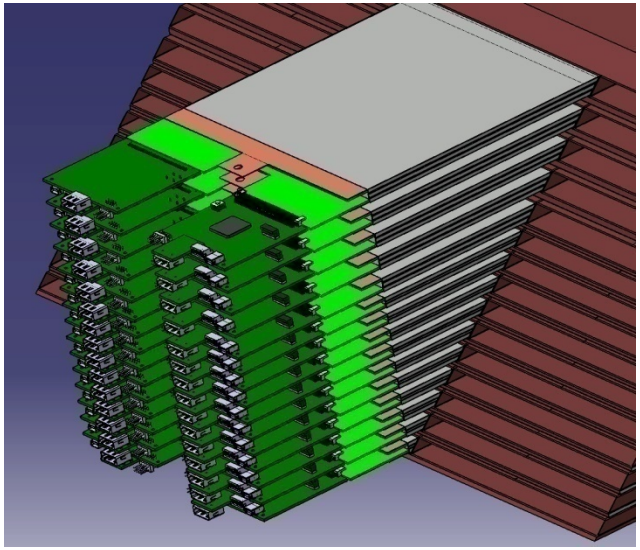
→ wide sensors (81 cm², silicon),

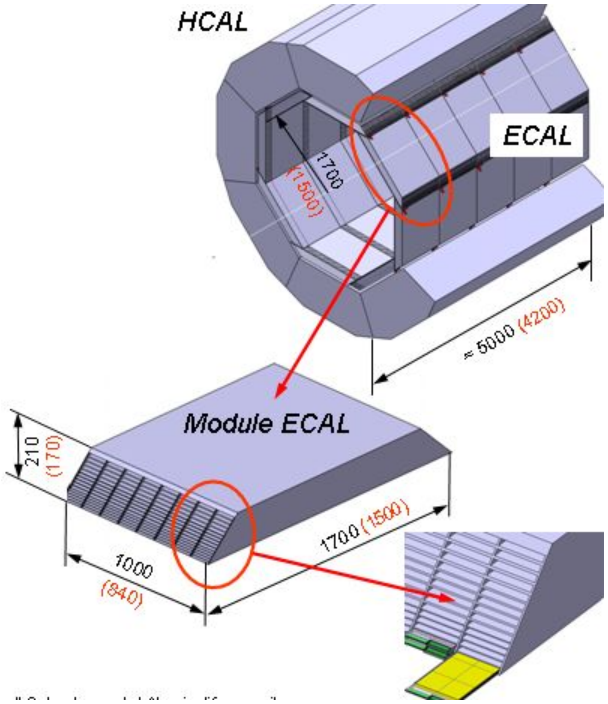
→ large composite mechanical structure,

→ readout technology insensitive to ~4T field,

→ integrated DAQ system

→ Long detector slab





Goal : demonstrator of 1 instrumented tower
(40k channels, 20 cm² crossection, 1/300th of full detector)

Revised to

→ few short slabs

→ 1 long slab

for cost & manpower reasons

Constraints for prototyping

Assumptions made (too) early wrt. to the engineering studies

Supporting structure : size of alveolii, in particular maximum allowed thickness
Ideal stack of materials w/o engineering feedback on feasibility
eg. :

Sensors must be glued on a perfect flat surface : had to x2 PCB thickness
Glue includes micro particle of silver : had to x2 glue thickness

Use of a prototype chip (skiroc2) w/o clear development plan

Confusion between expectations for final design and established performance
eg. Must /4 power consumption, needs (big) decoupling caps, PSRR,…

On going detector optimization
Intense R&D is still required : chip technology, long slab

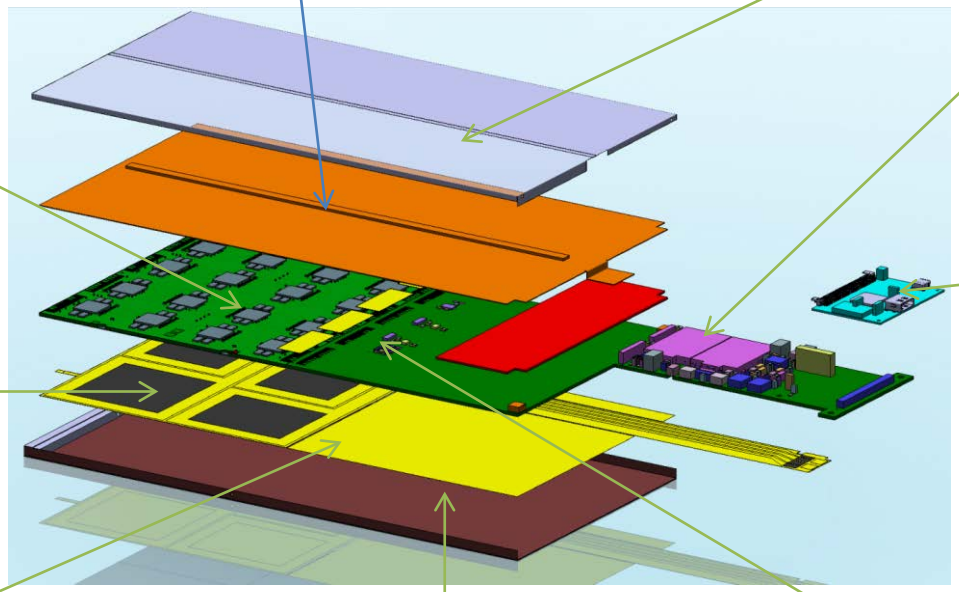
State of the art of a detector module

Coper sheet for cooling

Cover (EMI shielding)

PCB 1024 chn. 16x **SKIROC2**

Power pulsing circuitry (400 mF)



Detector Interface (DIF)

Si PIN diodes

Front-end, DAQ, TFC Not shown

HV kapton

A “short SLAB”

FCC Interconnects

Stiffener, Absorber Carbon fiber + W

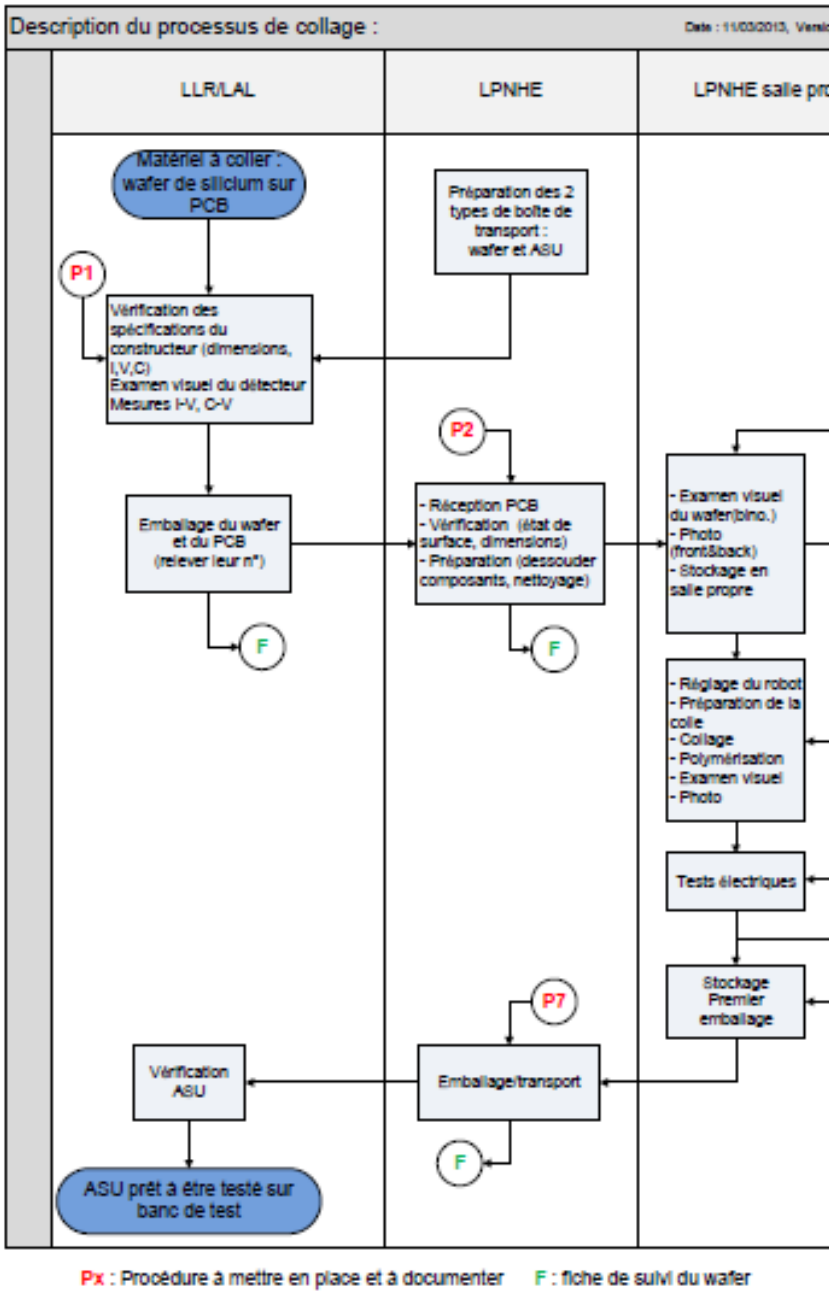
Single layer, ‘U’ stiffener

Quality control, planning, procedures, documentation

Big effort made (C. Clerc then S. Pavy)

Forge website
Task flow diagram
Planification
Quality forms

= a comprehensive approach of production at larger volume & experienced in reality



Large mechanical structure

Each layer build separately then “cooked” together.

Deeply simulated : mechanical constraints, thermal behavior

Next step : wider assembly with 5 columns

Tungsten plates wrapped into carbon fibre: 15 layers

7 mm tick detector slab

Prototyping & process ✓

‘U’ and ‘H’ stiffener ; long HV kapton ✓

To be optimized for final size ✗

Reliability tests ✗

Mass production ✘

II.1 - Modular alveolar structure - composite
W / Carbone HR – Assembly on HCAL

Moulding of one layer / 3 alveoli
L = 2.490 m wall thick. = 0.5mm

25,5 t – R~2050 mm
- 2 x 12
independent
modules

Safety coefficient

• Static: Sufficient / to the stress induced by weight of modules

• **not sufficient** / seism (s =3.2 for Japan?)
/ risks during integration and transport

-> increase nb of ext. plies...**Impact on ECAL dead zone**

See talk by D. Grondin

Sensors

The simplest design to control the cost
- Glued on PCB : Floating Guard Rings
- Reasonable cost trends

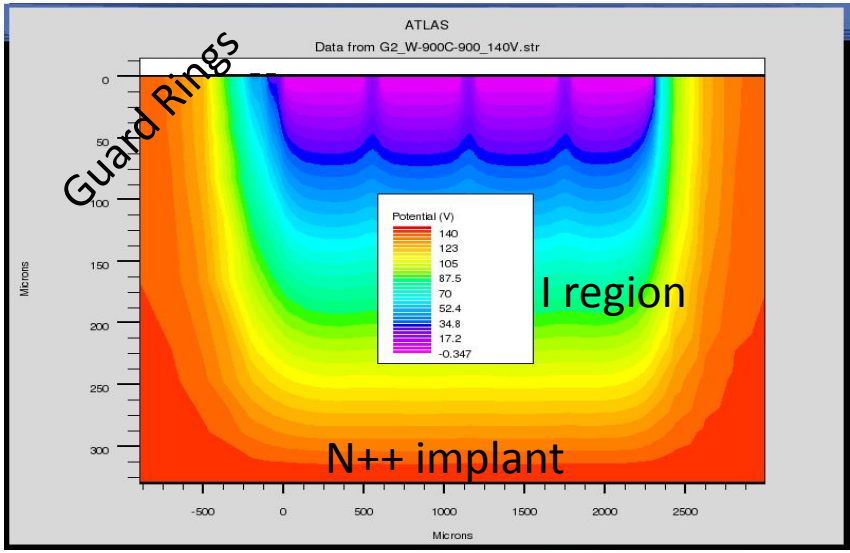
R&D in close collaboration with HPK
- Split GR and/or complete removal of GR
- Laser dicing : gain a factor 2 on dead zone

R&D with LFoundry
- 8 inches wafers : width >12 cm

Also tried edgeless techno. from VTT

Large matrices, reduced dead zone ✓
Crosstalk ✓
Optimization (dimensions) ✘
Mass production & automated tests ✘

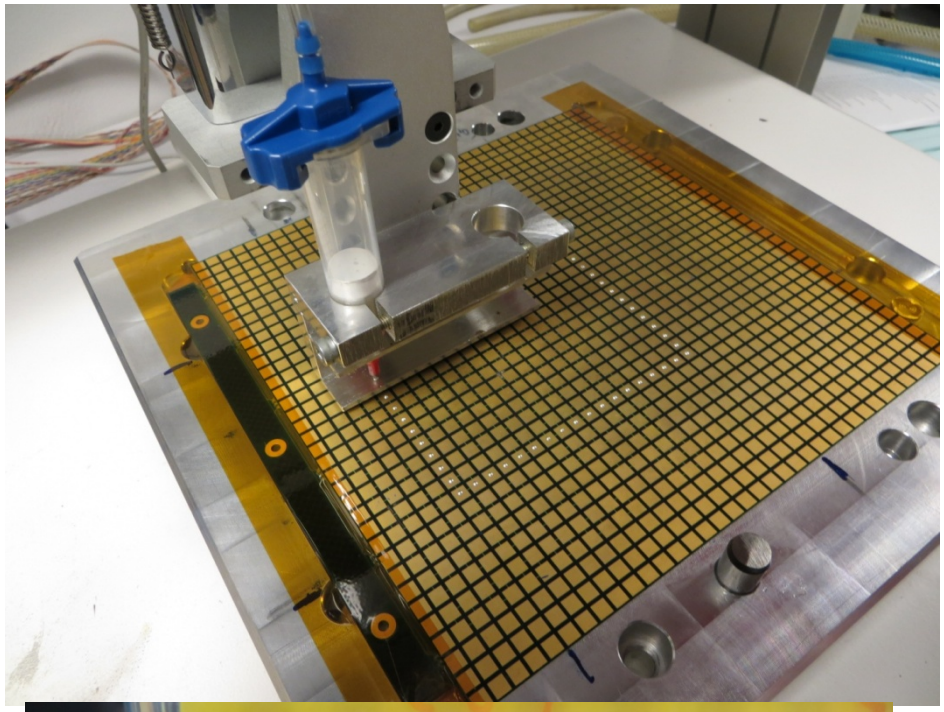
P++ implants (pixels)

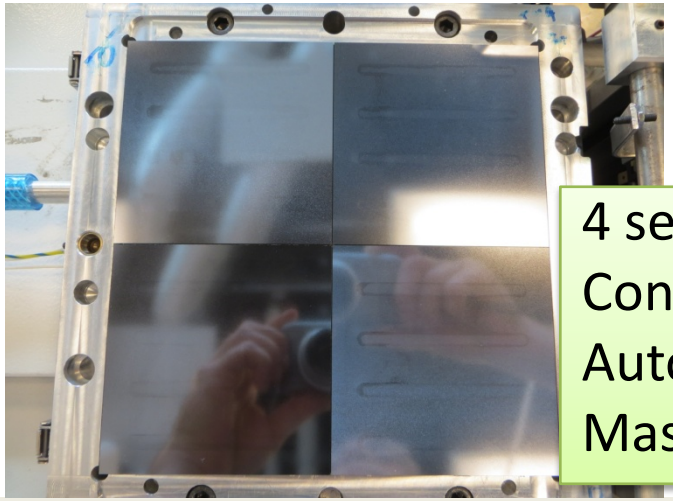


HPK : 9x9 cm², 256 pixels

Gluing process : an excellent reference design

- The parameters of the gluing robot have been optimized to glue 4 silicon sensor on a PCB : automation is on going
- The constraints on the PCB geometry have been identified:
  - Flatness
  - Parallelism of the edges
  - Uniform height of the ASIC soldered on the board



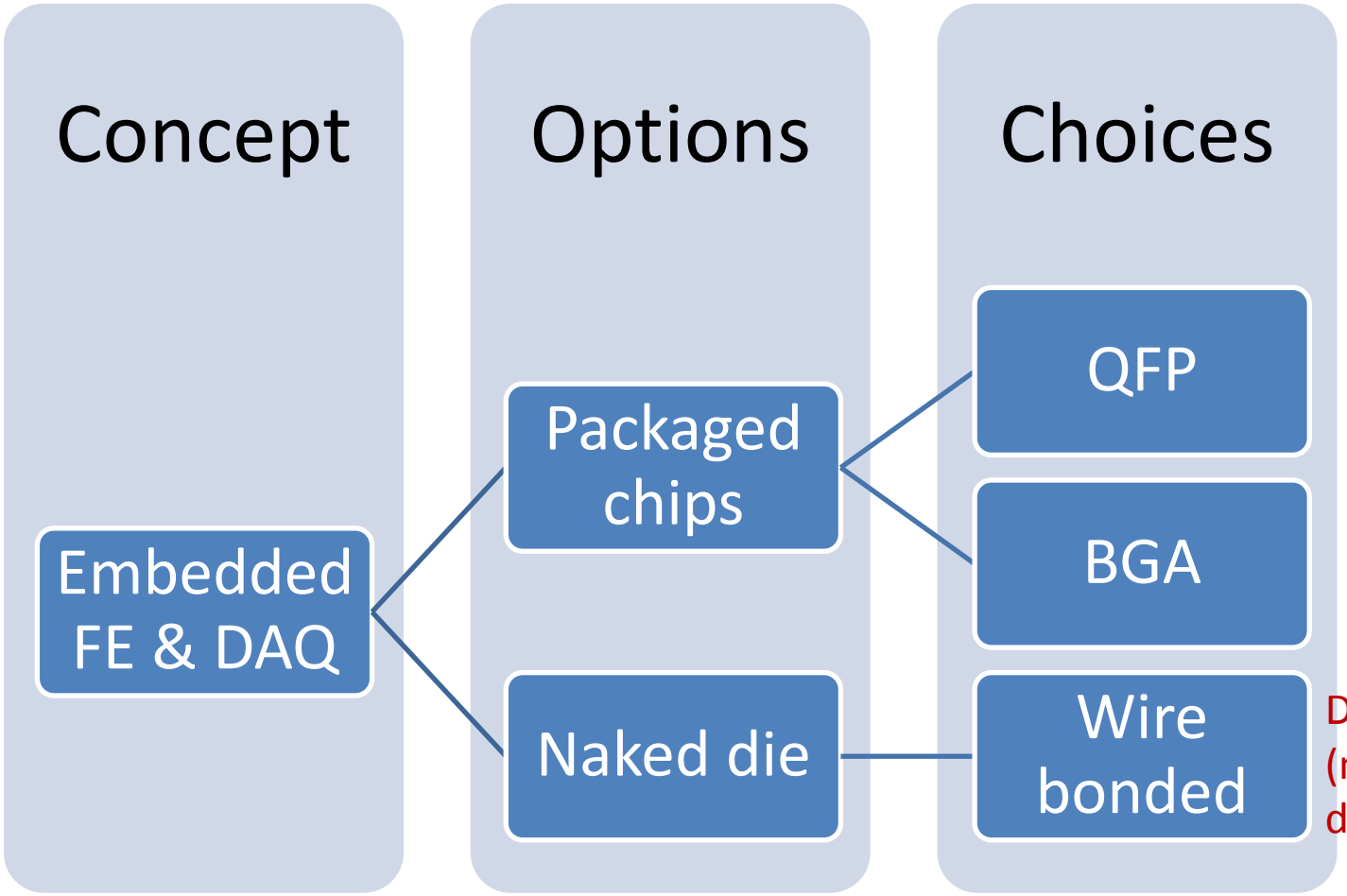


4 sensors, 50µm precision ✓
Constraints on PCB ×
Automation ×
Mass production & tests ×

PCB & chips integration

Prototyping phase includes several steps
Decision to explore alternative "branch" according to issues

- **Conservative option (packaged chips)**
- **High-end Technological option**



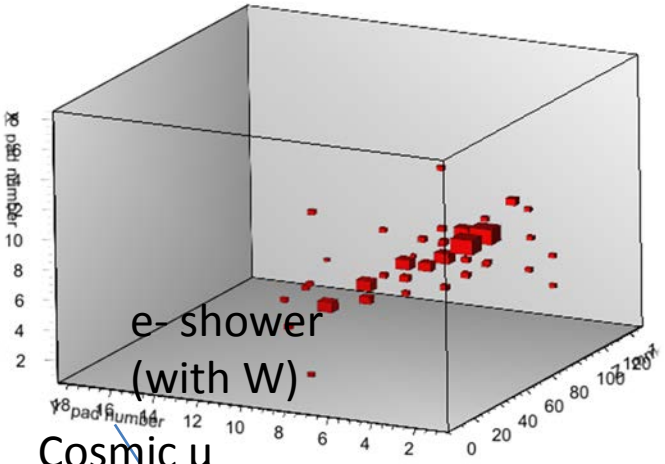
Initial baseline mostly relies on new chip design/technology

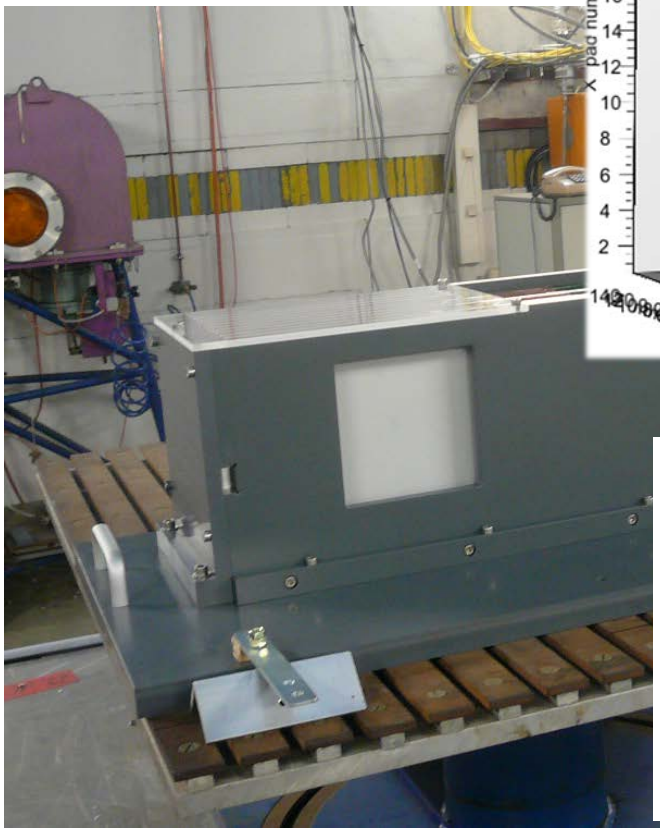
A conservative first version

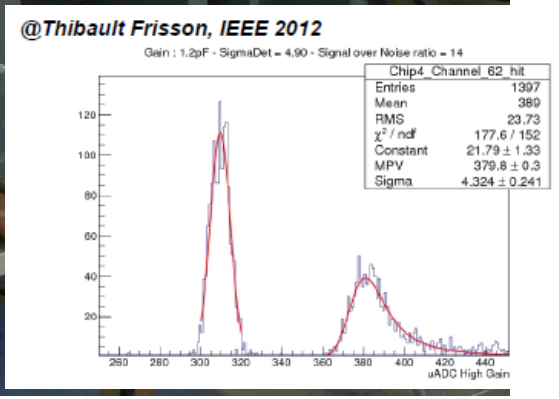
- **Single layer slabs**
- **¼ active area (4 chips = 256 chanels), 1/8 length**
- **QFP Packaged chips**

6 SLAB prototype : 1536 chn.
Test beam @DESY
S/N = [14..22] wrt. Chn#

Intermediate compactness ✓
Qualification of sensors and VFE (analogue) ✓







SKIROC chip

Excellent performance of analogue stages

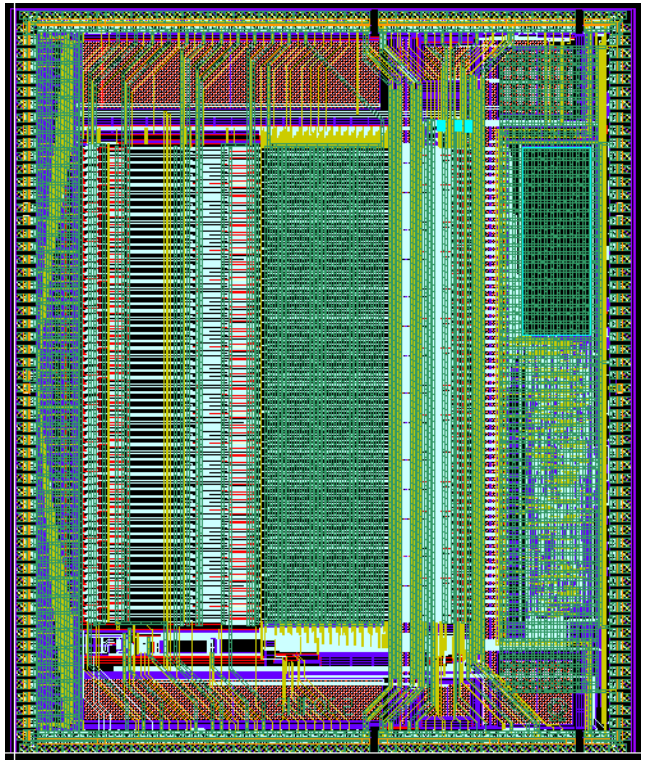
- Stand alone tests OK : chip is virtually very good

System level integration is not easy/feasible

- Trigger logic to be improved
- Optimization of power-pulsing (1 ms stabilization time on FEV boards)
- High sensitivity to CMRR, PSRR
- Optimization of ext. components

not finished

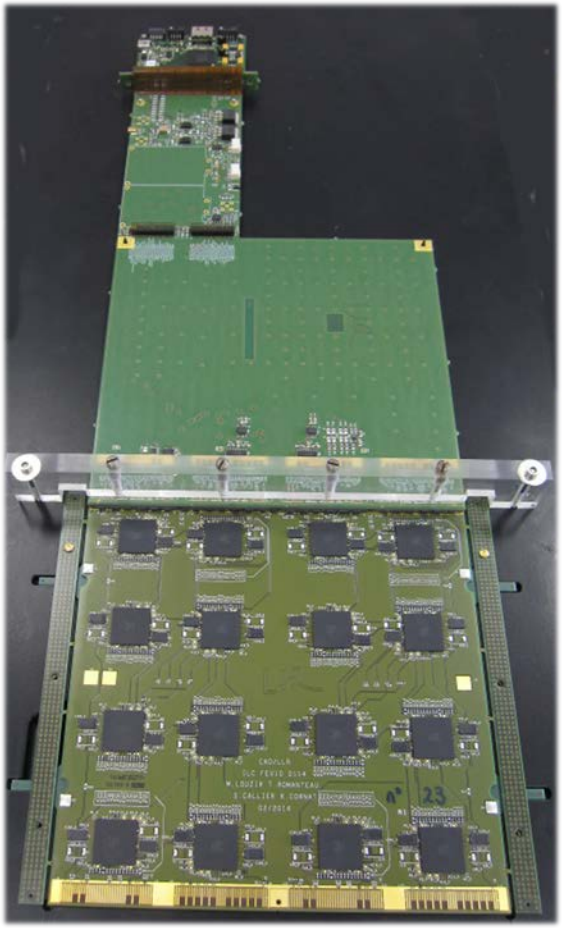
VFE (Analogue) ✓
Digital functions, power-pulsing ✘
Trigger ✘
Integration, FE board ✘

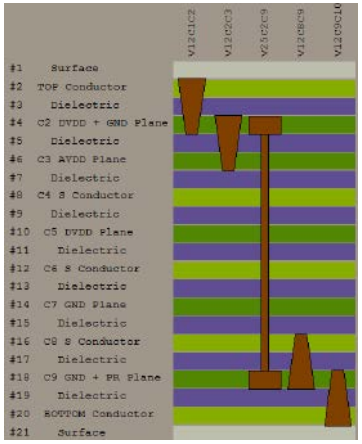


Front-end board (2nd prototype)

(2014-…)

18 x 18 cm^2 front-end board includes 1024 channels (16 chips),
100µm flatness required for gluing the sensors : symmetrical stacking





LFBGA packaged chips
⇨ 1.1mm thick components envelop

With packaged chips version the overall module thickness would be **5.5 mm (+absorber) : >4600 ch/dm^3**

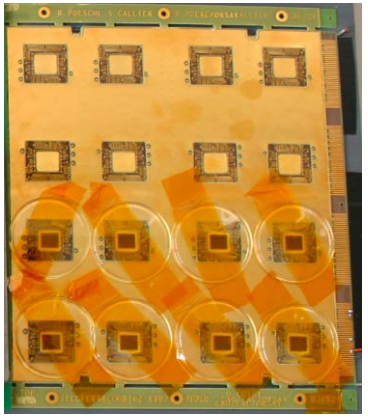
Prototyping ✓

Measurements ✗

Mass production ✓

Naked die version would provide optimal module thickness (<4mm in total, >6000 chn/dm^3)

Electrical tests are ok but flatness is incompatible with sensor gluing.



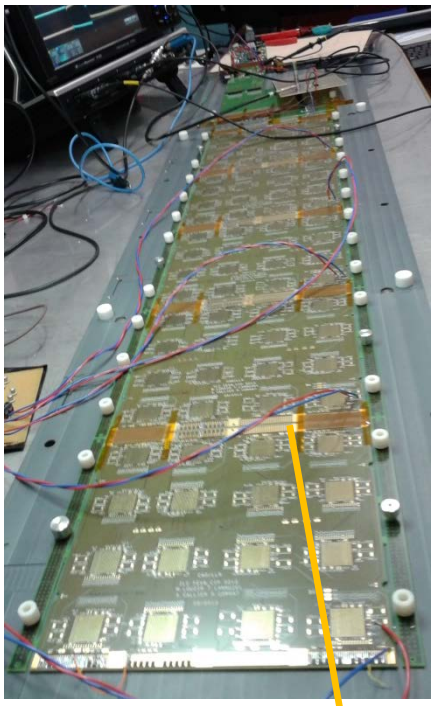
Long SLAB

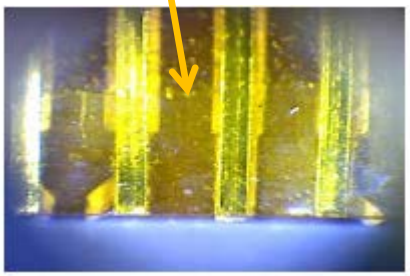
Up to 9 equipped PCBs interconnected to make detector slab

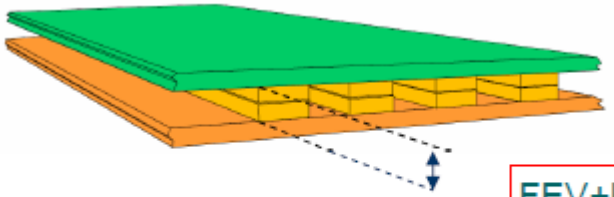
Electrical and mechanical connection made thanks to Kapton connecting cable

Technique under investigation

- Soldering with Flat Cable (Kapton)
- Easy for mass production







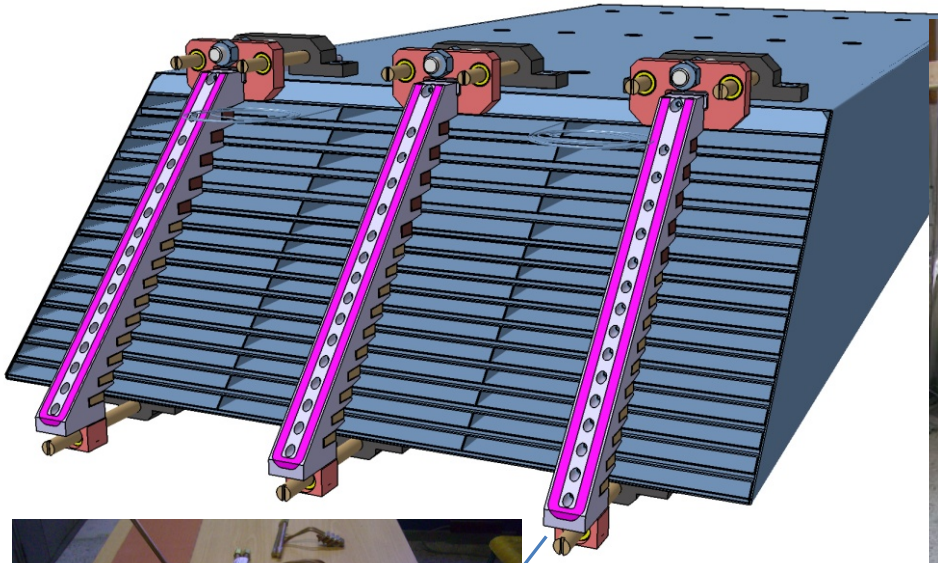
- Prototyping & process ✔
- B field ✔
- Signal integrity ✘
- Reliability tests ✘
- Mass production ✘

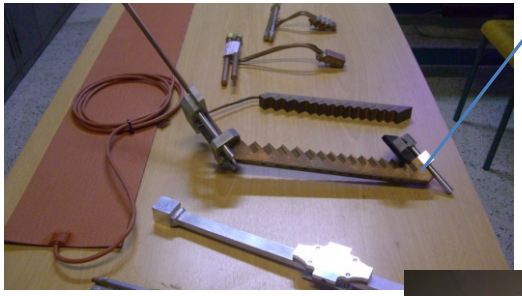
18 cm, 4 slots of 36 pins each

Infrastructure - Cooling

Study from the power source to the global cooling

II.2-1Mechanical tests of the heat exchanger



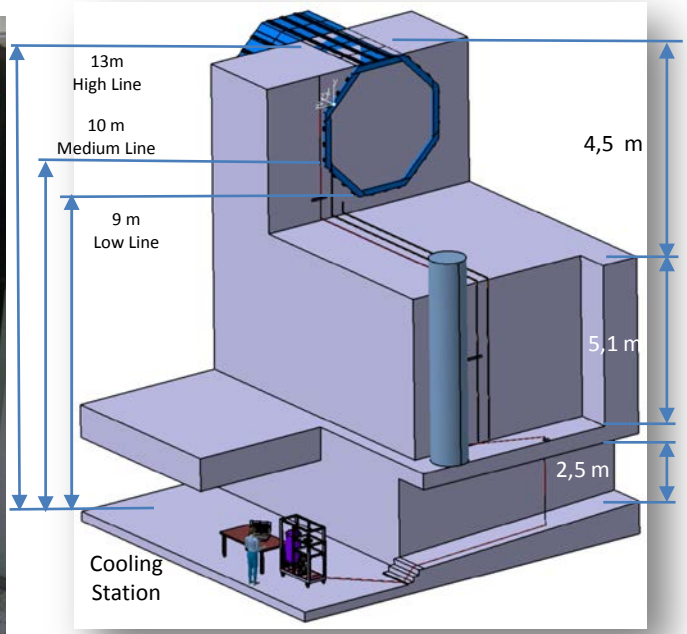


EUDET adaptation of Water heat exchanger

-Thermal simulations / power variations (limit of pulsing)
- Water heat exchanger design near detector

II.2-2 Full scale leak less loops

Validation of leakless system (<1atm)

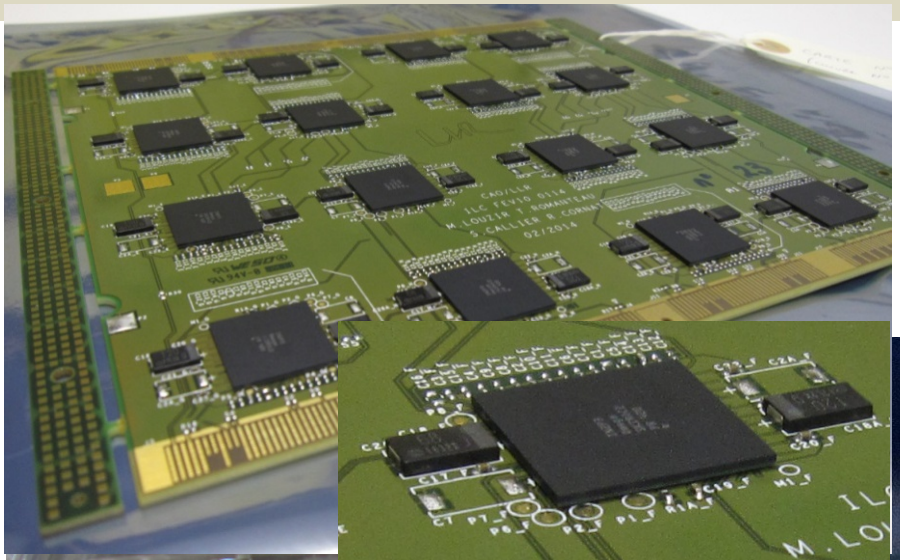


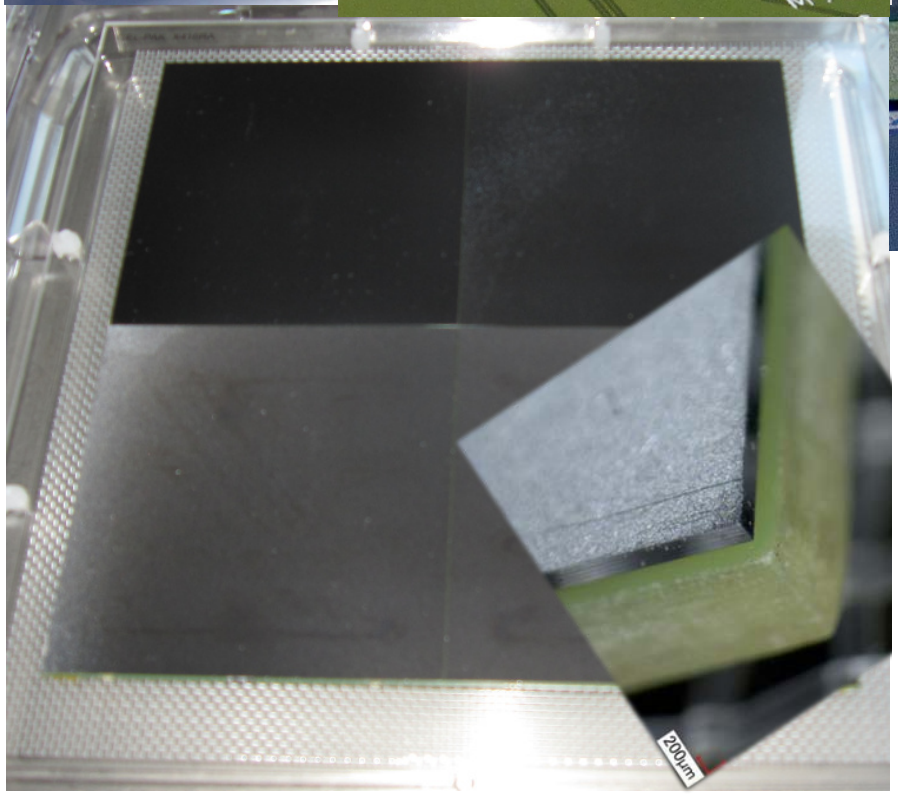
LPSC cooling test area with a drop of 13 m

Ongoing developments 2014-2015

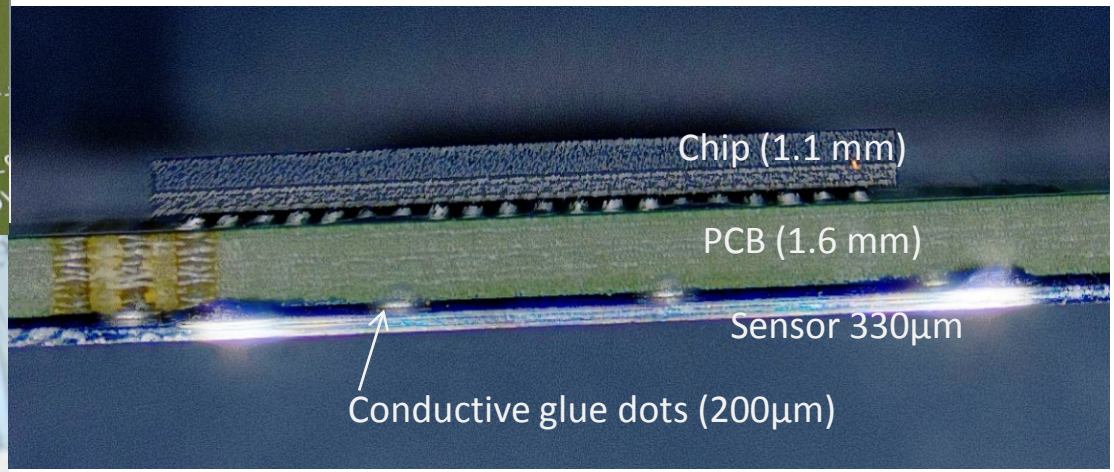
-Full scale leakless loop Integration
-Cooling station integration+ network
-Update of water heat exchanger / BGA
-Thermal tests & simulations / power variations (limit of pulsing)
-Design & test of a spreader (flat heat pipe)

Detector module assembly





Robots for gluing sensors are developed
Manual tools for the assembly of a short slab are existing



4 wafers 9cm x 9 cm wide can be glued with a 20 µm precision and reproducible process.
Glue is dispensed in order to form 200 µm thick dots

DAQ : hardware and software

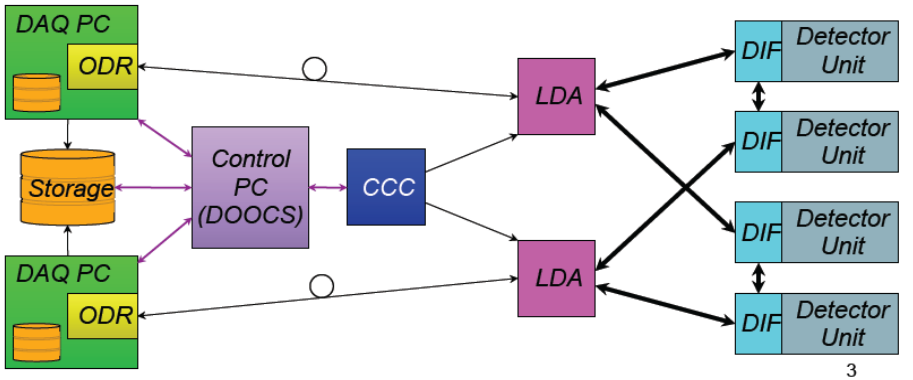
Scalable : Computing network architecture
Standard : Giga-Ethernet, Serial 8b10B

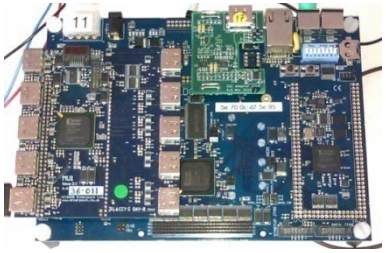
Compact

- "one cable for everything"

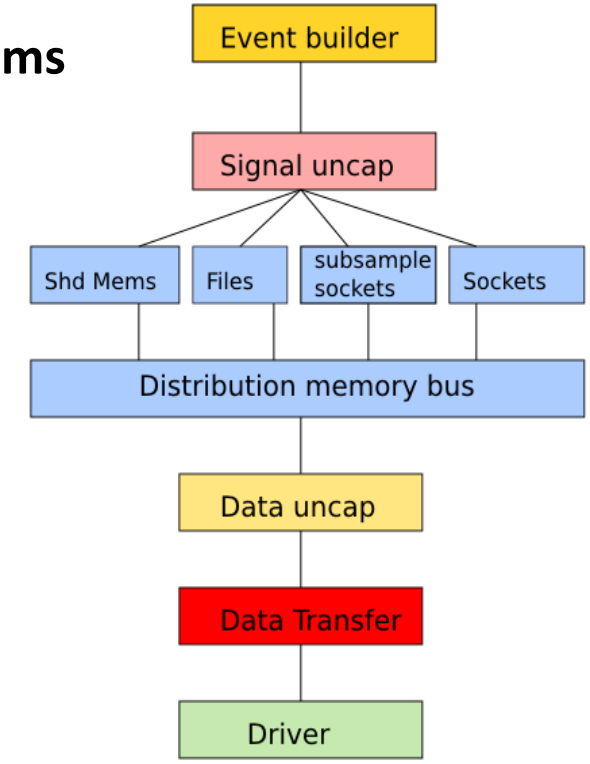
  Data Acquisition, Timing, Slow control

- Backplane-less : made for integration





Ran for test beams



Flexible and highly modular software

Multiple output formats

Files (offline), Shared memory (online High Perf.)
TCPSockets (remote online), Subsampling (real time processing)

Architecture for prototypes ✓
Reliability tests ✓
Coupling to supervisor/event builder (EUDAQ ?) ✘
Scaling to full detector size / redesign ✘

Priorities for next prototyping steps

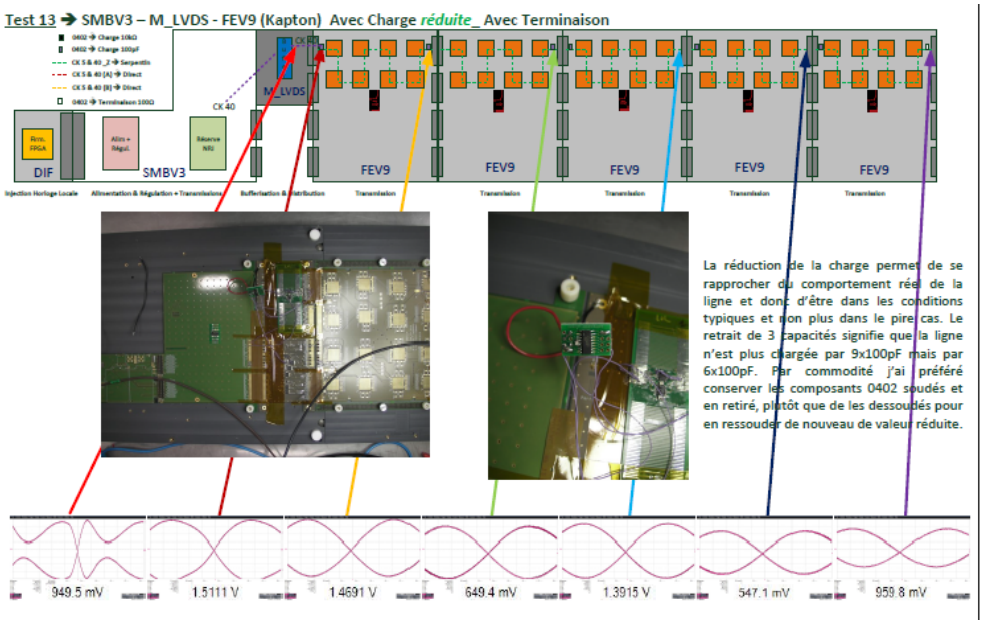
It is urgent to increase our knowledge about :

- **<u>Single</u> layer Long slab & signal integrity** (up to 2m long transmission lines)

- **Effect of power distribution, decoupling & power pulsing**

(only part of the issue with chips)

- **Integration procedures & training**



One can wonder is it is really necessary to spend too much time on understanding SK2 & its behavior one a slab

A development plan has to be established for VFE

Pending R&D

Optimization of FE board & decoupling cap. **but for SK2**

Larger size sensors & appropriate FE board

Pseudo- flip chip integration : may gain 0.5mm on layer thickness

Thinning FE board (keep same flatness) : may gain 0.4 mm on layer thickness

DIF/DAQ module at the top of a tower

Improvement of DIF-SLAB link (Replacing DIF by an ASIC ?)

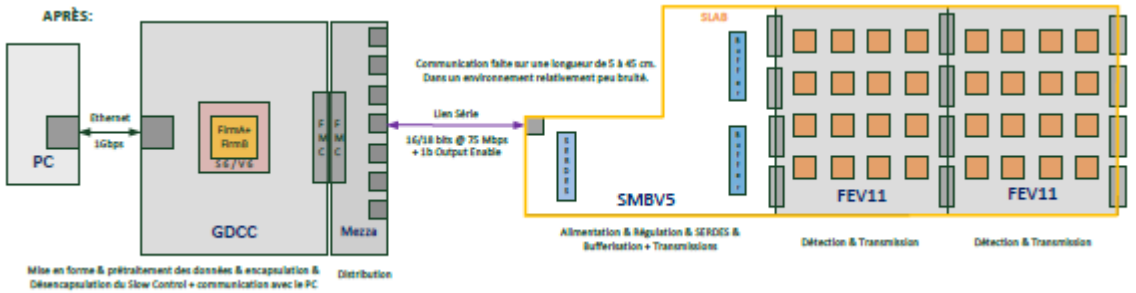
Feedback to/from detector optimization

Automation of integration

Adaptation of cooling to current design

Feedback to/from detector optimization

Effort is on going…



Example of a new design of the detector interface

We should look at this also :

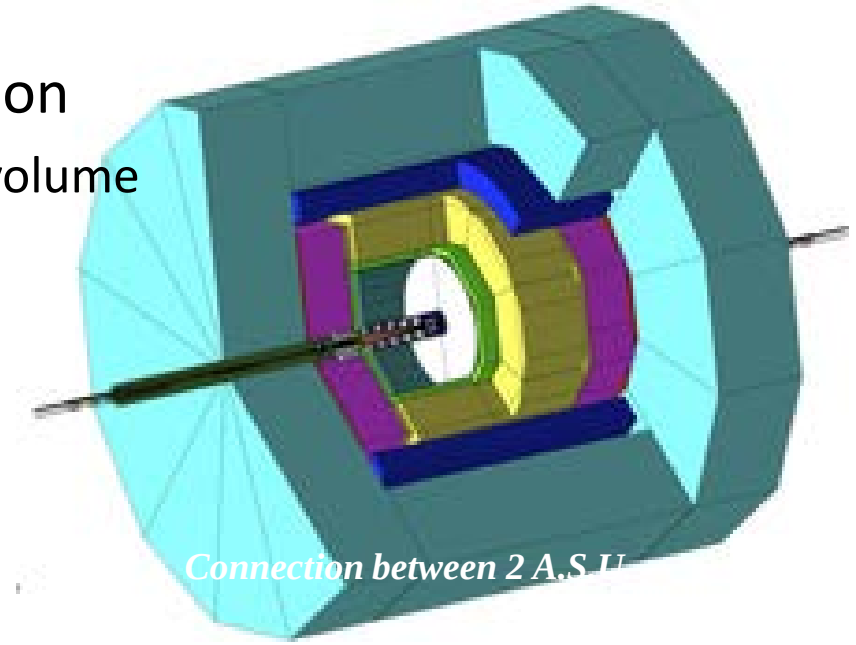
- Automated Integration tools, mass production, etc…
- LV distribution & control
- HV distribution & control
- Power supply for power pulsing (improvement)
- Monitoring & ECS
- Higher levels of DAQ HW (close to computers)
- Power pulsing of DAQ
- Qualification with beam (SK2 ?) : linearity etc… (as for physics proto)
- VFE Chip : understanding of CMMR, PSRR
  - PhD thesis on going (JB. Cizel) : SOI technologies & improved preamplifiers (not sufficient to fix the issue)
- Mass test tools
- Update of MDI, assembly process and work flow
- Mechanics : stress tests, earth quake simulations, …
- Ageing, radiation damage…

All those points should be look at (at least a first thought) thus the proposal could be complete
Contacts must be taken with industrials

Summary

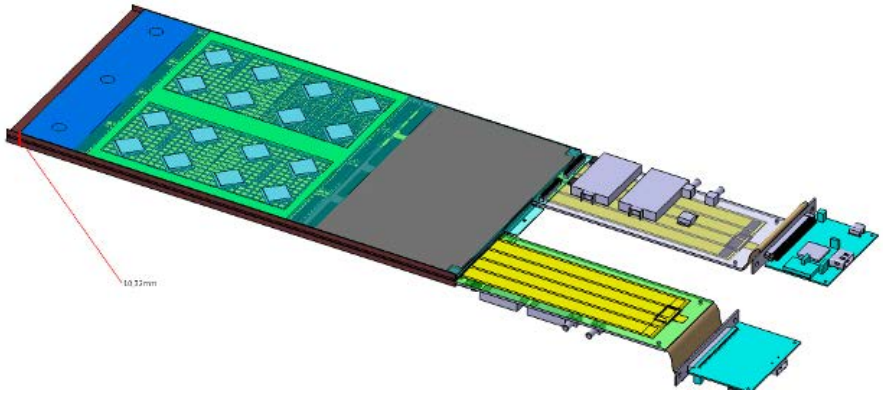
CALICE Si-W ECAL technologies with emphasis on

- Low power FE electronics incorporated in detector volume
- PCB optimization
- Sensor improvements & industrialization



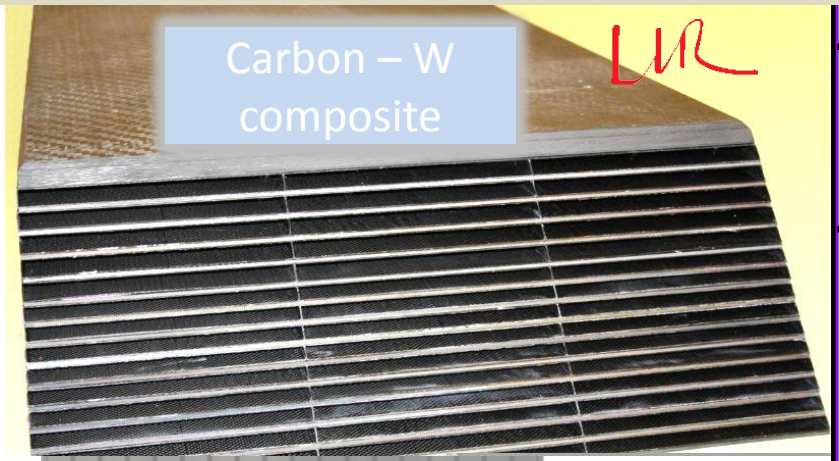
Optimization of overall design is based on physics simulations

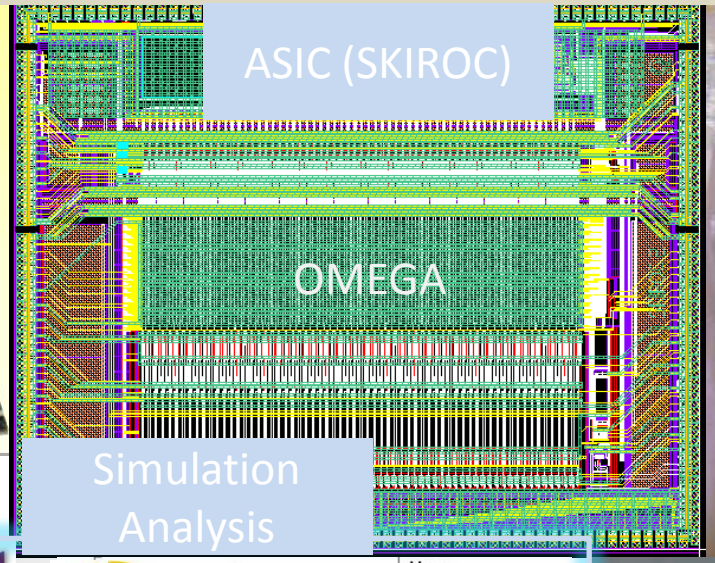
- Number of layers
- Number of pixels
- Dead area
- Allowed material

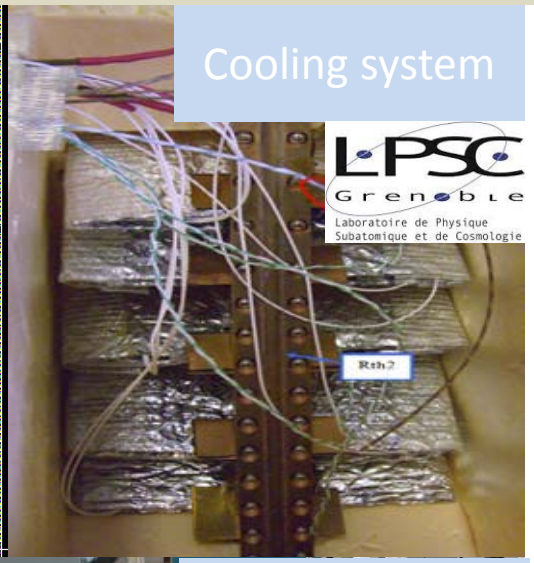


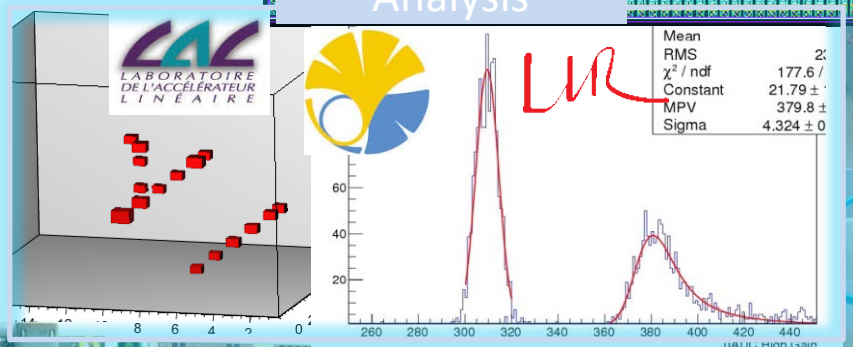
Progress in having good understanding of how to build a complete ECAL with affordable technologies but big amount of remaining work.

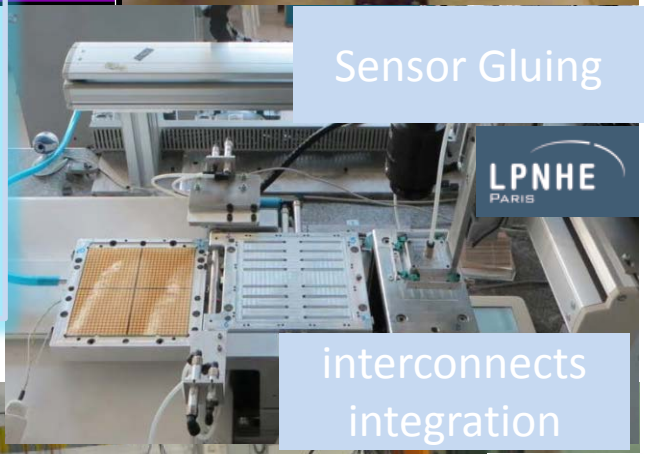
Prototyping : who is doing what

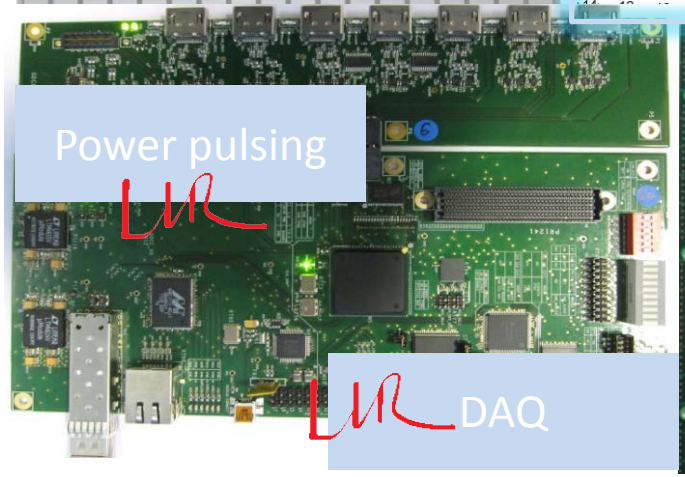


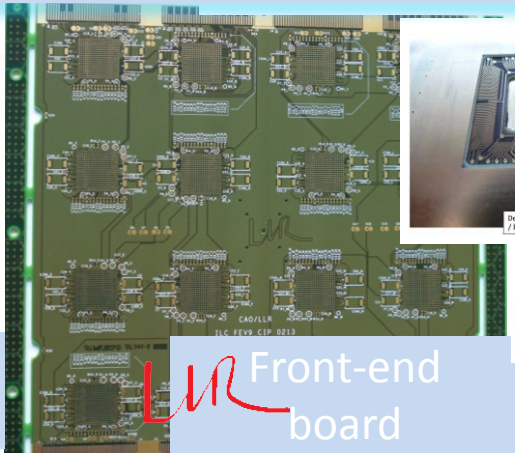


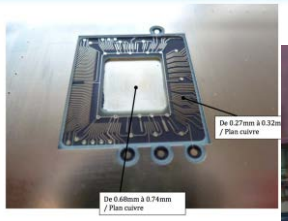


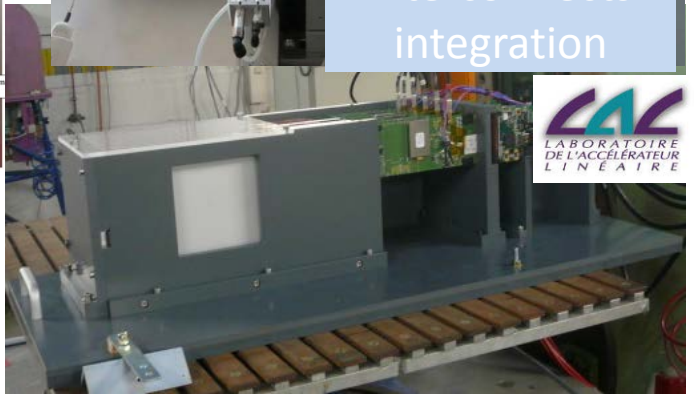




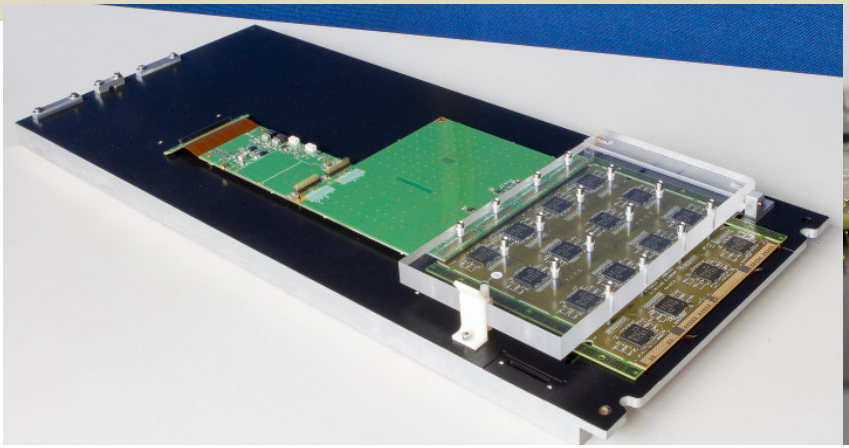


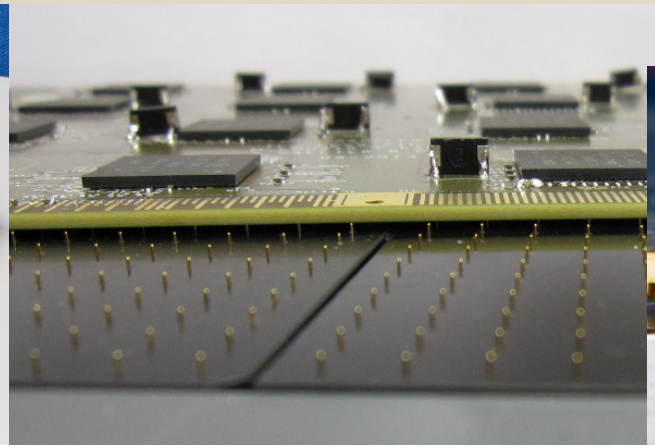


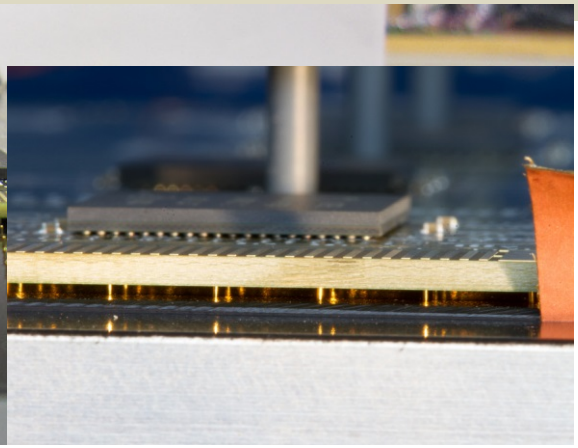


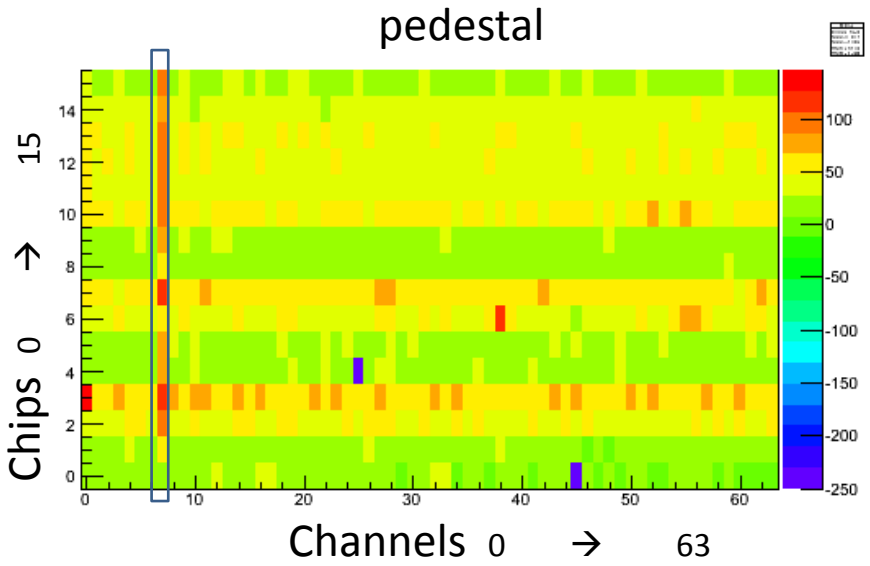


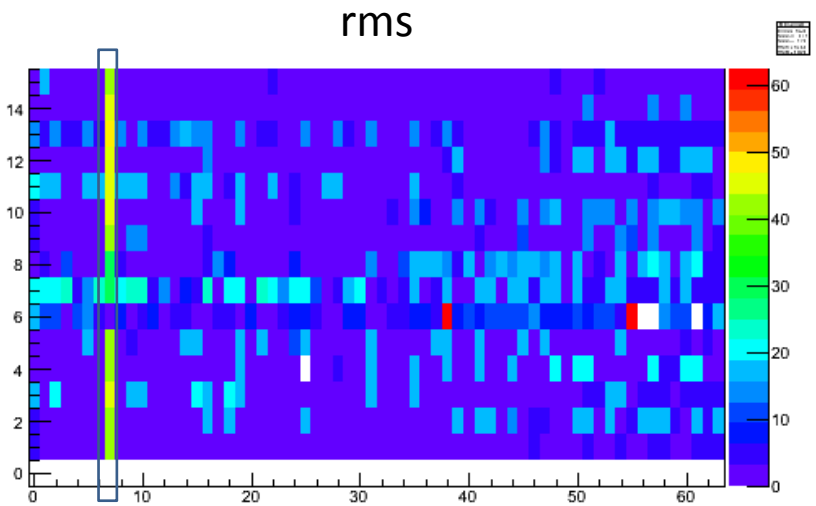
Desktop test setup with sensors











25% of channels are disabled for triggering, all 1024 channels are power pulsed
Chip is triggered injecting a signal on channel 7 (black frame)
Some non uniformity may be due to bad contacts with micro springs (being investigated)