SDHCAL Data Acquisition

Status and Plans

C.Combaret, G.Baulieu,L.Mirabito

Current Status

Hardware

- ➜ 50 planes (1m2 each) of GRPC equipped with HR2 chips, inside a stainless steel structure

- ➜ Clock and synchronous commands are sent using HDMI cables between a central SDCC and 7 DCC boards (1 DCC for 8 plane)

    - ➜ Three new DIF firmwares: The central DIF of each plane fan in/out clock, command and busy to the 2 lateral ones. Only one HDMI connection per plane

- ➜ Data is readout through USB2

    - ➜ A dedicated mezzanin is plugged on each DIF with USB2 FTDI chips

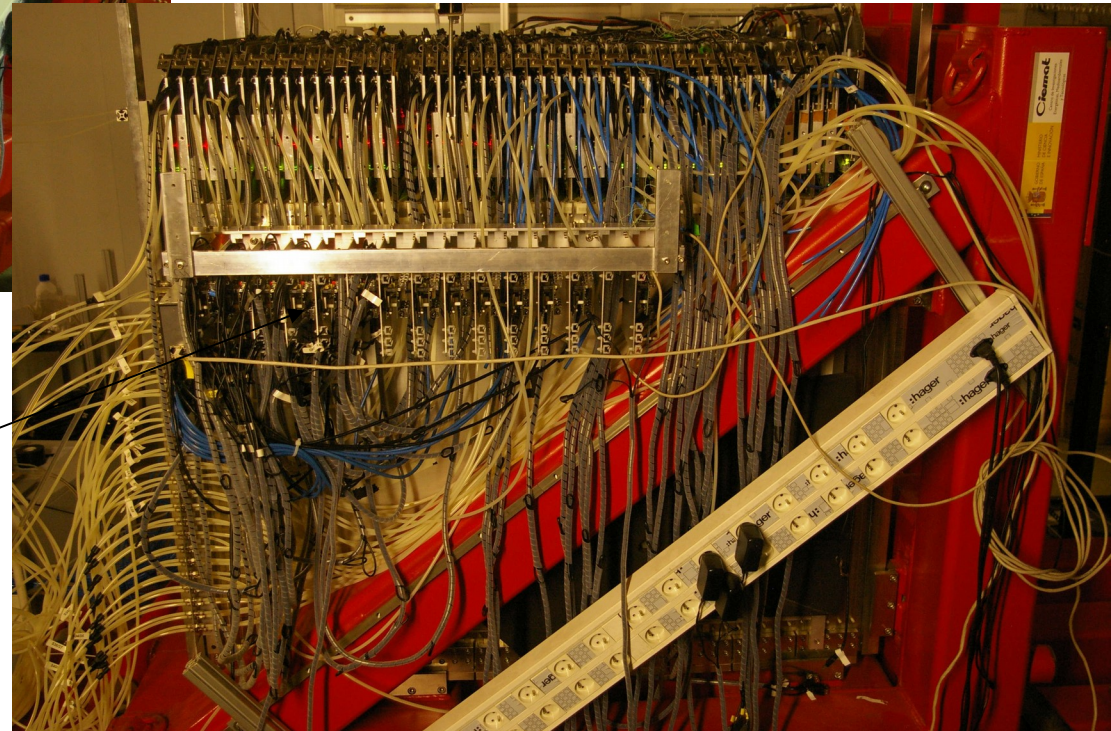   - ➜ Same firmware and software as with USB1 FTDI chip

Software

- ➜ Raspberry pi micro PC equipped with 12-ports homemade USB Hub as Daq frontend

    - ➜ 150 usb2 links to 13 Raspberry micro PCs (1 PC for 4 planes)

- ➜ XDAQ not yet supported on Raspberry PI

    - ➜ DAQ software migrated to DIM for communication between PCs

    - ➜ Possibility to keep XDAQ (or Eudaq) architecture in the backend
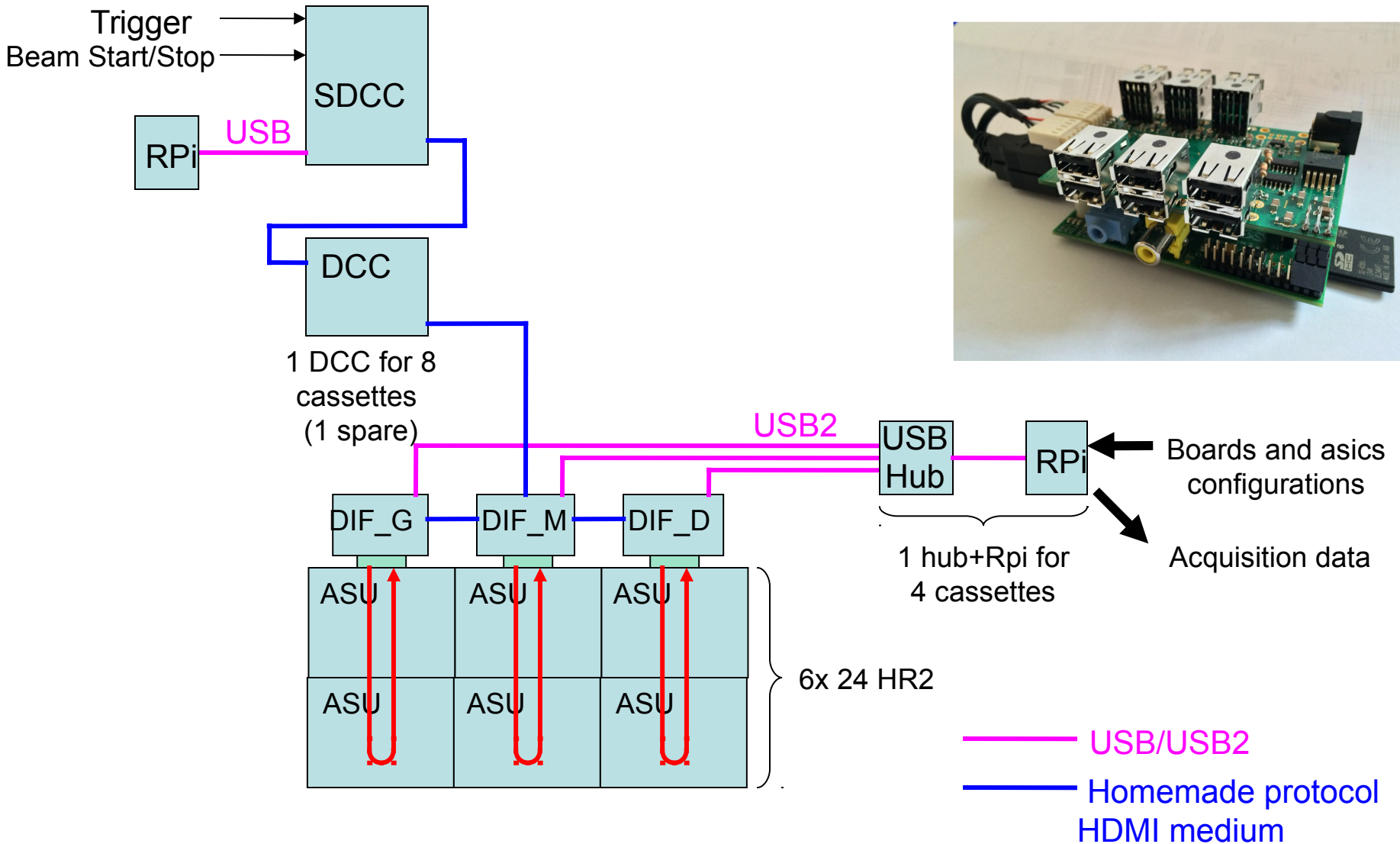
    - ➜ Same Data structure and DB configuration
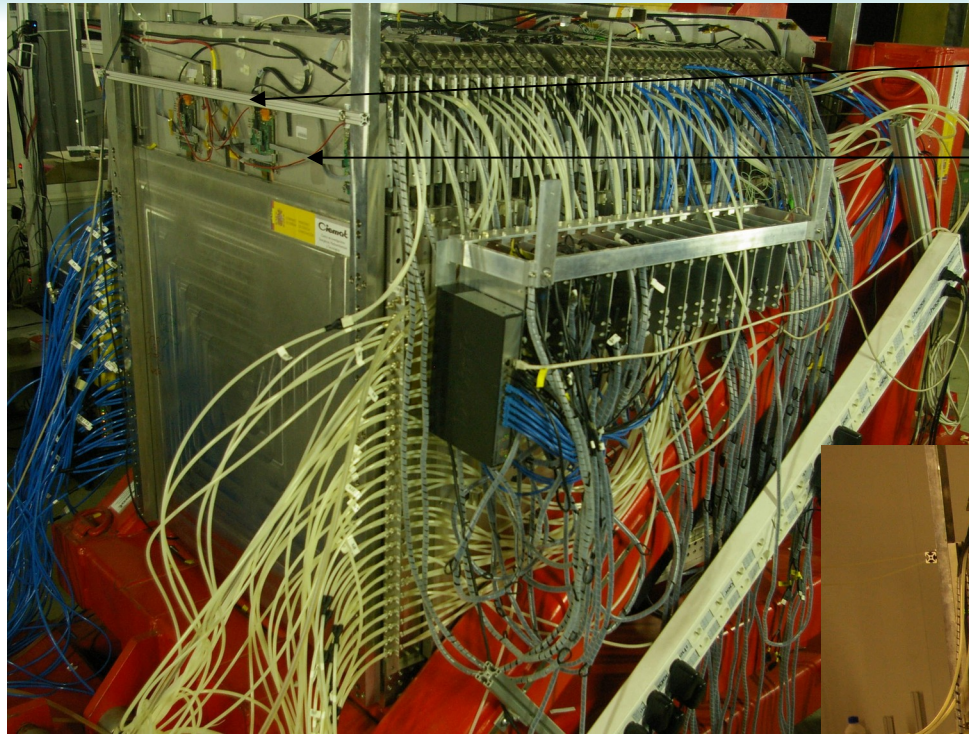
Unique HDMI connection per plane

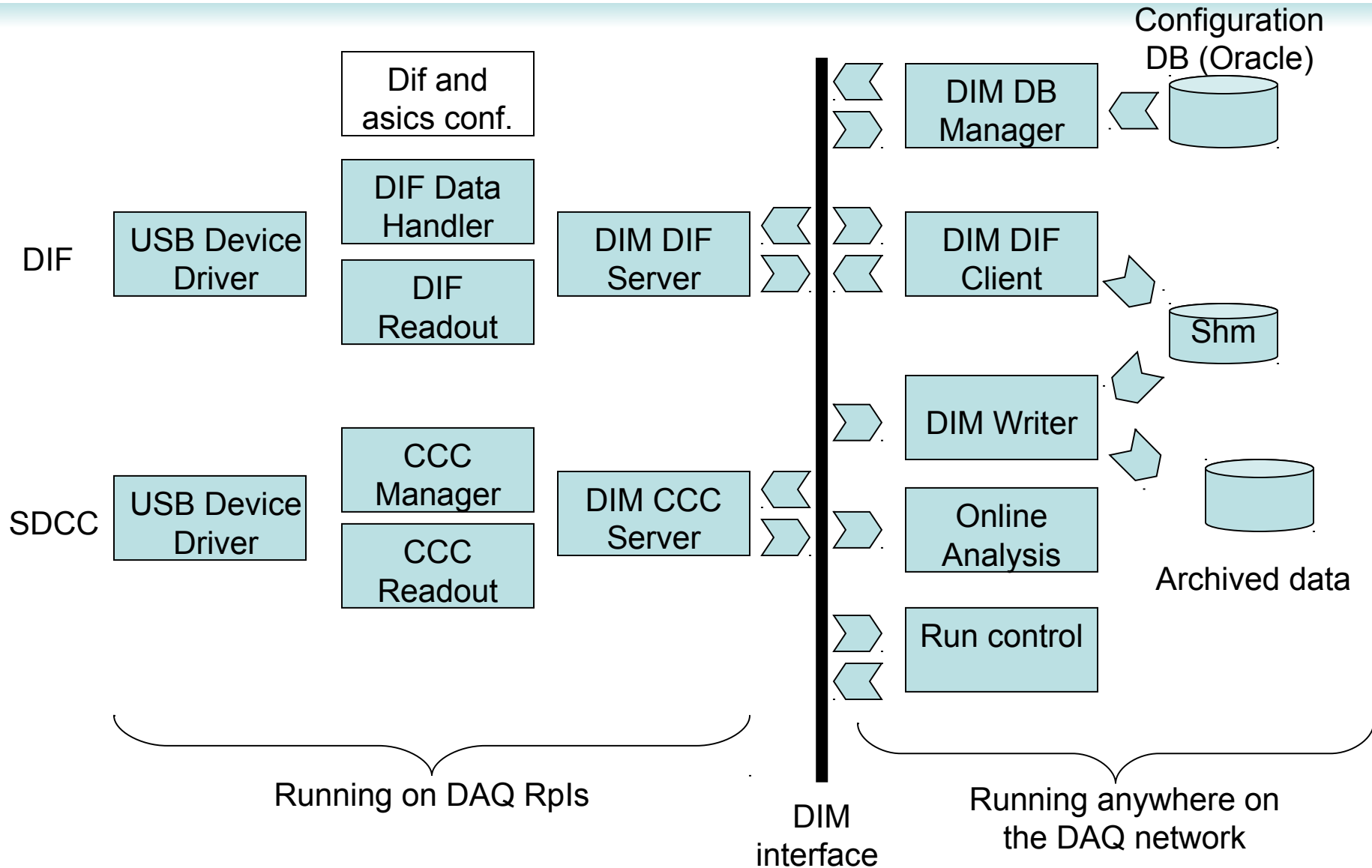Flat cable connection to lateral DIFs

13 RPI with
12-ports USB hub

Software General View of m3

DIF

SDCC

Dif and asics conf.

DIF Data Handler

DIF Readout

USB Device Driver

DIM DIF Server

CCC Manager

CCC Readout

USB Device Driver

DIM CCC Server

DIM interface

DIM DB Manager

DIM DIF Client

DIM Writer

Online Analysis

Run control

Configuration DB (Oracle)

Shm

Archived data

Running on DAQ Rpls

Running anywhere on the DAQ network

L.Mirabito

Plans

What is in progress (ILC)

➜ Common beam test with other CALICE detectors
  ➜ light(?!) adaptation of software, hardware and firmware to make it compliant with other detectors
  ➜ Main issue is the clock and command compatibility

What we plan to build very soon (ILC)

➜ A few (4) GRPC detectors (2 or 3 m2) equipped with HR3 chips
➜ One (new) DIF per plane
➜ Data is readout through TCP/IP links
➜ Clock and fast commands are sent to the DIF using dedicated TTC protocol
➜ Software still based on DIM

What we plan to build very soon (CMS)

➜ A few (tbd) GRPC inside leak tights cassettes with TDC/Petiroc electronics
➜ Eventually Daq will need to be CMS compliant (GBT use?) and integrate inside the CMS DAQ/Trigger framework
➜ Soon, a TTC compliant DAQ is sufficient.

TCP/IP +TTC solution

Advantages

➔ No need of HW implementation, all TCP stack is already implemented in the Wiznet chip
➔ TTC protocol well known, many hardware and software implementations already exist
➔ TTC hardware well known, many boards already exist and are available (especially at CERN pool)
➔ Could be compliant quite easily with m3 prototype (tbc) to be used as tail catcher
➔ Current baseline for ILC SDHCAL

Disadvantages

➔ Require 1 ethernet cable per DIF for data and 1 for TTC
➔ TTC technology becomes old
➔ Not compliant with CMS upgrade plans

GBT solution

Advantages :
➔ CMS upgrades compliant technology
➔ Lighter in term of cables (everything on 2 fibers)
➔ More modern technology

Disadvantages
➔ Requires more expensive hardware (tbc)
➔ Designed for CMS -> overkill for ILC in terms of bandwidth
➔ Power consumption quite high for ILC (even if LP-GBT exists with <1W dissipation)
➔ Both Hardware and Software high quality work has already been performed in the CMS collaboration

Ideas
➔ Can be used as 1 GBT link per « super module » if someone design a concentrator board to accommodate DIFs
➔ Maybe a lighter (slower, lower bw, less consumption) GBT can be imagined between DIFs and concentrator (but is it really neededl?)

Summary: What will/could be done?

ILC :

Develop HR3 system with current baseline (TTC & TCP/IP DIF).
-> mandatory to have a technological prototype of SDHCAL with HR3

CMS :

Use the new DIF as a GBT experimentation platform to read Petiroc+TDC

Otherwise use a Glib board (FMC board to accommodate ASU link required).