The New DIF for the SDHCAL

HGC4ILD - High Granularity Calorimeters for ILD WS

LLR (Paris) 2-Feb-2015

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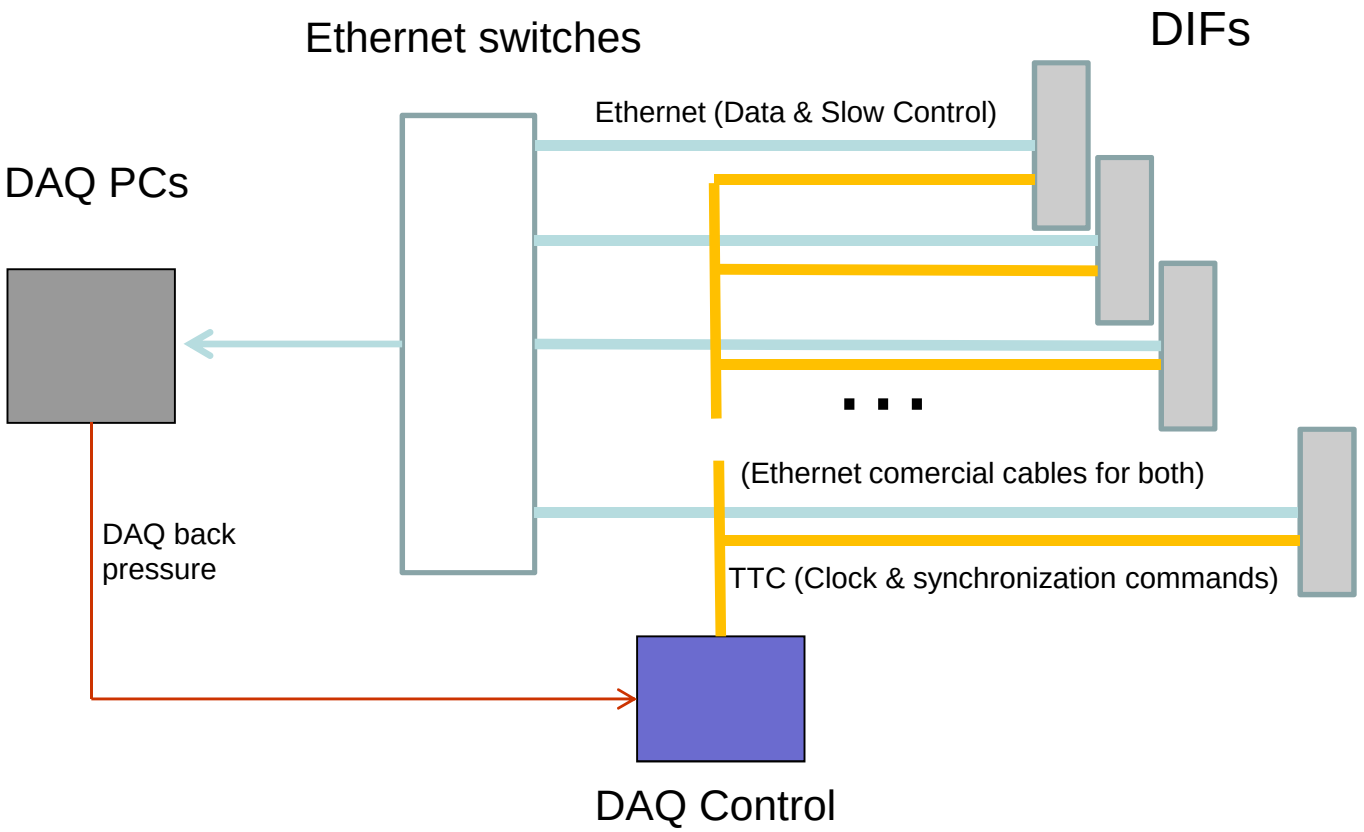
Next SDHCAL DAQ achitecture

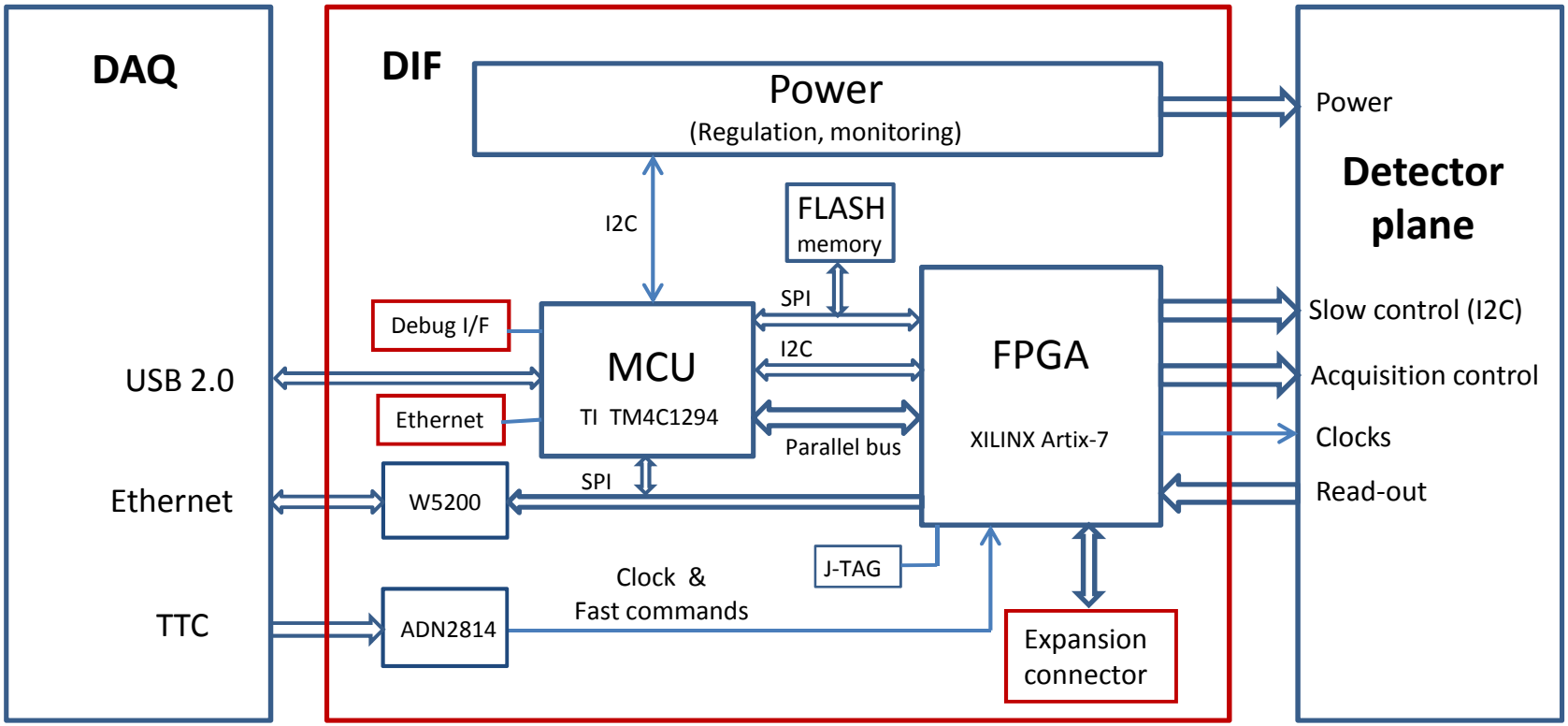


- Slow control & readout by Ethernet using commercial switches for concentration
- Clock and synchronization by the TTC system used in LHC experiments

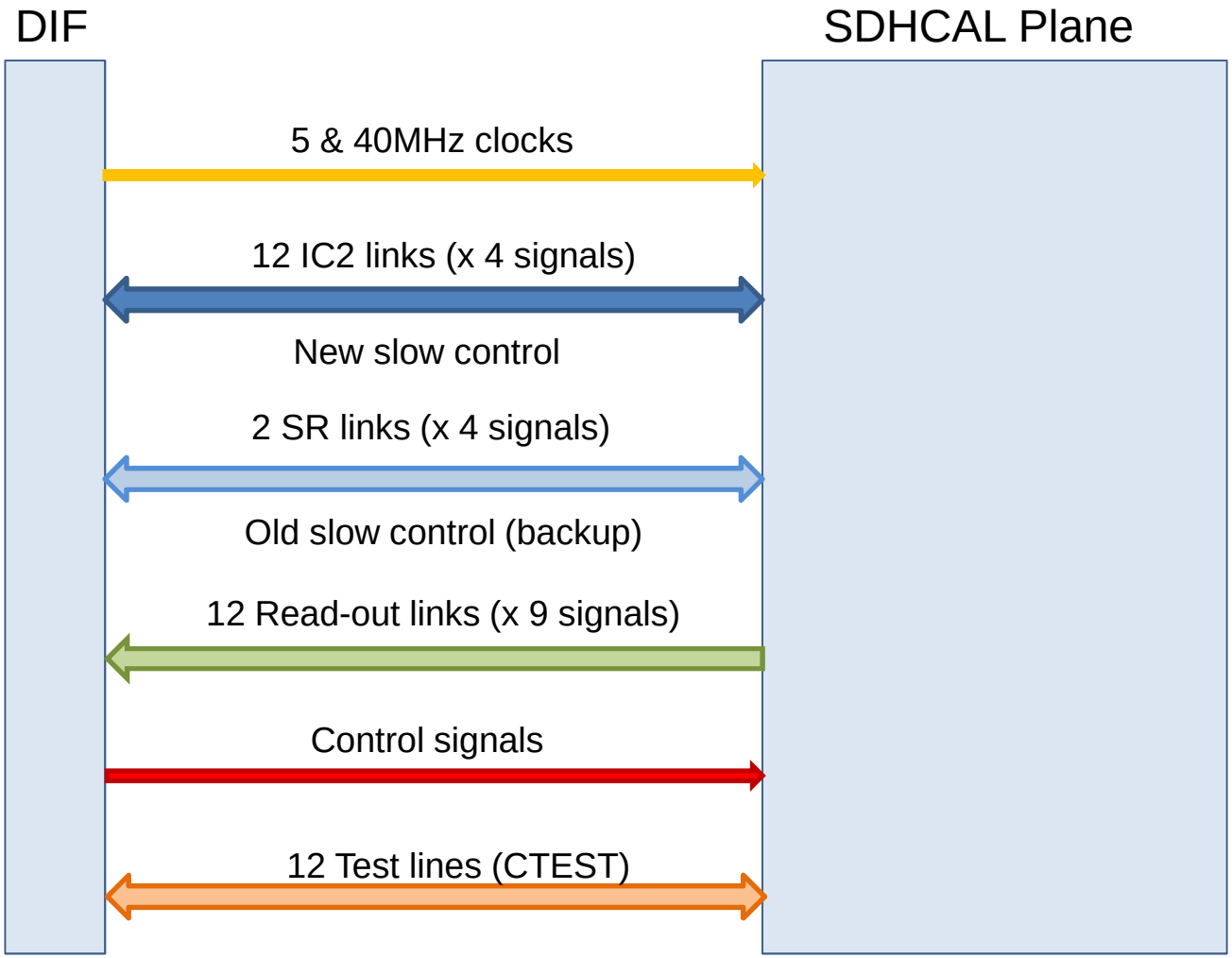
New DIF features

- Only one DIF per plane (instead of three)
- For the longest plane (1x3m) the DIF will handle 432 HR3 chips (vs 48 HR2 in previous DIF)
- HR3 slow control through I2C bus (12 IC2 buses). Keeps also two of the old slow control buses as backup & redundancy.
- Data transmission to/from DAQ by Ethernet
- Clock and synchronization by TTC (already used in LHC)
- 93W Peak power supply with super-capacitors (vs 8,6 W in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade USB 1.1 to USB 2.0

New DIF block diagram



DIF to plane interface



Micro Controller (MCU)

Main Functions:

- Receive and execute DAQ commands
- Receive, store locally and send HR3 chips configuration data.
- Control the power supply of the plane (power pulsing).
- Read the power and temperature sensors.
- Update FPGA configuration.

TM4C1294NCPDT Microcontroller Main Features

- ARM Cortex-M4F processor core
- 120-MHz Operation; 150 DMIPS performance
- 1024 KB Flash memory
- 256 KB single-cycle System SRAM
- 6KB of EEPROM
- Four SSI modules with Bi-, Quad- and advanced SSI support
- Ten I2C modules with four transmission speeds including high-speed
- USB 2.0 OTG/Host/Device
- Two CAN 2.0 A/B controllers
- 10/100 Mb Ethernet MAC & PHY
- Eight UARTs
- 20 12bits ADC channels
- …

Xilinx Artix – 7 FPGA

Main Functions:

- De-mux I2C links form the MCU to the plane.
- Multiplex the 12 readout links from HR3 chips into one SPI.
- Synchronization and transmission of TTC clock to the plane.
- Transform fast commands coming from TTC into signals for the detector plane (Reset, Start_Acq, Triger_ext) and informs the processor about the new state.

- Artix-7 family Belongs to the last generation of Xilinx FPGAs optimized for low power & low cost
- FGG484 package (23 x 23 mm) chosen for the size vs pin count ratio, user pins are 3.3V compatible, has several gigabit transceiver to implement GBTs an also because …
- The same footprint is compatible for all the members of the family from XC7A35T to XC7A200T

Main features:

- Logic cells: from 33280 to 215360
- RAM: from 1800 K b to 13140 Kb
- User I/O @ 3.3V : from 240 to 285
- GTP Transceivers (6.6 Gb/s): from 4 to 16

Previous DIF FPGA (Altera Cyclone III)

- Logic cells: 15408
- RAM: 516 Kb

Plane Power Requirements

HR3 has increase the power requirements vs HR2:

	HR2		HR3	
Power mode	mW/ chip	mW/m²	mW/ chip	mW/ m²
Allways active	91,2	13132,8	155,52	22394,88
Power-Pulsing (0,5% duty cycle)	0,48	69,12	0,78	112,44

During the 1m³ prototype tests the plane power measurements where higher than the expected for only the HR2. This is due to the extra circuits in the plane and the DIF.

Power mode	**Measured**	**HR2**	**DIF**	**Extra circuits**
Allways active	25,7	13,13	4,00	8,57
Power-Pulsing (0,5% duty cycle)	8,25	0,069	4,00	4,18

First prototype power measurements (W) and distribution

We can suppose that we will need similar extra circuits in the plane, so, extrapolating the first prototype measurements to the new plane with the new HR3, the power requirements will be as follows:

Power mode	**Extra circuits**	**HR3**	**1m² Plane**	**3m² Plane**
Allways active	8,57	22,39	30,96	92,88
Power-Pulsing (0,5% duty cycle)	4,18	0,112	4,29	12,88

New prototype (3m² & HR3) expected power (W) requirements

(Power pulsing average is calculated in 200ms with 0.5% duty cycle)

Power distribution

- At least two independent power supplies are required: one for analog and other for digital.
- The HR3 can be set to low power during inactivity times but the extra digital circuits in the plane can not.

Power mode	Extra circuits	HR3	HR3 Analog	HR3 Digital	Total Analog	Total Digital
Allways active	25,71	67,17	47,02	20,15	47,02	45,86
Power-Pulsing (0,5% duty cycle)	12,54	0,336	0,24	0,10	0,24	12,64

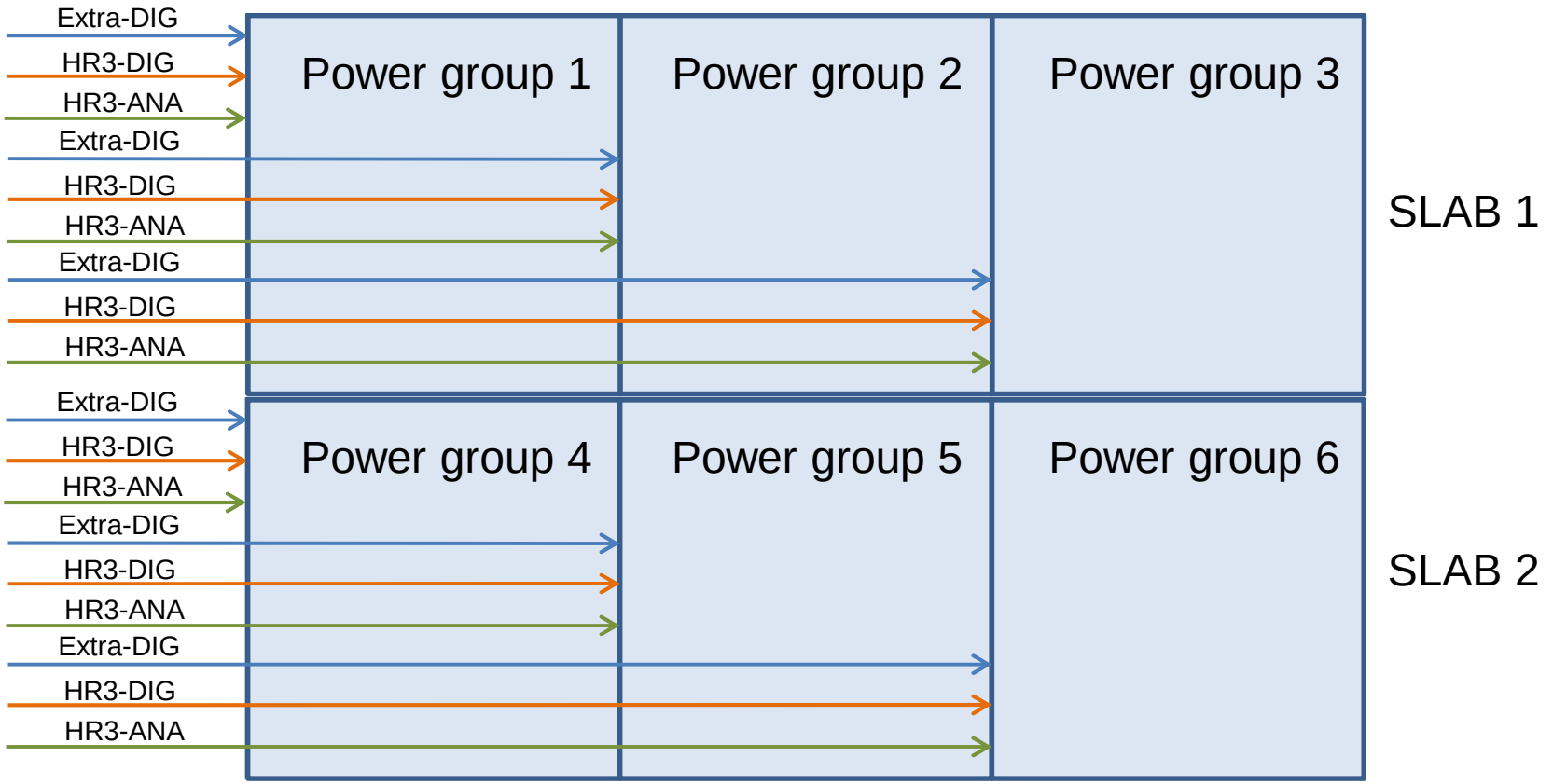
Power(W) estimations for the 3m² plane
(based on 1m² prototype measurements and HR3 requirements)

Power mode	Extra circuits	HR3 Analog	HR3 Digital	Total
Allways active	7,79	14,25	6,11	28,15
Power-Pulsing (0,5% duty cycle)	3,80	0,07	0,03	3,90

Expected current (A) required by the plane for the different power lines

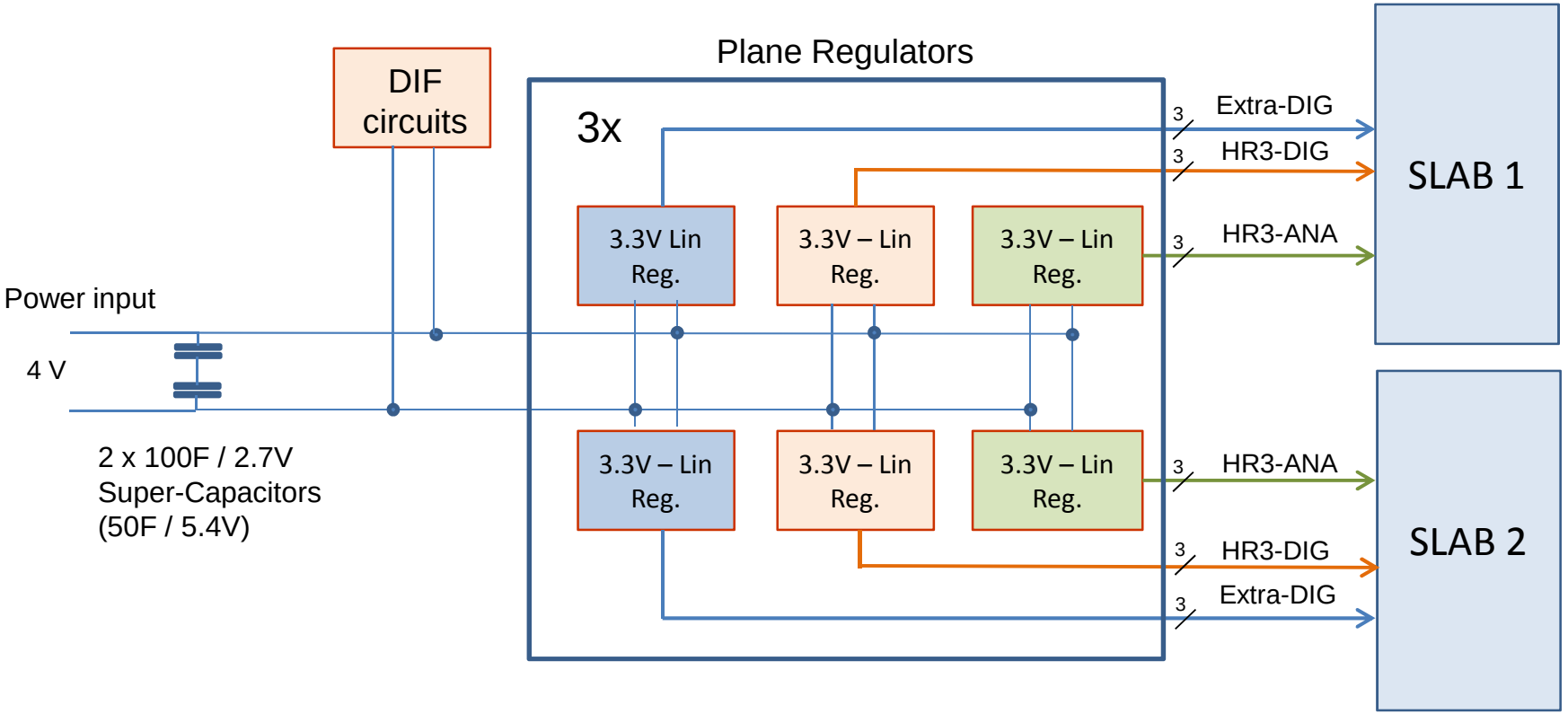
- To be able to switch OFF the “extra circuits” when they are not needed, we have splitted the digital power lines in two: one for the HR3 other for the “extra circuits”.

Power distribution- PLANE



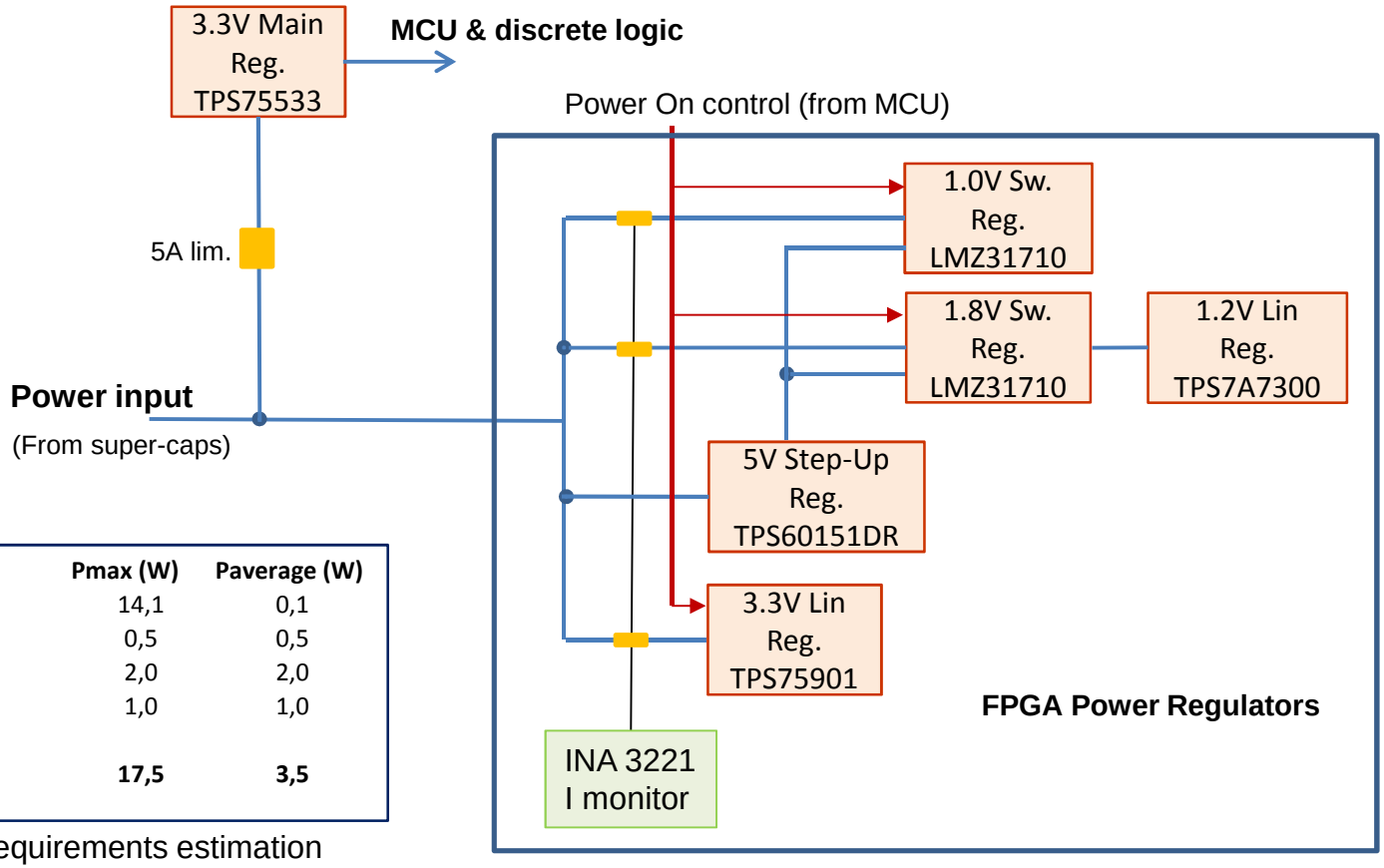
- To increase granularity (power fail reliability) the plane has been divided in six power groups
- Each group will be powered by a independent regulators at the DIF
- Voltages independently set for each group to compensate the voltage drops in the lines
- Each power group will contain 2 or 3 ASUs (depending on ASU size)

Power distribution - PLANE



- 18 Regulators needed to power the plane.
- All the regulators are low dropout type (about 500mV max). The input voltage can be as low as 3.8V to minimize the power dissipated in the regulators.
- Current monitoring and over-current protection per output voltage and slab (INA226)

Power distribution – DIF circuits



	Pmax (W)	Paverage (W)
Plane Regulators	14,1	0,1
DIF Regulators	0,5	0,5
FPGA	2,0	2,0
MCU and others	1,0	1,0
Total	**17,5**	**3,5**

DIF power requirements estimation

- FPGA and MCU can be set, also, to low power mode between bunches but it's difficult to calculate now the power savings in this mode
- Switching regulators have been chosen for lower voltages (1.0V and 1.8V) to reduce the power dissipation.
- FPGA Power ON sequencing will be done from the MCU.

Super Capacitors

- The main advantage is that the global power supply can be dimensioned to provide the average power and not for the maximum, as should be without the super-caps.
- The super-caps are the local storage for the current needed during the detector sort active period (0.5% of the time)
- In addition they provide some UPS effect. In case of power failure can provide some time (milliseconds) to recover data and switch off in a controlled way.
- The selection of the capacitors is based on the max current that they can provide and not in the needed energy to provide to the plane (with this criteria they would be much smaller).
- According to the power calculations the super-cap must be able to provide 30A @4V
- Most super-capacitors have a working voltage of 2.7V so we must use two in series to have the required voltage.

Current plane layout

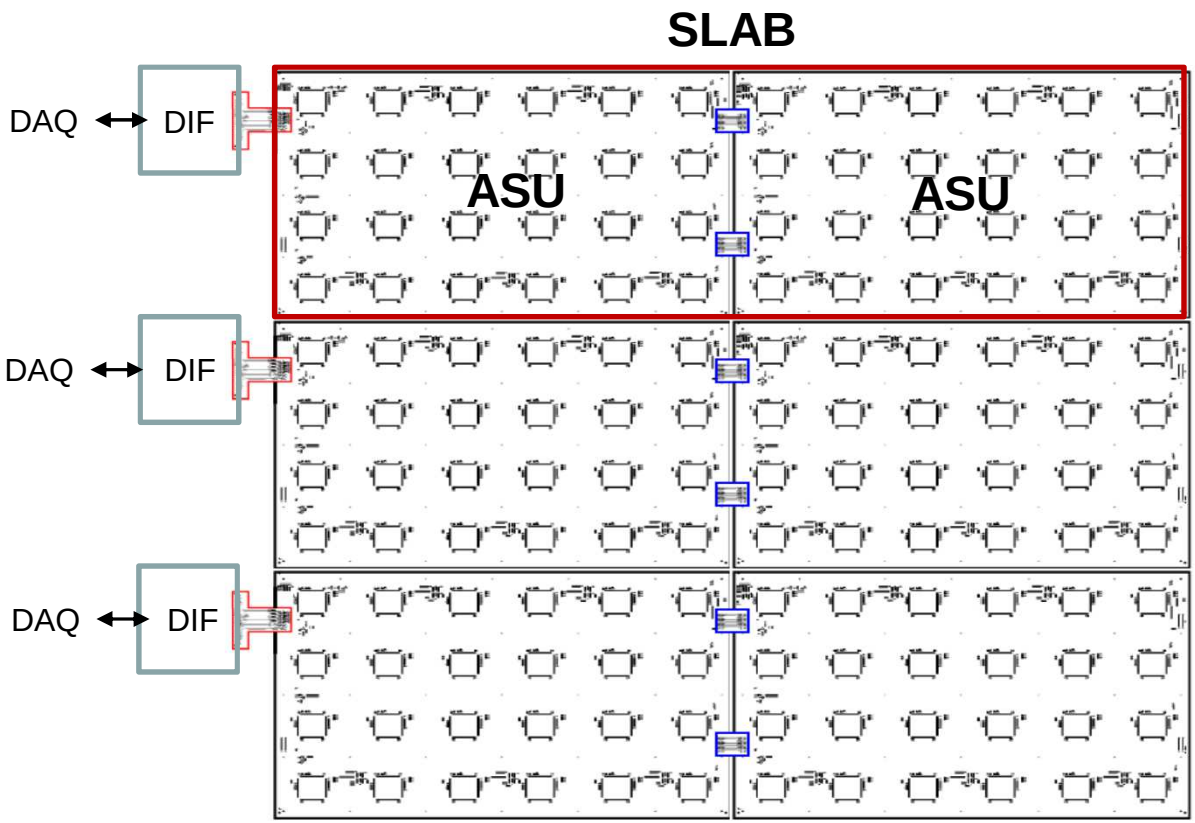
As it was not possible to produce the 1m² PCB in one piece, it was built assembling 6 ASU (Active Sensor Unit) boards

There are 144 HR in the 1m² plane and each ASU hosts 24 HARDROC (HR) chips.

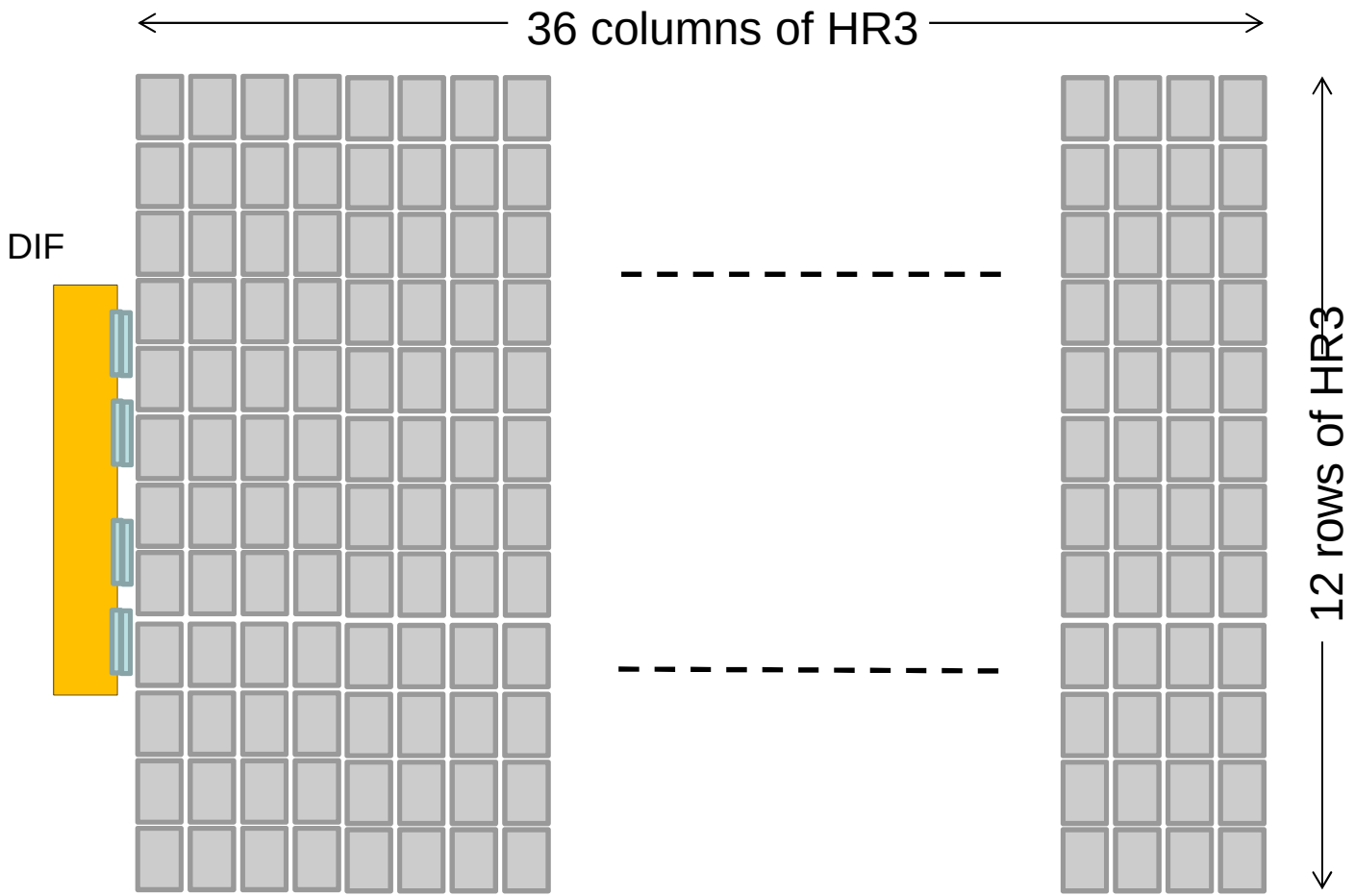
ASUs are connected two by two to form a 'slab'.

Each 'slab' is connected to a DIF (Detector Inter-Face) board

3 DIFs are needed for the 1m² plane



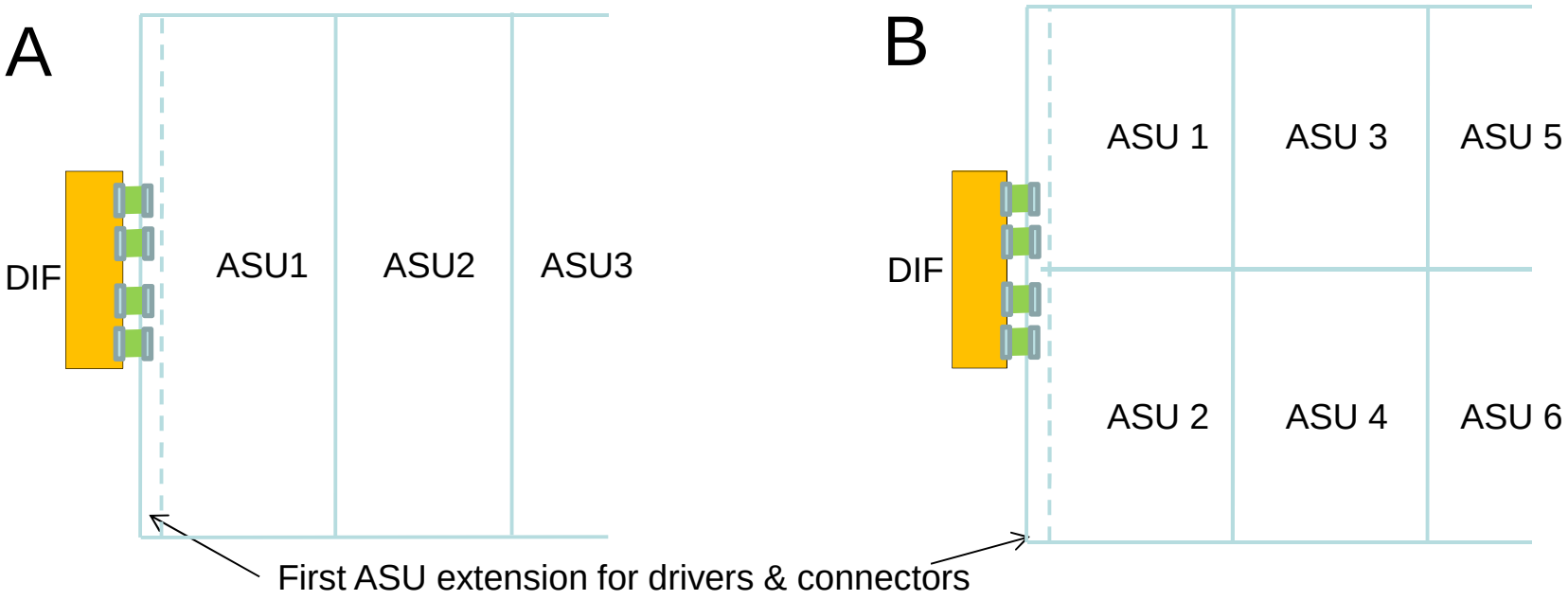
SDHCAL longest plane prototype: 3m x 1m



New DIF must be able to handle the SDHCAL longest plane
It will have 432 HR3 chips be splitted in several ASU boards

New plane layout options

As there will be only one DIF per plane, the distribution of the ASU boards in the plane could be rearranged to reduce the number of connections between the DIF and the plane

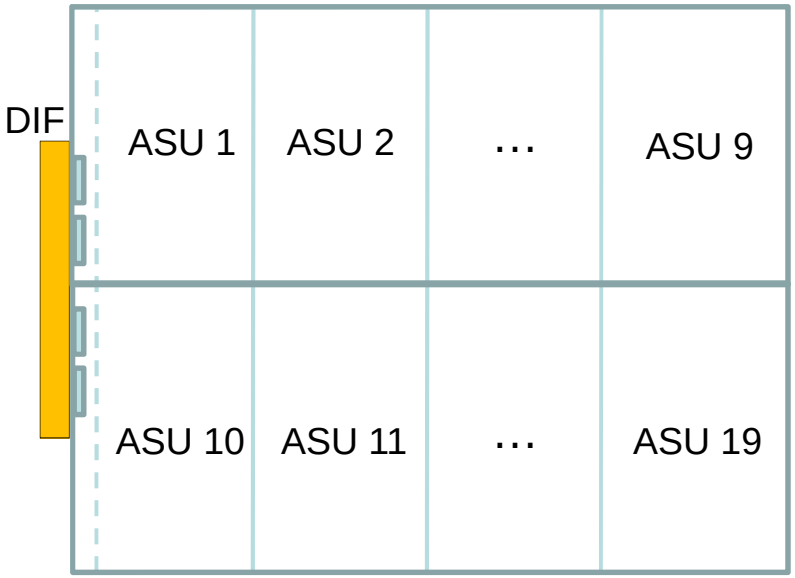


- Option A was the preferred because requires less pins on the DIF to plane connection because common signals can be sent only once. But it’s been discarded because it’s still not possible to produce the 1m long boards.

- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines.

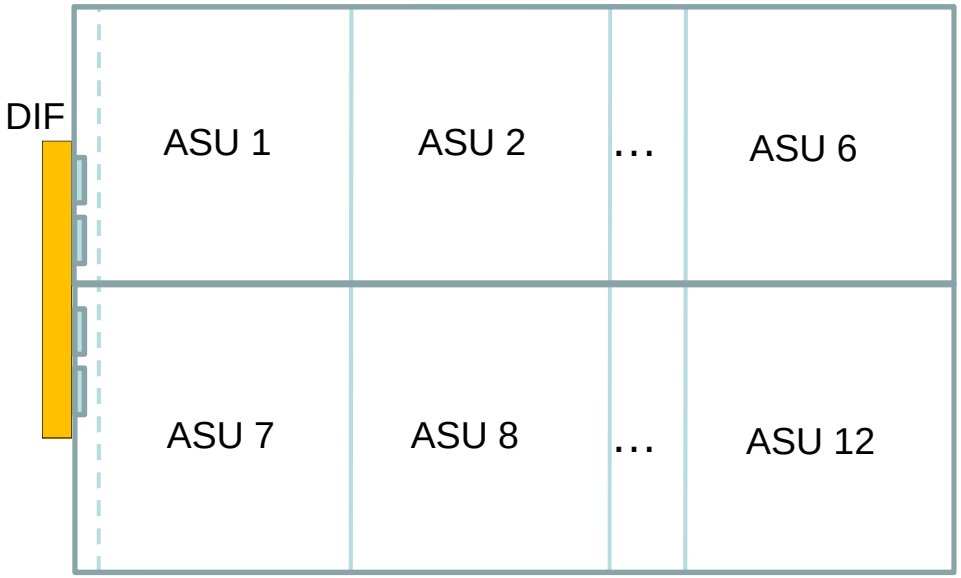
New plane layout options

B1



Layout with current ASU size (50 x 33 cm)

B2



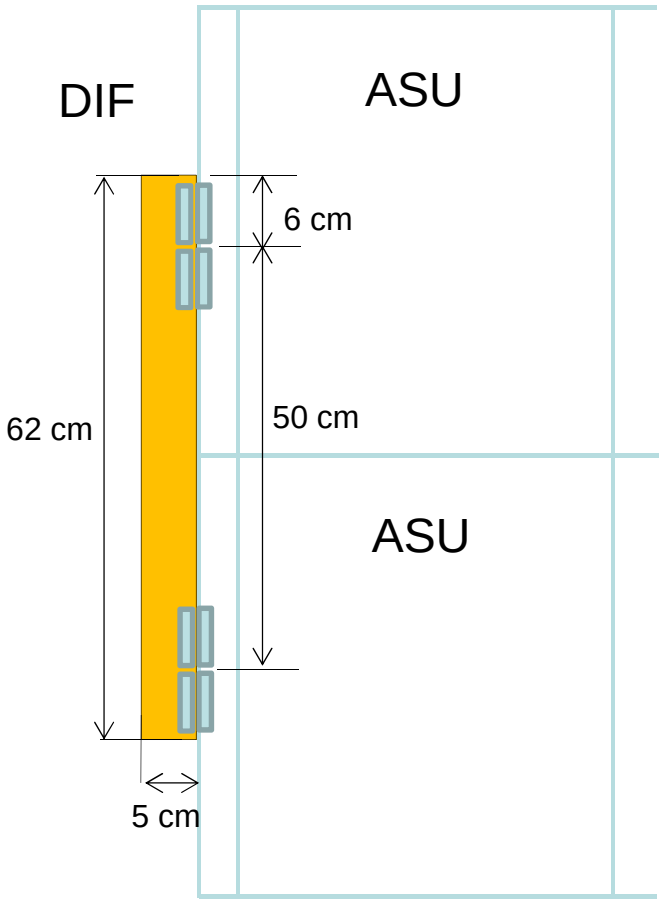
Layout with squared ASU (50 x 50 cm)

The less ASU boards in a SLAB the best because we reduce the number of connectors and this means:

- Lower voltage drops in the power supplies lines. Less power pins required for the ASU to ASU connectors.
- Lower resistance and capacitance in the data lines -> higher speeds

DIF to ASU connection

First approach – Direct connection



The selected connector (80 pins ERNI 1.27mm SMC series) requires 6cm long.

•Pros:

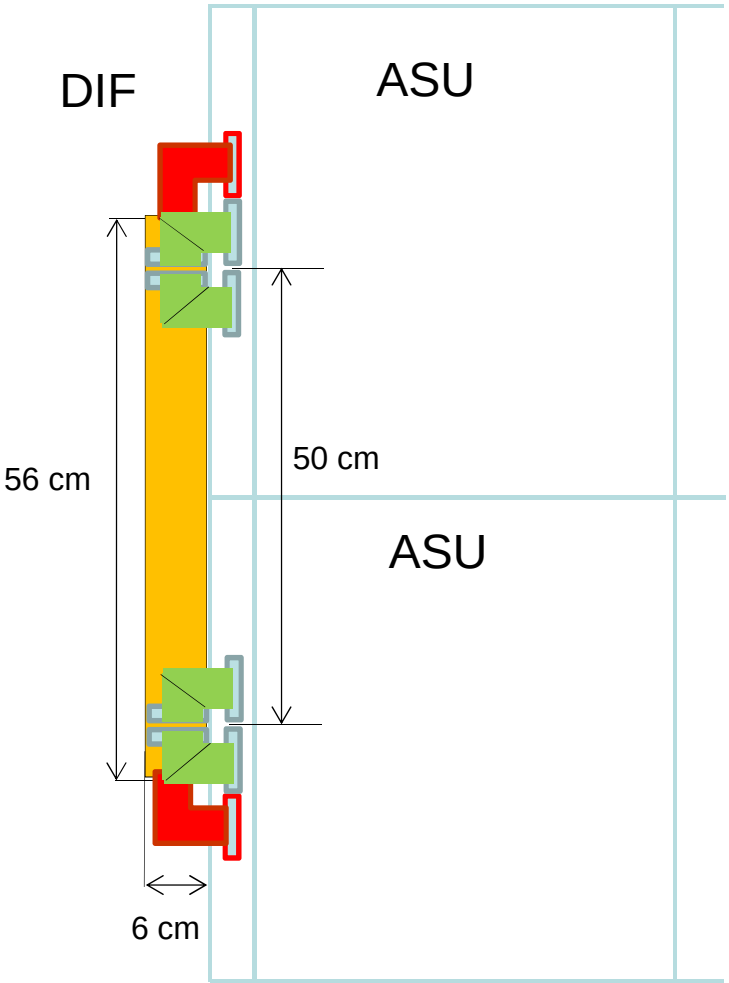
- Less connectors needed

•Cons:

- If the connectors are centered on the ASU the DIF should be 62cm long. The manufacturers we know only produce PCBs up to 60cm.
- If the connectors are not centered on the ASU:
  - Two different ASU layouts are needed or
  - The same layout can include connectors in two positions (only one equipped). But this will produce a lot of stabs (signal degradation)

DIF to ASU connection

Second approach – Cable connection



Pros:
- Decouples the DIF and ASU physical constrains.
- Can be produced at a known manufacturer.
- Same ASU layout with power connector in two possible positions.

Cons:
- Requires a 6cm width DIF and extra connectors for power lines.

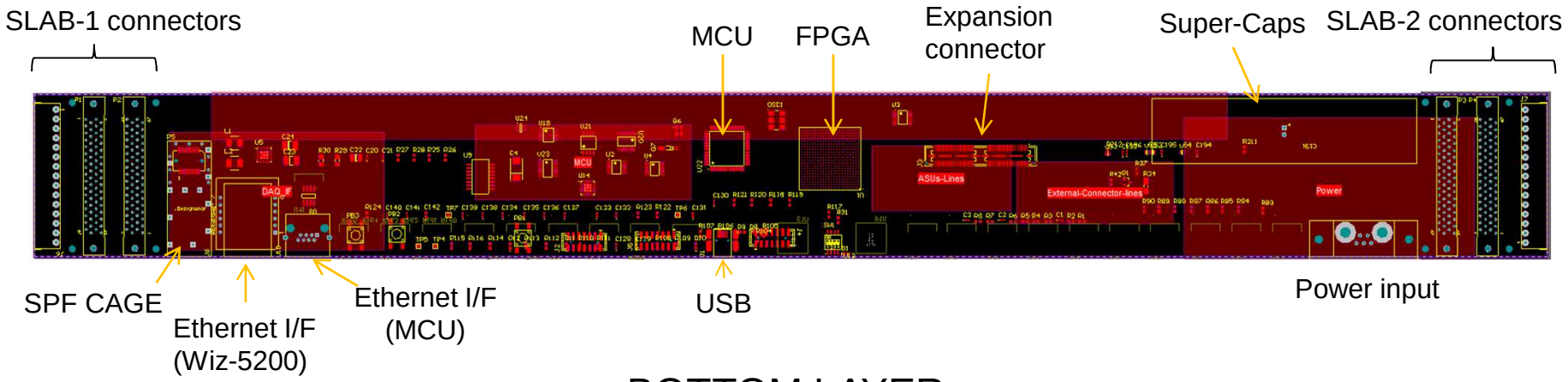
Direct connections are specified for 1A/pin but cable connectors are only specified for 0.5A /pin. As we will need about 15A per slab we would need about 60 pins (30 for power and 30 for GND) per slab. Almost one connector only for power.

ERNI connector + cable was discarded because they don't sell the cable connectors alone but the cable+connectors assembly. As it's not a very common connector size the cables are produced under request and the delivery time is 10 weeks. Other similar connector selected: KEL 8830E-068-170SD (widely used at CERN)

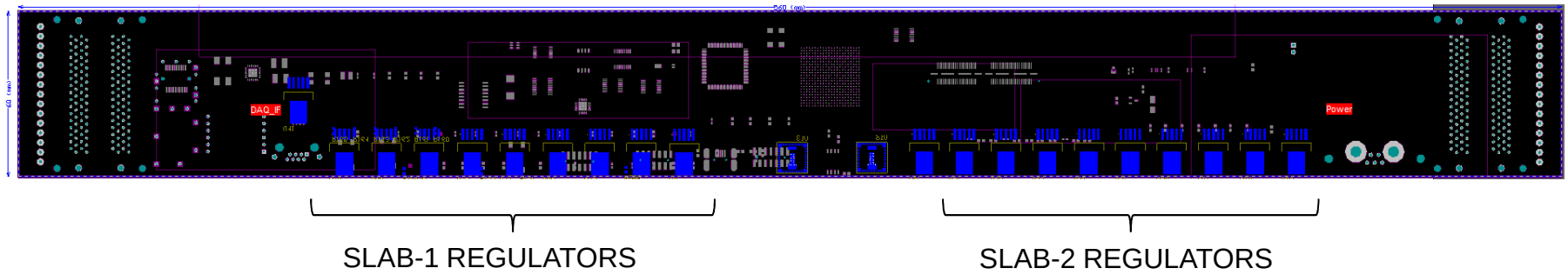
Power connector
Phoenix 1844346

DIF layout

TOP LAYER

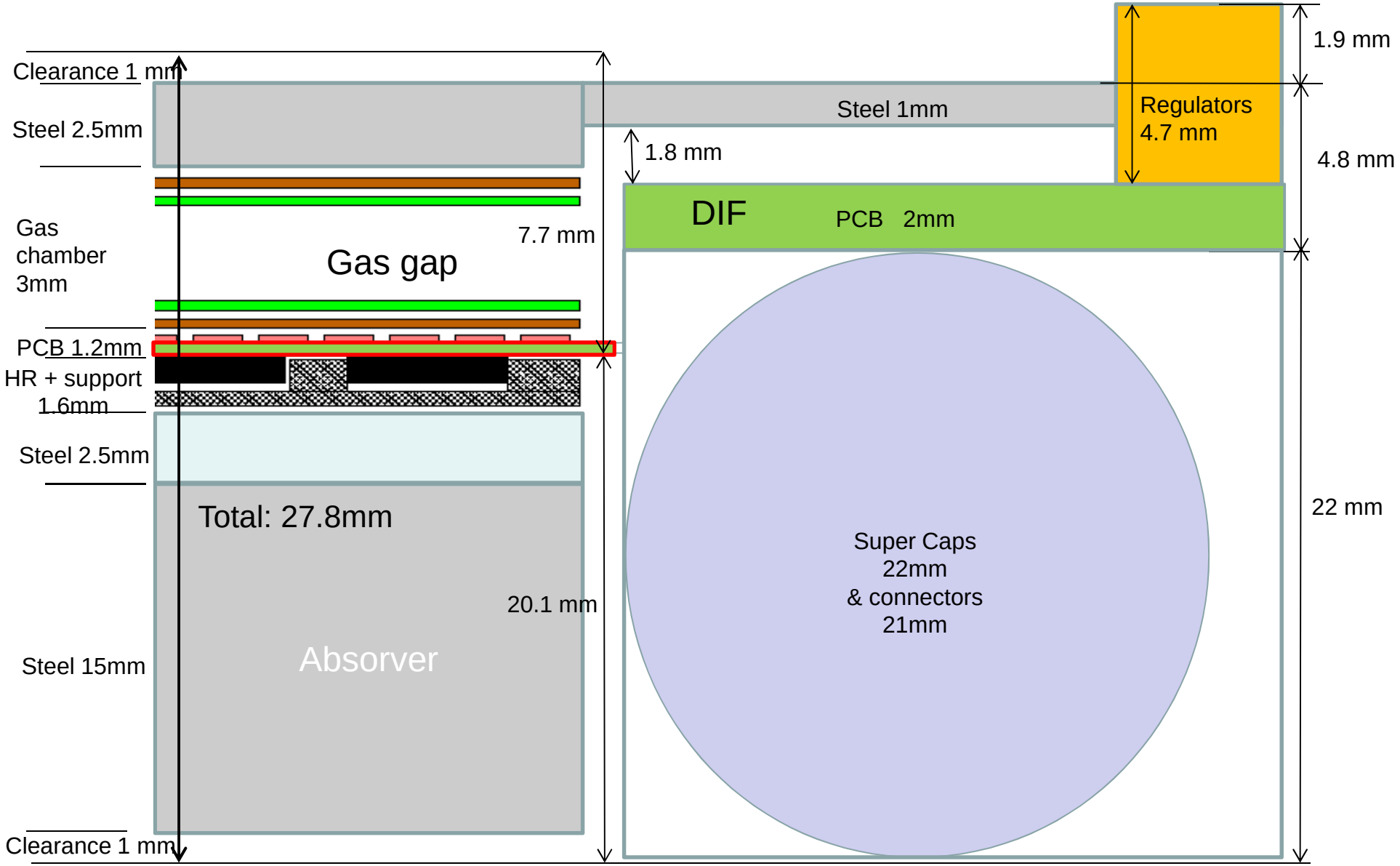


BOTTOM LAYER



- 60mm x 560mm, 2mm thickness and 12 layers board
- One of the goals of this DIF is to test the feasibility of its integration in the final detector plane where only 5cm will be available for it.
- If this layout is used 6 cm instead of 5 are needed due to the connectors length

DIF & Plane section view



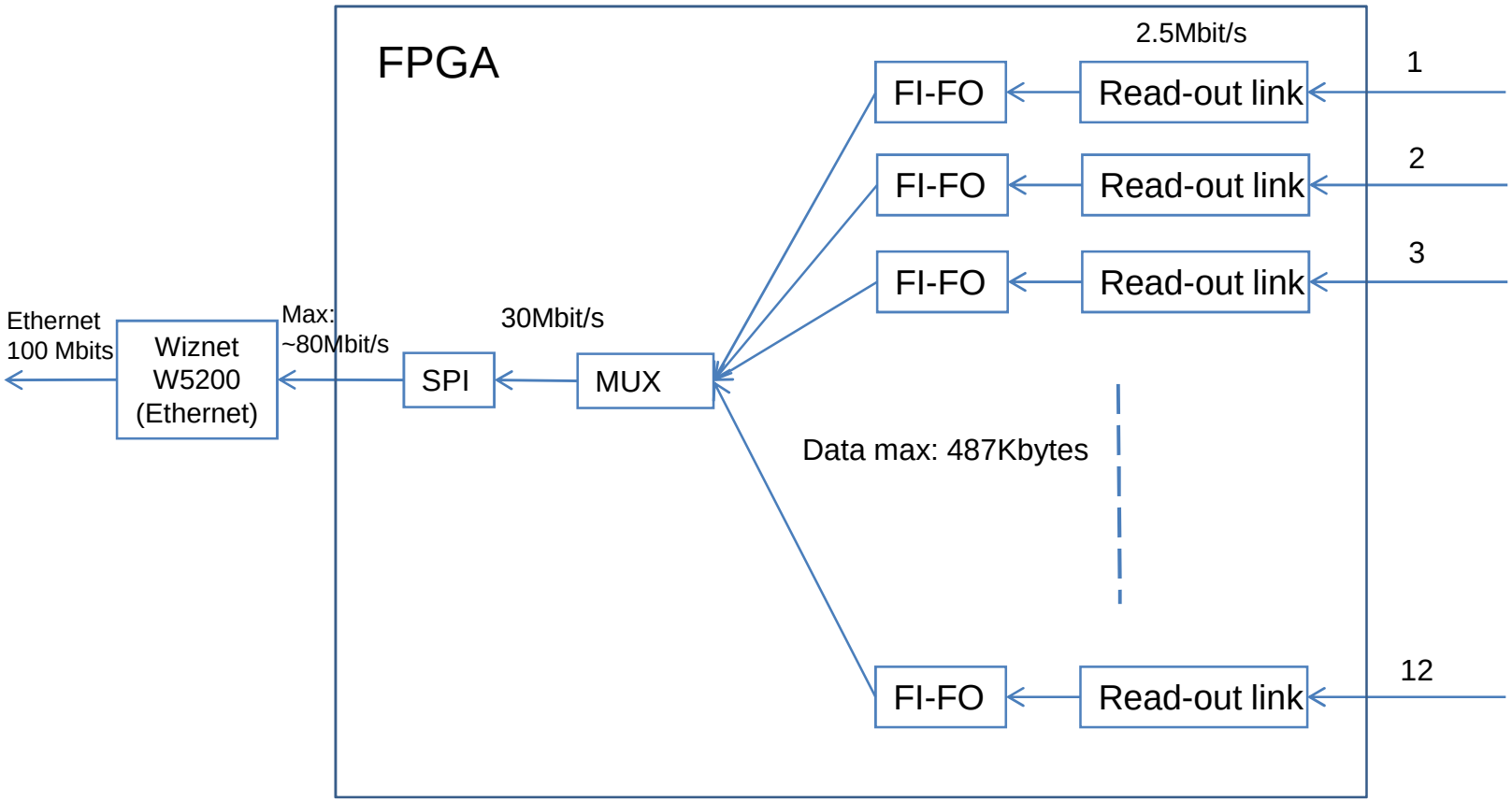
Plans

- Agree the DIF to ASU connectors placement with the SDHCAL team
- Continue with the PCB design
- First prototypes could be ready in 6 months.

End

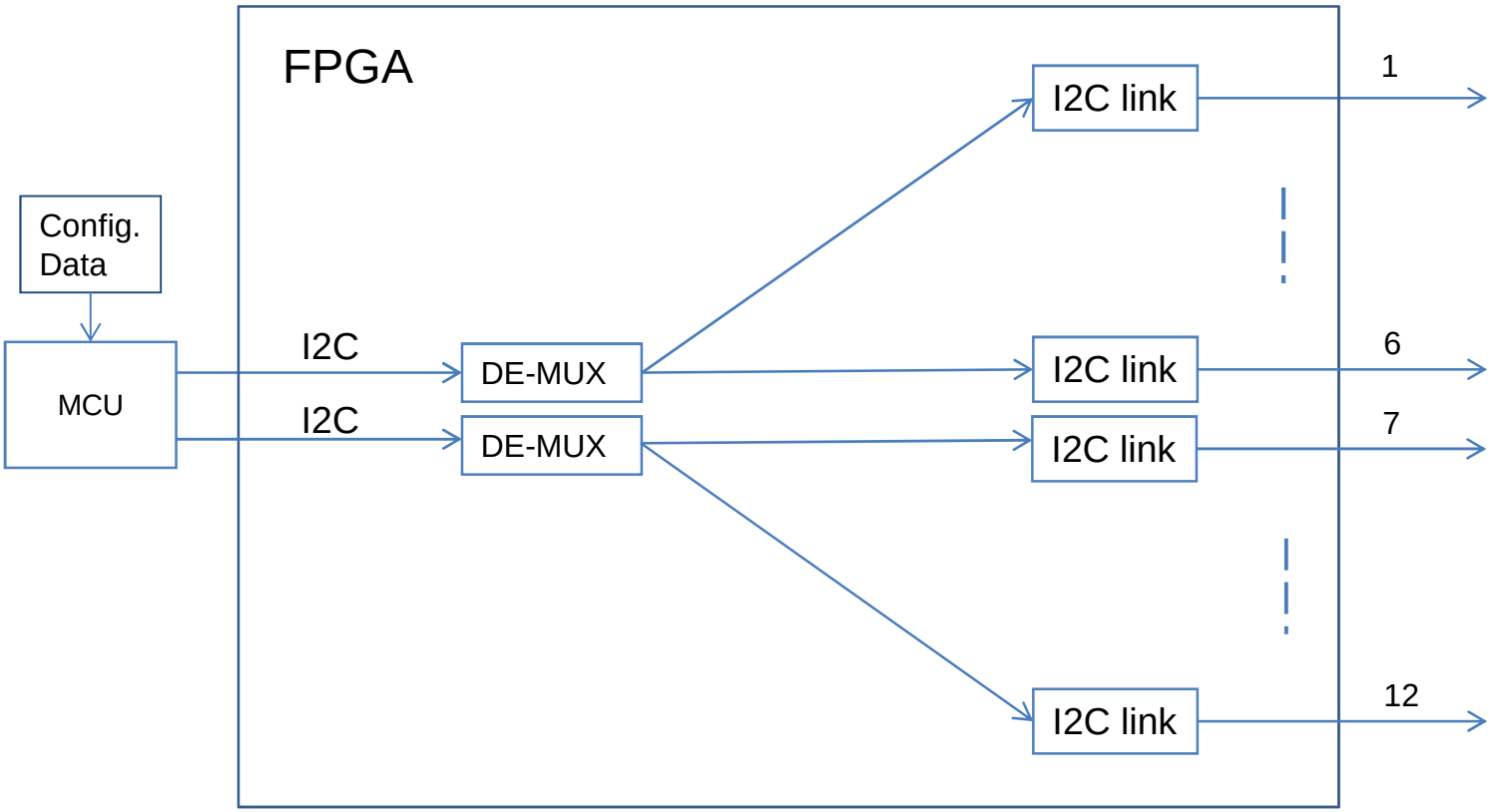
BACKUP

FPGA plane read-out



- Maximum read-out speed of the plane (30Mbit/s) is bellow the capacity of the output links.
- Data can be sent to the DAQ in real-time and there is no need of local storage in the FPGA during normal operation

FPGA I2C de-mux

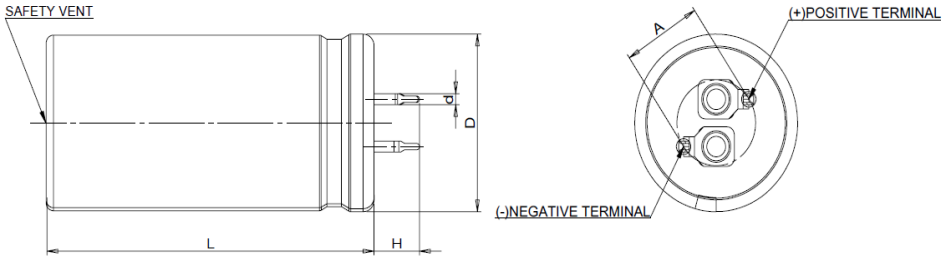


- Configuration data will be stored locally in the MCU flash memory
- It can be sent simultaneously both slabs
- With I2C can be sent only the registers to be updated

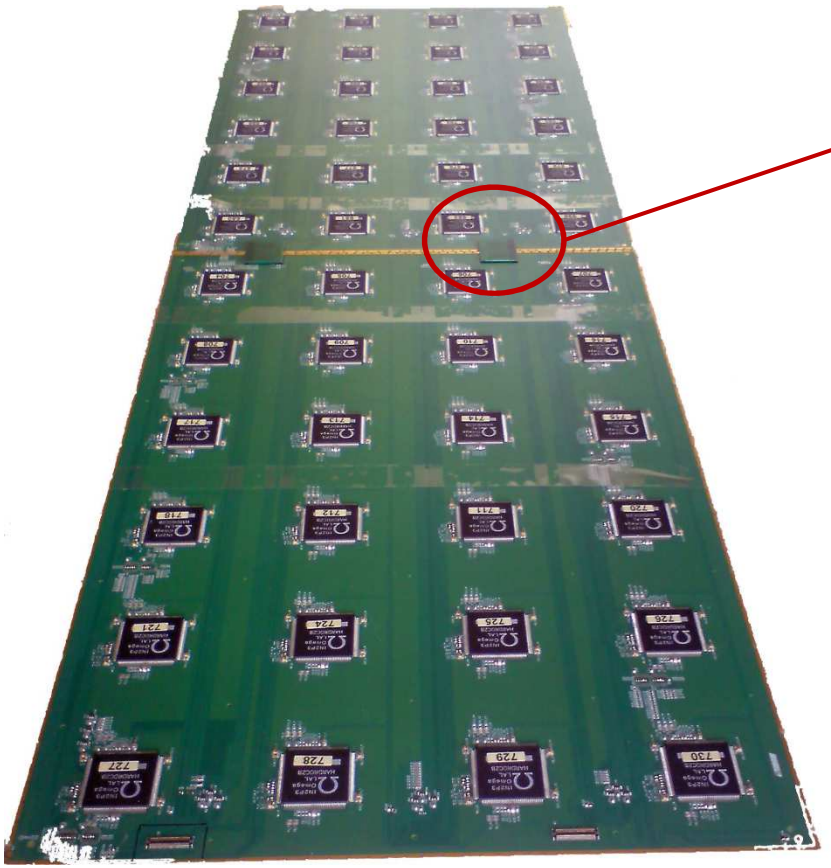
Super Capacitors

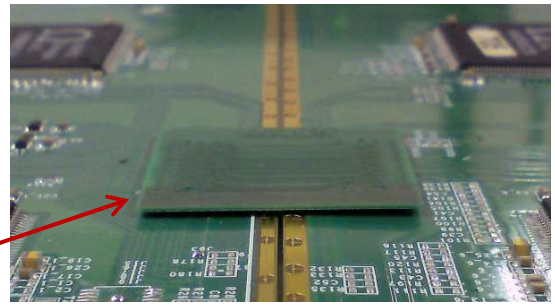
For the required current and taking into account the size constraint we've found that the capacity more suitable of us is 100F. There are several manufacturers that have these capacitors and they have similar specifications.

	Nesscap	Maxwell
Main characteristics	**2.7V / 100F**	**2.7V / 100F**
Maximum Continuous Current (40ºC)	17A	11A
Maximum Peak Current	52A	36A
ESR avg/max	8/12mΩ	15mΩ
Diameter (mm)	22	22
Length (mm)	45	45
Life	500000 cycles	
	10years @ 25ºC	
Price	10 €	9 €

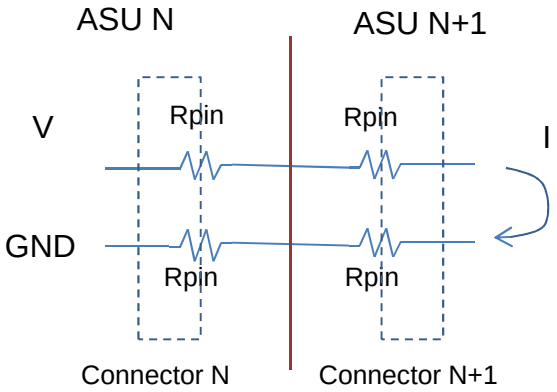


Voltage drops in the plane - ASU board





Detail of the ASU to ASU connector



- Each ASU to ASU connection adds 4 times the resistivity of one connector pin.
- The only way to reduce this resistivity is to increase the number of pins per power supply line.

Voltage drops in the plane (18 ASUs)

Assumptions:

- One power plane for HR3 digital
- One power plane for digital 'extra circuits'
- One power plane for analog
- One plane for analog GND
- One plane for digital GND
- ASU power plane resistivity: 0.3mΩ (assuming 35µm Cu thickness)
- Typical resistivity of a small connector: 60mΩ / pin
- Max current/pin in a small connector: 0.5A /pin

HR3 Requirements:

- Vdig from 3.1V to 3.5V
- Vana from 3.2V to 3.5V

Power line	ASU1	ASU2	ASU3	ASU4	ASU5	ASU6	ASU7	ASU8	ASU9
D_HR+3.3V	3,47	3,37	3,28	3,21	3,15	3,10	3,06	3,04	3,03
D_+3.3V	3,47	3,36	3,27	3,19	3,13	3,08	3,04	3,01	3,00
A_+3.3V	3,47	3,36	3,27	3,19	3,13	3,07	3,04	3,01	3,00

Out of specs

Voltage at each ASU with 3.5V at the DIF and **2 pins/ Ampere** in the ASU to ASU connectors

Power line	ASU1	ASU2	ASU3	ASU4	ASU5	ASU6	ASU7	ASU8	ASU9
D_HR+3.3V	3,47	3,42	3,38	3,34	3,31	3,29	3,27	3,26	3,26
D_+3.3V	3,47	3,42	3,37	3,34	3,30	3,28	3,26	3,25	3,24
A_+3.3V	3,47	3,42	3,37	3,34	3,30	3,28	3,26	3,24	3,24

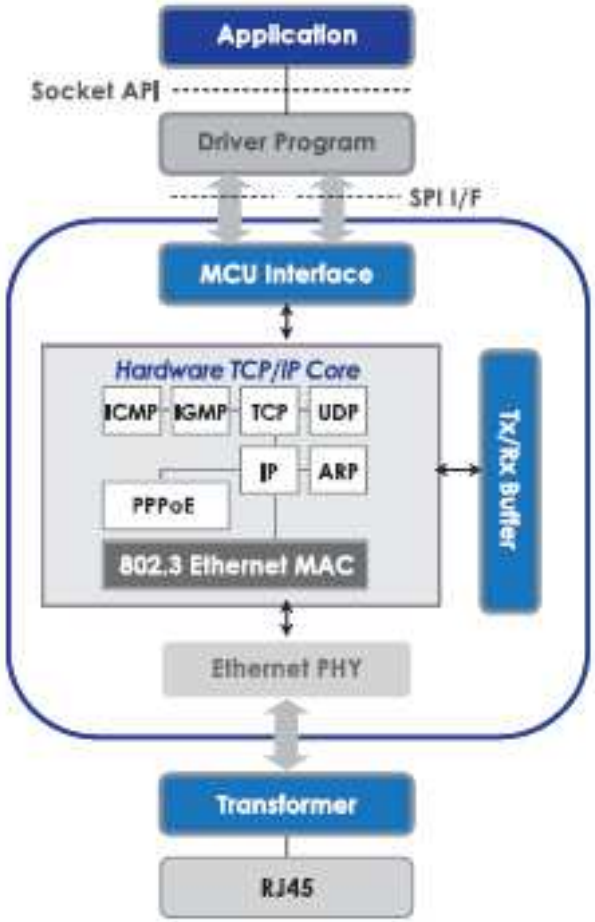
Voltage at each ASU with 3.5V at the DIF and **4 pins/ Ampere** in the ASU to ASU connectors

Ethernet chip W5200

iEthernet W5200

: Fast SPI Ethernet Controller

- Supports High Speed Serial Peripheral Interface (SPI Mode 0,3)
- Hardwired TCP/IP Protocols : TCP, UDP, ICMP, IPv4, ARP, IGMPv2, PPPoE, Ethernet
- 10 Base T/ 100Base TX Ethernet PHY Embedded
- Supports Auto Negotiation (Full & Half Duplex)
- Supports Auto MDI/MDIX
- Supports ADSL Connection (with PPPoE Protocol & PAP/CHAP Authentication Mode)
- Supports 8 Independent Hardware Sockets
- Internal 32 Kbyte Memory for TCP/IP Packet processing
- Supports Power Down Mode
- Supports Wake-On LAN
- 3.3V Operation with 5V Tolerant IO
- 48 Pin QFN Package



Ethernet module Wiz820io

SPI to Ethernet