HARDROC 3 for SDHCAL

02 / 02 / 2014 **- HGC4ILD Workshop**

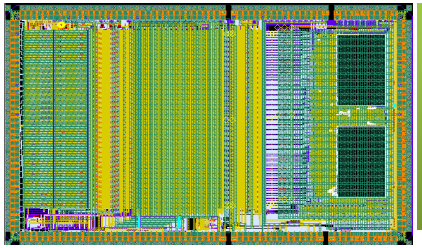
OMEGA microelectronics group

Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

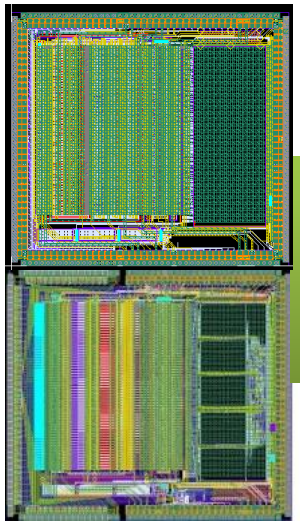
Organization for Micro-Electronics desiGn and Applications

ROC chips for ILC prototypes

Omega



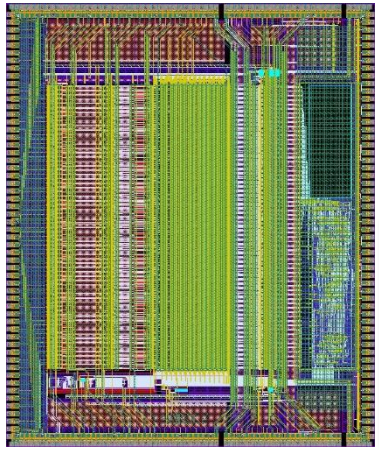
SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
June 07, June 08, March 10, Sept 11



AIDA

HARDROC2 and MICROROC
Semi Digital HCAL (sDHCAL)
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept 06, June 08, March 10

EUDET



Agence Nationale de la Recherche
ANR

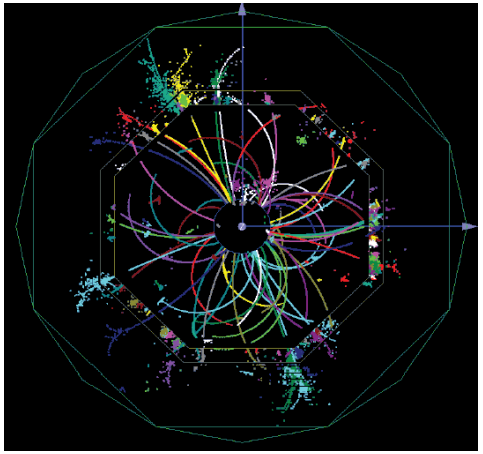
SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
March 10

CALICE
Calorimeter for ILC

ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (Eudet/Aida funded)

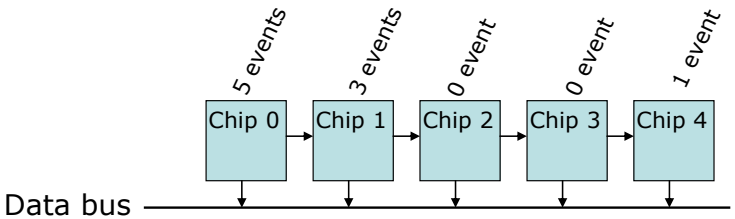
Requirements for electronics

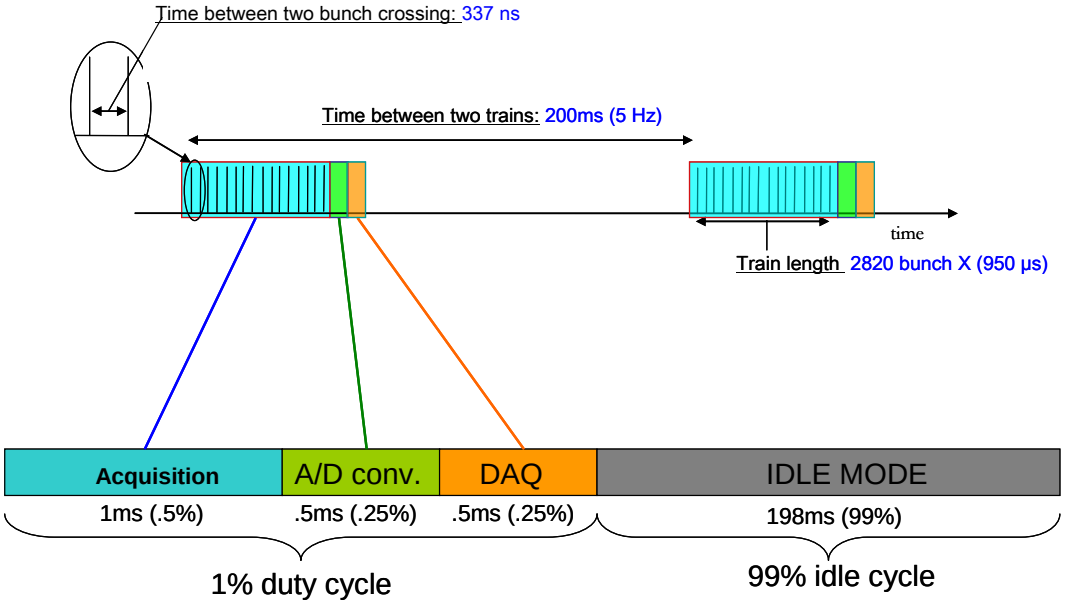
- Large dynamic range (15 bits)
- Auto-trigger on ½ MIP
- On chip zero suppress
- **10^8 channels**
- Front-end embedded in detector
- **Ultra-low power : 25µW/ch**

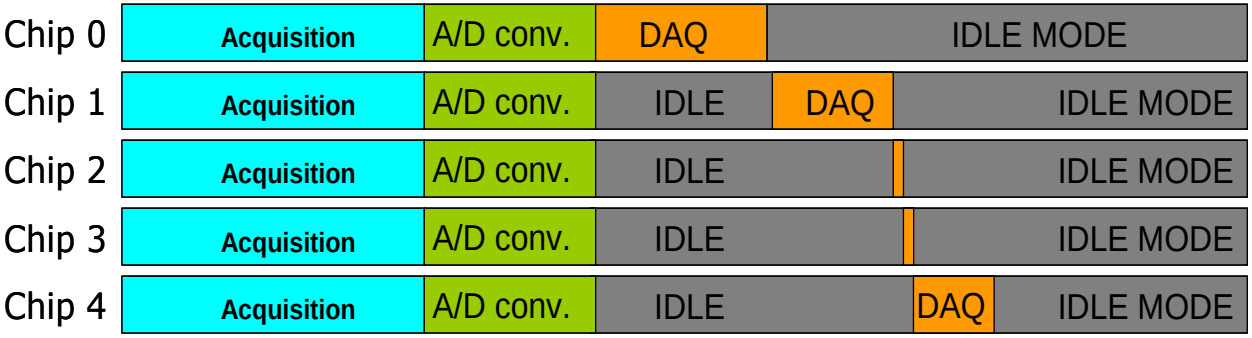


From 2nd generation…

- **2nd generation chips for ILD**
  - Auto-trigger, analog storage and/or digitization
  - Token-ring readout (one data line activated by each chip sequentially)
  - Common DAQ
  - Power pulsing : <1 % duty cycle

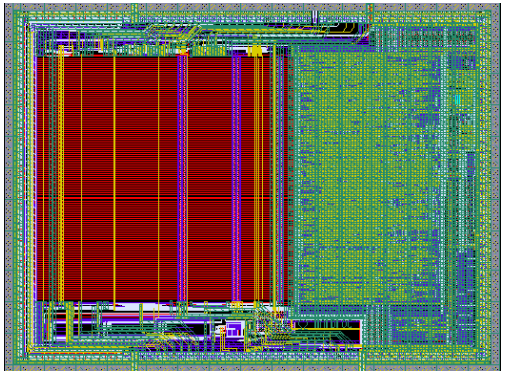




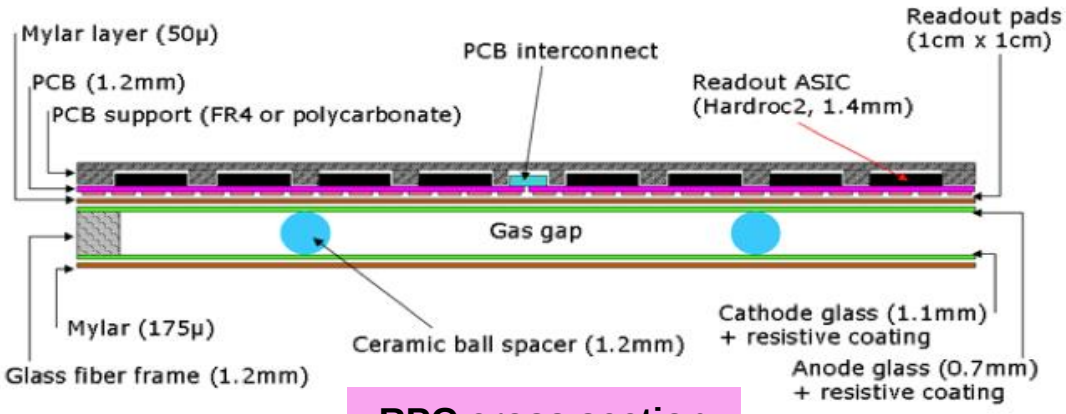


…To 3rd generation

- 3rd generation chips for ILD
  - Independent channels (zero suppress)
  - I2C link (@IPNL) for Slow Control parameters and triple voting
    - configuration broadcasting
    - geographical addressing



- HARDROC3: 1st of the 3rd generation chip to be submitted
  - Received in June 2013 (SiGe 0.35µm) (AIDA funded)
  - Die size ~30 mm² (6.3 x 4.7 mm²) - Packaged in a QFP208

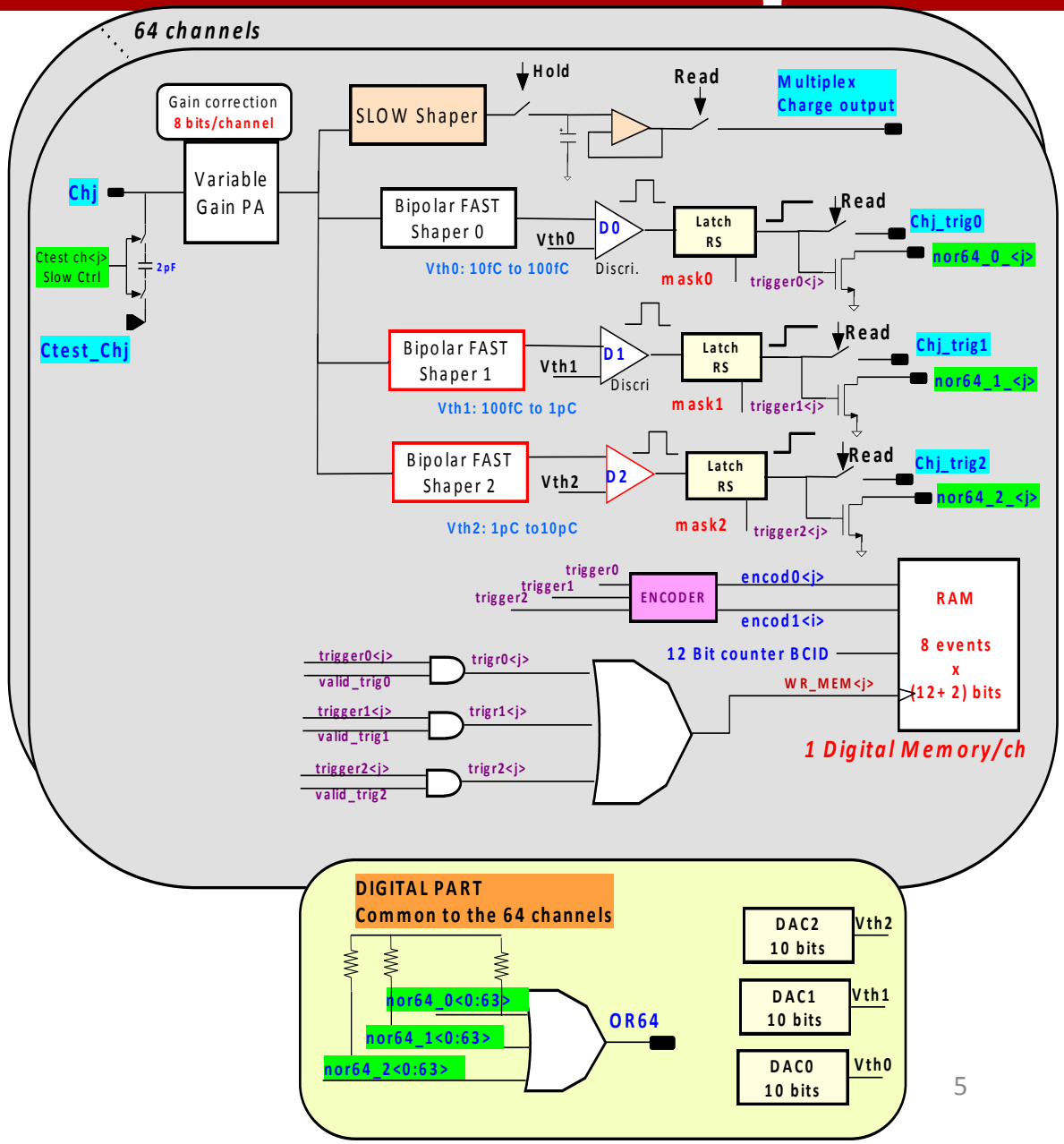


RPC cross section

1m² RPC [IPNL]

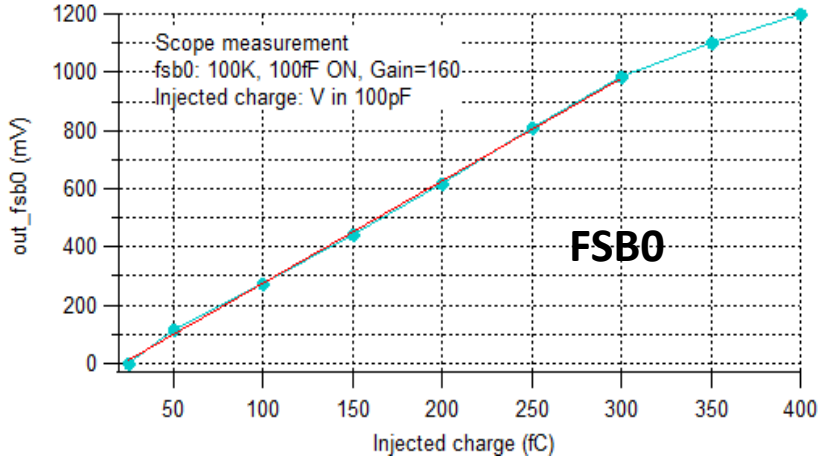
HR3: Simplified schematics

- 64 channels with current preamplifiers
- Trigger less mode (auto trigger 15fC up to 10pC)
- Gain correction (max factor 2)
- 3 shapers + 3 discriminators (encoded in 2 bits for readout)
- I2C link for Slow Control
- Independent channels with zero suppress
- Max 8 events / channel with 12-b time stamping
- Integrated clock generator: PLL
- Power pulsing mode

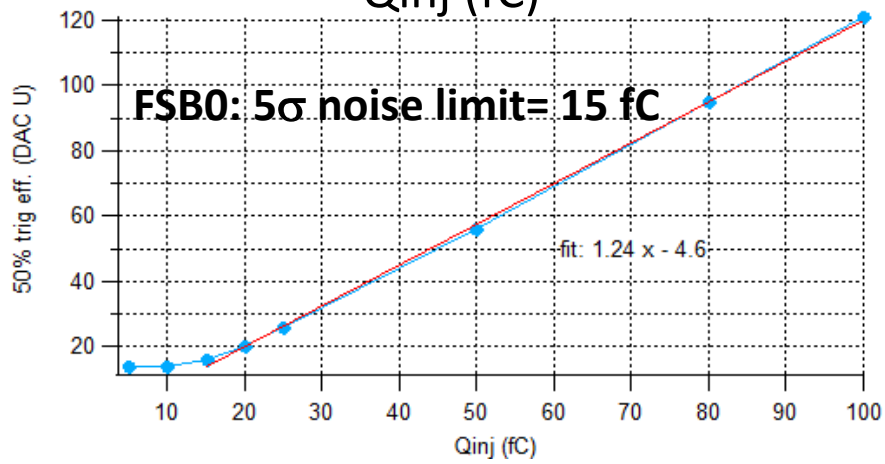


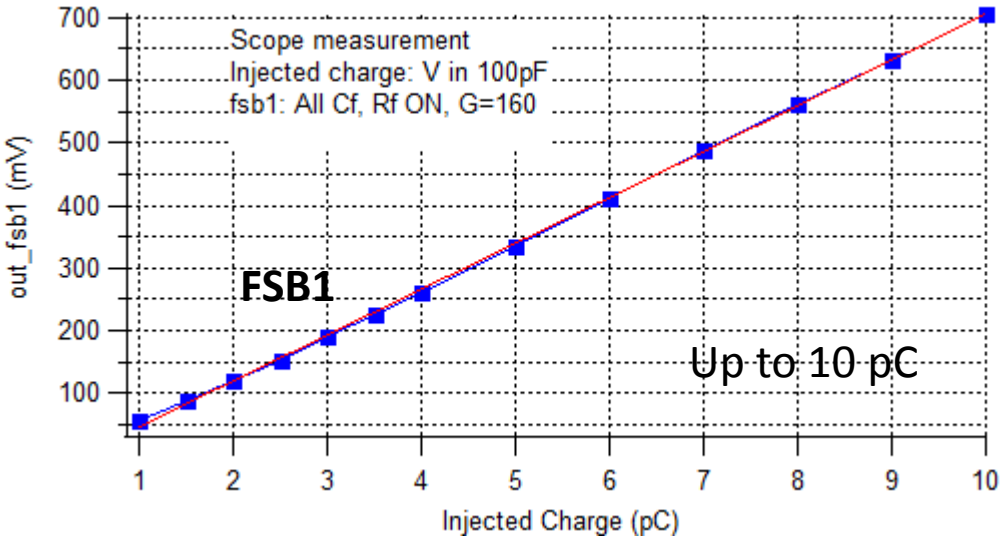
Analog Part: FSB Linearity

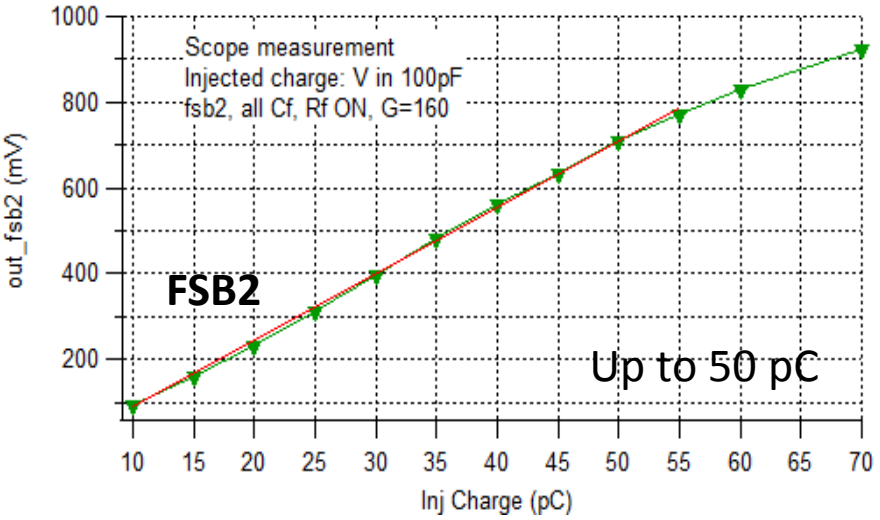
Fast shaper outputs (mV) vs Qinj (fC)



50% trigger efficiency (DAC units) vs Qinj (fC)



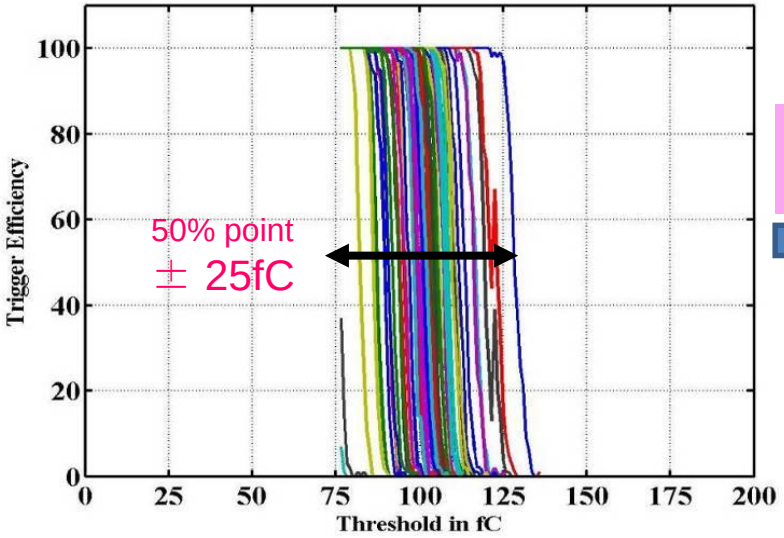




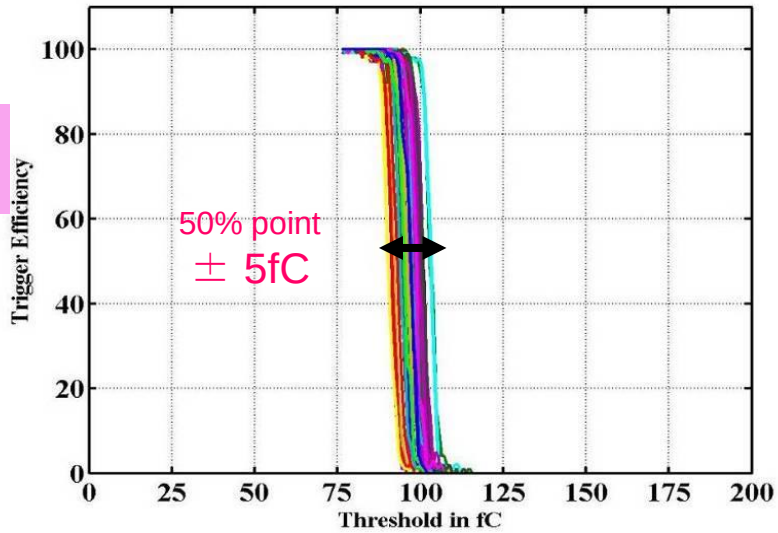
Dynamic range: 15fC - 50 pC

Gain correction / Scurves

Qinj=100fC



HR2 gain correction

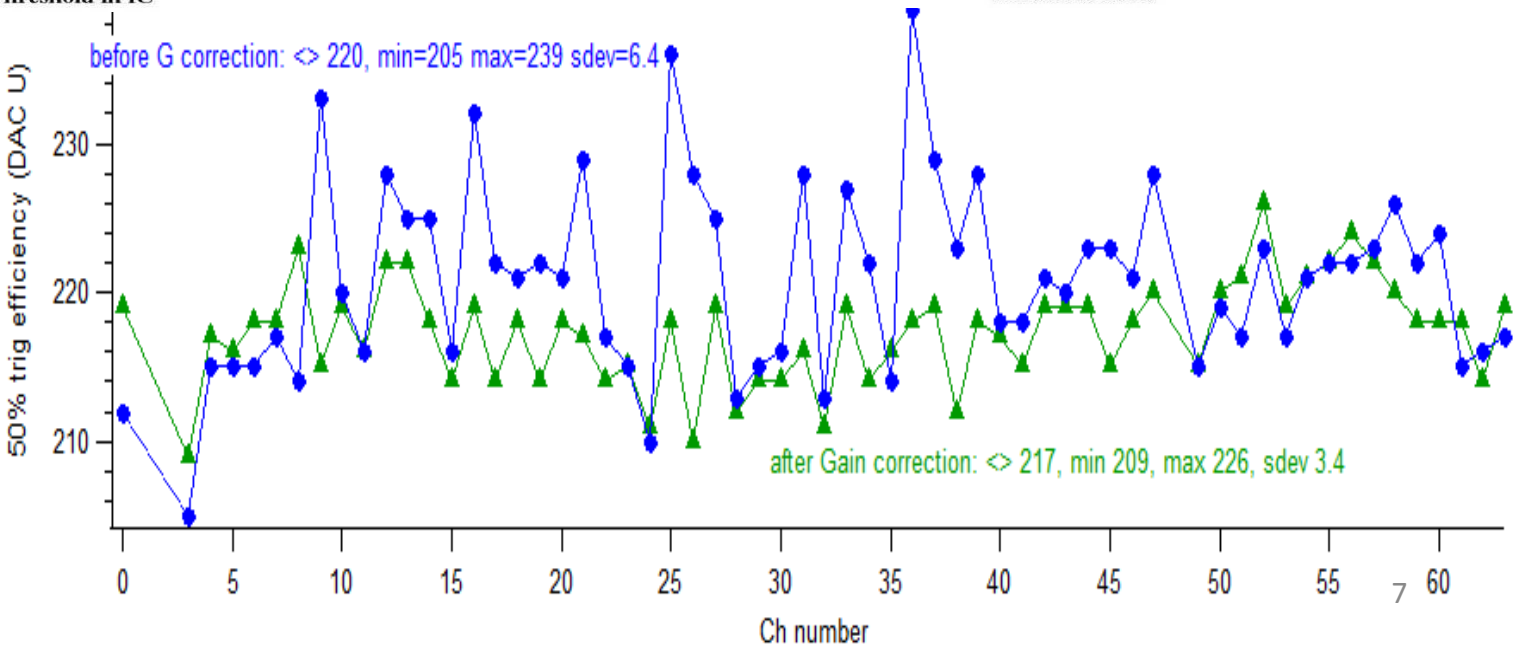


HR3: extracted 50% Scurves point vs Channel number

Before: ± 17 DACU

After: ± 8 DACU

(± 6 fC)

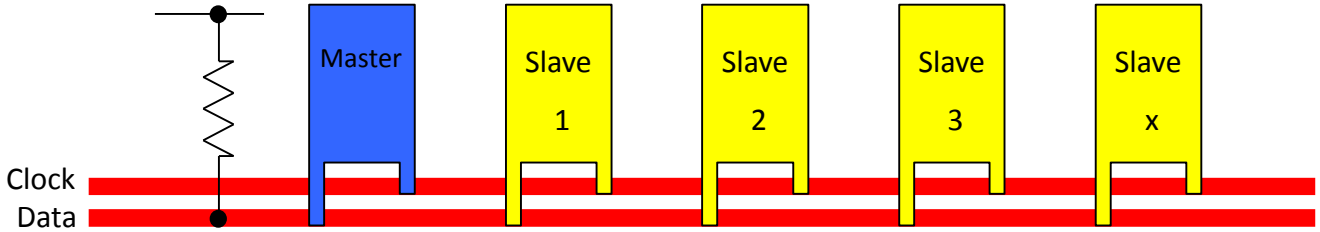


New Slow Control: I2C

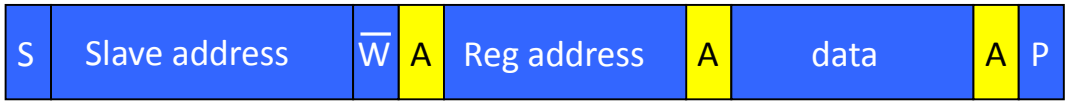
- I2C standard protocol access (max 127 chip / line)

- Possibility to broadcast a default configuration to all the chips
- Read and write access to a specific chip with its geographical address

- Triple voting for each parameter (redundancy)
- Read back of control bit (even if the chip is running / copy)



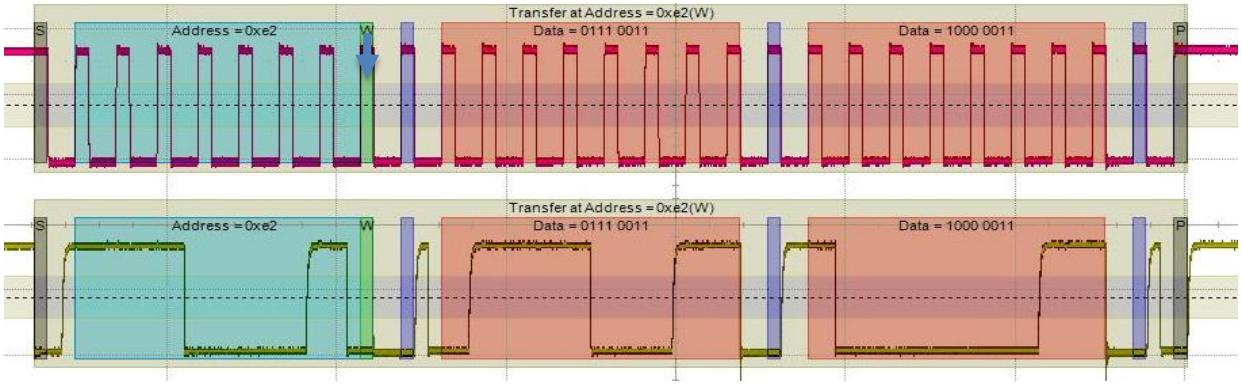
Write frame:



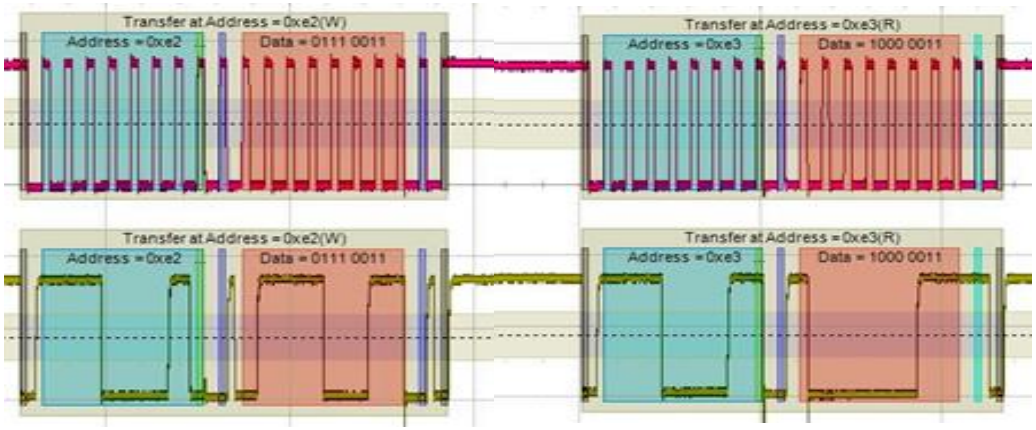
Read frame:

I2C measurements

- I2C Write acces : Chip number (ID): 0xE2 / Reg @: 0x73 / WrData: 0x83

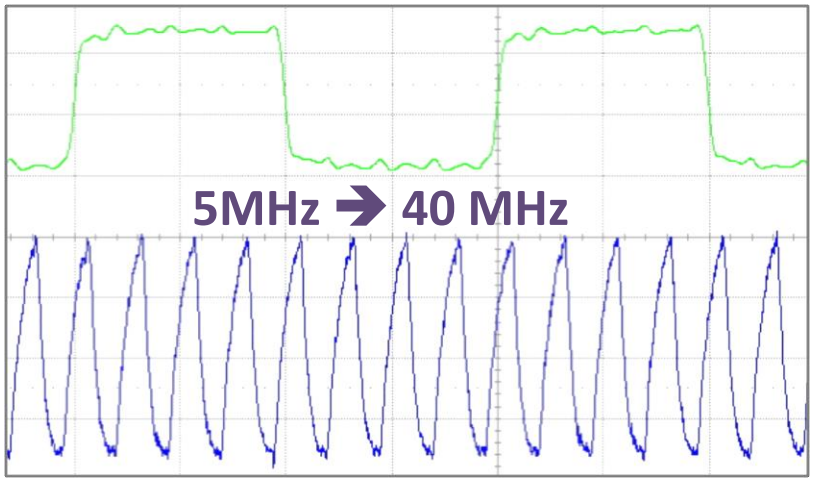


- I2C Read acces : Chip number (ID): 0xE2 / Reg @: 0x73

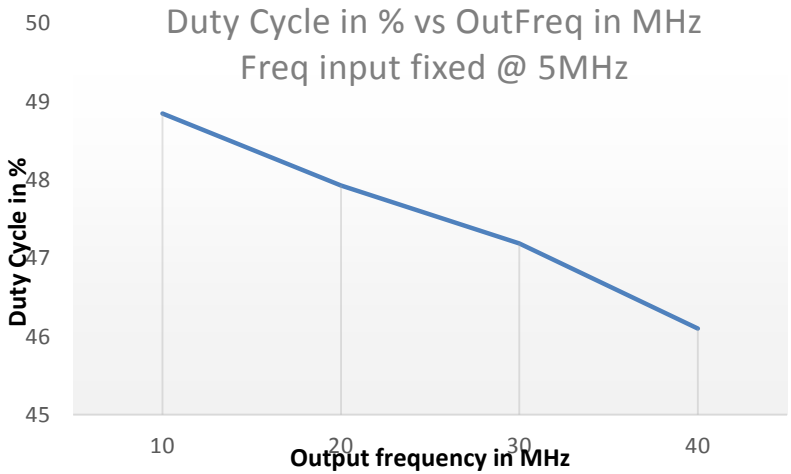


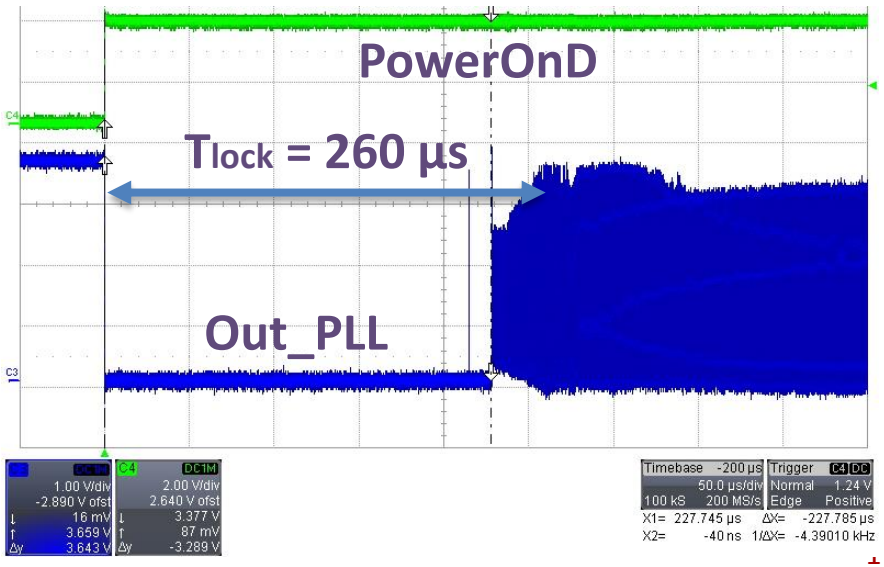
PLL measurements

- **2 clocks are needed to start the chip**
  - Slow Clock (1-10 MHz) related to the beam train (for Time stamping and data readout)
  - Fast clock (40-50MHz) for internal the state machines



- **A PLL (clock multiplier) has been designed to generate the fast clock**
  - Multiplication factor is (N+1) / N is a SC parameter (1 to 31)
  - Full chain tested using PLL

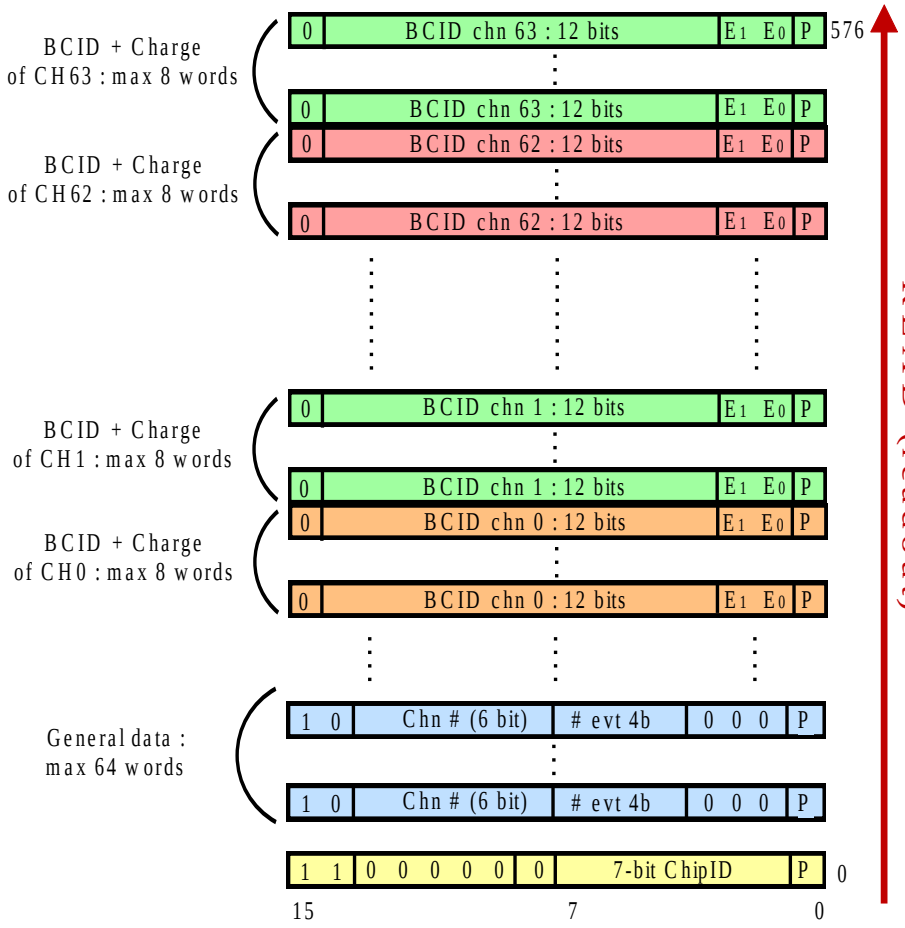




Zero suppress: Memory mapping

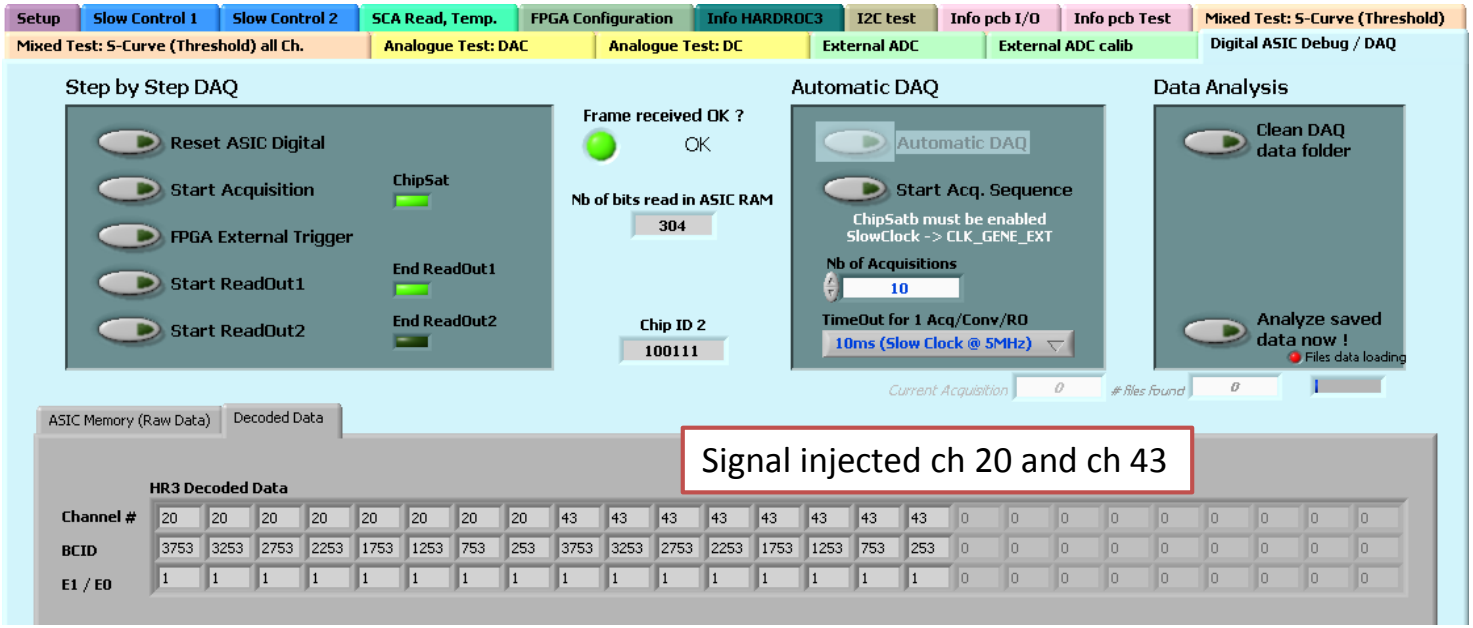
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



Zero suppress: Tests

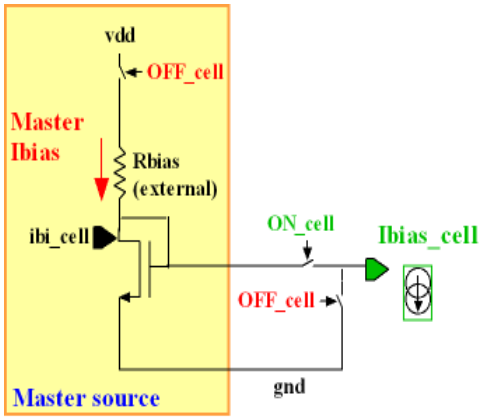
- Zero suppress (only hit channels are readout): test OK



- Roll mode SC : test OK
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : test OK
- "ARCID" SC (Always Read Chip ID): test OK
  - If ARCID = 0 ➔ Backward compatibility: No event ➔ No readout
  - If ARCID= 1 ➔ New behavior: No event ➔ Read CHIP ID

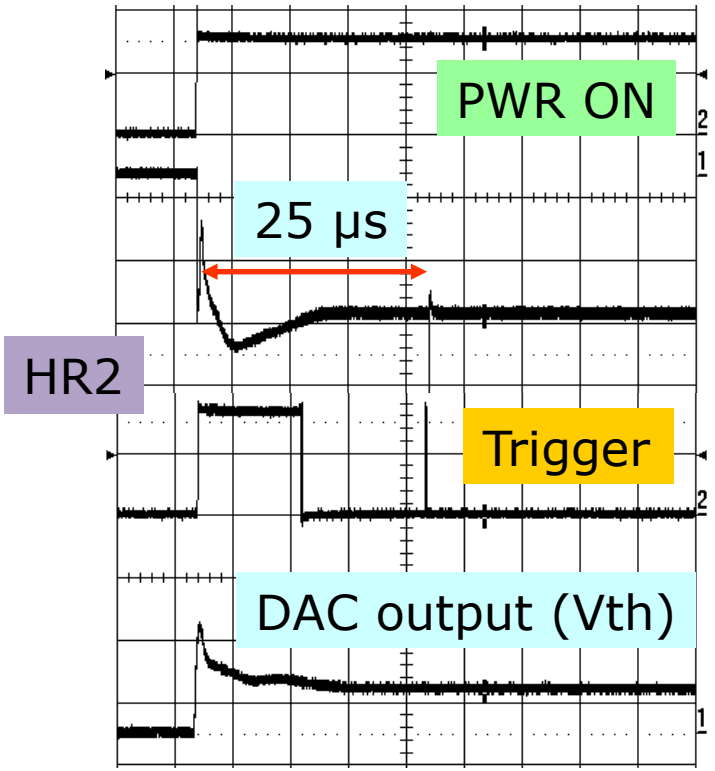
Power pulsing in HR chips

- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**



- Compared to HR2, HR3 power consumption is higher due to:
  - The extended dynamic range (from 15pC to 50pC)
  - The integration of the zero suppress algorithm
- If the PLL is used, the power consumption is increased by 3% (due to the PLL VCO)

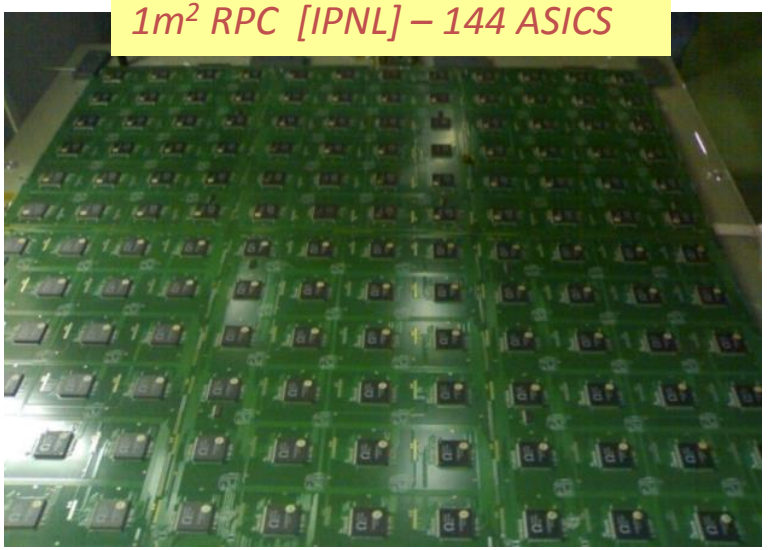
Power supply	HR3 with LVDS (5M + 40M) µW / channel	HR2 with LVDS (5M + 40M) µW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	**12,2**	**7,5**



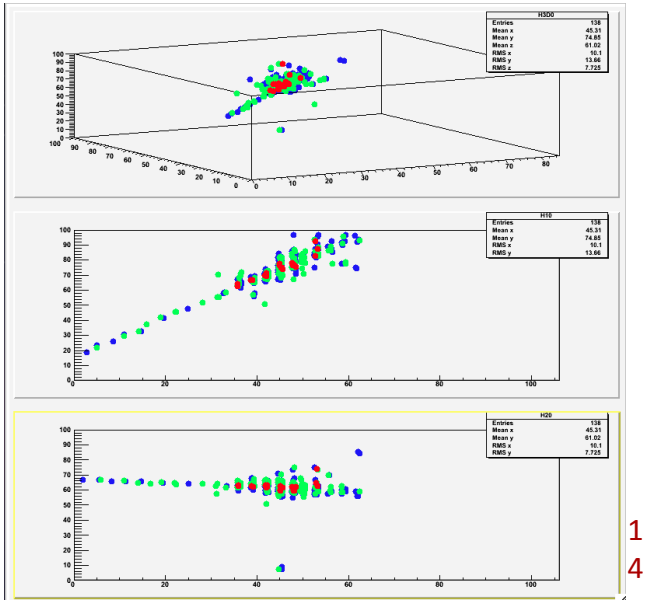
Power pulsing: Testbeam HR2

Omega

- SDHCAL technological proto with up to 5**0 layers** (7200 HR2 chips) built in 2010-2011.
- Scalable readout scheme successfully tested
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**



Vth0 Vth1 Vth2



Summary and next steps

- Good analog performances
  - Dynamic range extended up to 50 pC
  - Circuit is able to work with only 1 external clock (thanks to PLL)
  - New I2C tested successfully
- New digital features validated on testboard
  - Zero suppress, roll mode, ARCID mode and Noisy event mode
  - External trigger available to be able to check the status of each channel
- Next steps
  - Production run (HR3 + 11 others chips) will be submitted mid-February 2015
  - 2-3m long RPC chambers to be built and equipped with HR3 in 2015
- Moving SPIROC / SKIROC to 3rd generation
  - Much more complicated due to internal ADC / TDC / SCA management
  - Integration and tests of HR3 on the 2-3m long RPC will be very helpful