SiPM read-out ASIC

CTA-LAPP meeting

1/12/2014

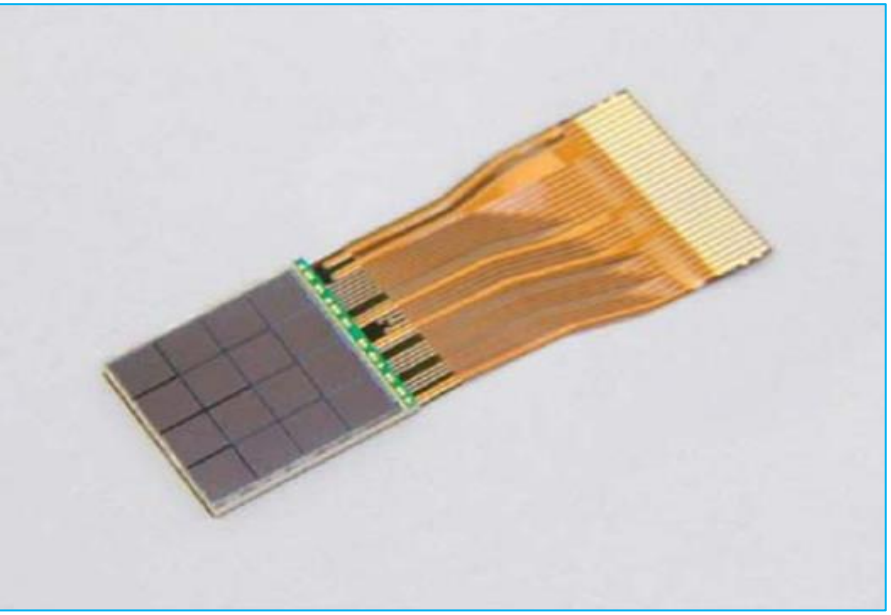
Work chain

- Characterization tests of a SiPM based detector.
  - Aim to conclude the readout circuit specifications
- Readout electronics:
  - Read-out ASIC design and simulation…ALPS
  - Board test design and test facilities preparation
  - ASIC performance verification with & without the detector

I. SiPM Characterization

- Project started on February 2013
- Presentation @ Munich July 2013 – SiPM advanced user workshop….

SiPM detector@ LAPP



- Hamamatsu detector:
  4x4 macro pixel array
- 1 macro pixel =3x3 mm^2 SiPM.
- 1 macro pixel = 3600 micro pixel(50µm).
- 1 macro pixel = an array of parallel-connected G-APDs

Goal:

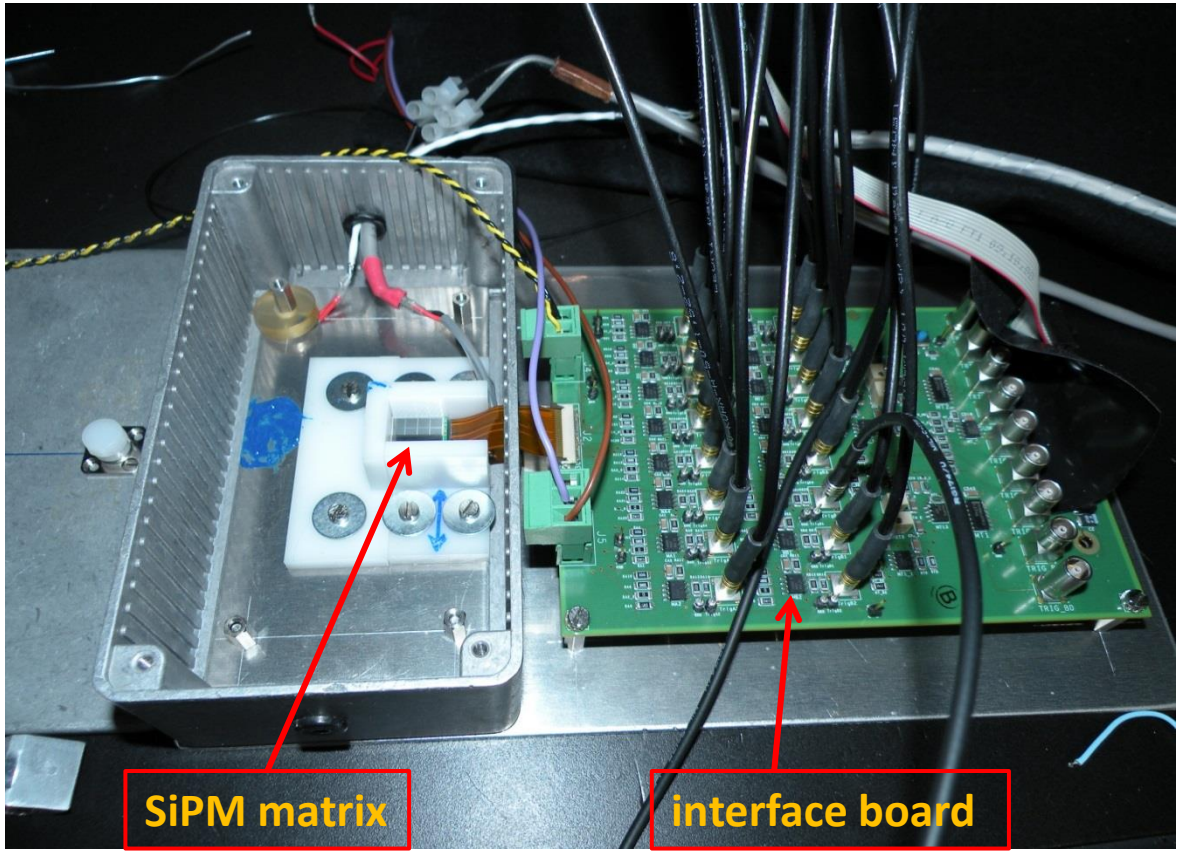
to extract our ASIC's specifications.

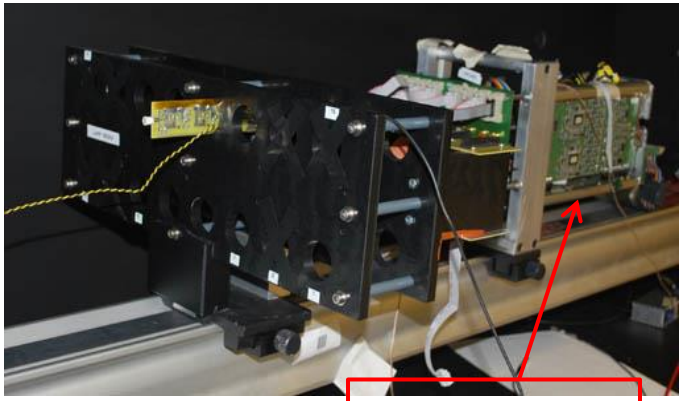
■**Specifications**

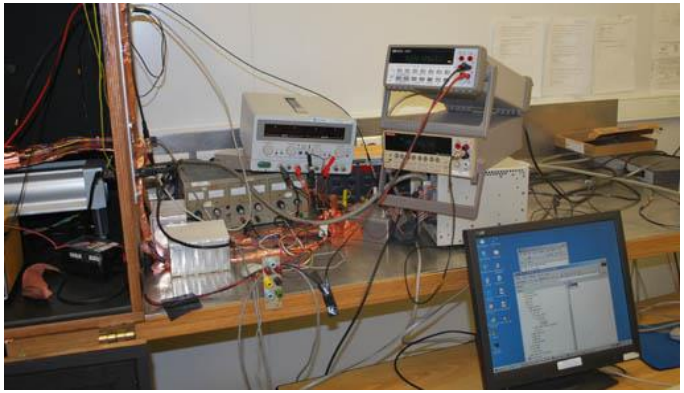
Parameter	Condition	Value	Unit
Number of elements		16 (4 x 4)	elements
Effective active area / channel		3 x 3	mm
Pixel pitch		50	µm
Number of pixels / channel		3600	-
Number of pixels / device		57600	-
Fill factor		61.5	%
Photon detection efficiency *	λ=440 nm	50	%
Dark current / channel	per channel	3	µA
Terminal capacitance / channel		320	pF
Gain		7.5×10^5	-

* Includes cross-talk and after-pulse

Test Bench

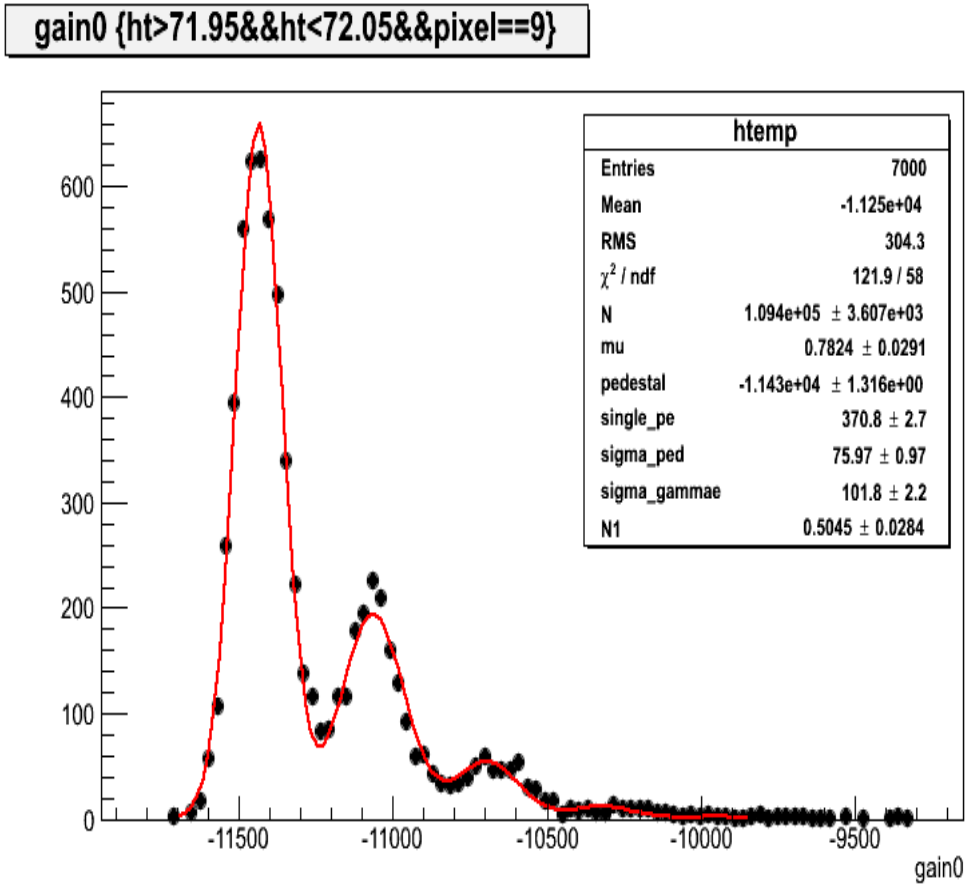






- Test with light source.
- An interface of gain stage and inversion => compatible with the HESS2 module.

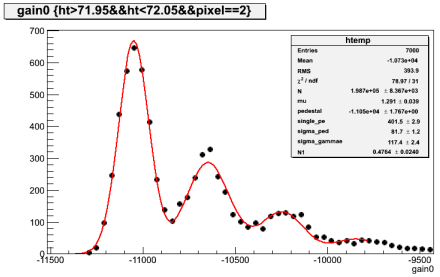
Photodetector tested: 4x4 MPPC Hamamatsu matrix (16 3x3 mm² pixels) : one pixel spectrum measured at room temperature

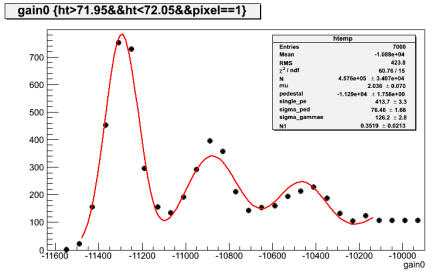


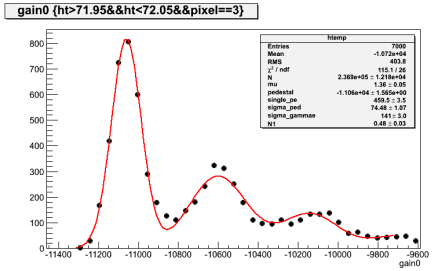
Temperature ~25 degrees

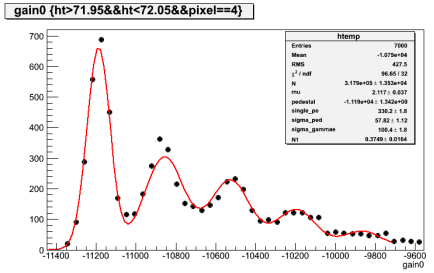
- Measurement on 16 pixels - 4x4 SiPM matrix (16 3x3 mm² pixels)
- with the LAPP test bench , using the HESS readout system
- **Optimal operating potential found: 72V**

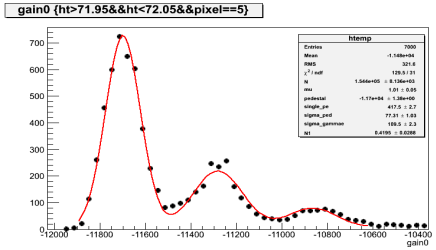
Photodetector tested: 4x4 MPPC Hamamatsu matrix (16 3x3 mm² pixels) : Measured spectra at room temperature

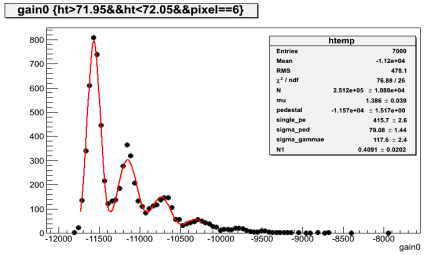


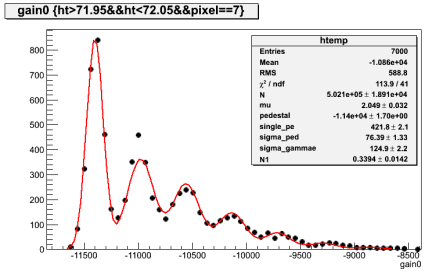


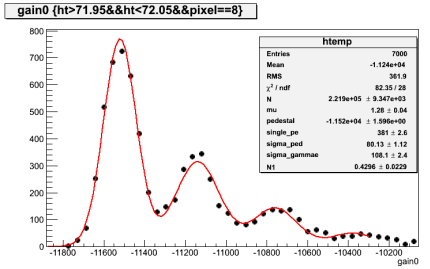


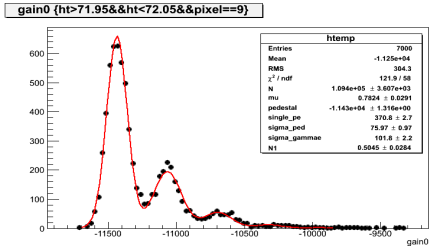


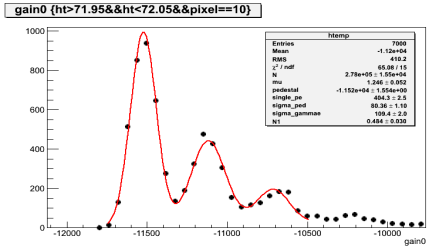


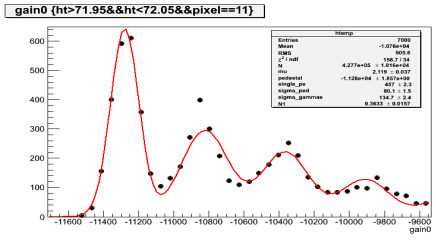


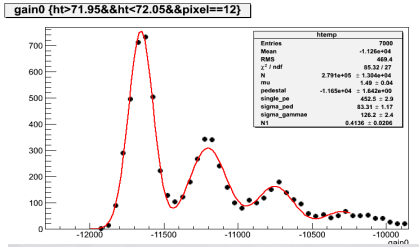


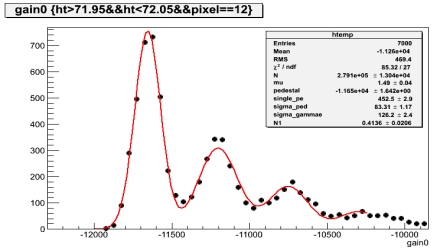


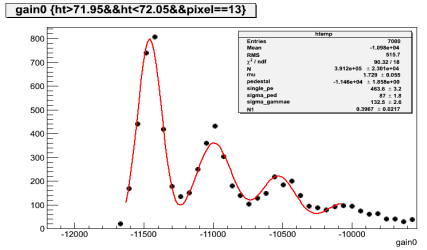












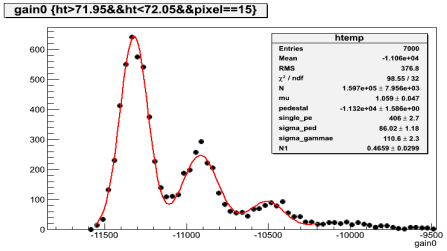
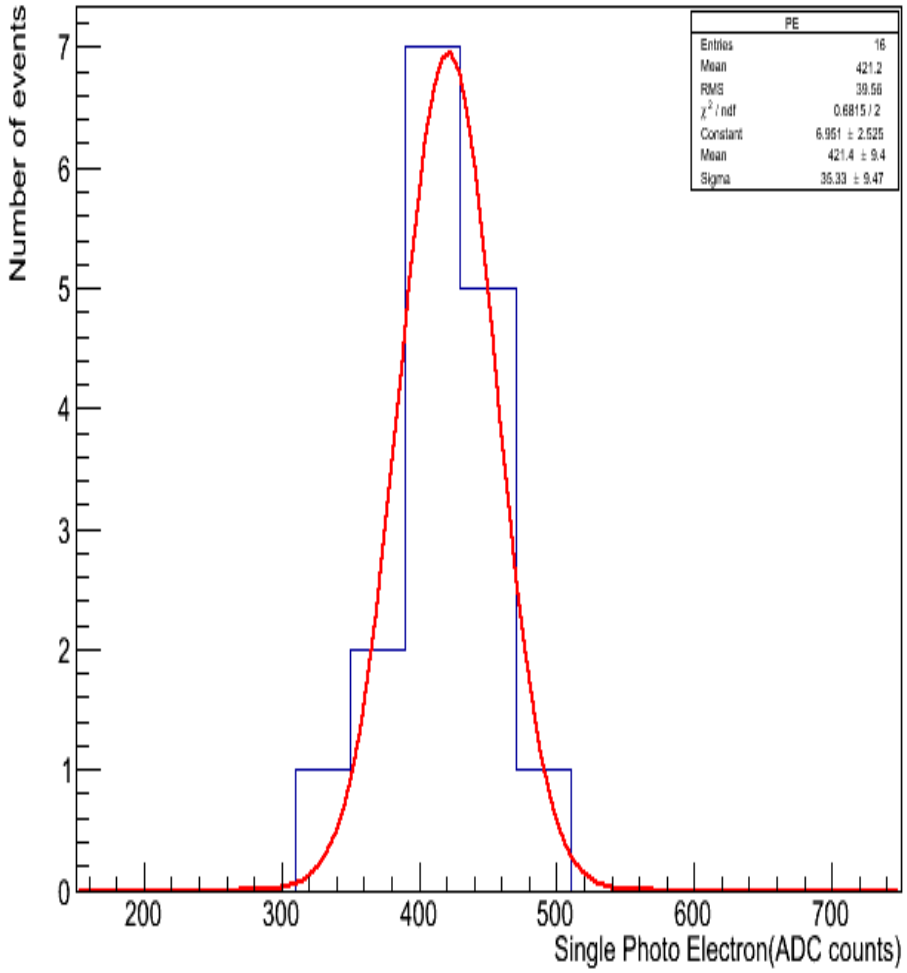


Photo detector characterization (conclusion)



@ room temperature ~25 degrees

- Photoelectron ranging from : 371 to 490 (ADC counts) for **HV=72 Volts**, equivalent to a gain of **5 10^5**
- **Spread ~ 10 %**

⇒ On-chip gain adjustment (pixel per pixel)

⇒ On chip pixel overvoltage adjustment

(performance optimization: gain and cross talk)

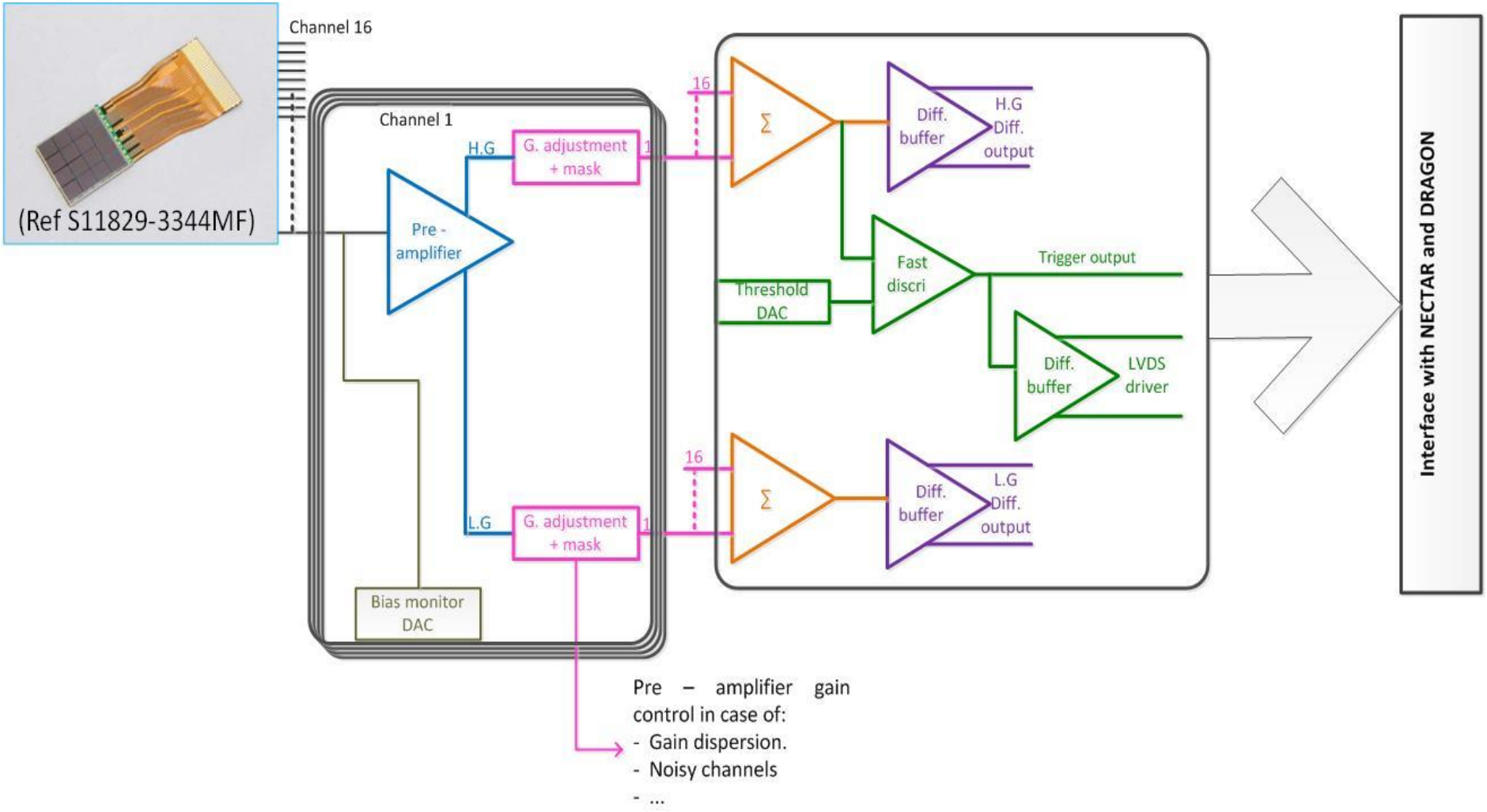
Read-out ASIC specification

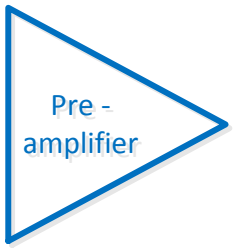
- 16 readout channels per chip
  - 1 p.e. measurement with S/N $\geq$ 5
  - 2000 p.e. full scale split in 2 gains
  - On-chip gain adjustment
  - On-chip DAC for pixel overvoltage adjustment
  - Trigger :
    - Fast discriminator with programmable threshold
  - 2 differential analog outputs
  - **Interface with NECTAR**
  - + Service functions: Slow control registres, DACs, …

II. ASIC design

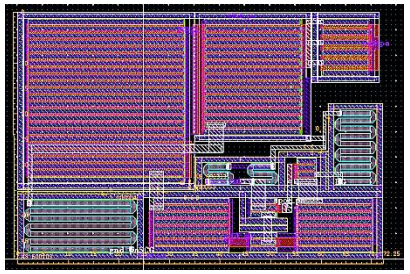
- Brain storming on the circuit
- Full custom architecture (analog electronics)
- Simulation of the ASIC -> transistor level
- Layout and verification
- Sent to foundry on March 2014

ALPS chip – bloc scheme





Pre-amplifier



- 16 channels: adapted to 4x4 SiPM matrix
- Principle:
  - Low input Impedance about 20 ohm.
  - Fast response < 5ns

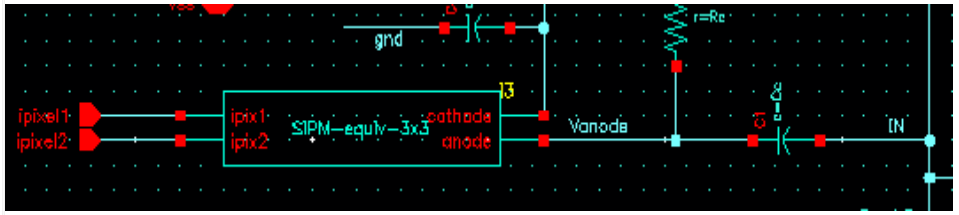
  => **Current mode**
- Dynamic range:
  - From 1 up to about 2000 photoelectron (pe)
  - Signal to noise ratio (SNR) > 5

  => **2 Gains**
  - HG covers from 1 to about 125 pe
  - LG covers from 11 to about 2000 pe

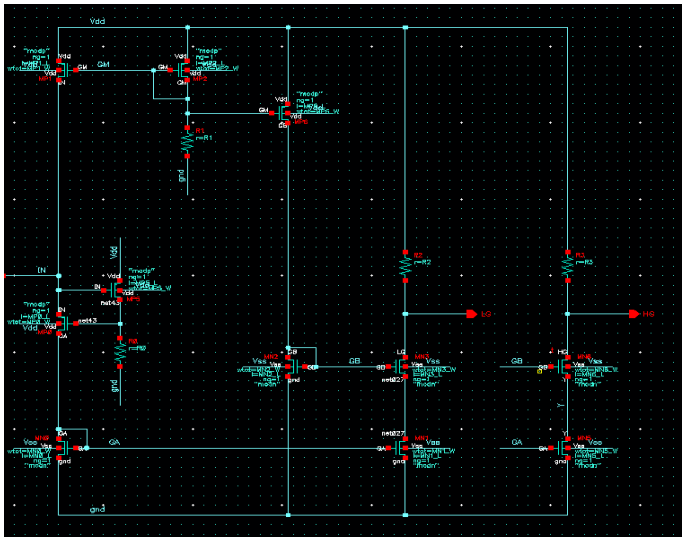
  Gain ratio about 92, gain overlap 1 decade
- Voltage output
- Low power consumption < **30mW** at this stage (from simulation)

Pre-amplifier simulation (1)

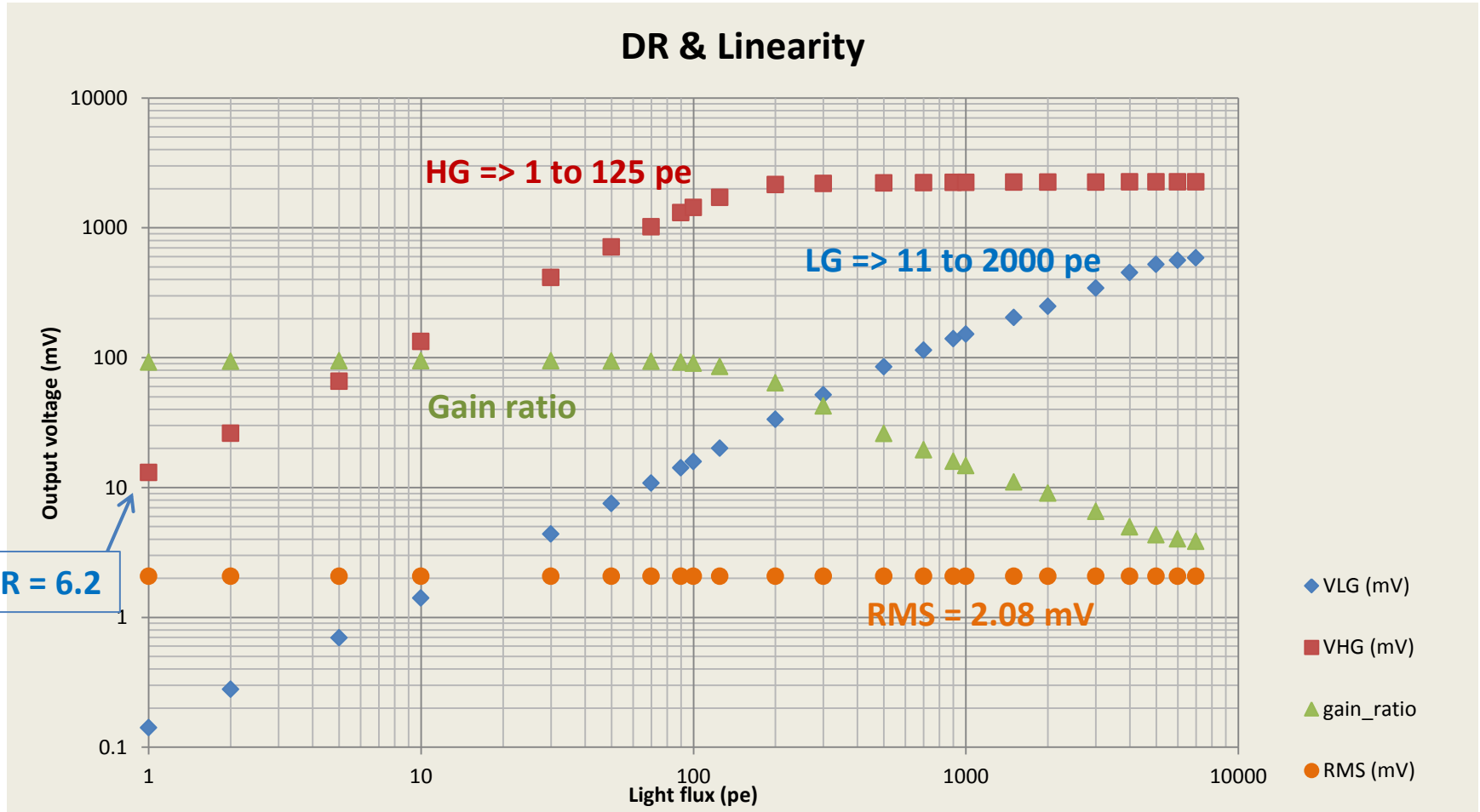
Simulated SiPM signal 1pe



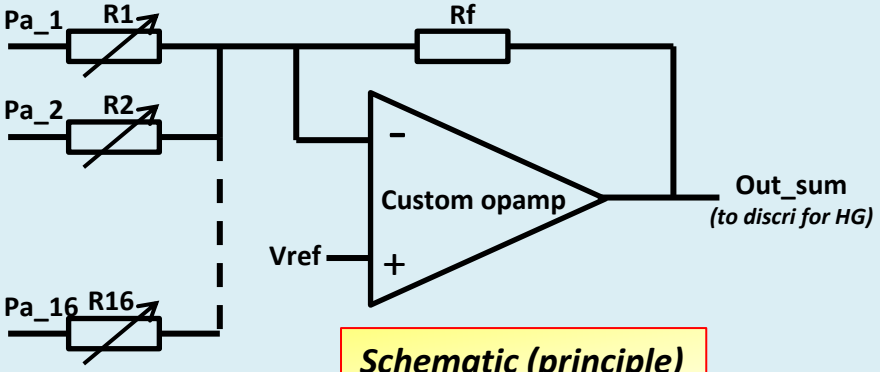
High gain response



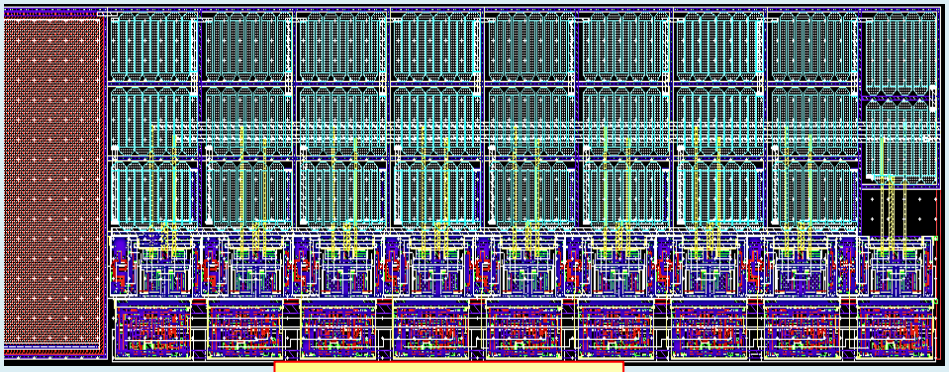
Pre-amplifier – simulation (2)



Analog sums and gain control



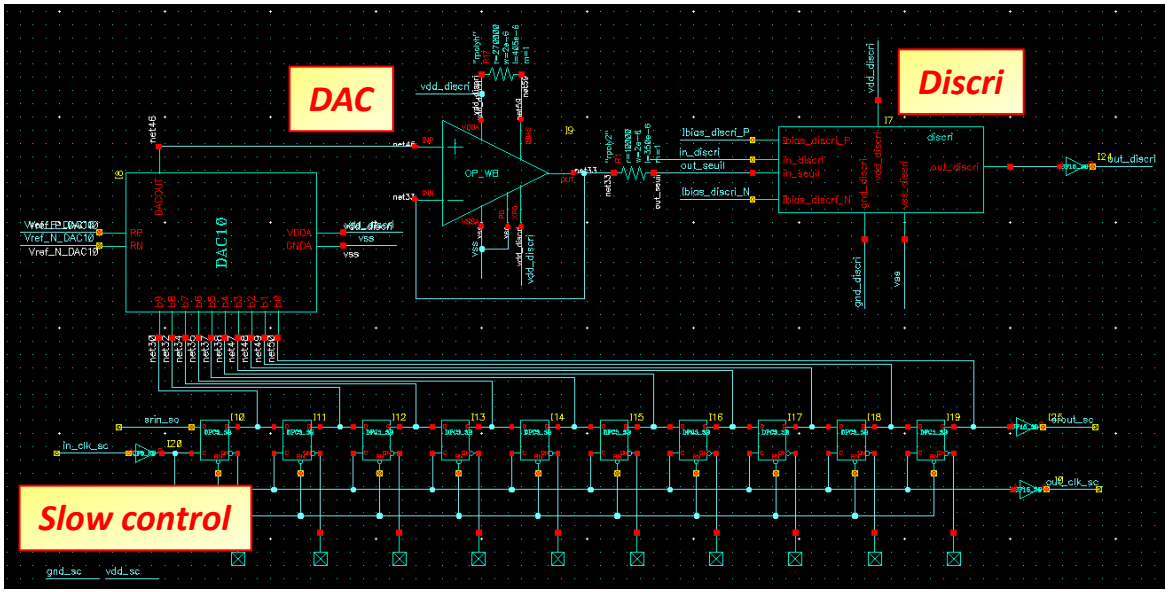
Schematic (principle)

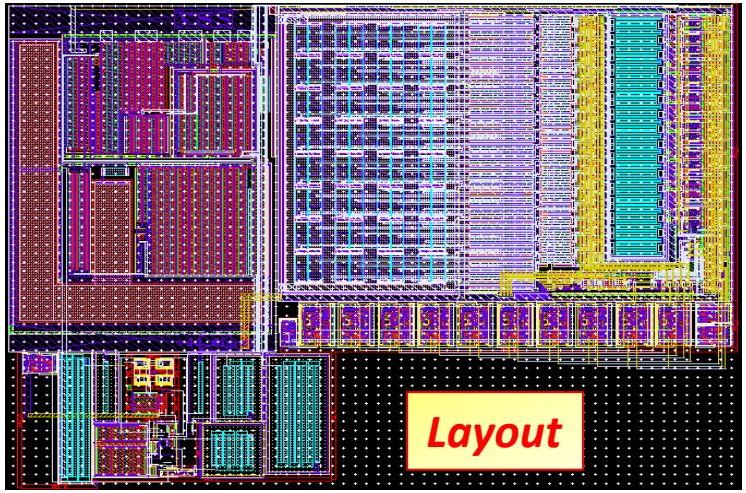


Layout of 1 resistor

- Weighted sum of the 16 preamp outputs by digitally controlled resistors
- Each resistor has a R-2R like architecture :
  - Preamp always sees the same load (better for linearity)
  - 8 bits resolution for gain adjustment
  - Noisy channels can be digitally removed
- CR shaping included in each channel
- Adjustable Vref to match the discriminator threshold

Trigger (DAC + discri)

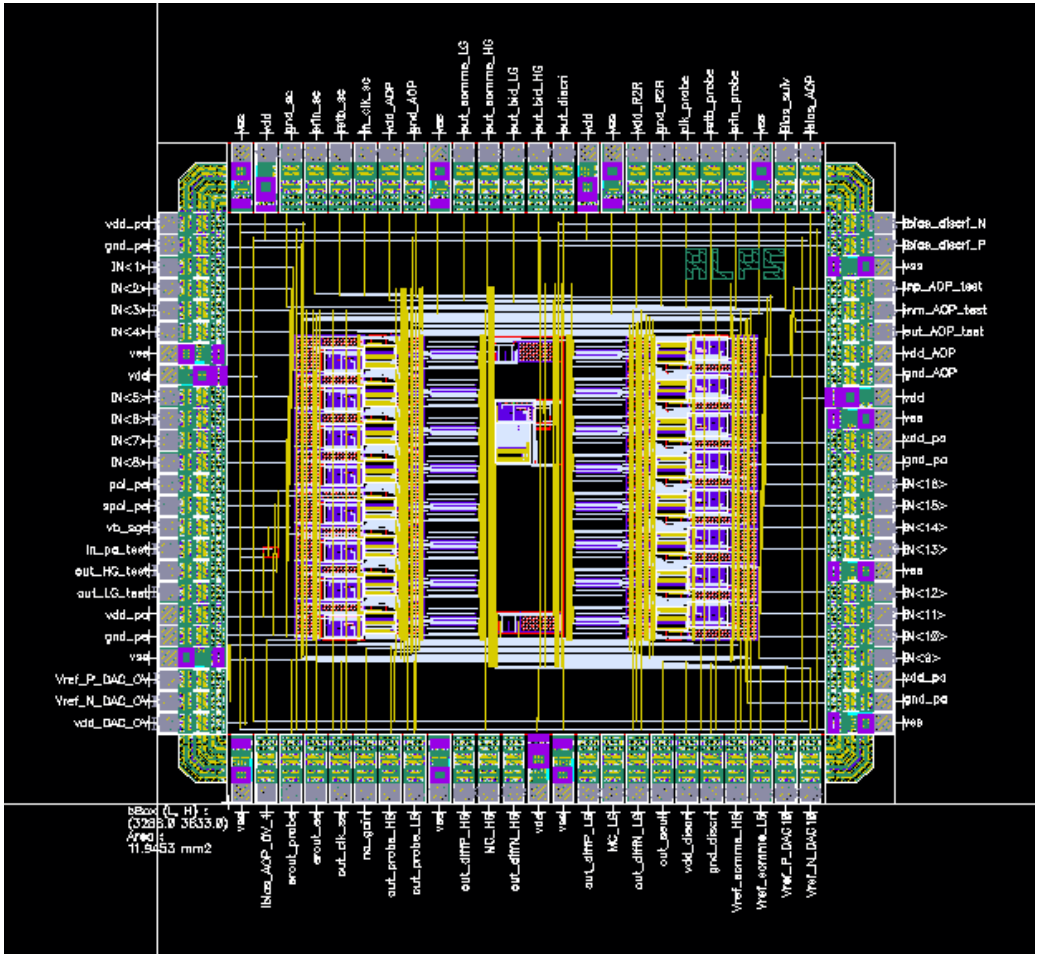




- Discriminator (full custom) :
  - Dual bipolar input stage to minimize offset
  - Self-biased
  - Buffered digital output for trigger
- 10 bits DAC for threshold
  - AMS standard cell
  - Digitally controlled threshold

ALPS chip– Layout

sent to fabrication 03/03/2014



- **AMS BiCMOS 0.35µm**
- **96 pin out**
- **Die size:**

about 3.673 X 3.298 mm²

It was programmed to be tested at the beginning of June…BUT the chip was only received at mid July, and the test board later.

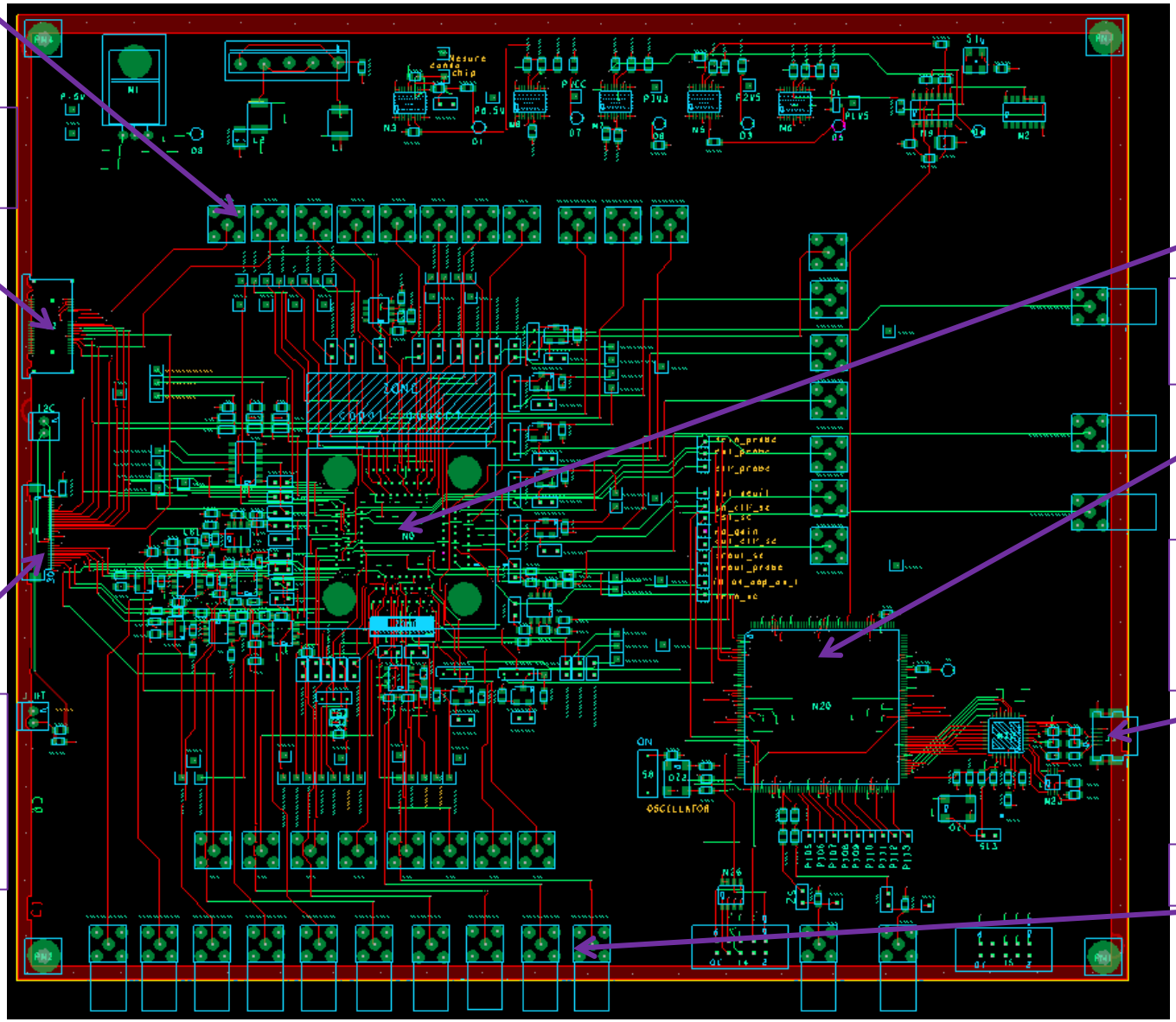
Tests started on September and are on going till present.

Test board- Scheme

Inputs:
Electrically generated

Inputs:
With interface

Inputs:
Photo - generated (from SiPM)



ALPS IC

FPGA Firmeware

USB connection Labview➔FPGA ➔ALPS chip

Analog Outputs

Test board- Labview Interface

ALPS Slow Control registers

DAC: overvoltage adjustment

High/low gain adjustment

DAC: discriminator threshold

ALPS Probe Registers

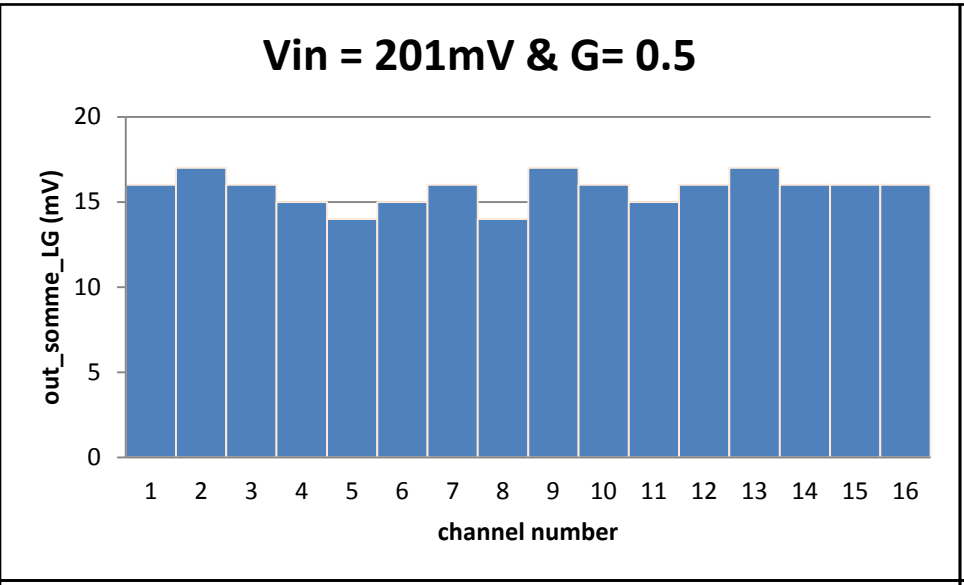
High gain output

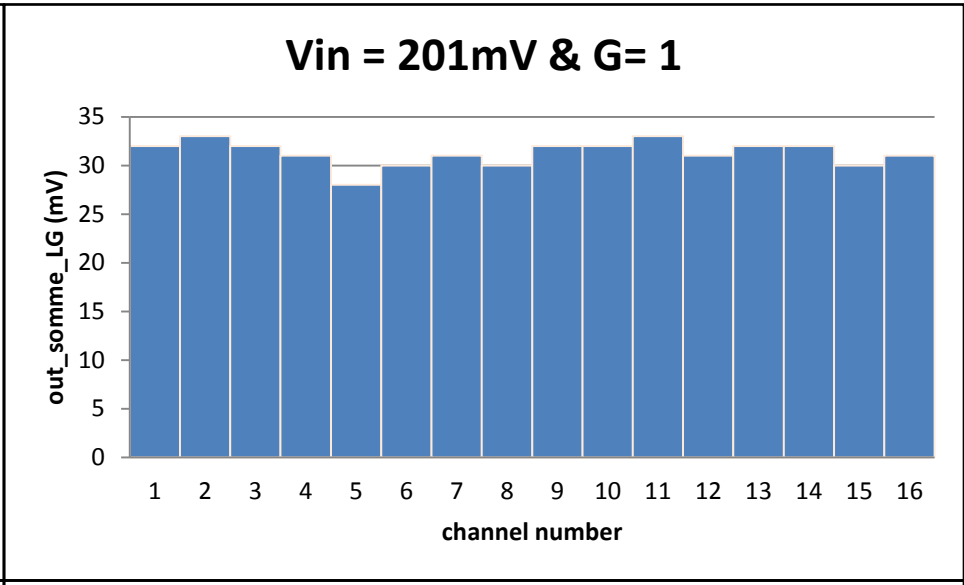
Low Gain output

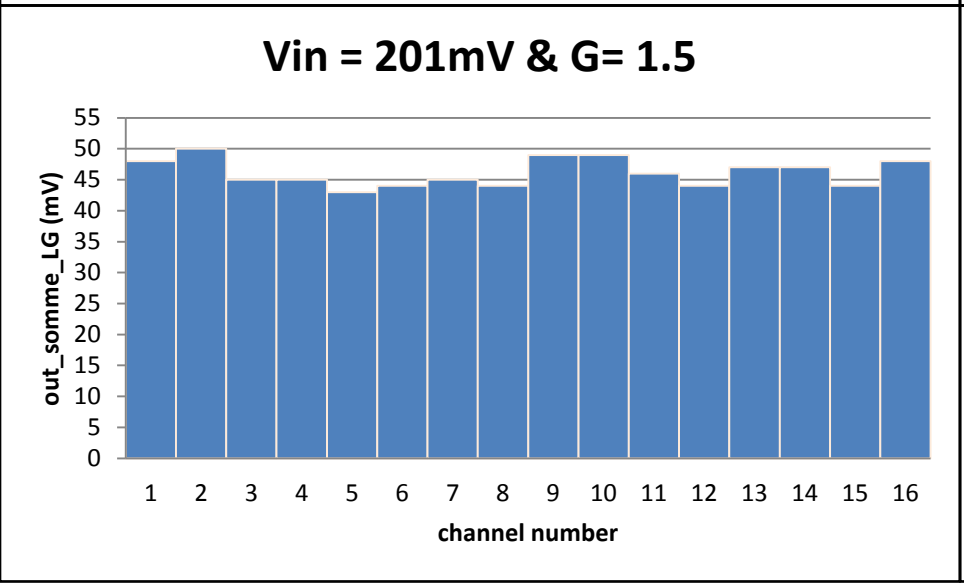
III. Tests to hold on ALPS:

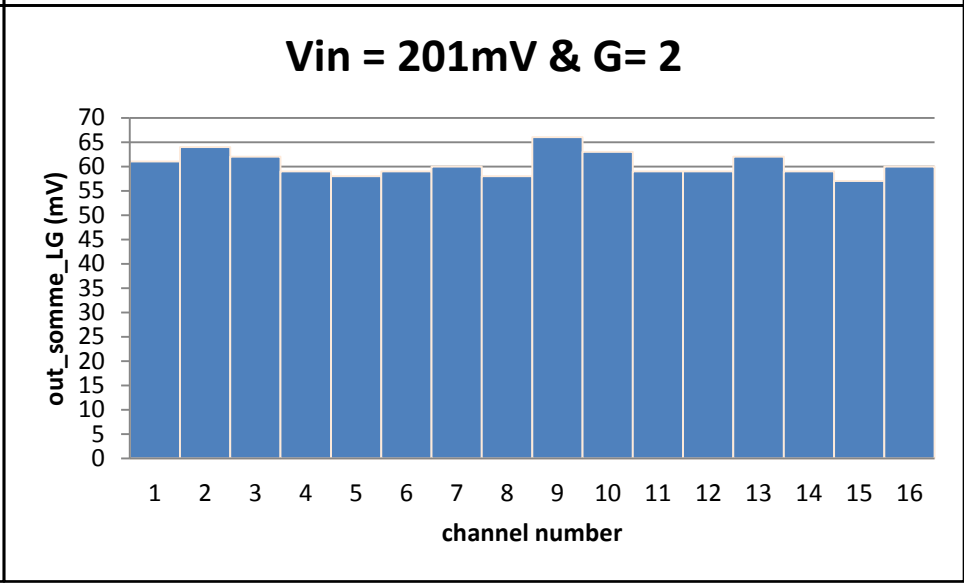
- Planned tests:
  - ALPS chip functionality and performance tests
    - Gain control tests
    - Sum function tests
    - Noisy channel suppression
  - Test and measurements with SiPM

Gain control function - LG

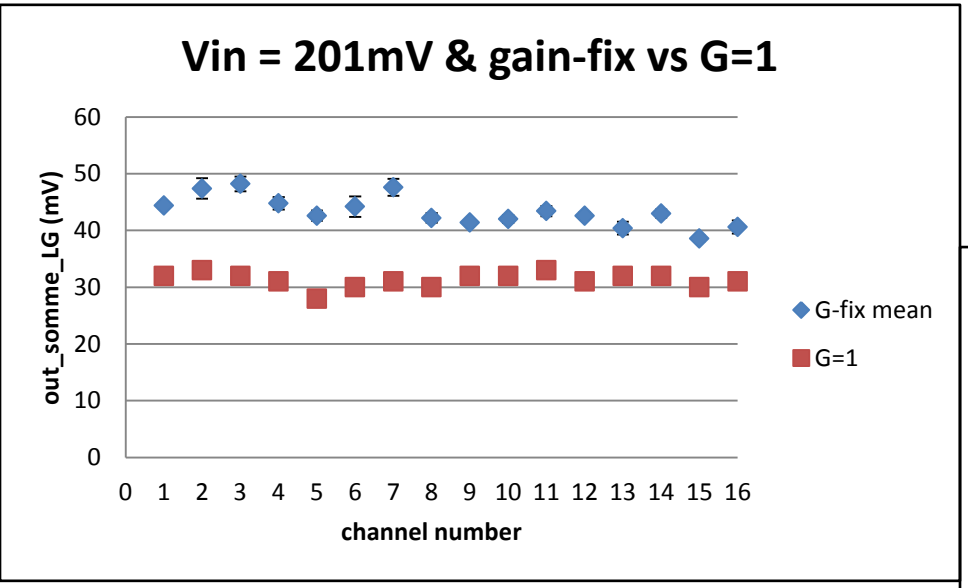


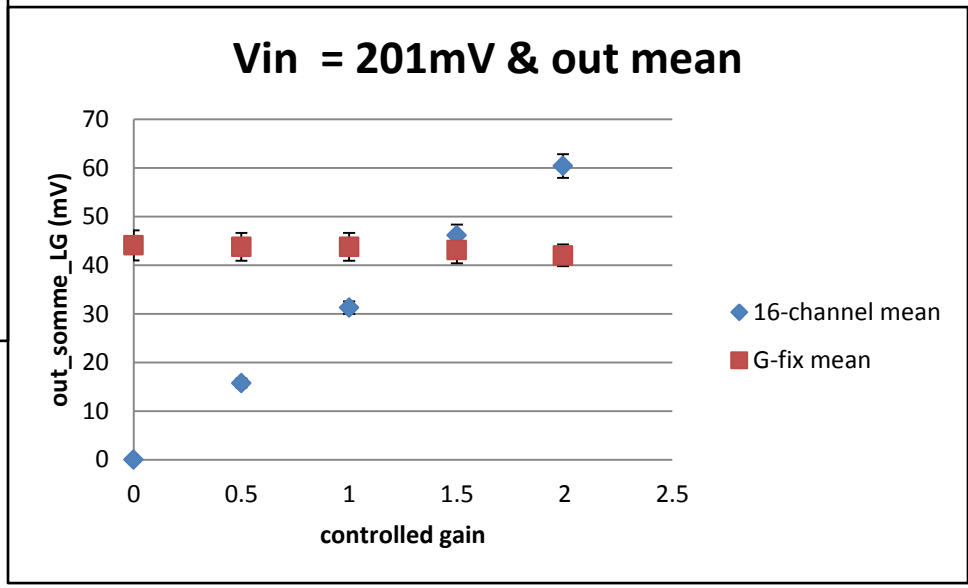




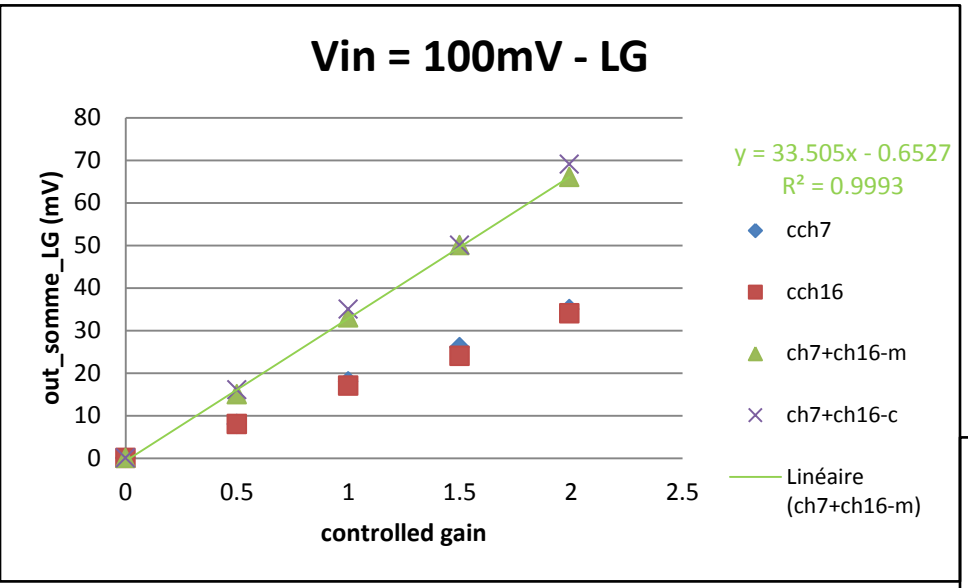


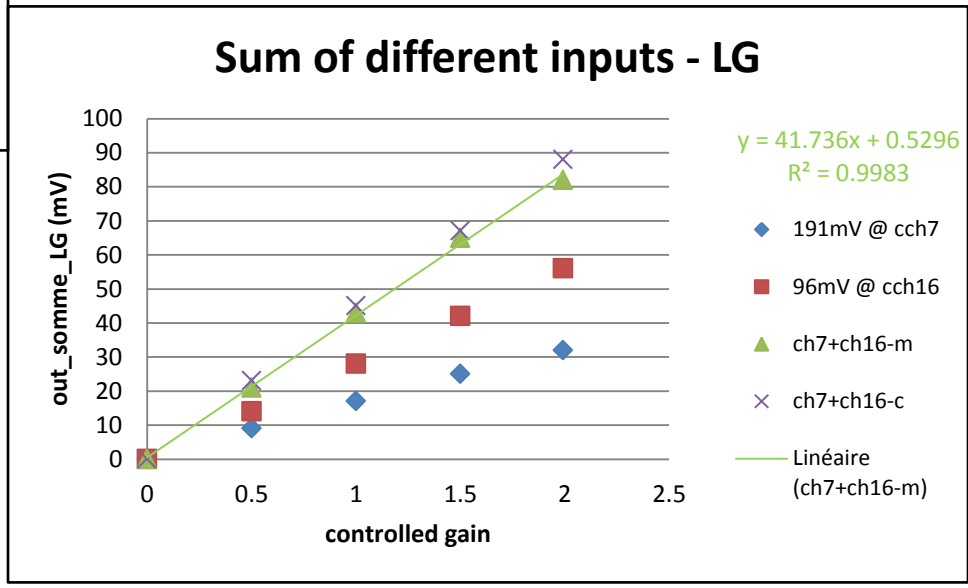
Gain control: gain-fix - LG





Sum function





New test board

- In order to test the performance of the pa
  - Output level
  - Timing
- Limit the parasitic effects and noise of the current board