



Laboratoire d'Annecy-le-Vieux
de Physique des Particules

Module Concept in the Alpine Layout

LAPP ATLAS group meeting
12.11.2014

A. Rummler



Content

- Impressions from the AUW
- Lab planning
- Next steps

Impressions from the AUW



Mixed stuff



Swiss interests

- Strong interest: **alternative layout** to the one of the Lol.
 - ▶ **Concept to be studied**: 6 pixel layers (3 planar & 3 CMOS) + 4 strips
 - ➔ Do we know how such a layout would perform ? and its cost ?
 - ▶ Being active on several fronts:
 - ➔ **ATLAS CMOS R&D** ("full-size demonstrator" task force; testbeams)
 - ➔ **mechanics** (**barrel 5th layer concept** under development:
alpine-like, but modular: **38% less silicon area**)
 - ➔ **simulation** (simulation tool to quickly built and simulate geometries under development; use of 8000 cores for 300 days/year from April 2015 requested to Lugano computer center)
 - ➔ **CMOS modules** (just starting discussions with other Institutes)
- Interest on track-trigger (contributing to the FTK)

Giuseppe Iacobucci (U of Geneva)

Review Outcome

		ATLAS <u>ITk</u> Initial Design Review	
ATLAS Project Document No. Project - System - Type - Sequential No. ATC-xxx	Institute Document No. XXXX	Created 17 th Oct. 2014	Pages 7
		Modified	Rev. No. 9

ATLAS ITk Initial Design Review



Report in preparation

Prepared by.: L. Pontecorvo	Checked by.: 	Approved by.: P. Allport, B. Di Girolamo
For information, contact : L. Pontecorvo - INFN Rome - ludovico.pontecorvo@cern.ch		

1. Distribution: EB and TC members, management of the project, participants to the review.

- The reviewers congratulate the ITK community for the huge effort made to clearly define the ITK project, and in particular for the very good material provided during the review.
- A Report is in preparation, We hope to distribute it within ATLAS by the end of next week.
- Preliminary comments on each agenda item have been collected and a summary can be found in the next slides

The IDR report and reviewers recommendations

- The IDR document itself will be updated in the light of the reviewers recommendations and outstanding comments in CDS.
 - A notification will be sent to atlas-itk-general when this is complete.
- We received the reviewers summary very recently.
- It has now been circulated to PLs, authors, and activity coordinators. When the text is agreed and niggles sorted out it will be circulated to ATLAS.
- *I would very strongly urge the groups (especially group leaders) to read the document.*
- The conclusions and actions arising will be discussed at the next ITk-SC in December.

Stephen McMahon



ITk Pixel Design Group 1+2 (Monday 9:00)



TWP Conclusion and Plan

Slide by
Vitaliy Fadeyev

We are sampling BW vs material for one concrete version of the cable: twisted pair. Some of the cables are rather sophisticated (plated, multi-strand).

We have seen a strong improvement in the cable performance with the use of impedance-matching board and pre-emphasis.

There are indications of fast on/off-stave data transmission on TWP with use of 8/10B and pre-emphasis:

- 6.22 Gbps *) at 1 m for multi-stranded cable
- 3.1 Gbps *) for 4 m for solid core cable
- 1.2 Gbps *) for 6 m for solid core cable (preliminary)

*) This is raw BW. The useful rate is 8/10 of that.

The environmental effects of cable and CF surface proximity can be important (in progress).

For the next steps:

- Need to figure out where/how to make multi-stranded TWP with polyimide.
- Should probably radiation-test the thin solid-core TWP cable anyway. There will be Los Alamos irradiation run in December.
- It would be interesting to do a more comprehensive mockup with CML drivers/wirebonding along with the cable.
- It would make sense to investigate “hybrid” solution of TWP followed by twinax.



Cable Measurements: Attenuation & Bandwidth

- A BERT (Bit Error Rate Test) test on the 0.5m cable was performed by Vitaliy at UCSC/SLAC
- Good results were obtained to 3.11 Gbit/sec using 8/10 b encoding
- We are preparing to send the 0.875 m cable to Vitaliy for a similar test, but we are waiting for a differential signal transformer to perform a true differential signal measurement.
- Maurice has encouraged us to try new dielectric materials, optimized for faster signals
- We are obtaining samples of Dupont Pyralux TK (Teflon/Kapton) and a custom polyimide formulation by our vendor (Qflex)
- Both of these materials have Dielectric Constant = 2.5 (instead of 3.4)
- Also these materials allow for thinner dielectric and thinner copper in a differential microstrip design – about half the radiation length of present design
- We are having sheets of these materials sent to us. On the sheets we are having a serpentine microstrip design made onto them with four lengths (0.5 m, 0.75 m, 1.0 m, 1.25 m).

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Neil McFadden, UNM

Stage and Optics pricing



X stage 800mm, Y stage 400mm, Z stage 100mm
X and Y stages PRO 165 series
Aligned and calibrated as an assembly
Accuracy +/- 2.5um

quote £26K

Mitutoyo Long Working Distance Objectives:

[http://mitutoyo.incony.de/web/mitutoyo/en_GB/mitutoyo/1358419146666/10X%20lens%20\(WD%20:%2051%20mm,%20NA%20:%200.21\)/\\$catalogue/mitutoyoData/PR/375-039/index.xhtml](http://mitutoyo.incony.de/web/mitutoyo/en_GB/mitutoyo/1358419146666/10X%20lens%20(WD%20:%2051%20mm,%20NA%20:%200.21)/$catalogue/mitutoyoData/PR/375-039/index.xhtml)



3x NA=0.09 WD=77mm limit=3um £475

5x NA=0.13 WD=61mm limit=2um £767

10x NA=0.21 WD=51mm limit=1.5um £635

Camera (plus cheap webcam!):

http://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=4024

1/2" CMOS (6.66mm x 5.32mm), 1.3 MPix

5.2 um pixels

Max 25 fps

8-bit

£250

John Matheson



ITK: CMOS

(Wednesday 8:30)





Outline of the Demonstrator programme

Effort led by Norbert Wermes

- In order for CMOS Pixels to enter the TDR as a to-be-further-pursued option it needs to be demonstrated that a reasonably sized CPIX detector detects particles in an understandable and efficient way in a test beam by next year (i.e. end 2015).

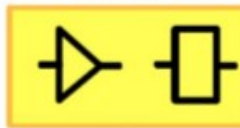
FOR pp - experiments @ LHC

smart pixel
~200 trans/pixel



diode +
preamp +
discr.

FE-chip: FE-I4 -> FE-Tx?
> 100 M trans



FE chip

fully monolithic



Diode + Amp + Digital

Too complex

- This we call a **DEMONSTRATOR** with the following features:

- a pixel module
- reasonable size (1-4 cm²)
- bonded to FE-I4
- irradiated to 10¹⁵ cm²
- simple on the main issues
- characterized with pulses, rad. sources
- => test beam.

Goal of the
CPIX demonstrator
"Task Force"

Introduction to CMOS Pixel effort





Time frame of the Demonstrator programme

- Goal: Have reasonably sized modules characterised by end of 2015
 - build upon small test-chip (MPW) submissions with many technologies
 - aim for “large” (MLM/engineering) submissions with 2-3 technologies
 - common specifications for demonstrator submissions currently being written up, release next week

- ❑ Aug-Nov 14: submissions and decision on designs for “large-size” design commonalities
 - ❑ condition: test results from previous submissions needed
 - ❑ Task force (key designers + few) set up -> proposal by Oct 14

- ❑ Nov14 – Feb15: submission of optimized designs in 2-3 technologies

- ❑ April-July 2015: characterization in lab (stand alone)

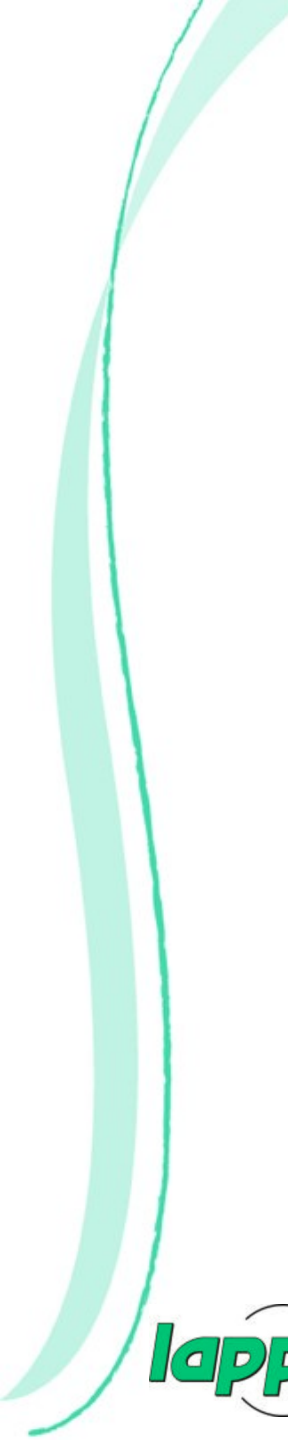
- ❑ June-Aug 2015: module assembly and lab characterization

- ❑ Sep-Dec 2015: preparation and demonstration in test beams

N. Wermes

Introduction to CMOS Pixel effort





ITK: Common electronics (Wednesday 11.00)

QA During R&D

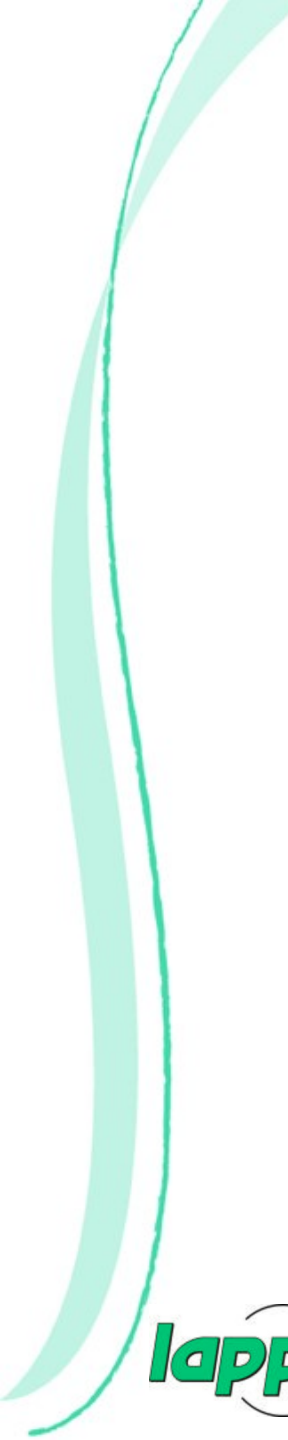
- **Stress tests on sample basis**
 - Elevated temperatures
 - Elevated humidity
 - Thermal cycling
 - Thermal shock
 - Low temperature operation
 - Vibration tests
 - Long term tests
- **Should be discussed before PDR**

AUW Nov. '14 ITk common
electronics

Tony Weidberg

Alpine: Take into account
for our own stove testing⁵
program

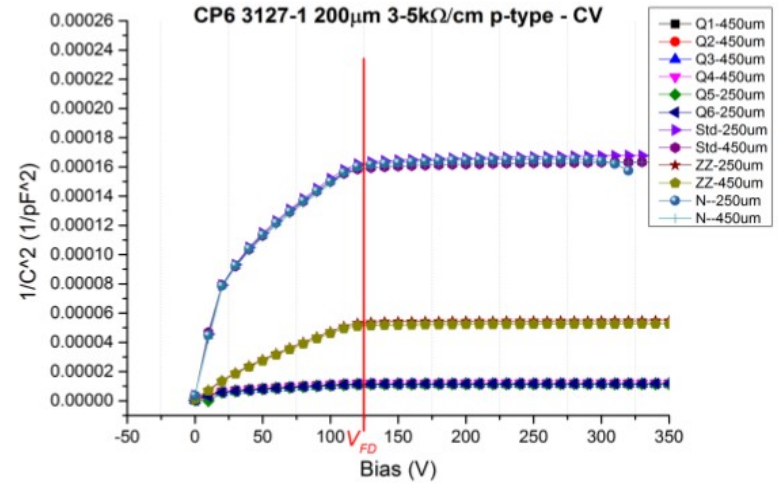
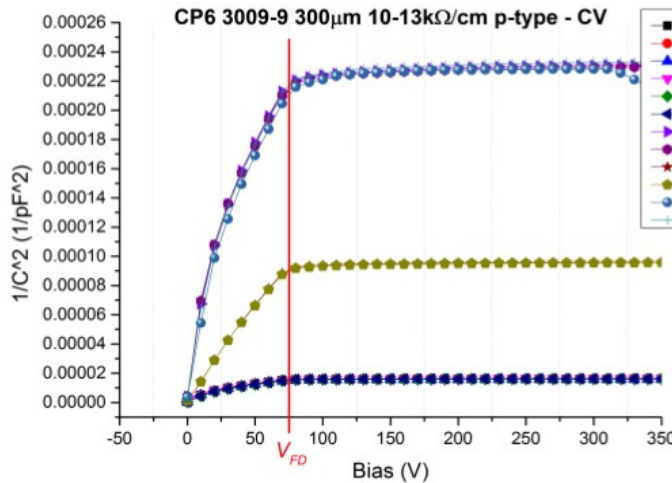




ITk: Pixel Module Sensor 1+2 (Wednesday 14:00)

- working on larger experimental chips but no schedule for full size FE-15 soon due to lack of man power, etc.

CVs, Full depletion voltage & Wafer yields



Batch no.	VFD [V]	Total no.	Singles	S.Yield1	Quads	Q.Yield1	Std-250	Std-450	ZZ-250	ZZ-450	N--250	N--450	Quad-250	Quad-450
3127 (200um)	125V	48	24	100%	24	96%	100%	100%	100%	100%	100%	100%	100%	75%
3009 (300um)	75V	36	18	100%	18	100%	100%	100%	100%	100%	100%	100%	100%	100%
Batch no.	VFD [V]	Total no.	Singles	S.Yield2	Quads	Q.Yield2	Std-250	Std-450	ZZ-250	ZZ-450	N--250	N--450	Quad-250	Quad-450
3127 (200um)	125V	48	24	63%	24	96%	50%	100%	75%	100%	0%	100%	88%	94%
3009 (300um)	75V	36	18	83%	18	100%	100%	100%	100%	100%	0%	100%	100%	100%
Batch no.	VFD [V]	Total no.	Singles	S.Yield3	Quads	Q.Yield3	Std-250	Std-450	ZZ-250	ZZ-450	N--250	N--450	Quad-250	Quad-450
3127 (200um)	125V	48	24	50%	24	63%	50%	75%	25%	100%	0%	50%	50%	69%
3009 (300um)	75V	36	18	72%	18	83%	100%	100%	100%	100%	0%	100%	100%	100%

*Yield1 – Breakdown voltage > VFD + 50V, I_{leak} < 1 µA @VFD

*Yield2 – Breakdown voltage > 500V

*Yield3 – Breakdown voltage > 1000V

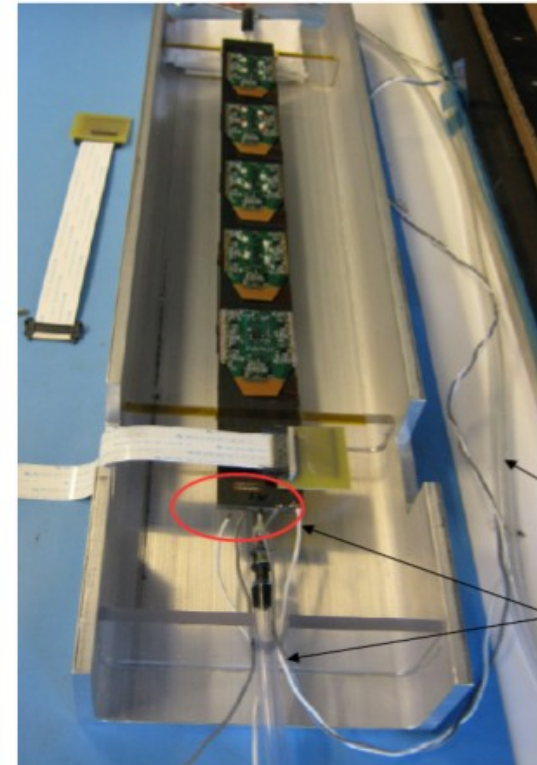


- New SP stave prototypes with **FE-I4B quad modules** are in preparation at **Uni Bonn and LBNL**
 - 70 cm long stavelets with possibility of having two SP chains of 4 and 5 modules

Main focus of the SP stave tests

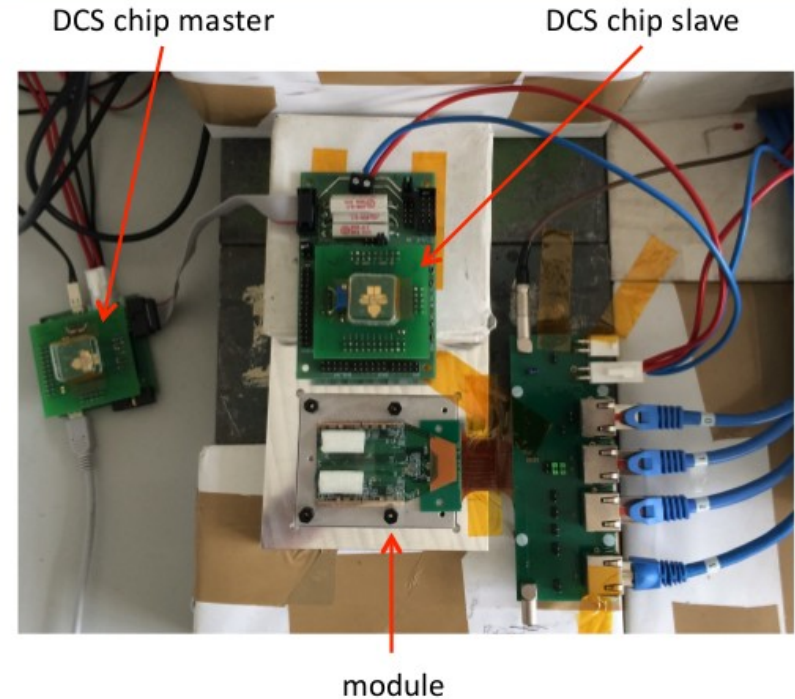
- **Module bypass element**
 - **HV distribution**
- Alpine staves prototypes with serial powering are in preparation at Lapp
 - A. Rummler, <https://indico.cern.ch/event/349855/contribution/4/material/slides/0.pdf>
- Work started also for SP pixel disks prototypes (Liverpool)

Stavelet at LBNL



DCS chip + quad

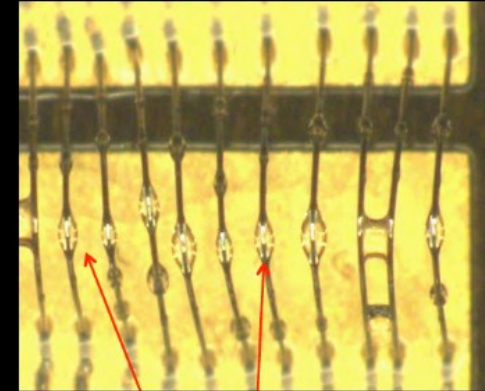
- The DCS chip has been tested in parallel to a quad module
- One day of testing → results all very preliminary
- Module ON/OFF on command (**slow control**) and upon overvoltage (**fast response**) demonstrated
- Setup still needs to be optimized, in particular ground connection for stable and reliable data communication



- Distribution of the HV to bias the sensors in a SP chain has to be done according to the current distribution scheme, to avoid shorting the SP chain
- Convenient solutions **for prototyping**
 - One HV supply per module
 - Group all modules in a SP chain to one HV power supply, and connect the HV return line to the local grounds of the modules (used for SP stave prototype with FE-I4A). Drawback: independent monitoring of sensor leakage current not possible, same HV bias to all modules in the SP chain
- **For detector operation**
 - One HV supply for module
 - HV switch could also be considered
- No activity yet on this topic

Spraying Cellpack D 9201 Polyurethane

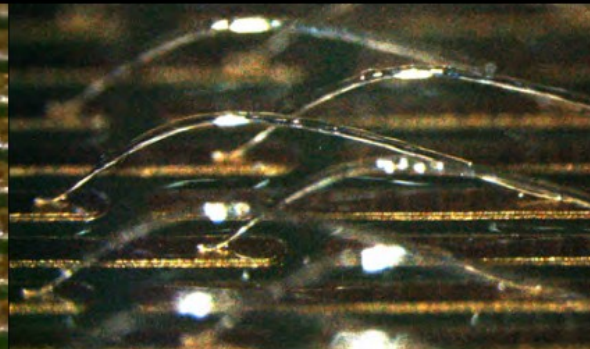
- PU spray can application unsatisfactory
 - This spray is too heavy
 - PU consistently forms drops
- Talon Airbrush
 - Adjustable flow rate
 - 0.25, 0.38, 0.65 mm nozzle/needle
 - 0.65 mm appropriate for PU
 - Smaller needles clog



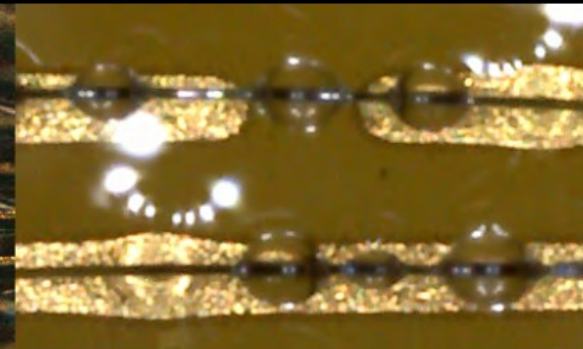
From PU spray can



– too fine



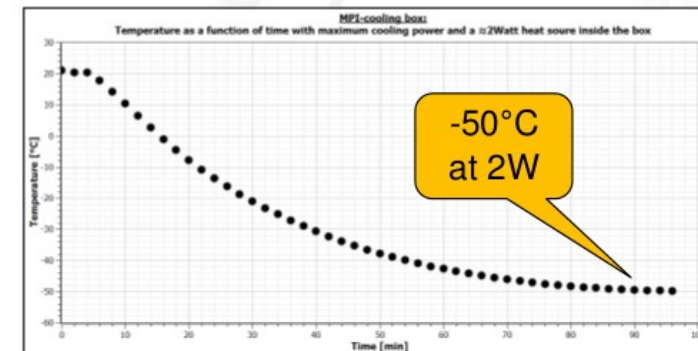
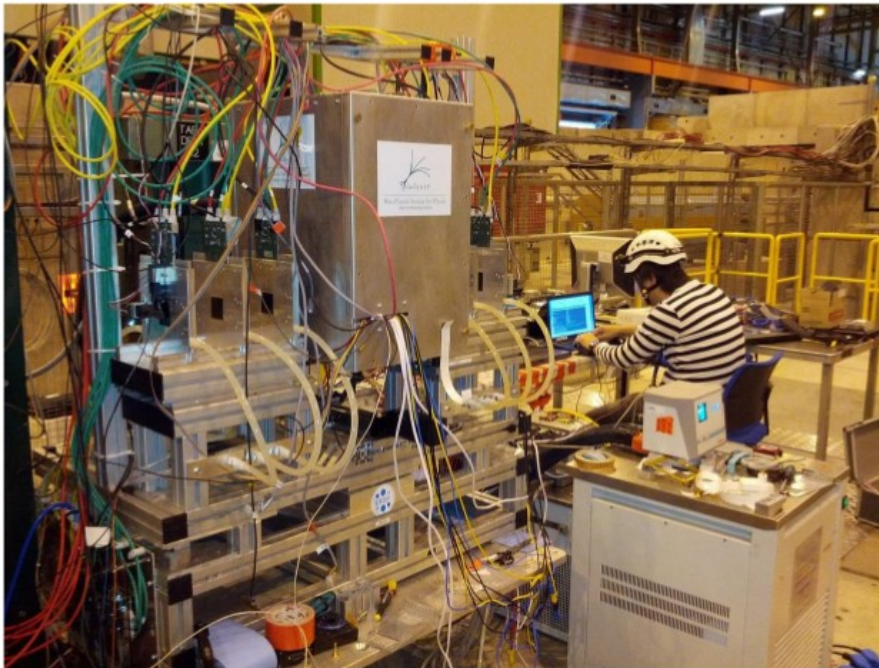
– good



– too heavy

New MPI cooling box

- circulates chilled air, using high-power chiller
- very good insulation
→ achieved -45°C on an irradiated SC sample
- new heavy-duty xy-stages from PI, incl. control s/w
- samples mounted on baseplate outside the box → easy access
- lot of material → only used at CERN



11/5/2014

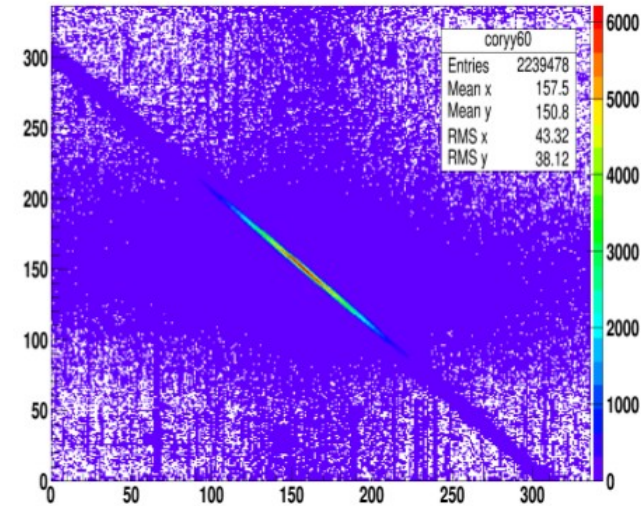
AUW Meeting

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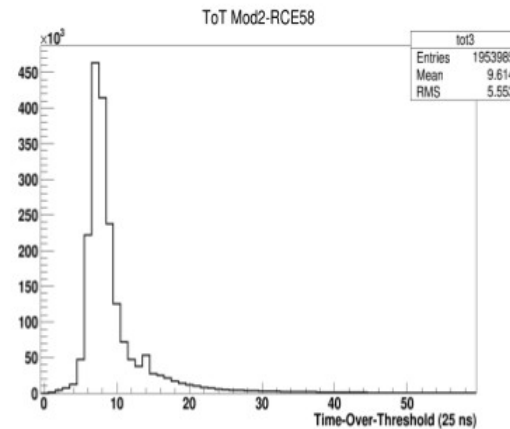
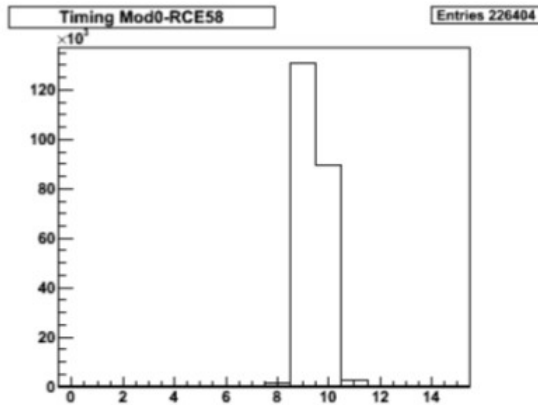
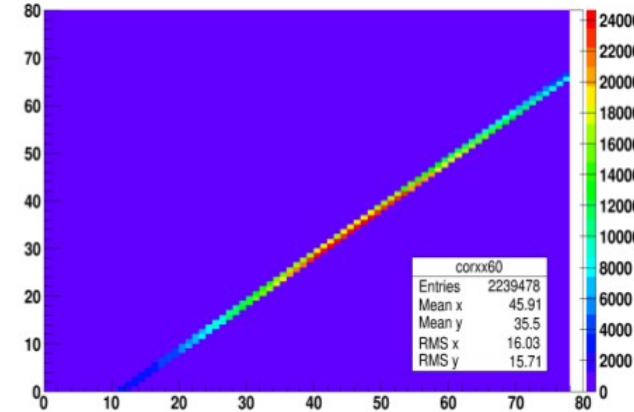
Online Monitoring/Reconstruction

- Telescope copes quite nicely with the beam at | SPS
 - | 180 GeV pion beam
- DAQ runs very stable → No problems in days
- Triggered on Hitbus of telescope planes
 - Up to 7000 trig/spill (spill length: ~400ms)
 - | ~20000 trigger/ spill
- Timing as expected for unirradiated IBL sensors
- Quite clear correlations,

Row-Row Correlation Mod1-RCE59 x Mod2-RCE59



Col-Col Correlation Mod1-RCE59 x Mod2-RCE59



ATLAS Upgrade Week, ITk: Pixel module/

SPS Data

05/11/14

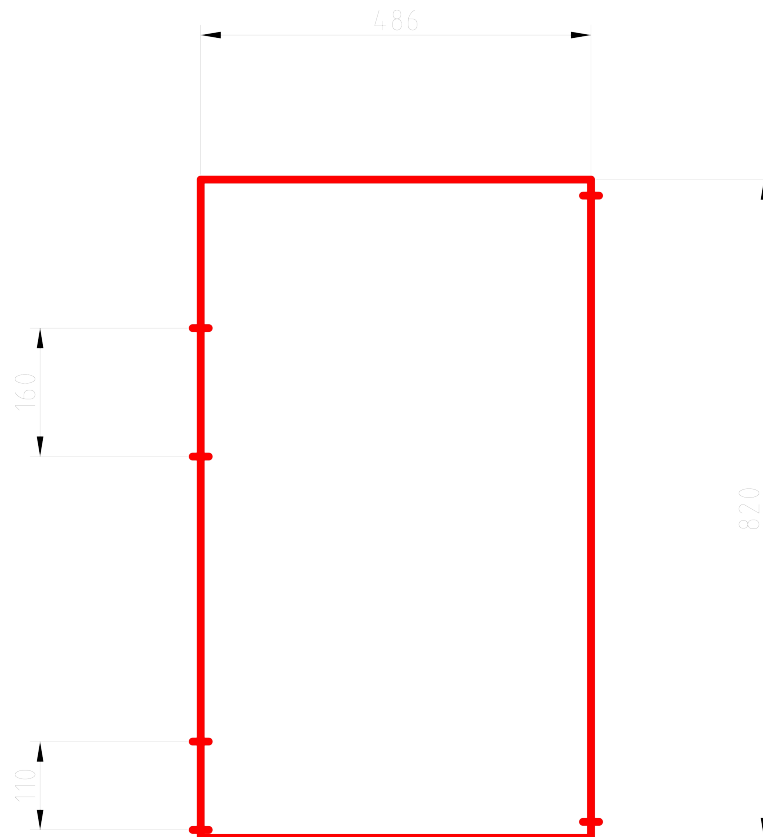


Lab planning

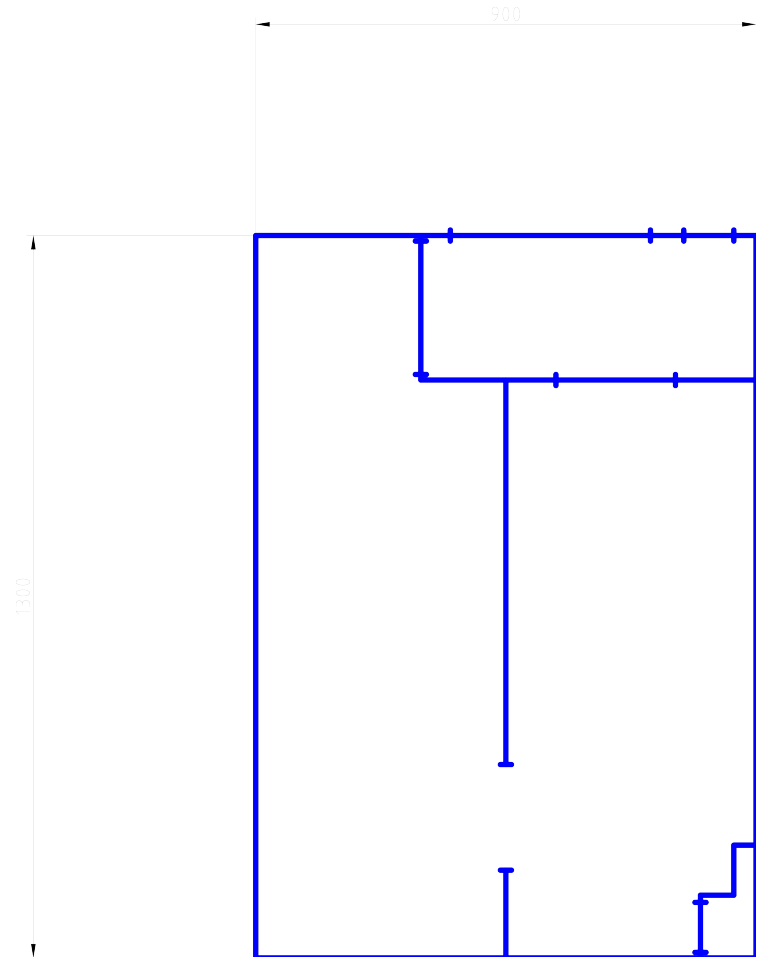


Floor Plans

Mecatronique



Clean room



Floor Plans

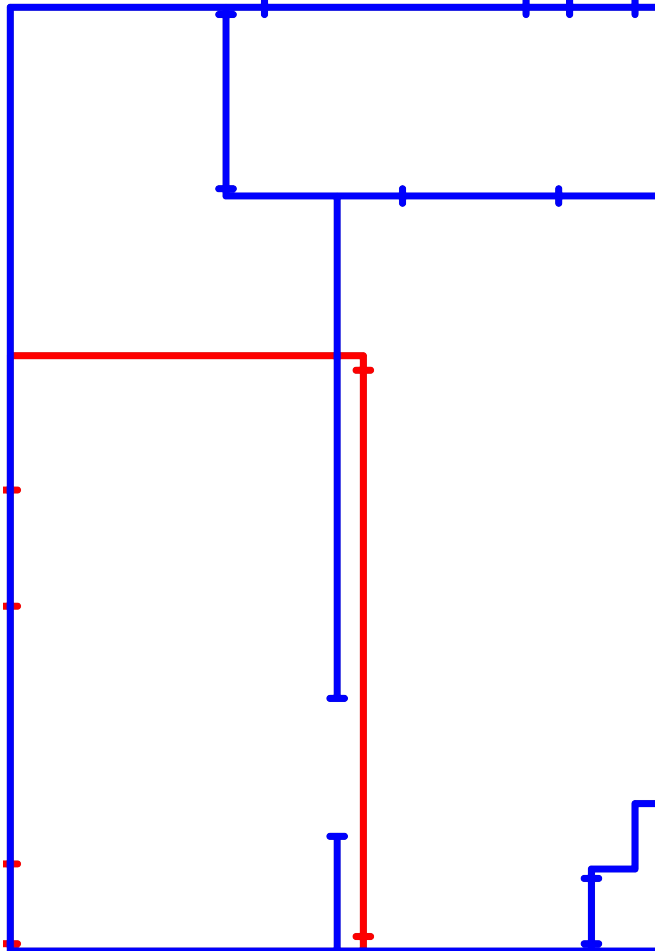
Mecatronique



Clean room

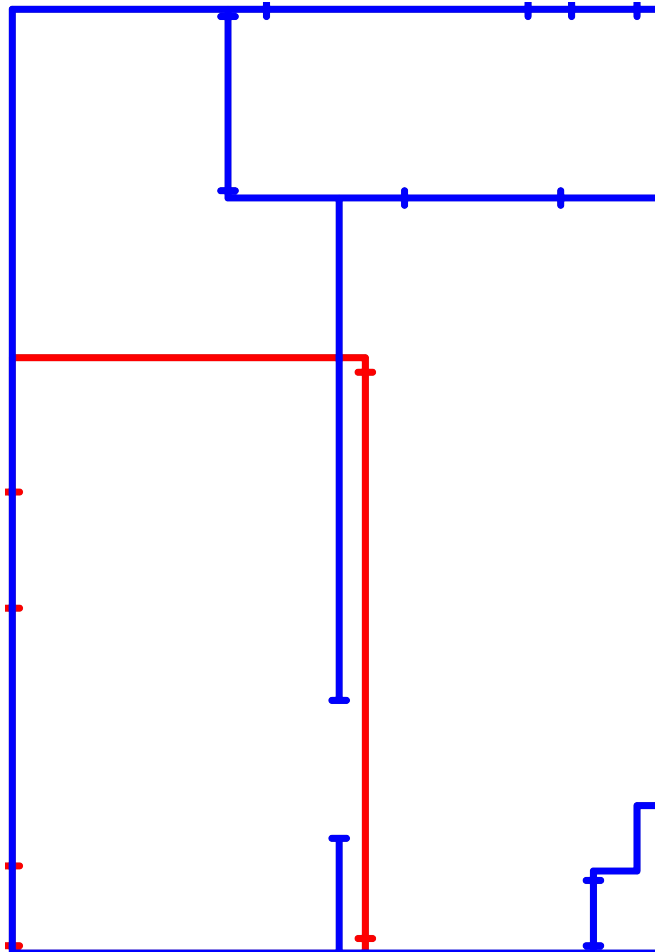


Floor Plans



- **Space :**
 - Mecatronique : 40 m²
 - Clean room : 100 m²
 - Assumption that it is useful to keep everything together in one room or at least in vicinity (or are there drastically different needs?)
- **Cleaniness :**
 - Not required during IBL construction « but should have been » (opinion of involved persons)
 - Grey room during Pixel construction
 - Constant effort necessary to make proper use of clean room
 - Alternative : laminar flow hood/tent for gluing ?
- **Supplies :**
 - Dry (oil less) compressed air
 - Nitrogen
 - Electricity
 - Vacuum
 - Network

Floor Plans



- Stations :
- 2 Module measurement (USBpix, light tight box, scintillator trigger, computer, work station, shielding prepared for work with radioactive source, probably cooling) à $(2+1)*1$ m
- Module construction mechanics, glue preparation, glue storage (fridge?), parts storage, module storage, work space, tooling à $3*1$ m
- Stave loading jig, tooling à $4*1$ m
- Stave testing similar to module testing, but different read out à $5*1$ m
- Climate chamber
- Source storage
- General works space
- Cooling

Radioactive source(s)

- Necessary for module testing
- Sr-90 and Am-241 traditionally used
- Extremely long buerocratic lead time : need to start radiation protection organization now

Next steps

- Finalizing module flex design and production
- PSPP commissioning
- Follow up sensor and read out status
- Lab planning

