# Expression of Interest: R&D on Tile Calorimeter Electronics for the sLHC

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## Abstract

The increased radiation levels expected at the sLHC will exceed the levels for which many Tile Calorimeter electronics components were designed. In this Expression of Interest we outline the R&D necessary to replace those components, as well as to accommodate the changes in architecture and core infrastructure systems likely to be required by modifications in the LAr and TDAQ systems. It appears likely that a large part of the readout electronics for the Tile Calorimeter will need to be redesigned and replaced.



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*Distribution List*

**ATLAS High Luminosity Steering Group**

# *1 Introduction*

The major mechanical and optical structures of the Tile Calorimeter are expected to continue to perform satisfactorily at the sLHC. This is true in spite of a significant loss of light from the optical components because of natural ageing and radiation effects. The predicted loss of light by the end of the sLHC running period is 50% to 65% in the first row of tiles, giving a yield of 25 to 35 photoelectrons/GeV. This number should give satisfactory calorimeter performance. The cryostat and perhaps the gap scintillators will need however to be replaced, even before the end of LHC running. The life time is estimated to be approximately 5 years for an estimated maximum local dose of ~ 1KGy/year (at $10^{34}cm^{-2}s^{-1}$). The construction, installation and fibre routing has been worked out in order to facilitate the easy removal and installation of new scintillators.

Significant parts of the TileCal on-detector electronics, however, are known to be insufficiently radiation hard at luminosities beyond $10^{34}$ $cm^{-2}sec^{-1}$ and must be redesigned. Also some subsystems will be reaching the end of their normal life cycle and will not be reasonably maintainable. This is highlighted by the fact that many components needed for the maintenance are already becoming obsolete and unobtainable.

Use of new components will require redesigned PCBs and represents an opportunity to improve both the electrical and mechanical architecture based on experience with the existing system. The modified design will have to be proven radiation tolerant enough for the upgraded luminosity. The modified system will also have to be compatible with updates to other parts of the ATLAS electronics system with which TileCal electronics must interface. These include a possible upgrade of the TTC, CANbus and DAQ systems, to the gigabit transceiver system, GBT [1]) which is currently in development and might be adopted by ATLAS. More substantively, there may be significant modifications in the TDAQ system such as bringing all the digitized data to pipeline and derandomizer memories in the counting room. This would make more detailed digital information available to the first level trigger sharing the same calibration as the DAQ. It will be a goal of this R&D to study appropriate modifications in the readout architecture and strategy appropriate to the higher luminosity and advances in technology.

# *2 Participating Institutions*

The following institutions to date have expressed interest in participation in this R&D project. It is expected that others will join in the near future.

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## *3 Topic(s) and goal(s) of the R&D proposal*

### a) Optical Systems

Although we expect the current scintillators, fibres, etc., to continue to perform well for sLHC, some studies should be continued to amplify and validate what has already been done:

- Perform more precise estimation of fibers and scintillators light loss under irradiation Complete natural and accelerated ageing studies for straight fibers and fibers under mechanical stress.
- Perform radiation damage studies of typical tile-fiber-profile sets.
- Continue ageing studies on the modules deployed in the cavern.
- Monitor the transparency of the light mixers installed on the detector.
- Continue lab tests to measure PMT gain variations.

### b) On-detector Electronics

Starting with the input to the electronics, it is thought that PMTs will not need to be replaced. It also appears that the current in the voltage divider is high enough to accommodate sLHC rates. If this proves true, existing PMT blocks, except for the 3 in1 cards could be retained.

By contrast, the rest of the front-end system including 3in1 cards, mother boards, mezzanine cards, digitizers, and optical interface card, will need to be completely replaced for reasons of radiation hardness and obsolete components. Some of the architecture can be retained. However, the number of independent PCBs needs to be reduced so there are fewer interconnections. Great care needs to be taken with the power connections to ensure maximum reliability. Some parts will need to be redesigned to work with the GBT system or other replacement for the current TTC and CANbus systems.

We will seek to upgrade from 10-bit to 12-bit ADCs with appropriate radiation hardness and to optimize the dynamic range and overlap of gain ranges. Also in the digitizer part we may need to adapt to the GBT system. The major change to be studied here would be the adoption of the strategy to move all digitized data off the detector. This would facilitate the goal of reducing both the count and variety of PCBs in inaccessible locations.

The following items associated with electronics in the drawers need in-depth studies:

- Preliminary studies indicate that the current parameters of pulse shaping and AC coupling can be retained in the new designs and that strategies are available for coping with the higher rates at sLHC. We should confirm these conclusions and investigate strategies such as clipping to reduce the PMT pulse width, which would then permit an overall shorter pulse shaping. This would, in turn, imply higher sample rates, probably 80 MHz to achieve the sample precision.
- Identification of components which can meet the radiation requirements. These include op amps, FET switches, an ADC, a DAC, voltage regulators, and an FPGA. Commercial parts should be tested for possible use by detailed tests of tolerance to TID, NIEL, and SEE. If no commercial parts are available a custom development program will be needed.
- Simplification of interconnections. Electrical connectors are perhaps the single-most troublesome component in a large system. Significant effort is needed to reduce this potential failure mode, including elimination of daughter boards, reduction of internal connectors, selection of robust signal connectors and cables, selection of robust power connectors, etc. Selected connectors must be qualified through detailed and explicit testing.
- Study the possible link technologies that can be used to transfer data from the drawer to the counting room. The raw DAQ data rate from the drawer would be about 46 Gb/s plus slow control. If this is formatted according to the GBT requirements the total rate would be about 80 Gb/s. Options need to be developed for dealing with this rate.
- It is probably difficult to add cables and fibers for communication between drawers and USA-15. It is thus highly desirable to find ways by which this can be avoided. Wavelength multiplexing presents such a possibility. The ideal case would be to combine all in- and outgoing fibers to one of the present fibers leaving the other as spares. This possibility should be thoroughly investigated.
- Slow controls and monitoring. Wireless technology is becoming mature, and it may be feasible to provide slow control and monitoring functions through the use wireless communication. Alternatively the use of the GBT may be desirable for this function. A careful evaluation of the options is needed.
- Study of the possibility of reducing the length of individual mechanical assemblies in the drawer system. Thus, the current system of two sub-drawers of length 1.5m each could be replaced by four sub-drawers of 0.75m each, weighing considerably less than the current 50 kg. This change will bring benefits of access for installation, maintenance, and service, but is likely to conflict with the goal of reducing failure-prone connections. The mechanical optimization of the system will therefore need to be done with considerable care. It is also likely that the photomultiplier magnetic shielding structure could be made considerably lighter, yielding much lighter drawers.

In addition to increased radiation hardness, we will pursue goals of much closer integration between the low voltage power supplies (LVPS) in the fingers and the electronics in the adjacent readout drawers. To that end, we will study replacement of the current two-stage LVPS distribution system with a three-stage system incorporating local regulators at multiple points in the drawers. We hope to significantly reduce the current complement of 8 independent voltages through appropriate choices of components in the drawers and the use of local voltage regulators. We hope to take advantage of the

resulting simplification of the LVPS by adding redundancy in the provision of power and hence the ability to recover from single failures.

The principal issues for study will be the following:

- Study of radiation-hard components. Assuming that the basic internal scheme of the LVPS remains the same, the goal is to select new components that have a higher level of radiation tolerance. This will involve the selection of new components, the development of appropriate test circuits, and testing them in a variety of environments that includes neutron, proton, and gamma radiation. Given the desire to move toward a three-stage architecture, of particular importance in this study is the selection of low-current voltage regulators that can be used by local circuitry in the front-end electronics.
- Study of alternative power supply schemes. While the buck-converter used in the current supplies is well-known and mature, there are other techniques that might be brought to bear for this application. One possible technique is the use of resonant converters.
- Reduction in the number of voltages produced by the LVBOXes. Some of the present voltages have very small loads, and could be generated by (rad-hard) voltage regulators in the front-end electronics. In general, a strategy for the future should be to regulate locally in the FEE where possible. This will relax the stringent requirements on the output voltages of the LVBOXes, make for better regulation at distal loads, reduce or eliminate the need for "tuning" of output voltages, and add some noise rejection, at the expense of an increase in dissipated power by the regulators. The addition of local regulators will make this a 3-stage power distribution system.
- Increased LVPS efficiency. The maximum efficiency of an LVBOX is only 65% when powering barrel super drawer electronics, and 60% when delivering power for extended drawers. Up to 90W of dissipated power has to be water-cooled inside of each LVBOX. This is due to the attempt to use a single design for all bricks over the wide range of output voltages and loads. This resulted in a non-optimized dc/dc converter design for each output voltage, in several cases necessitating the use of dummy loads for weakly-loaded bricks to provide stability.
- Star-distribution of power in drawers. The current system suffers from voltage-drop problems in the drawers due to serial "daisy-chaining" of power between modules. This will need to be developed carefully within the goals above of making the system more modular.
- Redundancy. Power supplies can be a primary mode of single-point failure. We will study and develop architectures that allow for the efficient and robust use of redundant power supplies for the front-end electronics. Areas of investigation include cold-starting of one of a redundant power pair, fail-safe architectures, and remote control techniques.
- System issues. Related to the above, it is clear that the performance of the overall system could be substantially improved with an "integrated system design" approach, involving FEE design, mechanical design, and power system design. These include load-balancing, choices of output voltages to optimize voltage regulator operation, requirements on power-sequencing and fault conditions, cooling, reduction in (and choice of) connectors, etc.
- Provision of remote configurability features throughout the LVPS/Drawer system.

### c) Back-End (off detector) Electronics

#### 1. Introduction

The ROD system has to provide high speed communication with front-end drawers in order to be capable of receiving the digitized data at bunch-crossing rate, pipeline and transmit pre-processed data to the L1 trigger system and transmit the required data to the Read Out System.

Hence, the new ROD design would include four differentiated parts (Figure 1):

1 Input stage
2 Data pipeline and L1 trigger pre-processing algorithms communication with trigger system
3 Data processing and data transmission to ROS.
4 Configuration and monitoring system and TTC interface.

The R&D needed should investigate the four different parts of the ROD system as separated stages and taking into account the interaction with the outside world. The input stage will depend on the on-detector system; the L1 pre-processing algorithms have to be studied with L1 trigger upgrade specifications and requirements and the output stage will depend on the ROS upgrade.

Hence, the R&D proposals are:

- To perform a technology analysis for the input stage. Based on the need for new fiber connections from the front-end electronics and the BE RODs we should study the signal transmission using state-of-the-art optical transceivers.
- Study the consequences of moving pipeline and derandomizers from the drawers and the L1 trigger pre-processing algorithms and communication with the rest of the trigger system into the ROD environment.
- Investigate and evaluate Digital Signal Processing algorithms limits for the data processing and data transmission to ROS and how this can be implemented in FPGAs. We should evaluate different FPGA models and clock frequencies for the L1 trigger rate and event format. Determine the output data bandwidth needed to transmit the data to the ROS system. Depending on ROS upgrade specifications the output system of the ROD has to be specified.
- Configuration, monitoring and synchronization (i.e. the former TTC interface) have to be investigated in connection with the performance of new crate communication systems to replace the VME protocol. We should evaluate the performance of the Advanced Telecommunications Computing Architecture (ATCA) as well as the more compact μTCA standard. These systems provide higher data transmission allowing higher amount of data transmission for control, monitoring and other purposes. Evaluate the performance and gain experience with these standards. Determine data transmission capabilities through the bus for control, monitoring and any other data transmission requirements (data transmission to L1 trigger system, data communication between RODs for most complicated reconstruction algorithms,...etc). The TTC interface using the GBT or any other device following CERN requirements should be investigated. If the GBT is chosen it will also necessary to interface the ROD system with the DCS.

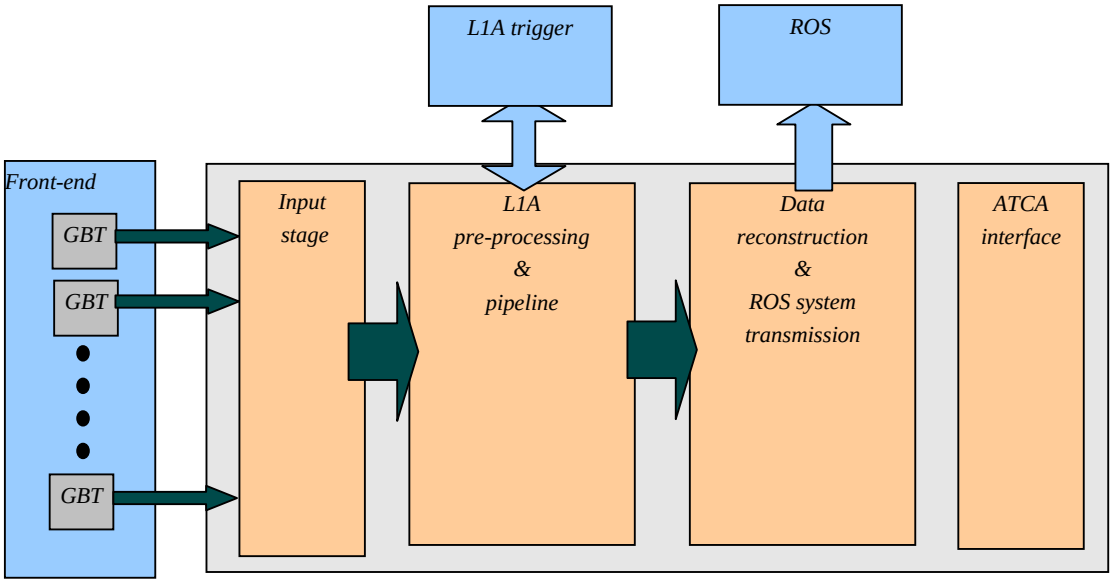


*Figure 1. ROD system upgrade architecture.*

d) Off-detector power supplies and controls

High voltage (HV) power supplies are designed to power 10 000 TileCal photomultipliers. They are realized by 16 pieces of 19“ crates 6U high. Each crate has 8 two channel cards. The HV power supply thus delivers altogether 256 HV channels. Each channel can be set to one of two levels of negative voltage -830V and -950V and delivers maximum current 20mA. The channel supplies one electronic drawer in the pit with up to 64 photomultipliers. Each photomultiplier in the drawer has an HV power divider that exactly sets the photomultiplier’s voltage.

Off-detector low voltage (LV) power supply system is more complex in comparison with HV. The USA15 power supplies deliver 200V DC power to the pit where it is split to the individual channels (drawers) and is then converted by the finger power supplies to all low voltage levels needed in the drawers. Together 24 units are installed in USA15. Each unit has 3 channels; each channel is 200V DC and current up to 10A. In the pit, 64 channels are split and each channel powers 4 electronics drawers. For control and safety of the low voltage power system, so called 64 AUX boards, 4 DSS-LVPS interlock cooling cards and 4 pieces of CAN OPC servers (maintained by DCS) are installed.

Whether the functionality of these two sets of power supplies will still be appropriate to the needs of TileCal for sLHC will depend on the results of the redesign of the on-detector electronics discussed above. In any case, we must anticipate that these specially designed power supplies may not continue to be maintainable into the sLHC era because of unobtainable components and other lifetime issues. They will need to be replaced. Of course, replacement for the power supplies and controls should be planned in close coordination with the design of on-detector electronics.

## *5 Relation to existing efforts*

We intend to closely follow the R&D activities within the liquid Argon community [2]. There are important synergy effects to be gained and a unified approach is desirable where it does not conflict with

other considerations. However, the comparative simplicity and lower radiation exposure may allow simpler and less costly solutions. The development of the GBT project [1] will affect the choice of transmission solutions. The versatile optical link project [3] will also be monitored along with searching for suitable commercially available optical components. We also aim to collaborate closely with the level 1 calorimeter trigger community.

## *6 Schedule*

We will develop a schedule suitable for Phase II installation in the end of 2016 using our experience from the present activity. Initially we will need a 2-year period to complete much of the R&D activities presented in this document. After this we must turn to prototyping and production planning. The prototypes should be evaluated in a test beam environment. It would, of course, be very useful if the new system could be designed in such a way that it can be installed "adiabatically" on a drawer-by-drawer-basis.

## *7 Resources*

The work discussed in this EoI will start within existing budgets. This will lead to a slower start than would be optimal and some unevenness in what can be done at first in different countries and institutes. Applications will be made for funding for ATLAS Upgrade R&D to the relevant funding agencies. Approval of this EoI will be important for obtaining funds.

## References

1 The GBT, a Proposed Architecture for Multi-Gb/s Data Transmission in High Energy Physics, P. Moreira, CERN – Geneva, Switzerland, presented at Topic Workshop on Electronics for Particle Physics
September 3 - 7, 2007, Prague, Czech Republic

2 LAr reference

3 Versatile Optical Link reference