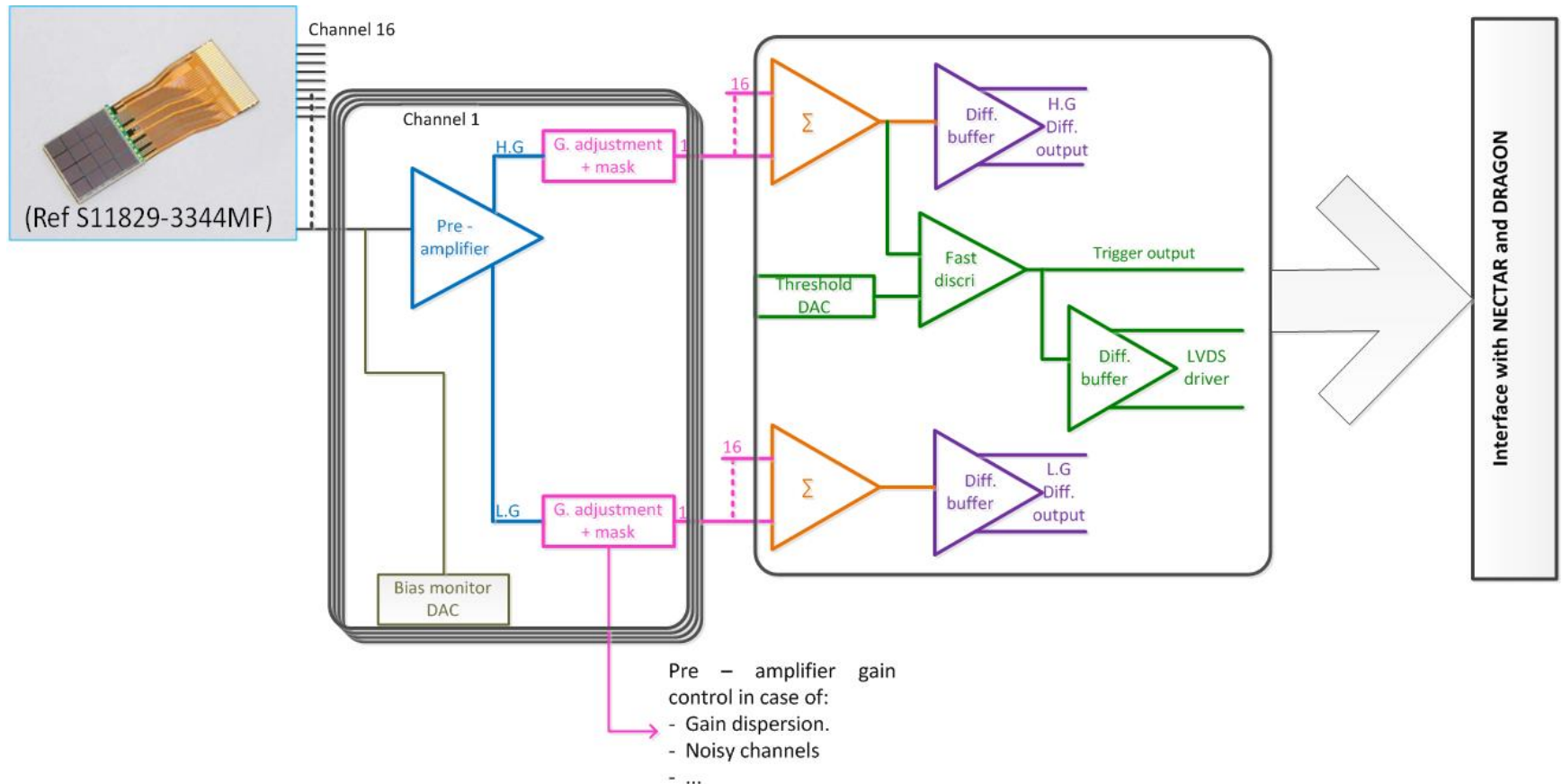


Readout ASIC for SiPM detector of the CTA new generation camera (ALPS)

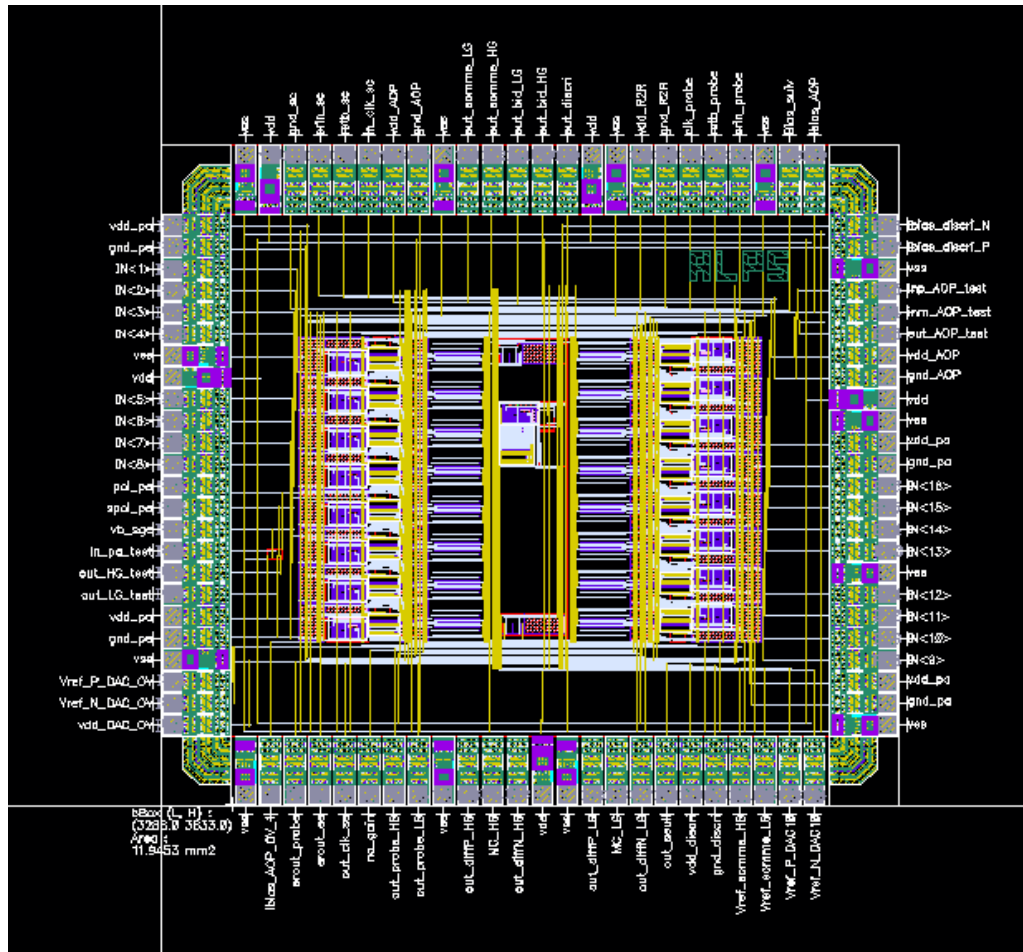
N.Fouque, R. Hermel, F. Mehrez, Sylvie Rosier-Lees
LAPP (Laboratoire d'Annecy le Vieux de Physique de Particules)

03/07/2014

ALPS chip – bloc scheme



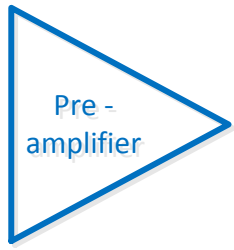
ALPS chip– Layout sent to fabrication 03/03/2014



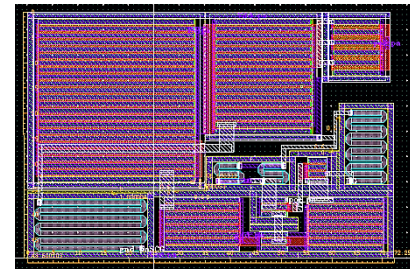
- AMS BiCMOS 0.35μm
- 96 pin out
- Die size:
about 3.673 X 3.298 mm²

We haven't received it yet!

To be tested at the beginning of June

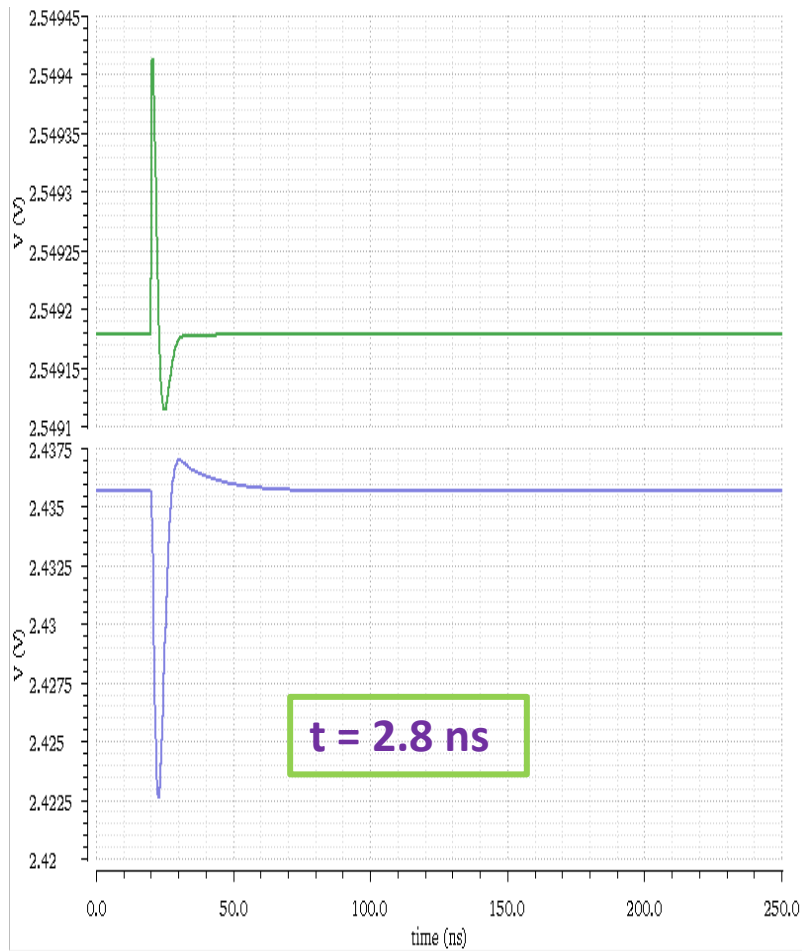


Pre-amplifier

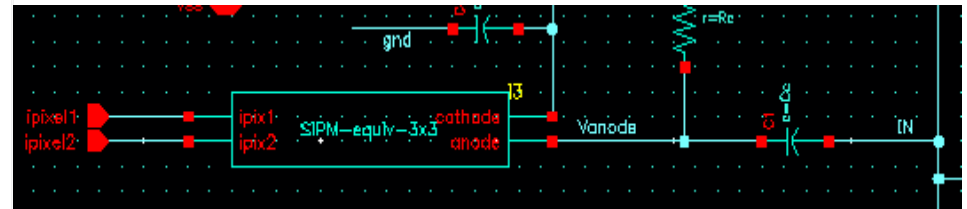


- 16 channels: adapted to 4x4 SiPM matrix
- Principle:
 - Low input Impedance about 20 ohm.
 - Fast response < 5ns
 - => **Current mode**
- Dynamic range:
 - From 1 up to about 2000 photoelectron (pe)
 - Signal to noise ratio (SNR) > 5
 - => **2 Gains**
 - HG covers from 1 to about 125 pe
 - LG covers from 11 to about 2000 pe
 - Gain ratio about 92, gain overlap 1 decade
- Voltage output
- Low power consumption < **30mW** at this stage (from simulation)

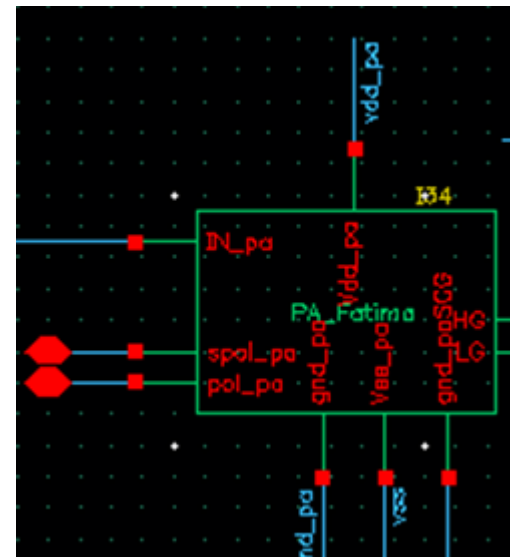
Pre-amplifier simulation (1)



Simulated SiPM signal 1pe

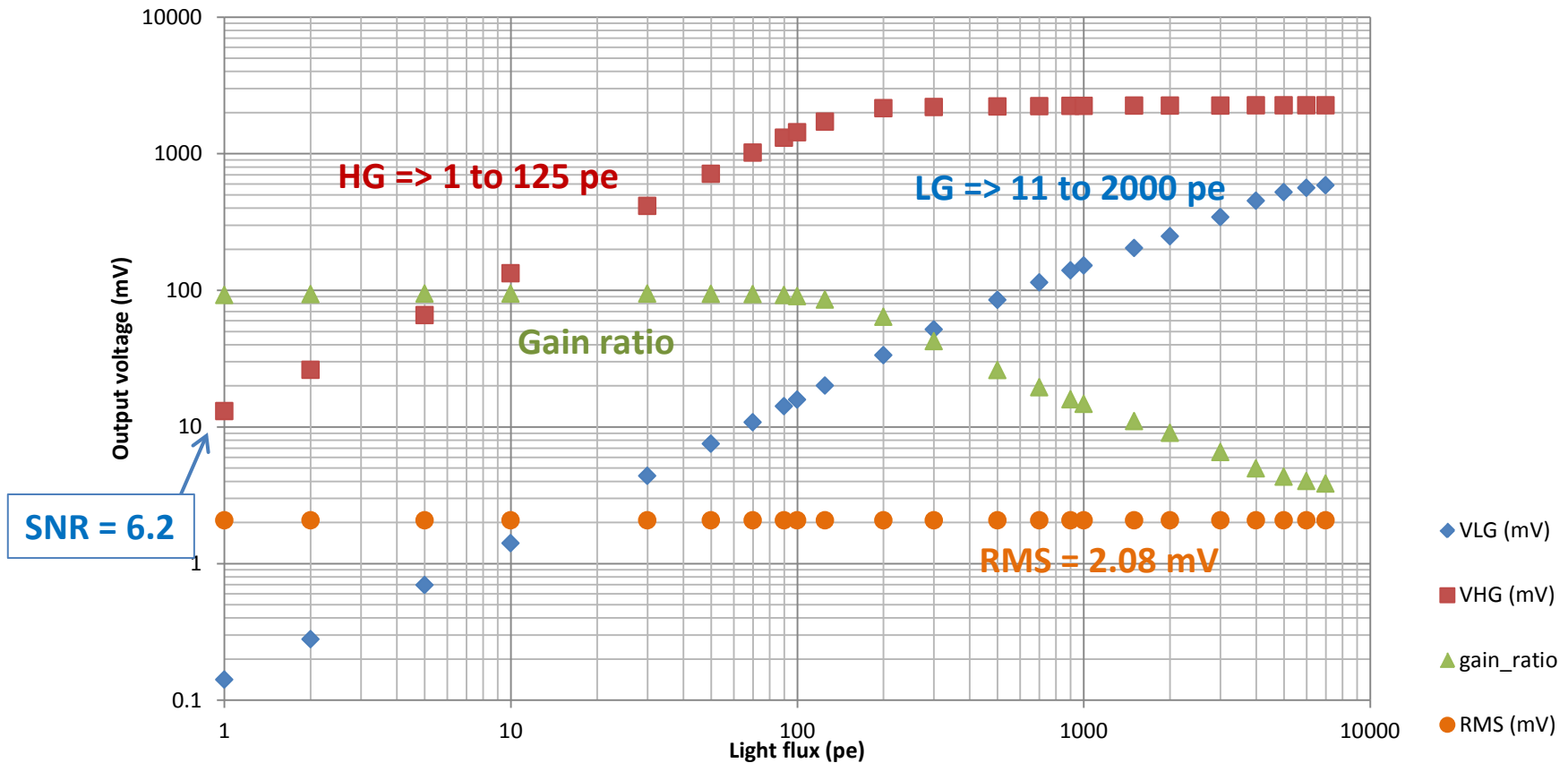


High gain response

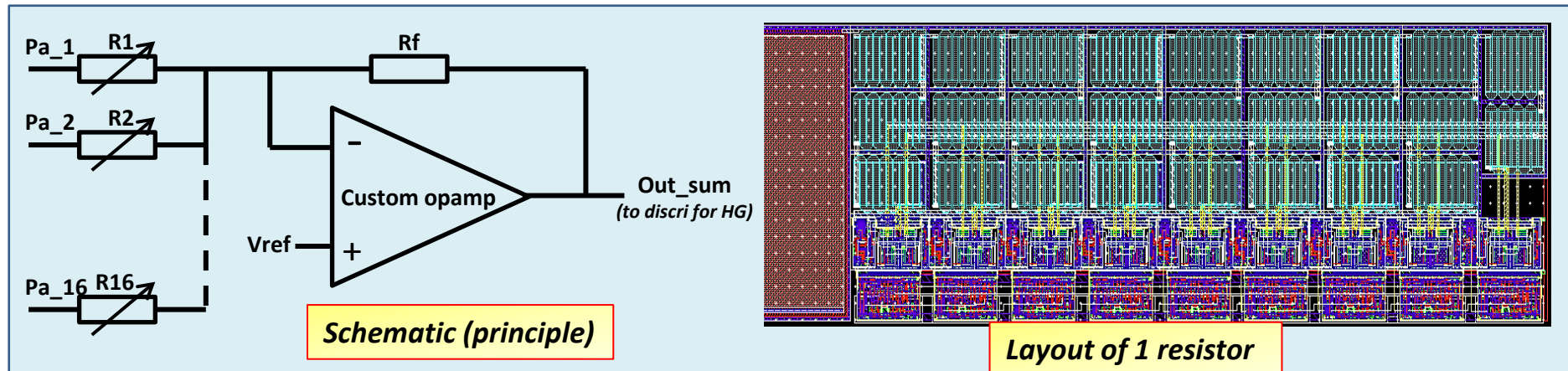


Pre-amplifier – simulation (2)

DR & Linearity

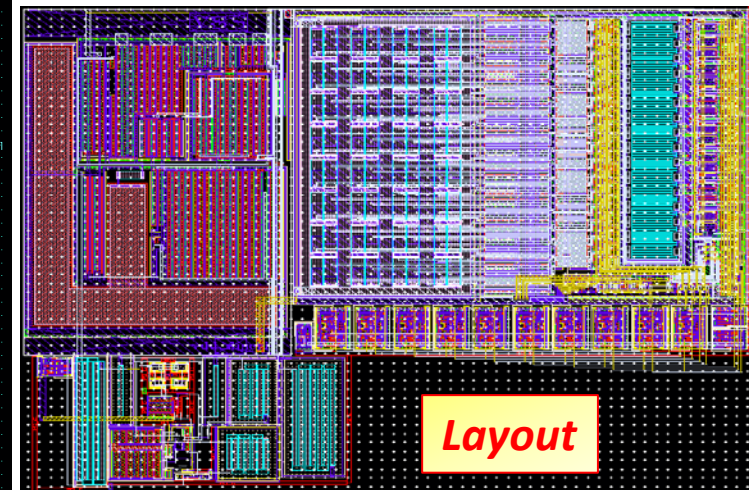
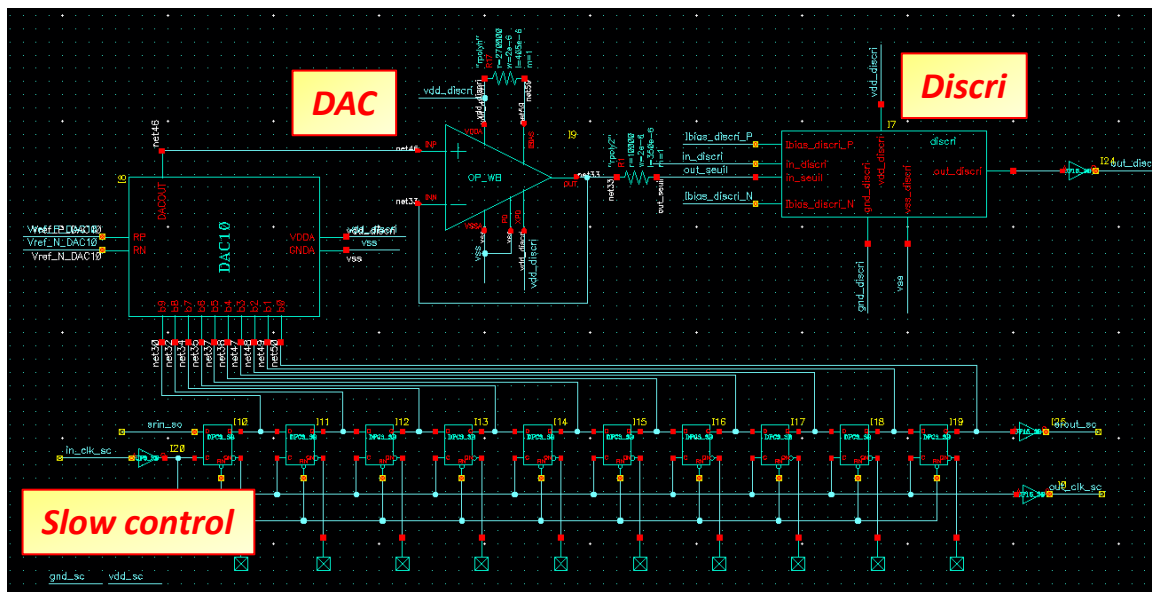


Analog sums and gain control



- Weighted sum of the 16 preamp outputs by digitally controlled resistors
- Each resistor has a R-2R like architecture :
 - Preamplifier always sees the same load (better for linearity)
 - 8 bits resolution for gain adjustment
 - Noisy channels can be digitally removed
- CR shaping included in each channel
- Adjustable Vref to match the discriminator threshold

Trigger (DAC + discri)



- Discriminator (full custom) :
 - Dual bipolar input stage to minimize offset
 - Self-biased
 - Buffered digital output for trigger
- 10 bits DAC for threshold
 - AMS standard cell
 - Digitally controlled threshold

Perspective:

- Test board (to measure the performance of the ALPS chip) has been designed and submitted.
- Collaboration?