

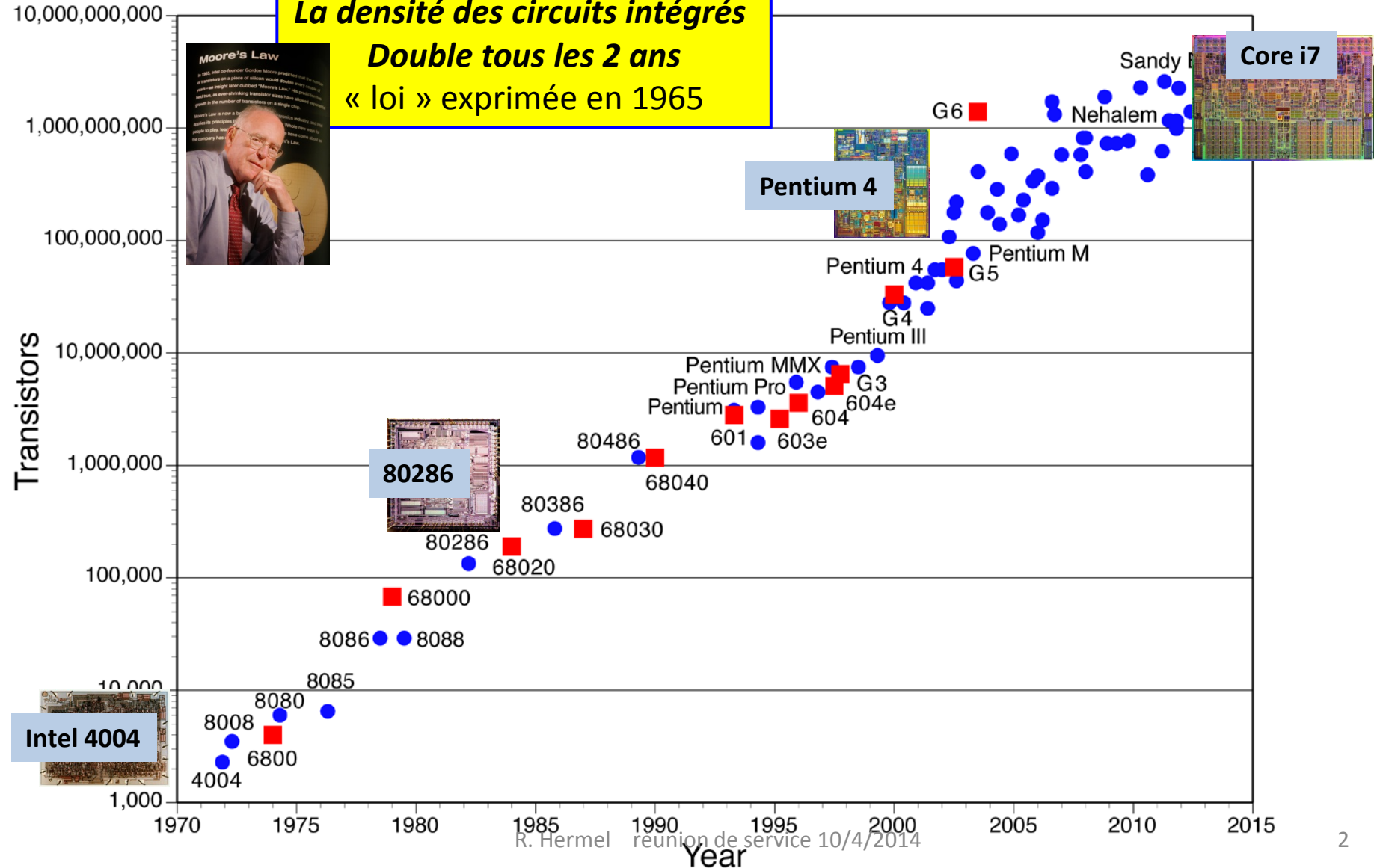
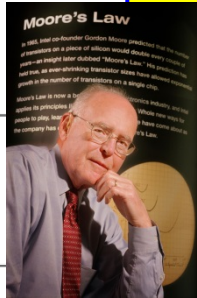
Microélectronique

(pour les « pas si nuls que ça ... »)

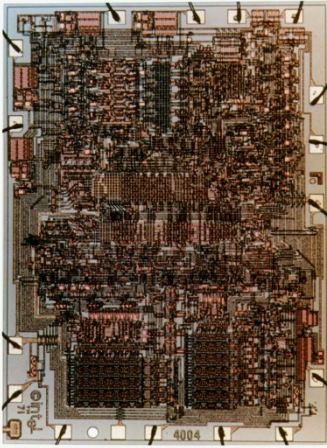
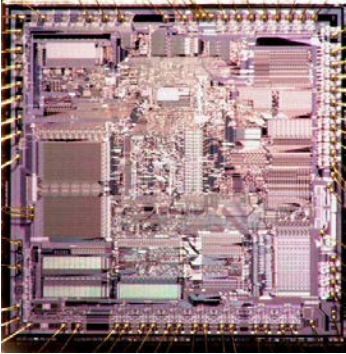
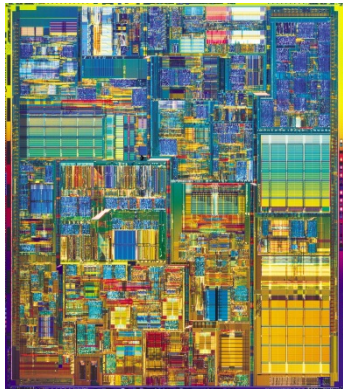
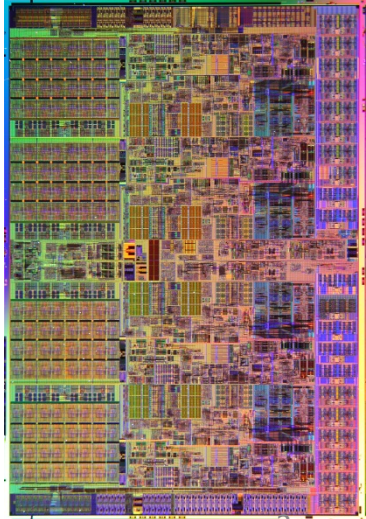
- Quelques ordres de grandeur
- La technologie BiCMOS AMS 0.35
- ASIC analogique : de la conception à l'envoi en fonderie

La « loi » de Moore

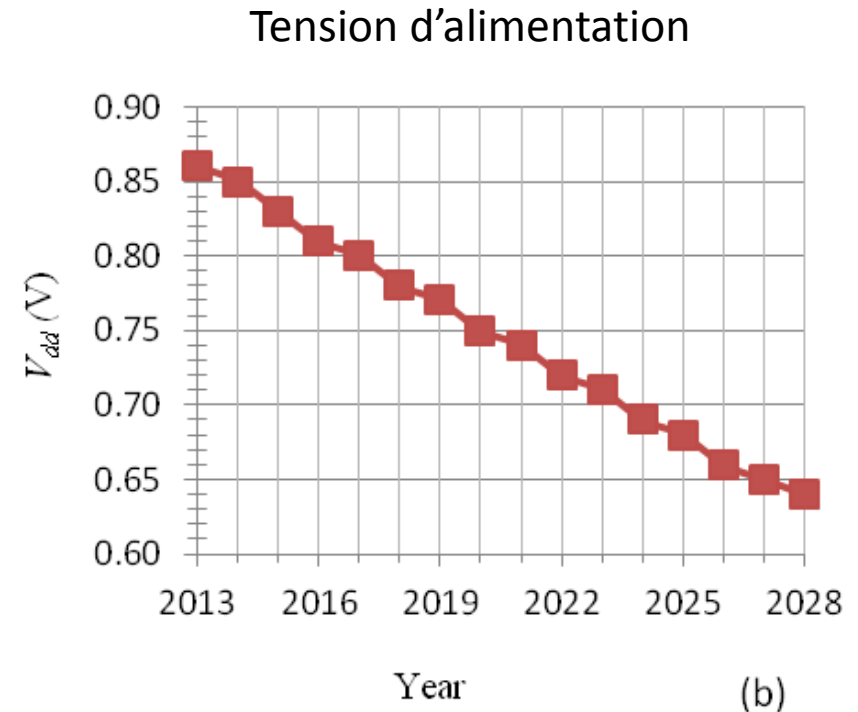
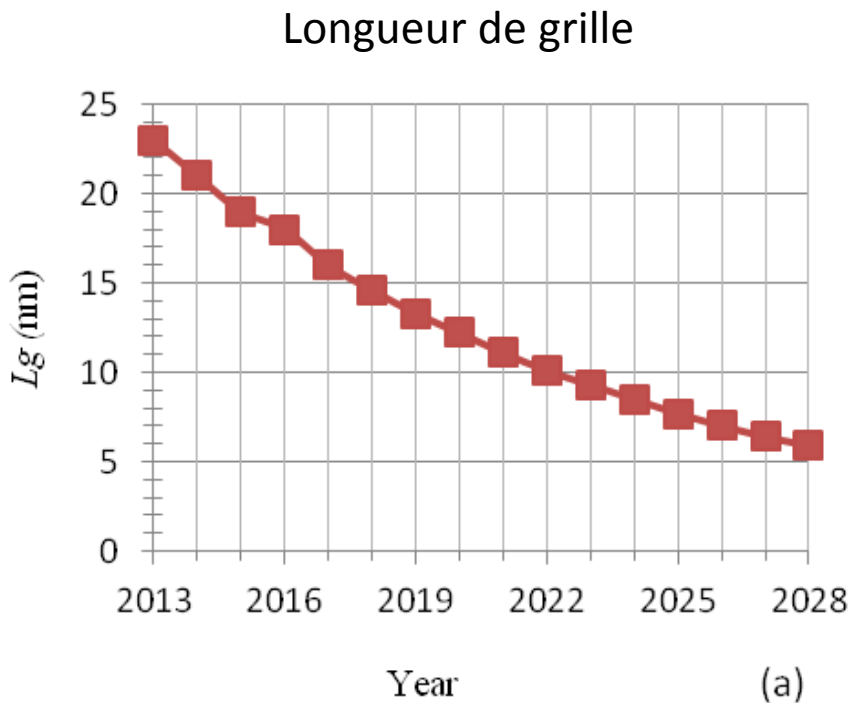
La densité des circuits intégrés
Double tous les 2 ans
« loi » exprimée en 1965



Quelques générations de processeurs... Intel

nom	4004	80286	Pentium 4	Core i7
Année	1971	1982	2000	2008-2014
Technologie	10 μm	1.5 μm	180 nm	22nm
Nb transistors	2300	130 k	42 M	1.4 G
Surface	12 mm ²	47 mm ²	217 mm ²	348 mm ²
F clk	740 kHz	20 MHz	1.2 GHz	3.4 GHz
Alimentation	12V	5V	1.3V	1.4-0.9 V
Boitier	DIP 16	PGA 68	PGA 243	BGA 1150
				

Evolution des dimensions / tensions



Source : THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2013

Technologie : perspectives

Year of Production	2012	2013	2014	2015	2016	2017	2018	2019	2020
DRAM ½ Pitch (nm) (contacted)	35,72	31,82	28,35	25,26	22,50	20,05	17,86	15,91	14,17
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	31,82	26,76	23,84	21,24	18,92	16,86	15,02	13,38	11,92
MPU Physical Gate Length (nm)	22,09	20,17	18,41	16,80	15,34	14,00	12,78	11,67	10,65
Number of metal levels (includes ground planes and passive devices)	12	13	13	13	13	14	14	14	14
Total interconnect length (m/cm ²) – Metal 1 and five intermediate levels, active wiring only [1]	3 125	3 704	4 167	4 762	5 291	5 917	6 667	7 463	8 403
J _{max} (MA/cm ²) – intermediate wire (at 105°C) [7]	1,32	1,50	1,68	1,79	1,81	2,01	2,29	2,34	2,59
Interlevel metal insulator – effective dielectric constant (κ)	2.82-3.16	2.55-3.00	2.55-3.00	2.55-3.00	2.40-2.78	2.40-2.78	2.40-2.78	2.15-2.46	2.15-2.47
Interlevel metal insulator –bulk dielectric constant (κ)	2.55-2.71	2.30-2.60	2.30-2.61	2.30-2.60	2.20-2.55	2.20-2.55	2.20-2.55	2.00-2.40	2.00-2.40
Copper diffusion barrier and etch stop – bulk dielectric constant (κ)	3.5-4.0	3.00-3.50	3.00-3.50	3.00-3.50	2.60-3.00	2.60-3.00	2.60-3.00	2.40-2.60	2.40-2.60

Exemple : Les interconnections

13 niveaux en 2014, Longueur > 4km/cm², Densité de courant : 1.7 MA/cm²

14 niveaux en 2020, Longueur > 8km/cm², Densité de courant : 2.6 MA/cm²



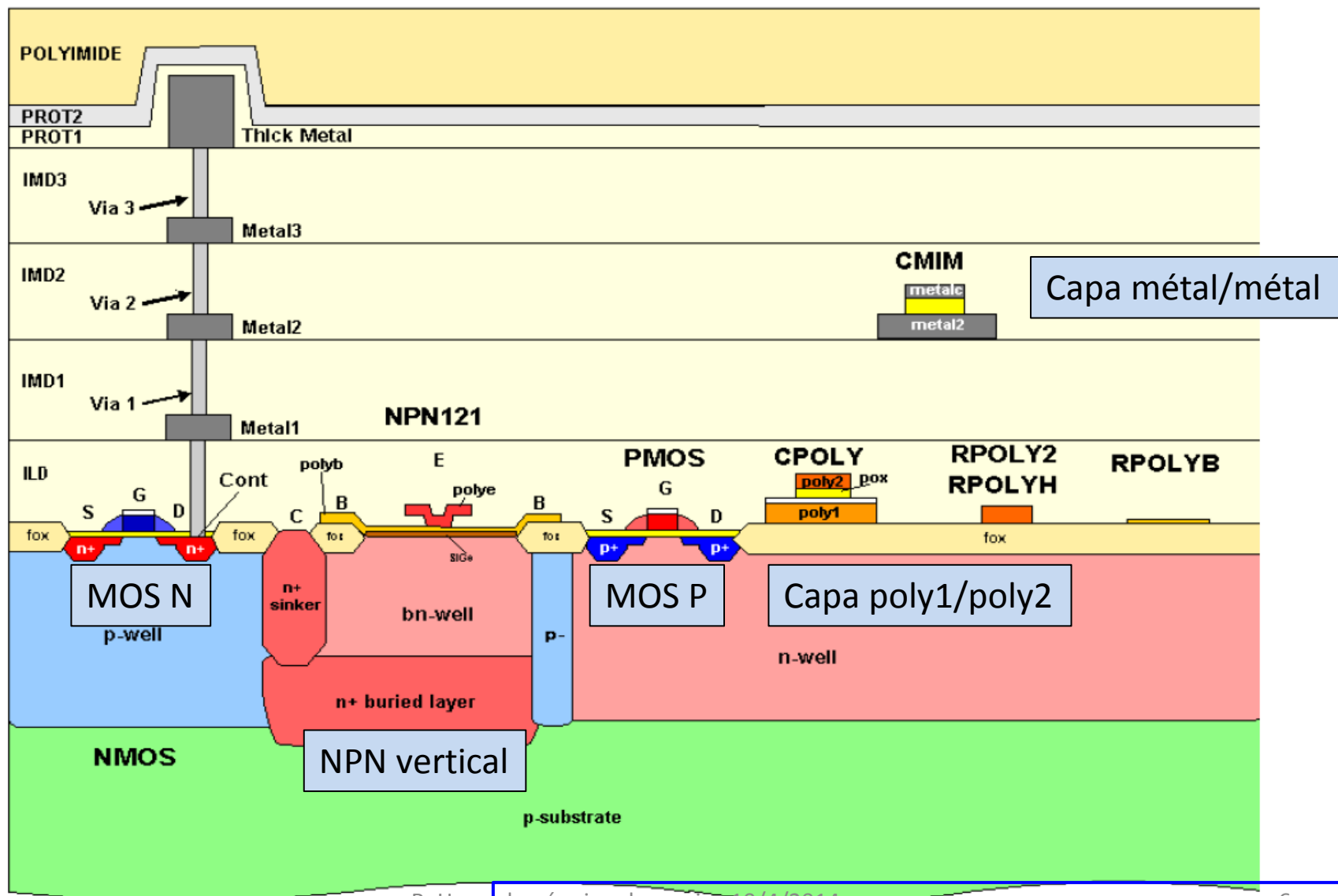
: Solutions en cours de développement



: Pas de solution connue actuellement

Source : THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2013

La techno AMS BiCMOS 0.35



ASIC analogique : de la conception à l'envoi en fonderie

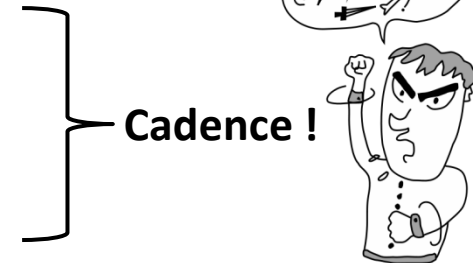
- Expérience

- Physicien(ne)s $\Rightarrow$ Idées (beaucoup !)
- Spécifications (approximatives ...)
 - Physicien(ne)s et électronicien(ne)s (beaucoup d'idées aussi ...!)



- Conception

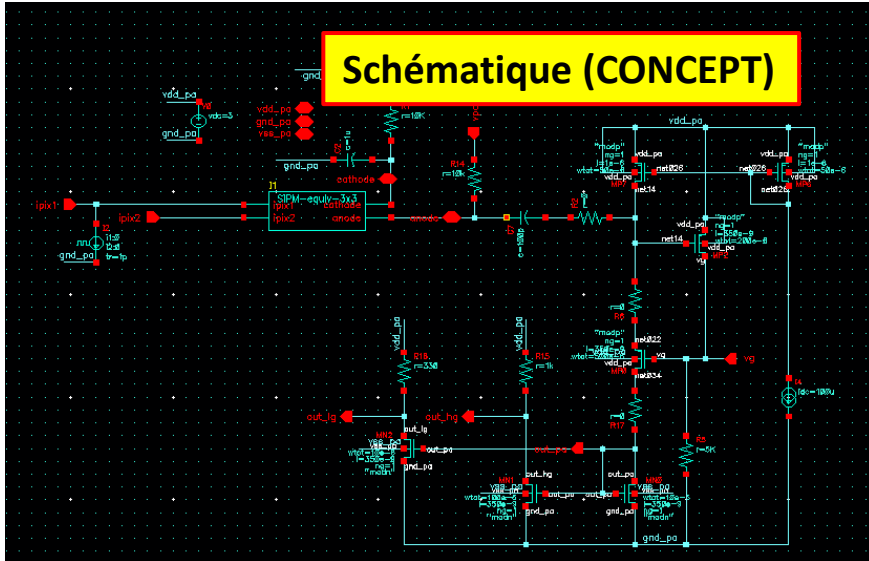
- Simulations
- Dessin des masques (layout)
- Vérifications



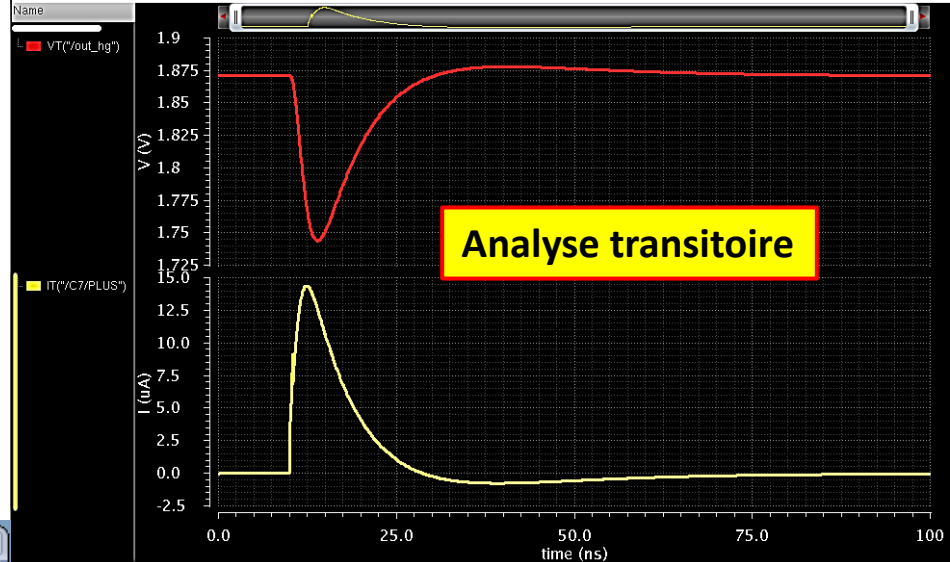
- Fabrication (fonderie) $\approx$ 3 mois
- Test
- Installation sur le détecteur ... (ou pas) ?

Simulations (SPECTRE)

Schématique (CONCEPT)



Transient Analysis 'tran': time = (0 s -> 100 ns)



Results Display Window

Window Expressions Info Help

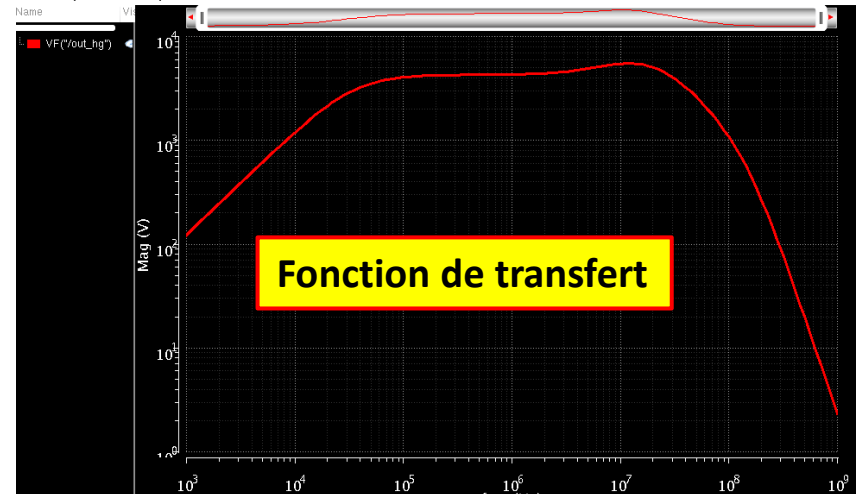
cadence

Device	Param	Noise Contribution	% Of Total
/MP2	id	3.24714e-06	65.79
/I1/R2	rn	7.36885e-07	14.93
/MP0	id	3.13001e-07	6.34
/R5	rn	2.35787e-07	4.78
/MN0	id	1.76357e-07	3.57
/MN1	id	6.75891e-08	1.37
/MP7	id	5.75235e-08	1.17
/MP6	id	5.15286e-08	1.04

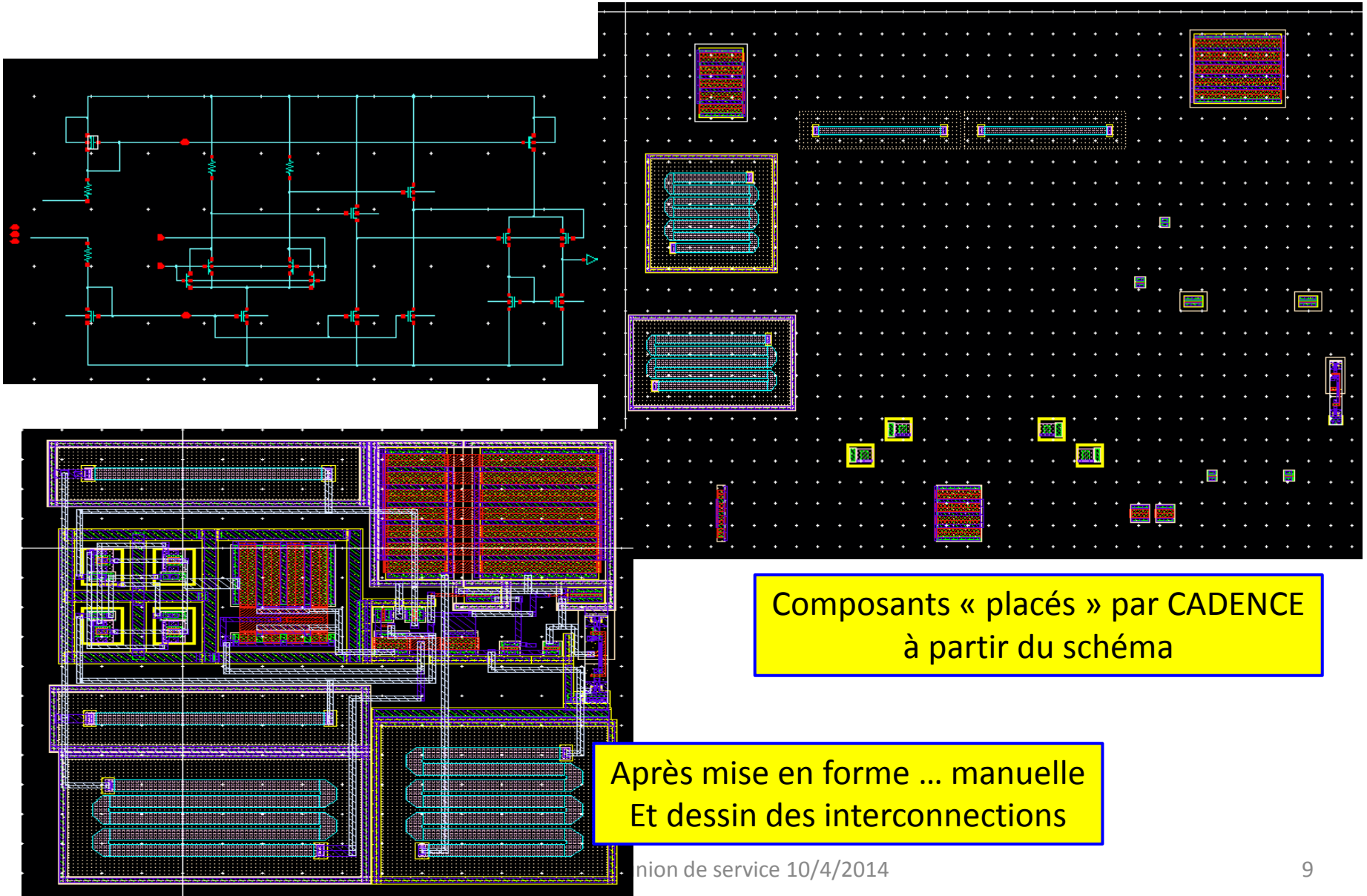
Analyse du bruit

Integrated Noise Summary (in V²) Sorted By Noise Contributors
 Total Summarized Noise = 4.93544e-06
 Total Input Referred Noise = 2.17895e-08
 The above noise summary info is for noise data

AC Analysis 'ac': freq = (1 kHz -> 1 GHz)



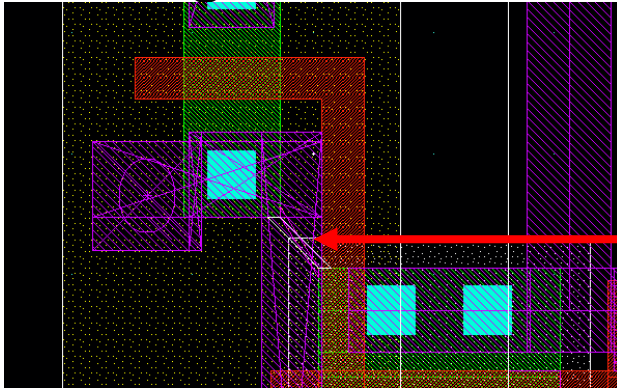
Dessin des masques (layout)



Vérifications

- **ASSURA** ou **CALIBRE** (outil Mentor)

- **DRC : Design Rules Check**



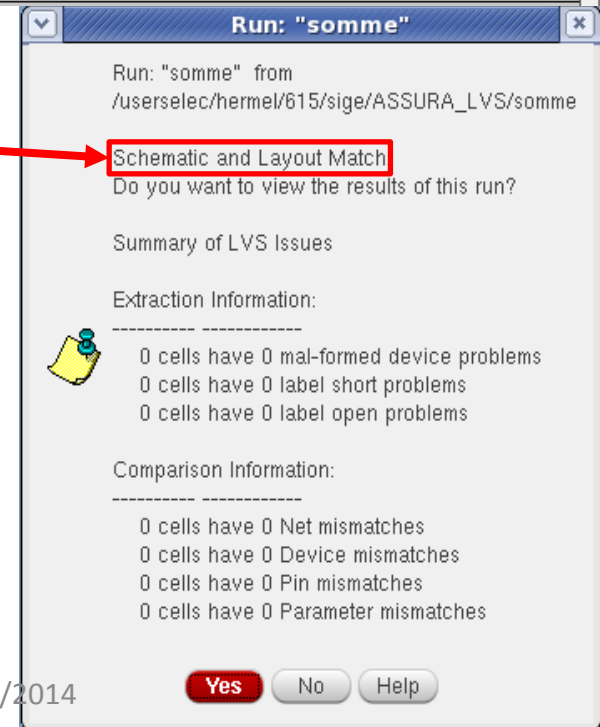
AV	NV
☐	[1] DEVICE Error: Illegal nmosh device
☐	[1] BAD_SUBSTR_SUBTAP_MULTCONN_ERC
☐	[5] BAD_NWELL_WELLTAP_MULTCONN_ERC
☐	[1] NMOSH_01/NMOSMH_01 Element Rule : Gate Overlap of Ntub =
☐	[2] NMOSH_E1/NMOSMH_E1 Element Rule : Poly Extension of gate
☐	[4] NMOSH_L1/NMOSMH_L1 Element Rule : Gate Length = 3.0 U
☐	[2] OD_W_1 Minimum DIFF width to define the width of NMOS /
☐	[2] OD_S_1 Minimum DIFF spacing = 0.6
☐	[1] OD_C_2 Minimum NDIFF to NTUB spacing = 1.2

- **LVS : Layout Versus Schematic**

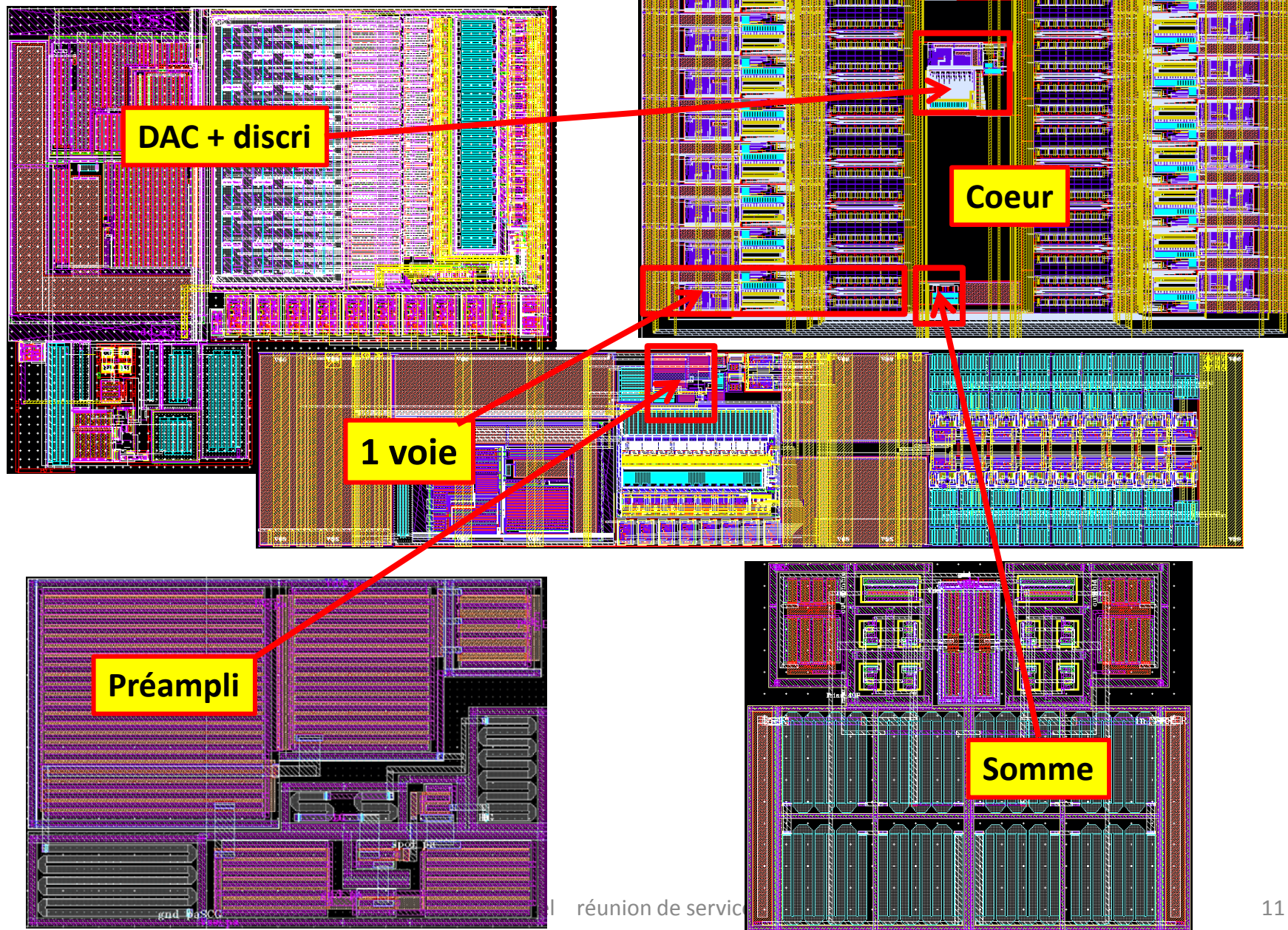
- Vérifie la correspondance entre le schéma et le layout

- **Simulation post layout : QRC**

- Prise en compte des éléments parasites Introduits par le layout



ALPS : Quelques blocs



Circuit final : Schéma + Layout

