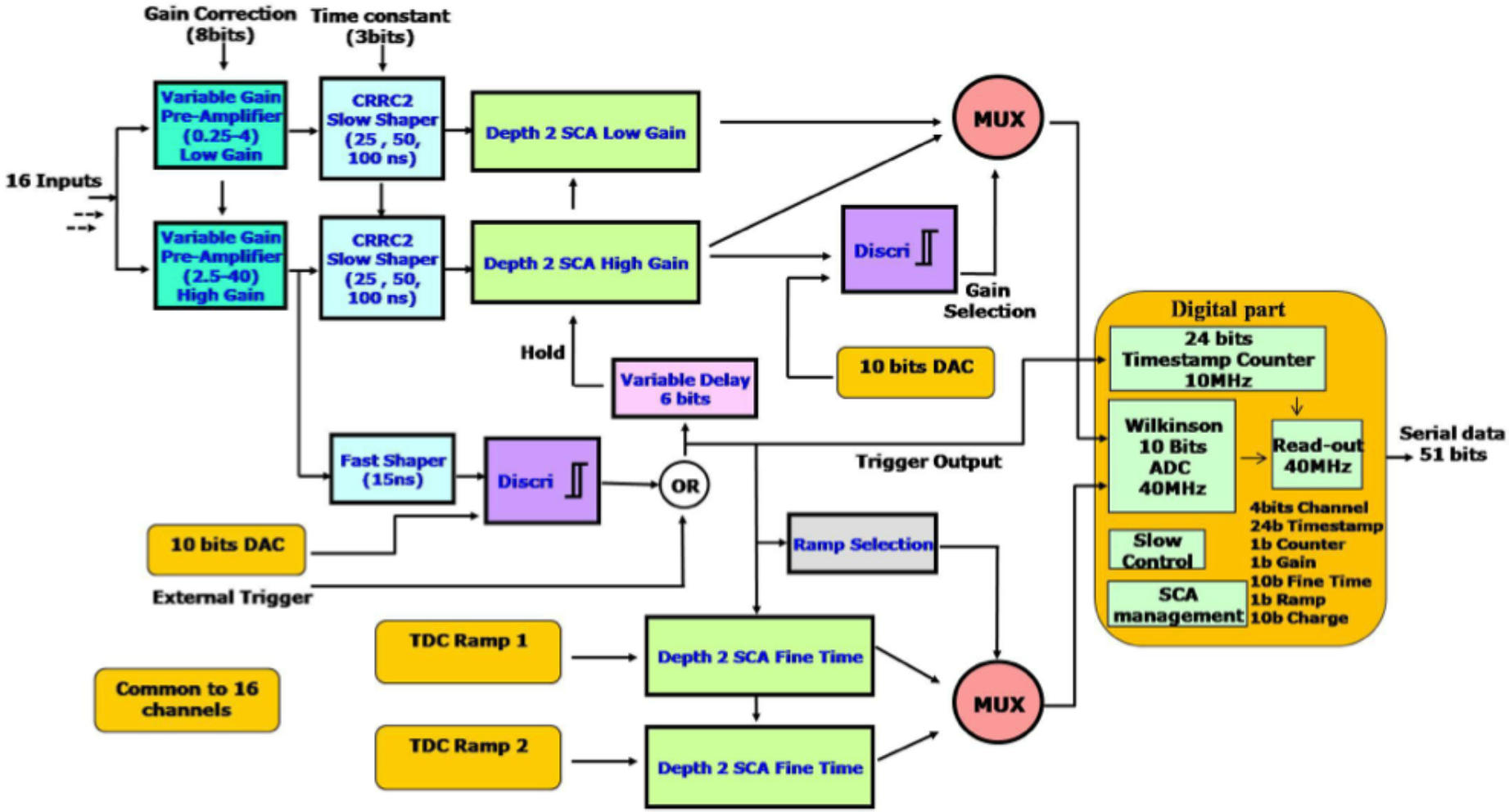
Réunion APC-LAPP
21-03-2014

Situation électronique
Pmm2 + PARISROC2

Specifications PARISROC2

- Variable gain to use a common high voltage for the 16 PMTs
- External 50Ω input impedance to terminate the PMT cable to the ASIC
- Auto-trigger on 50fC (1/3 of p.e. at PMT gain of 10^6)
- Charge measurement up to 100pC (600 p.e. at PMT gain of 10^6)
- Time tagging better than 1 ns (TDC)
- Internal conversion
- Sample rate up to 40 MSPS
- Single channel event rate up to 5 KHz

Architecture PARISROC2



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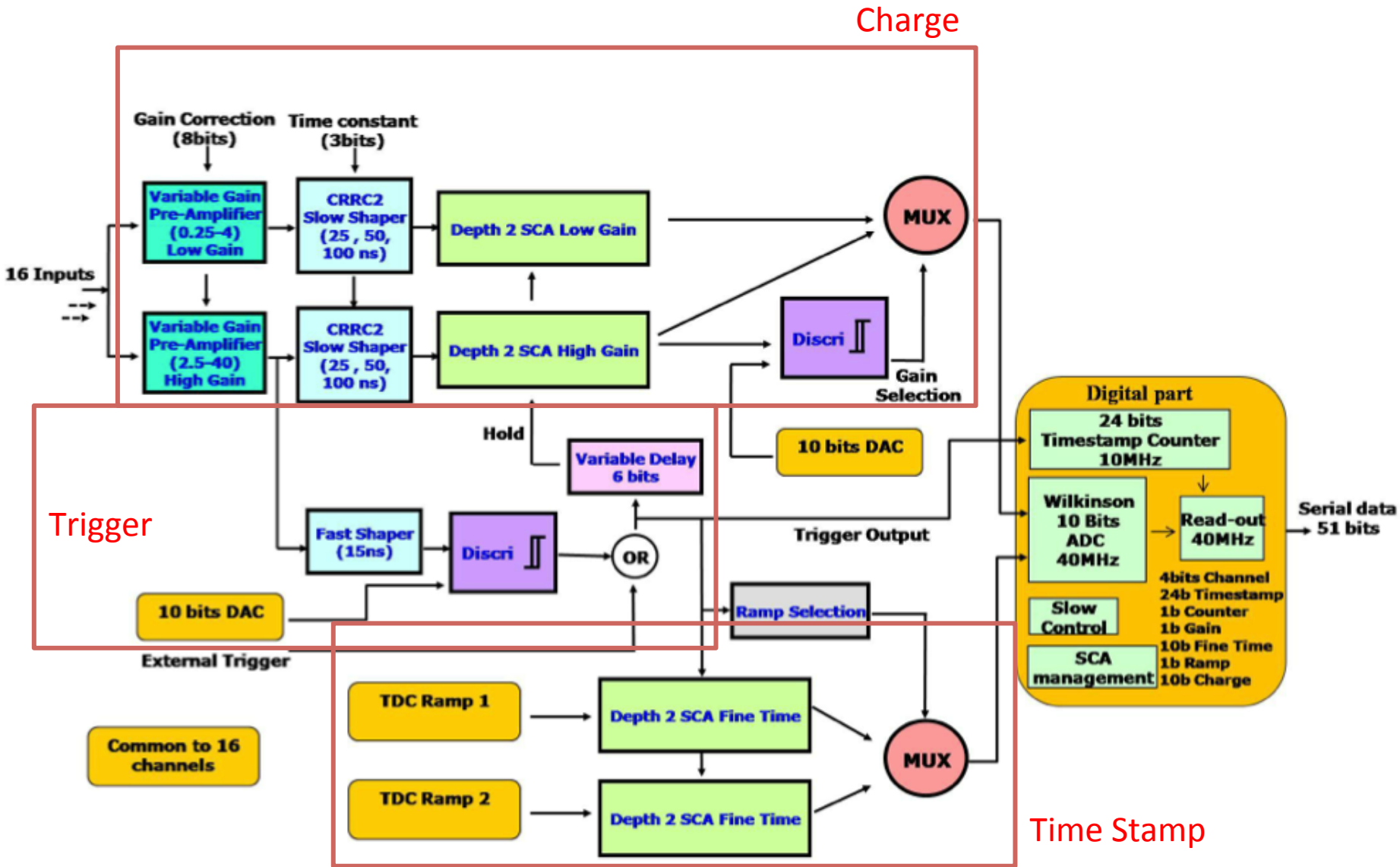

Key parameters

SCP	Purpose
Discriminator of DAC 0	*Setting threshold and adjustable step (0 to 1023, default = 0)*
Discriminator gain of DAC	*Setting the switch point of HG & LG (0 to 1023, default = 0)*
Trigger Delay	*Measuring the charge (0 to 64, default = 8)*
Slow Shaper Gain	*Setting the gain of slow shaper (from 16K to 64K, default =16K)*
Slow Shaper Time Constant	*Setting the time of shaper (from 0ns to 175ns, default = 50ns)*

Problems found

- Lack of proper documentation: Complex calibration
- Water on the card: Canal 1 out of service
- Only half of the ADC scale due to architecture: Increase of the shaping time aggravate the situation
  - Pmm2 board resistance under study
- Lack of sync mechanism