EXOGAM2 project

Digital instrumentation of the EXOGAM detector

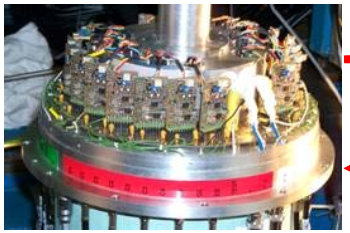
- Overview of the technical project
- Status of the digitizer prototype
- Synergy EXOGAM2 NEDA

M. Tripon

General architecture

Preamplifiers

16 clovers
=
64 crystals



7 analog signals per crystal
(ICR < 100kHz per crystal)

One test per crystal

Differential stages
and
test pulse generator

Connexion box

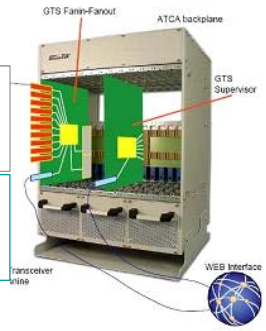
64 crystals
=>
64 boxes

7 differential analog links per NIM board

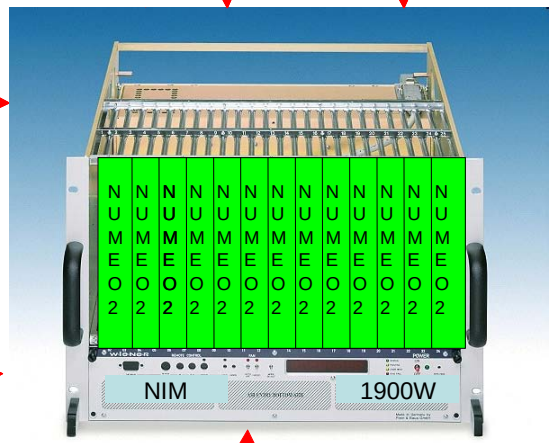
Control link

Global Trigger and Synchronization

1 GTS supervisor
and
34 GTS mezzanines



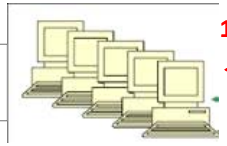
1 optical link per NIM board



Digitizing, Processing and Dating

1 crystal
Per
NIM board
=>
64 NIM boards

KALMAN processing



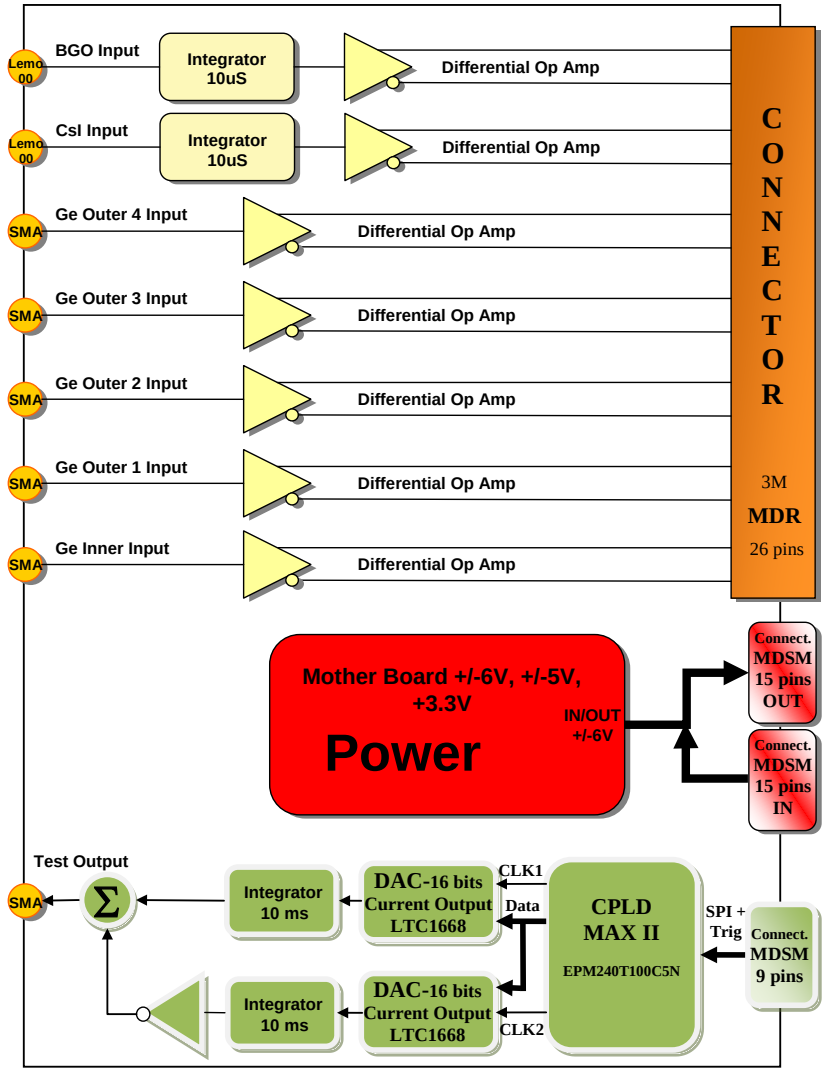
1 optical link per NIM board (< 2 Gb/s)

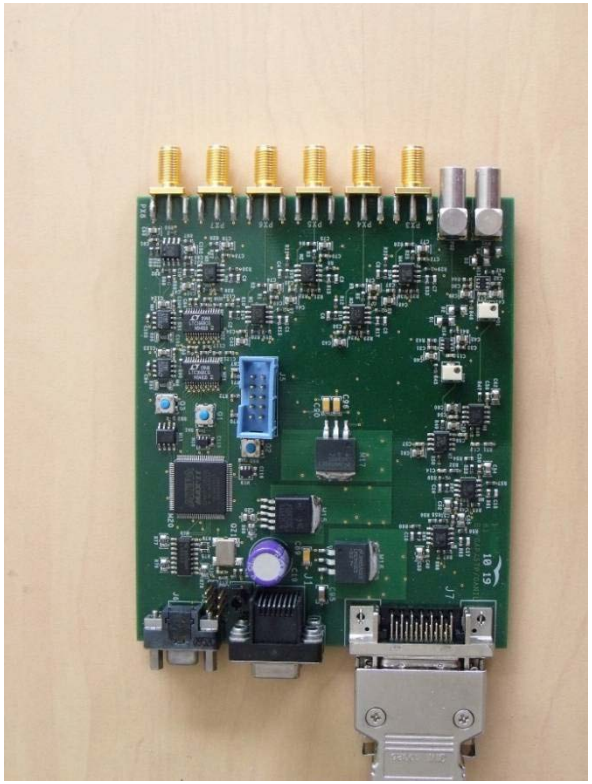
1 link
per NIM board
(6 MB/s per crystal)

Ethernet Switch

DAQ

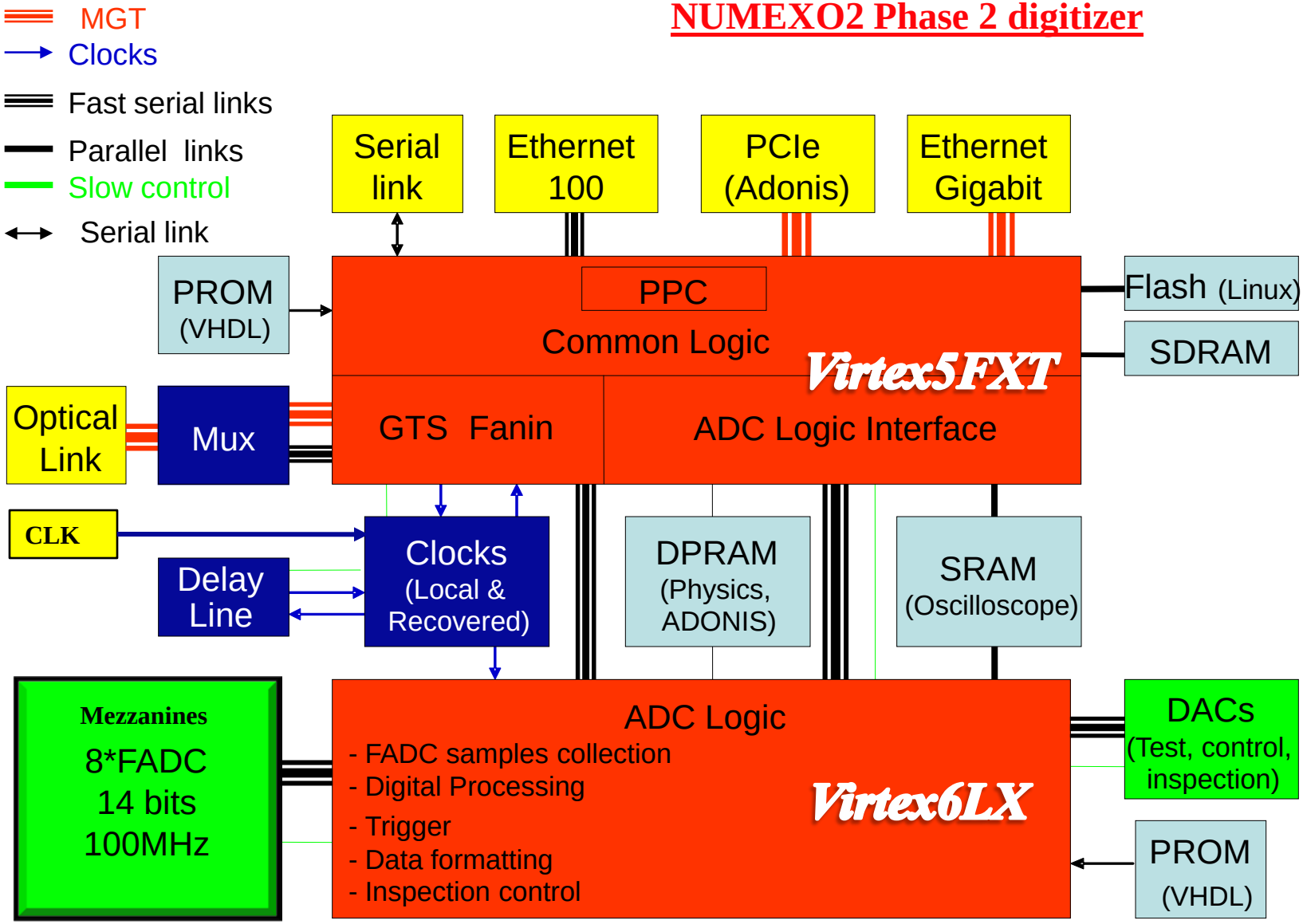
Connection box B3



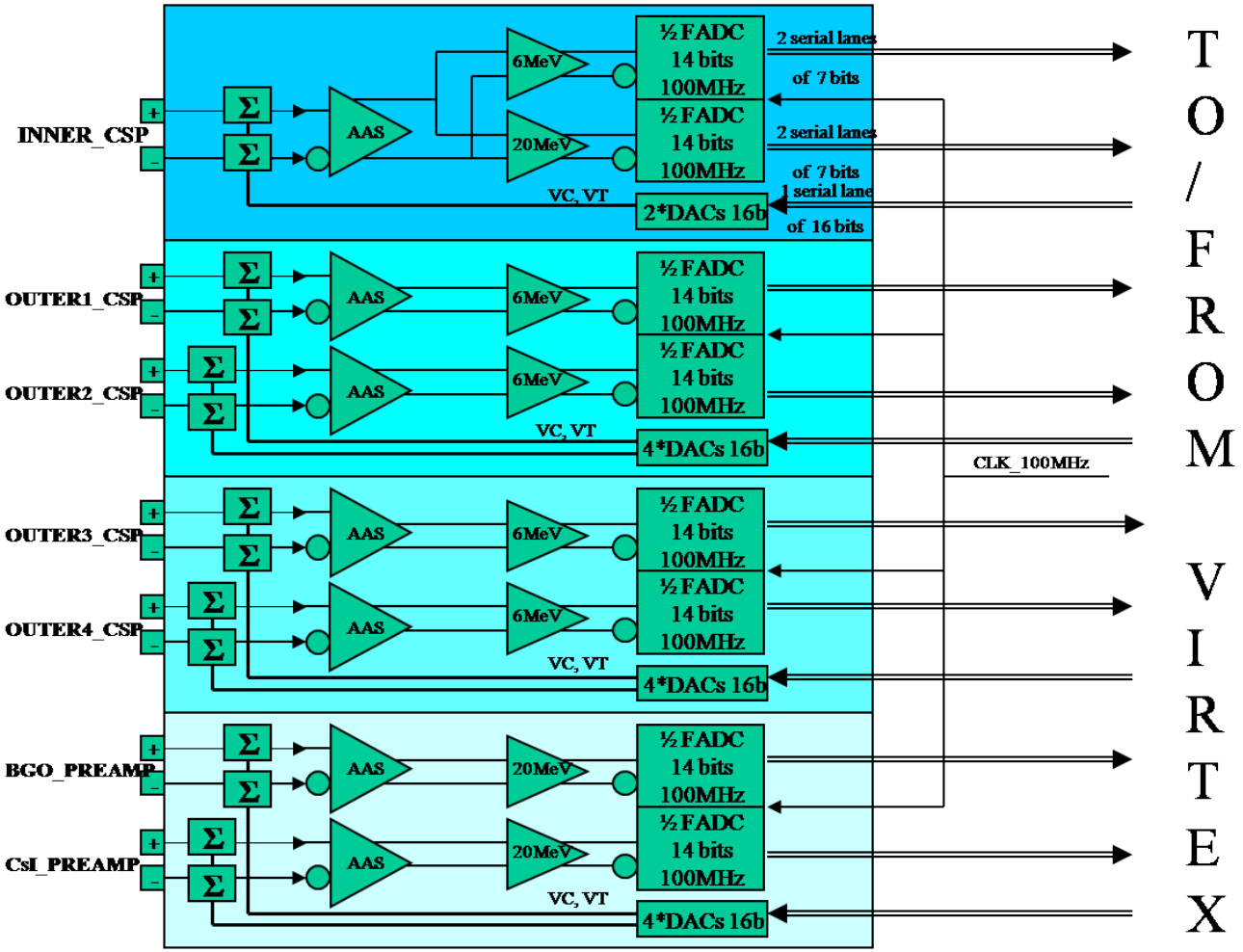


EXOGAM2

NUMEXO2 Phase 2 digitizer

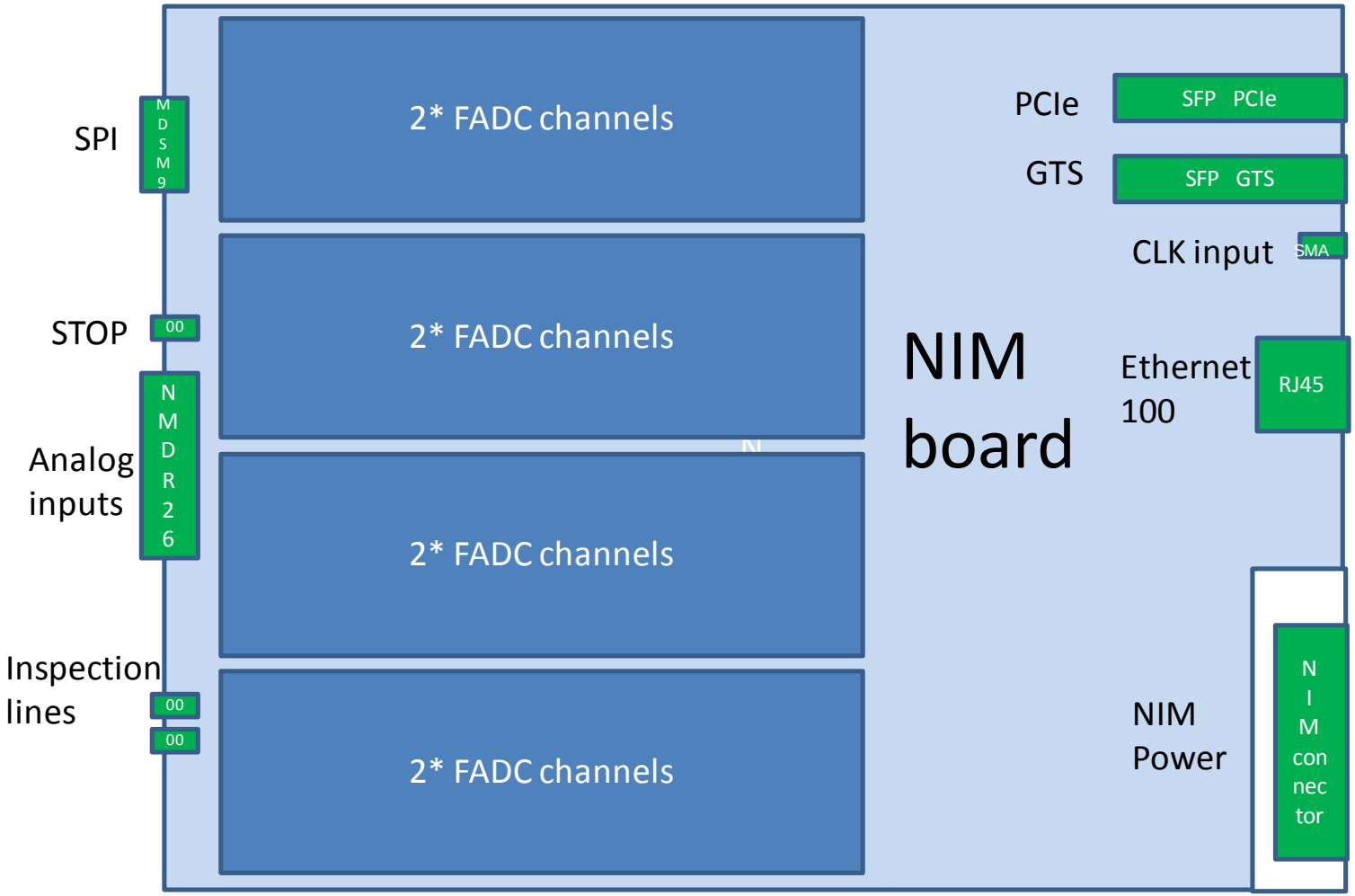


NUMEXO2 FADC mezzanine block diagram



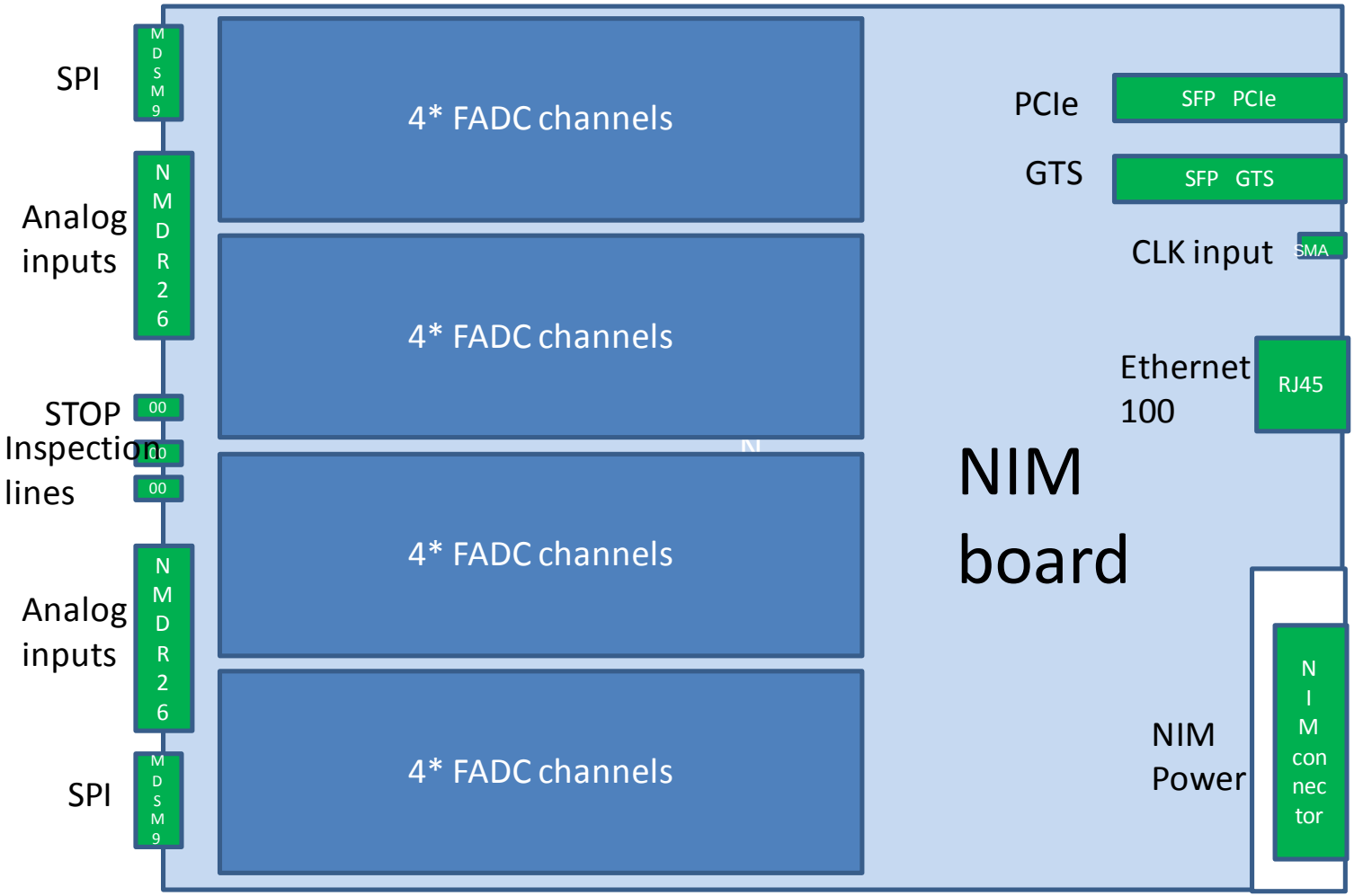
8 channels

NUMEXO2 phase 2: NIM module layout



16 channels

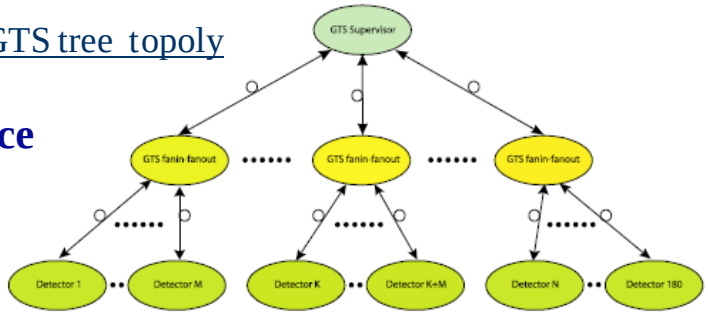
NUMEXO2 phase 2: 16 channels NIM module layout



GTS implementation

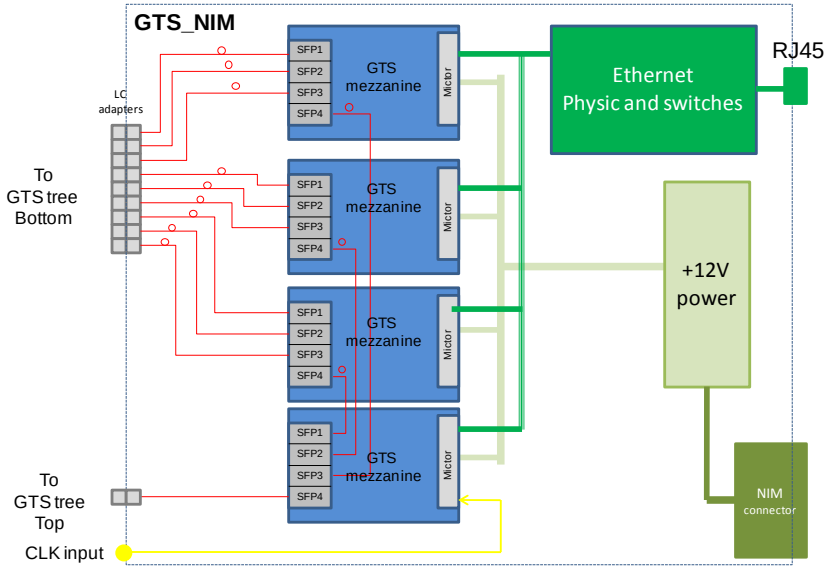
3 main functions
- 200 MHz clock source
-Time stamping
- Trigger

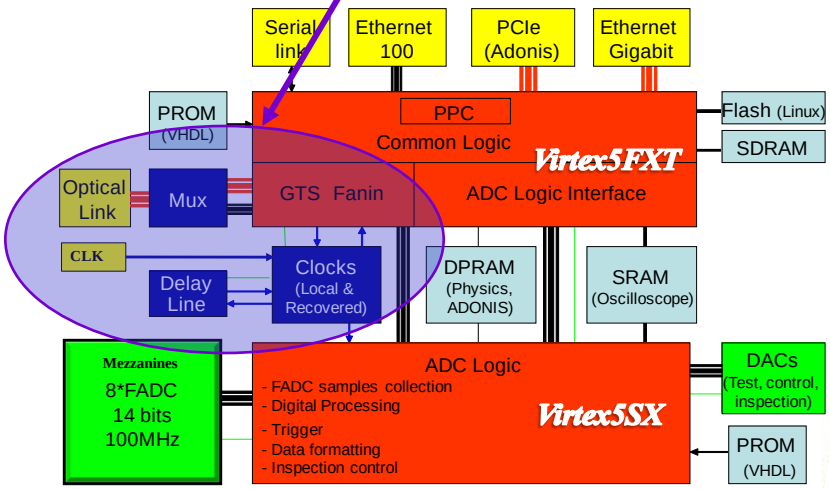
GTS tree topoly



GTS V3 mezzanine

EXOGAM2 GTS tree : 4 GTS mezzanines in one NIM module





EXOGAM2

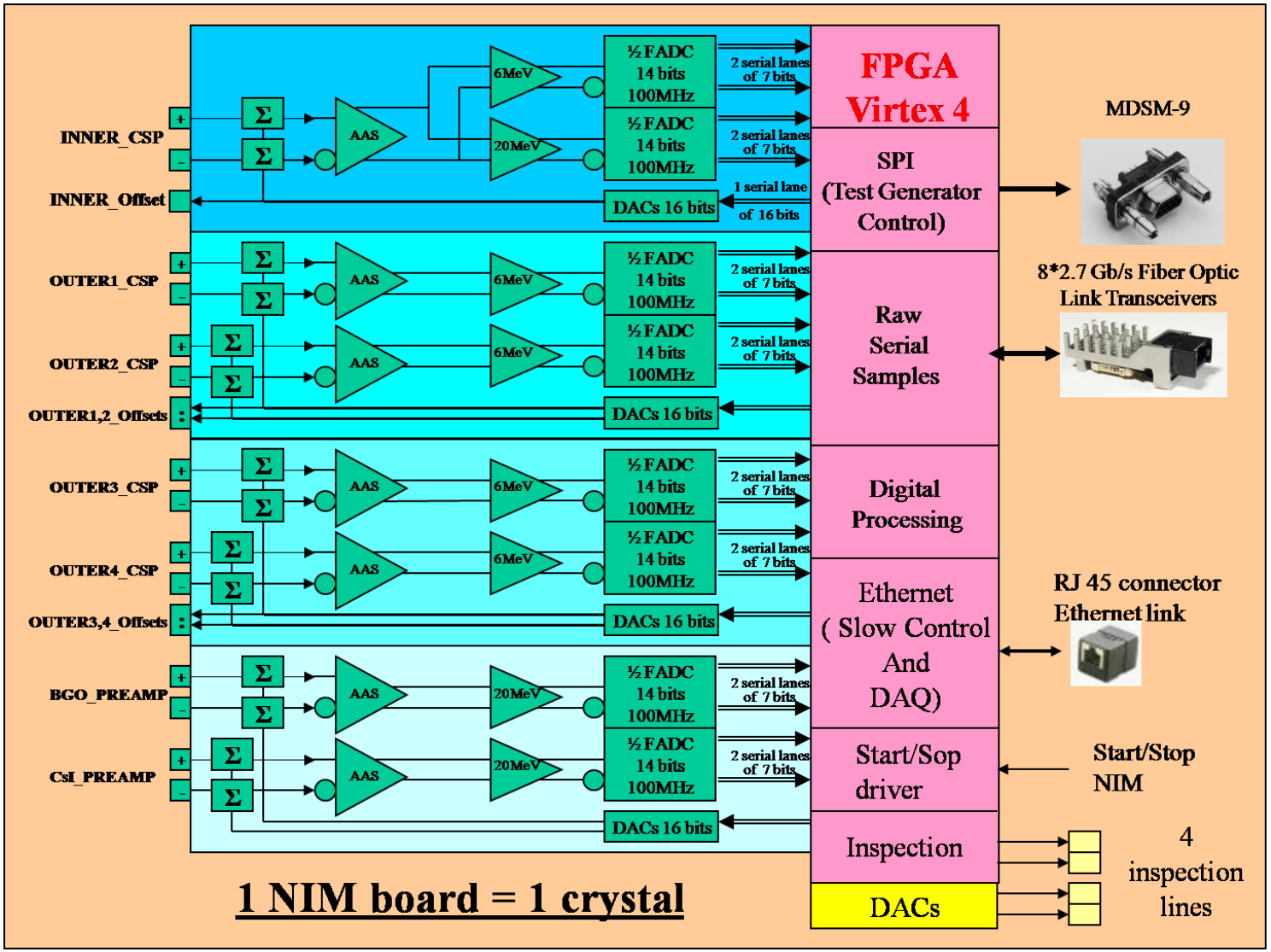
Schedule

	2009		2010				2011				2012				2013			
	Q 3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Prototype (phase 1):																		
- Studies																		
- Manufacturing																		
- Tests																		
Prototype (phase 2):																		
- Studies																		
- Manufacturing																		
- Tests																		
Mass production:																		
- Test bench																		
- Manufacturing																		
- Tests																		

Prototype phase 1 : digitizer (NIM) + connection box
Prototype phase 2 : digitizer + GTS + ADONIS + connection box
Studies : hardware design, VHDL and C files.

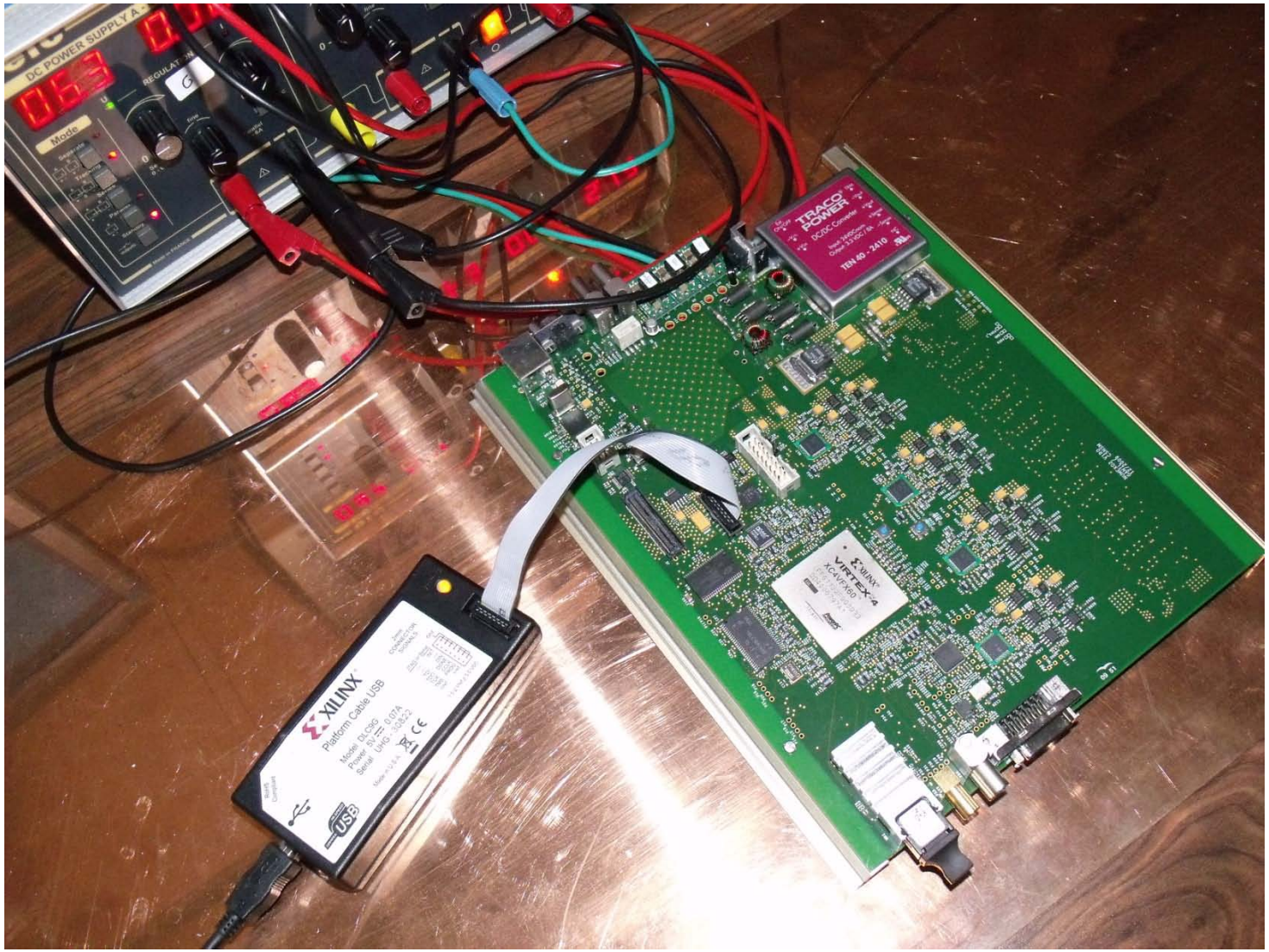
NUMEXO2, the NIM digitizer prototype (phase1)

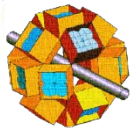
Block diagram



NUMEXO2, the NIM digitizer prototype (phase1)

Picture of the NIM prototype



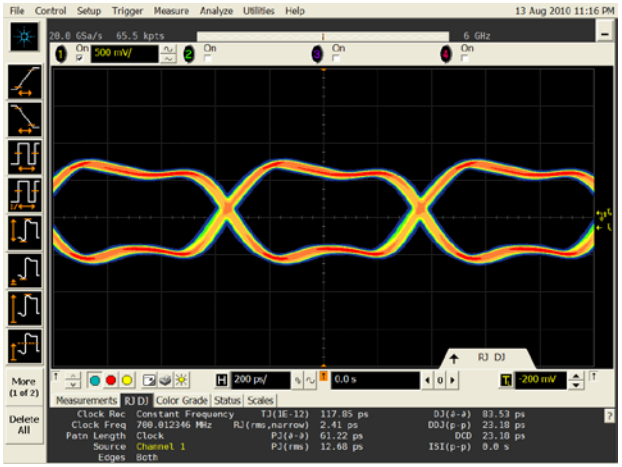


Current status (digitizer phase 1)

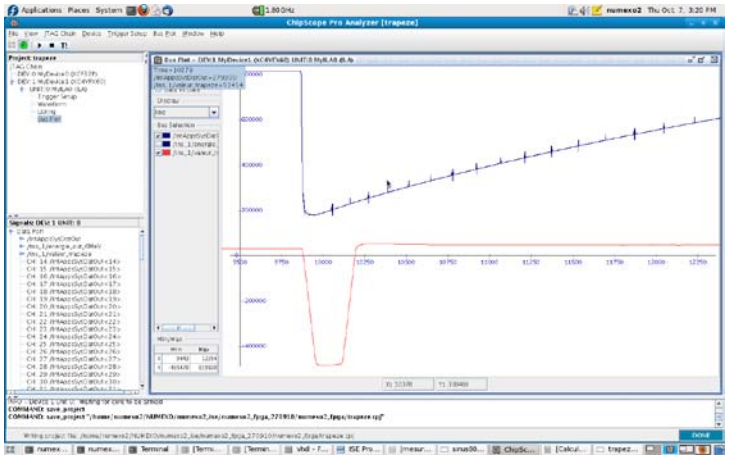
-Firmware
- Deserializer: 8 * (2 serial channels @ 700MB/s)
- Moving Window Deconvolution
- Discrimination
- FIFO interface

-Embedded software
- Linux 2.6.60
- TCP/IP protocol (Ethernet) @ 400Mb/s
- SPI driver and register server

-Software
- Characterization tools: traces, FFT, histograms, INL, DNL
- Generic user interface for slow control
- DAQ readout



FADC serial output channel eye diagram

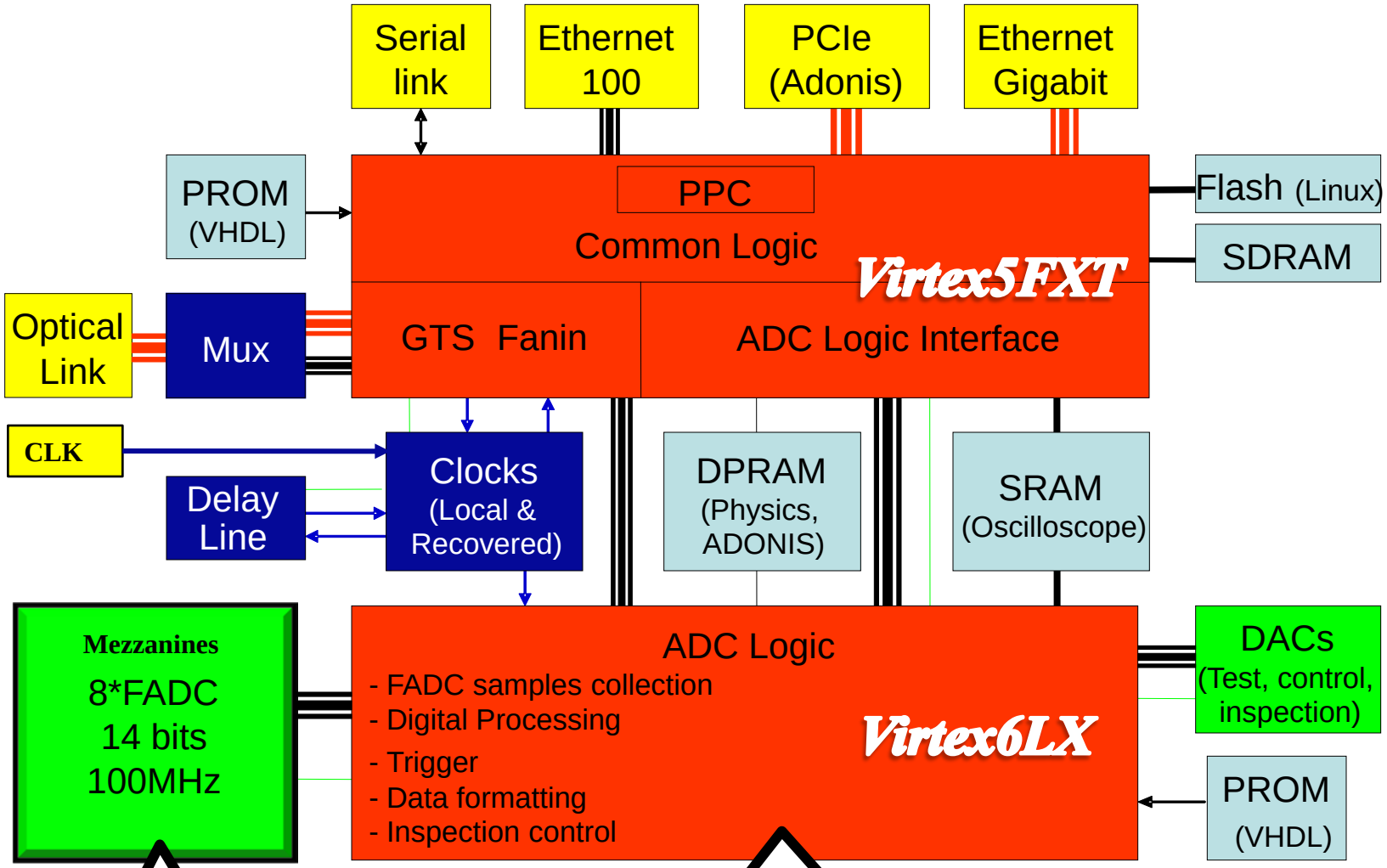


Moving Window Deconvolution processing

To do (digitizer phase 1):

- Validation of interrupt process for FIFO readout
- Characterization of the digitizer with a generator
- Characterization of the digitizer with a clover and a source

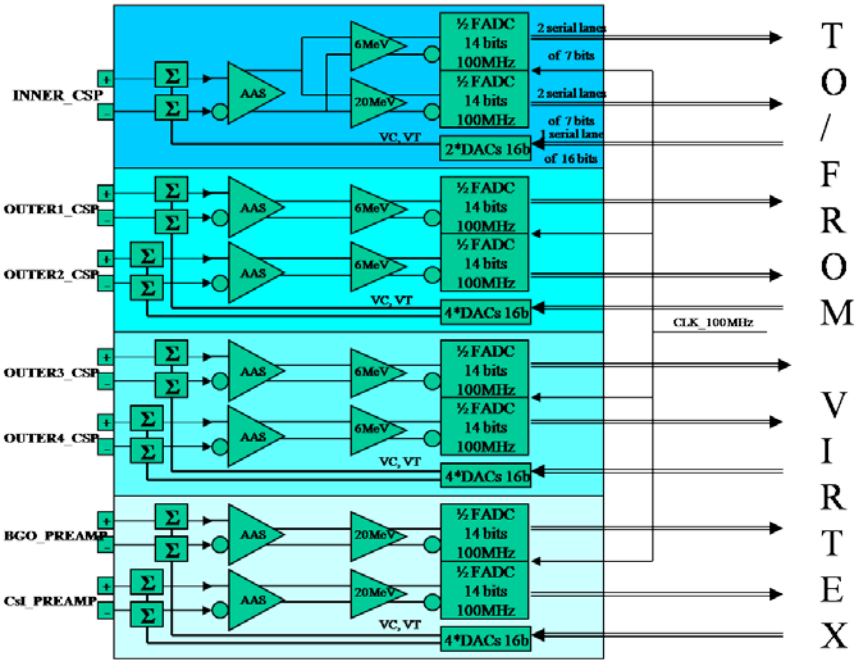
EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?



EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do ?

NUMEXO2 : 2*4 channnels FADC mezzanines block diagram

FADC: ADS6244, 14 bits, 100MHz, 2 binary samples serial lines @700Mb/s



Differential inputs

- **Binary samples serial lines**
- **Clock line**

⇒ **NEDA:**

FADC mezzanines must be redesigned according to frequency bandwidth of inputs

- **Sample frequency of FADC?**
- **Clock jitter?**
- **Number of binary samples serial lines?**
- **Power?**
- **MDR26 connector?**
- **SAMTEC connector?**

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

3M™ Mini D Ribbon (MDR) Cable Assembly

.050" High Speed Digital Data Transmission System - 26 to 26 Pos. 14526-EZ8B-XXX-07C

- Solution for Digital Displays, Datacom and Telecom applications
- Supports LVDS FPD Link™, FlatLink™, ChannelLink™, PanelLink™/TMDS™ electrical interfaces
- Each differential twin-ax pair has a foil shield and drain
- Entire cable bundle is shielded with foil and braid for additional signal protection
- Rugged MDR ribbon type contact
- Quick release latches
- RoHS* compliant

TS-0757-17
Sheet 1 of 4

Electrical

Voltage Rating:	30 V
Current Rating:	1 A
Insulation Resistance:	$> 1 \times 10^{8} \Omega$ at @100 Vdc
Withstanding Voltage:	350 Vrms for 1 minute
Individually Shielded Twisted Pairs	
Characteristic Impedance:	$100 \pm 10^{\Omega}$
Conductor Size:	28 AWG Stranded
Propogation Velocity:	1.25 ns/ft [4.1 ns/m]

NEDA:
MDR26 Cable and connector must be tested

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

Carrier-mezzanines connector: QFS-026-06-75-X-D-PC4

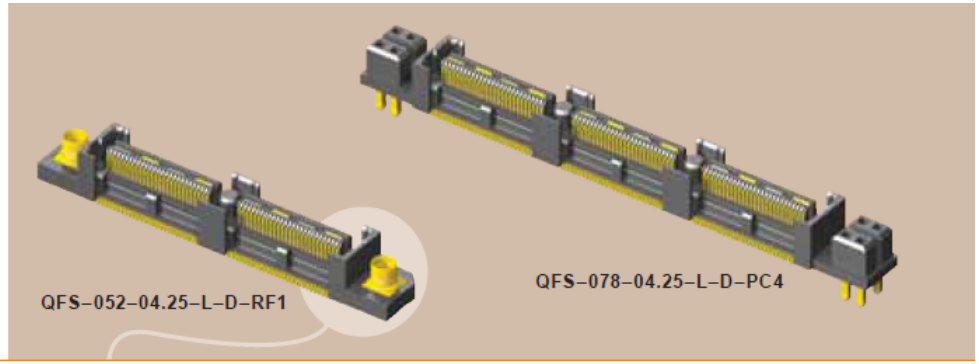
F-210-1

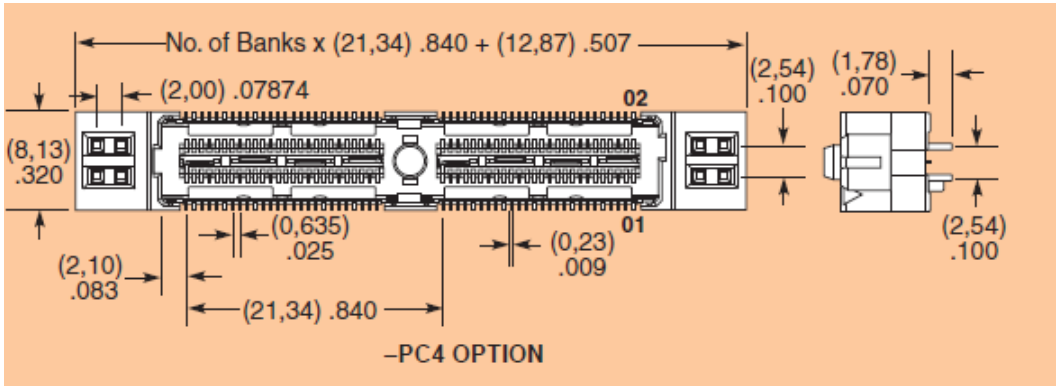
samtec

Q2™

(0,635mm) .025"

QFS-PC, QFS-RF SERIES





10mm Stack Height	Rated @ -3dB Insertion Loss
Single-Ended Signaling	9 GHz / 18 Gbps
Differential Pair Signaling	7.5 GHz / 15 Gbps

NEDA: Does pins diagram fit?

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

FADC highlights

TI FADC	ADS6244	ADS62P49	ADS5463
Résolution (bits)	14	14	12
Sample rate (MSPS)	105	250	500
Input channels	2	2	1
Interface	LVDS serial // (2 LVDS lines)	LVDS serial // (7 LVDS lines)	LVDS // (12 LVDS lines)
Analog BW (MHz)	500	700	2300
SNR (dB)	73	73	65
ENOB (bits)	11.7	11.3	10.4
Power (W)	0.9	1.2	2.3

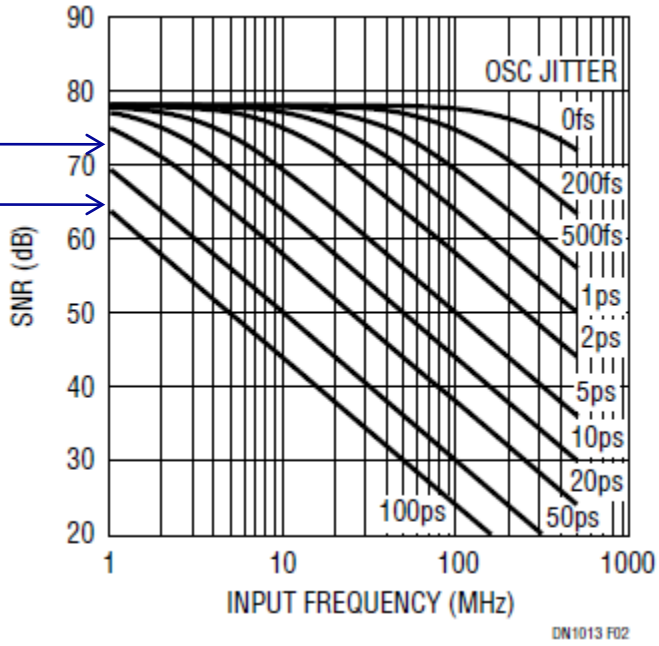
EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

Clock jitter specifications:

- FADC clock

14 bits

12 bits

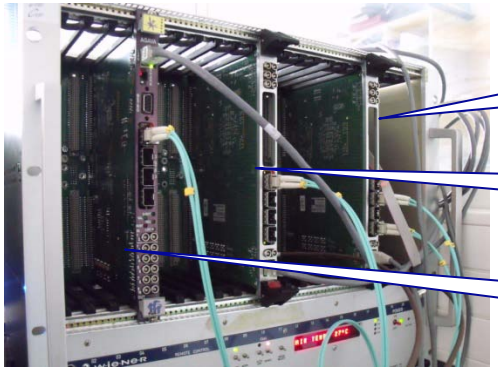


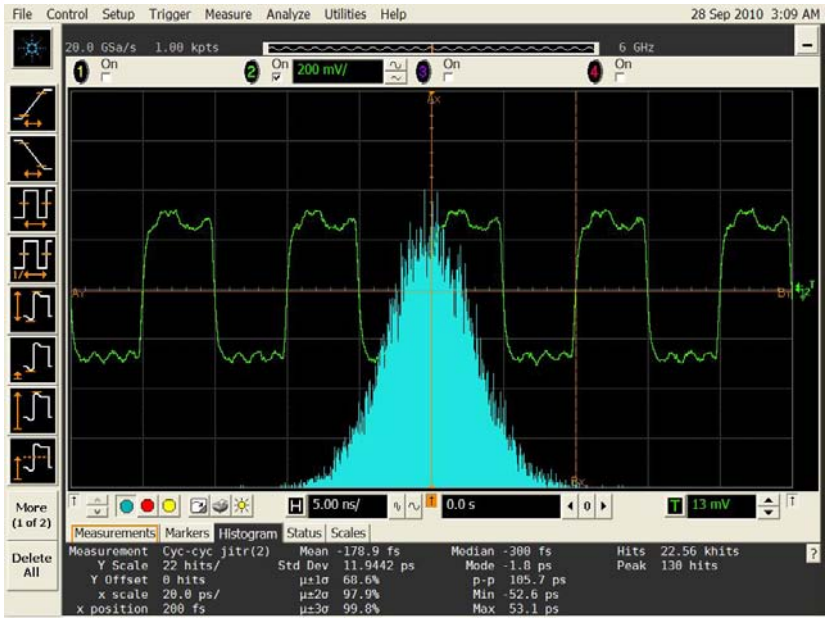
Jitter clock degradation of SNR

- High resolution timing

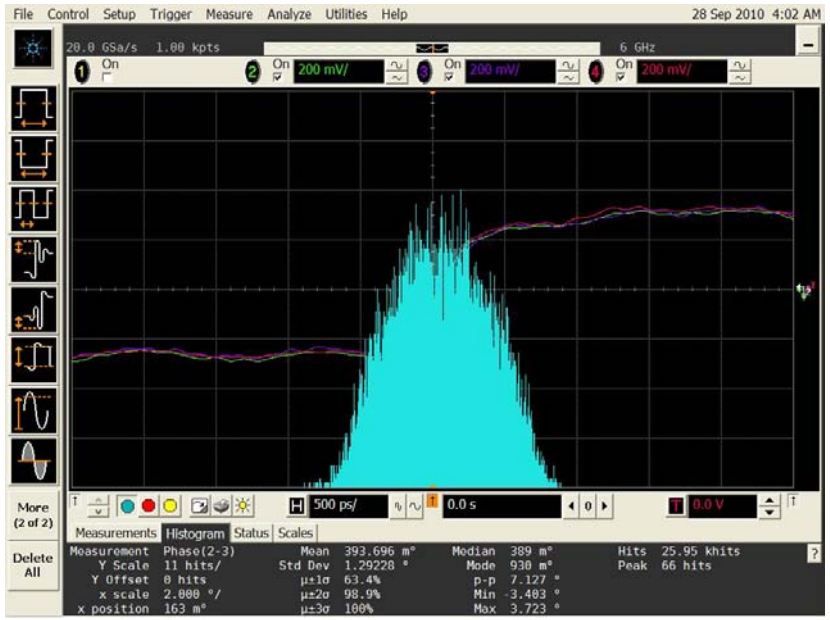
EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

100MHz recovered GTS clock jitter :





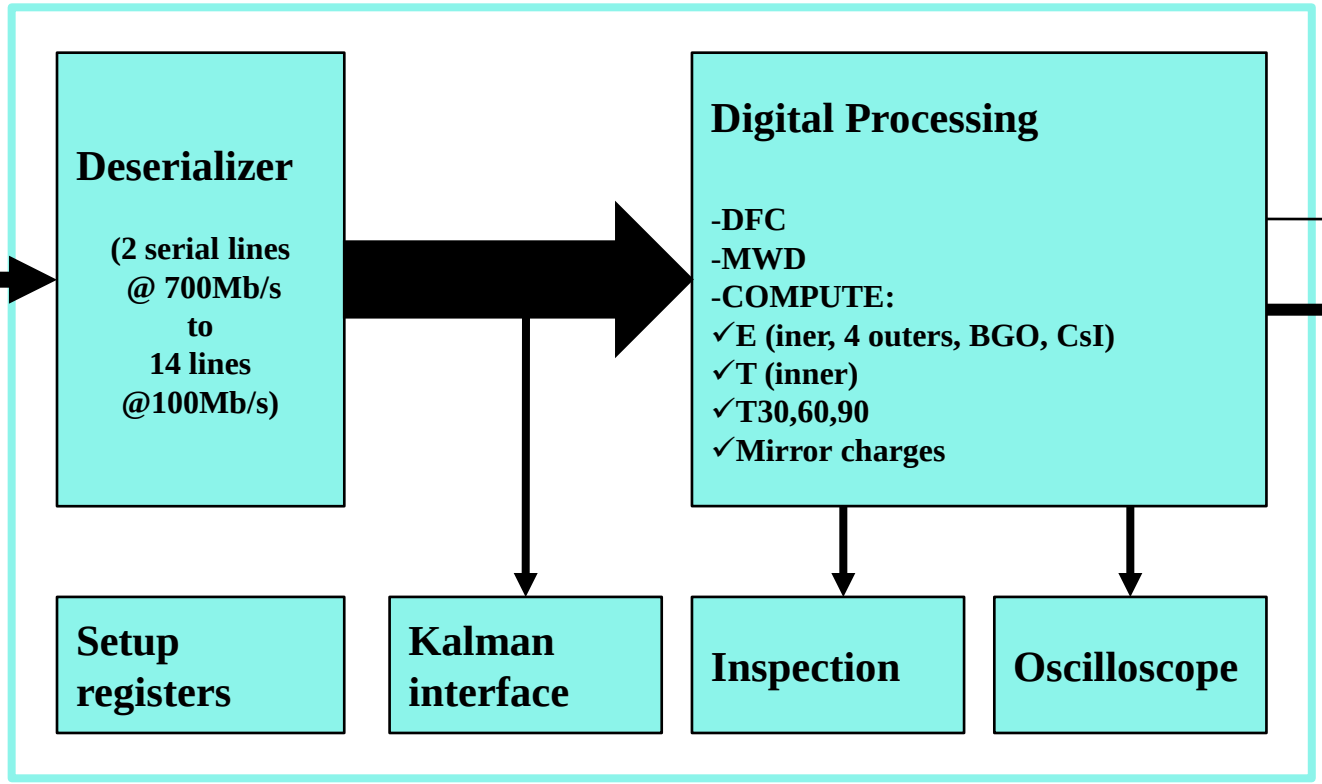
Std Dev (cycle to cycle)= 12ps



Std Dev (leaf to leaf) = 36 ps

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

Block diagram of EXOGAM2 signals processing



⇒**NEDA:**

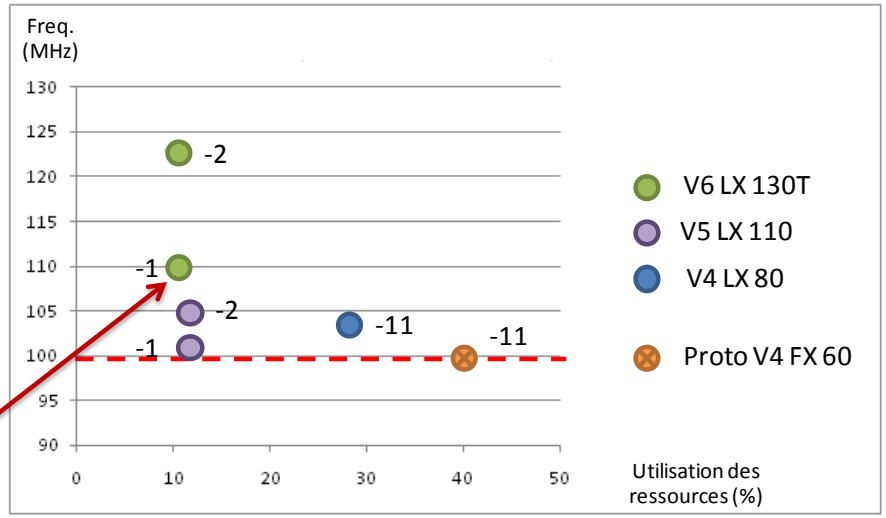
- **Deserializer and Digital Processing IPs must be written**
- **Kalman interface suppressed**
- **Number of Trigger Request signals > 2**
- **Setup registers, Inspection and Oscilloscope IPs must be modified**

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

FPGA target choice: Virtex 6 LX130T -1

PROJET EXOGAM2/NUMEXO2/FPGA TNS VIRTEX6

Quel composant VIRTEX4, 5, 6…



8 voies MWD

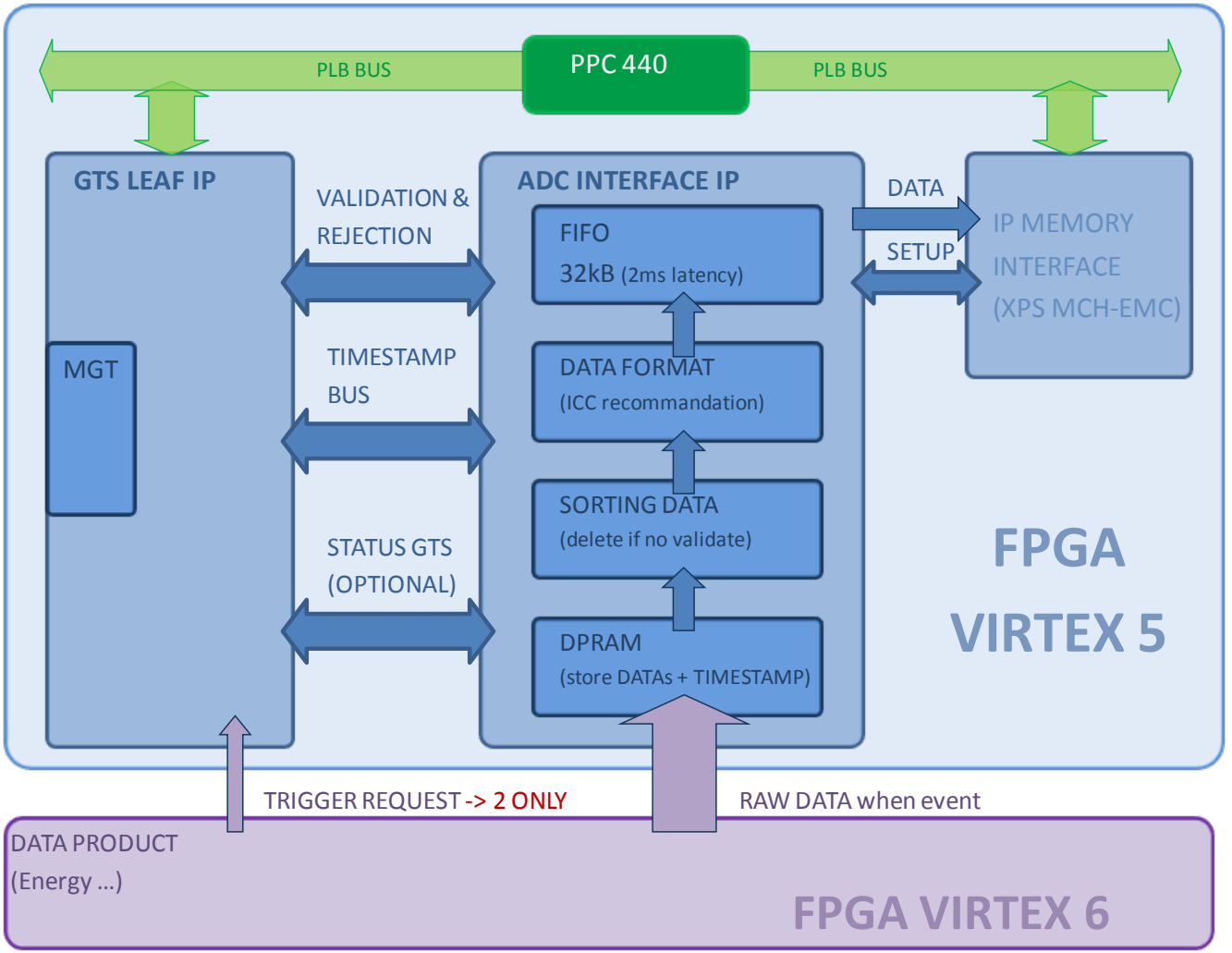
Cible choisie : Virtex 6 LX130T -1 *1094 $ - distributeur Avnet*

Marge de fréquence de 10% -> 40% désormais avec une optimisation plus poussée
Faible taux de remplissage

Is the Virtex 6 LX130T -1 powerfull enough for NEDA signals processing?

EXOGAM2 digitizer for NEDA instrumentation: What to notice and to do?

Block diagram of EXOGAM2 GTS and ADC interfaces



⇒**NEDA:**

- DPRAM and FIFO depths?

- Data format?