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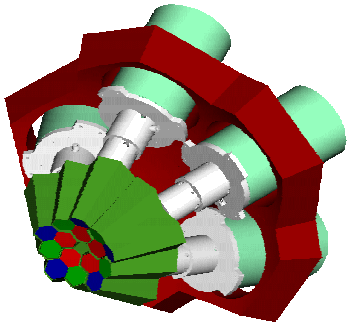
University of Milano
Department of Physics



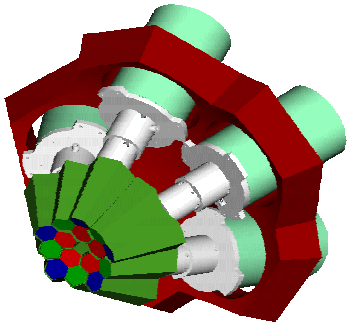
Digital Preamplifiers: Where we are ?

Alberto Pullia

10th AGATA Week
Nov. 22- 26, Lyon, France

Speaker: **Alberto Pullia**
Nov. 23, 2010

Philosophy



The general philosophy is "the Simpler the Better"

Separate and integrate as much as possible the FE and Far-End electronics

Move ADC + optical transmitters as close as possible to the preamps

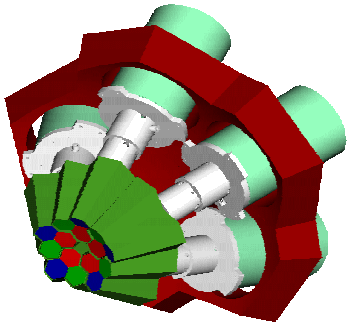
(this presentation)

Put optical receivers and pre-processing electronics into PC

(D. Bortolato's presentation)

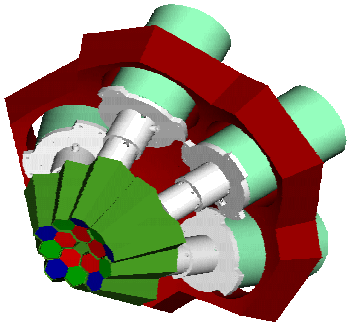
Direct optical link from detector to PC's

Issues



- System structure as simple as possible
  cost effective, compact, low power
- Precondition the preamp signal to match the ADC specs
  differential signal with proper common-mode level
- Use of state-of-the art ADC's and Transceivers
  performance @ low-power consumption
- Move ADCs/optical-transmitters close or on preamps
  low noise, no termination-resistor needed
- Minimize digital transmission errors
  8b/10b encoding

Power consumption



Estimation of power consumption for a 12-ch ADC module

ADC+8b/10b ser encoding: ~1200 mW × 6 = 7.2 W (3V, 1900mA - 1.8V, 800mA)
(NXP ADC1413D105)

Optical Transmitter: ~1.2 W (3.3V, 364mA)

Overall (nominal): ~8.4 W

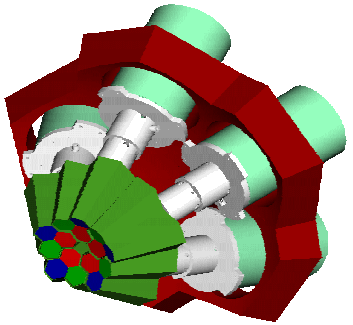
Assuming 20% more power for other functionalities (PS voltage regulators, clock distribution etc)
Overall (realistic): ~10 W (for n. 12 ADC chs w 8b/10b encoder, ser & optical transmitter)

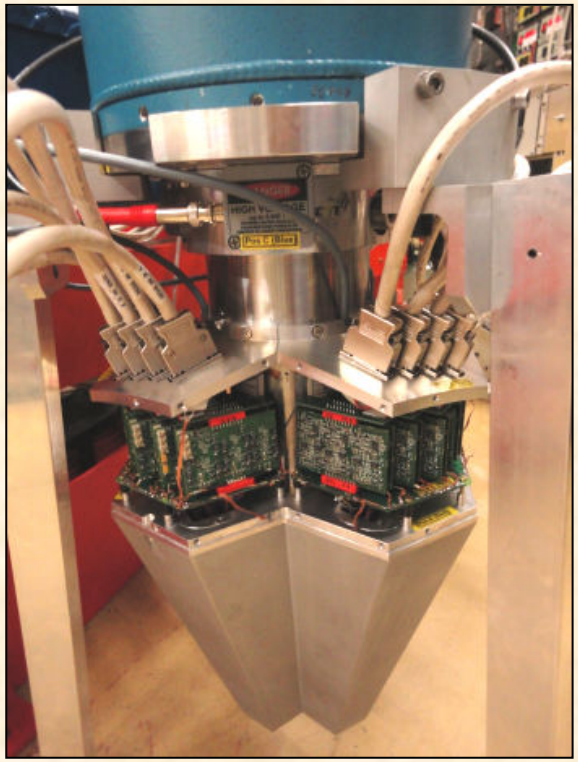
Power per digital channel: ~0.8 W/ch

(the most power-eager block is 8b/10b encoding + serialization, which sinks as much as 450mW/ch)
to be compared with 0.28 W/ch of the analog part (single segment preamplifier channel)

A digitizer + 8b/10b encoder + serializer + optical transmitter consumes three times as much as a preamplifier channel. Too much to be fitted into cryostat !

ADC optimal location

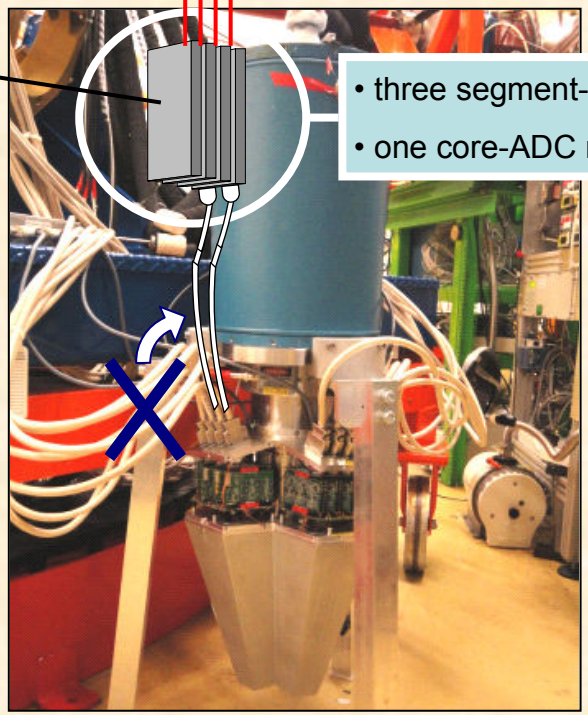




Four modules
L = 10 cm
H = 10 cm
W = 1.5cm

35 W power consumption overall (crystal)

Optical fibers

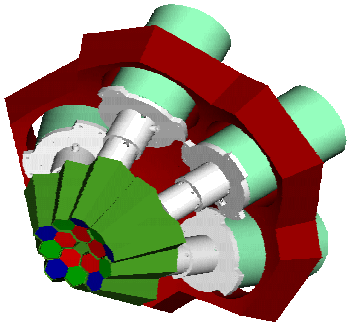


- three segment-ADC modules
- one core-ADC module

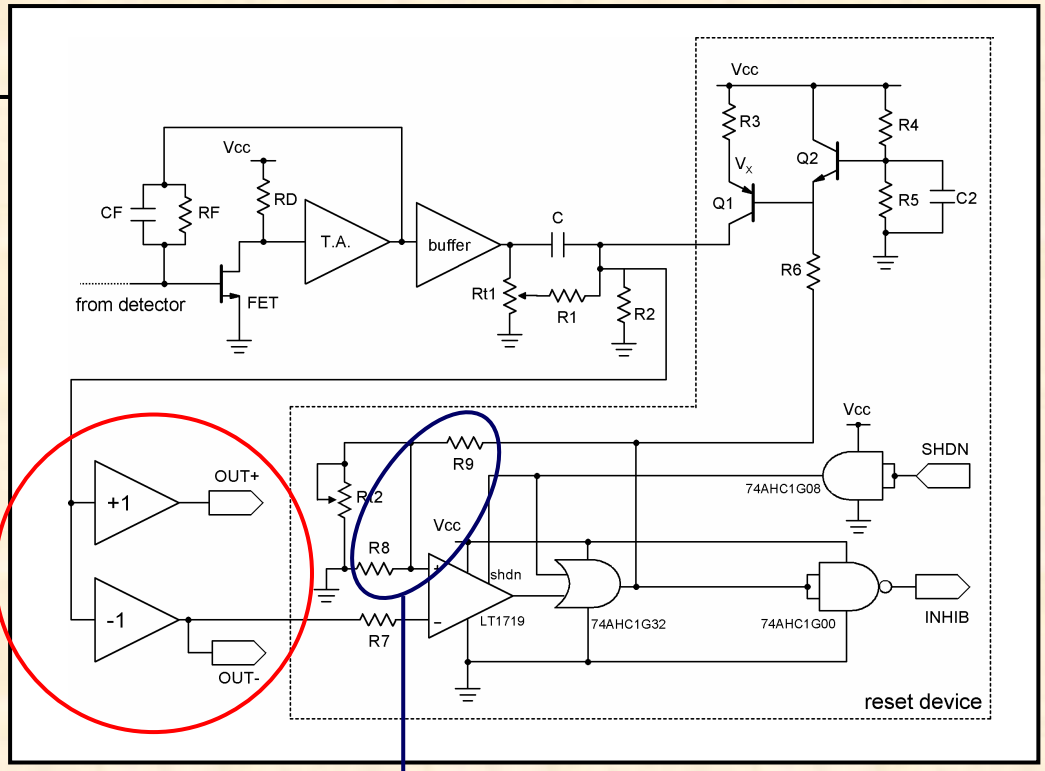
This scenario is much less “invasive” than putting the ADC’s on the preamps !

⇨ We will work in this direction first. The ADC (alone) could further move towards the preamplifier in a second R&D phase

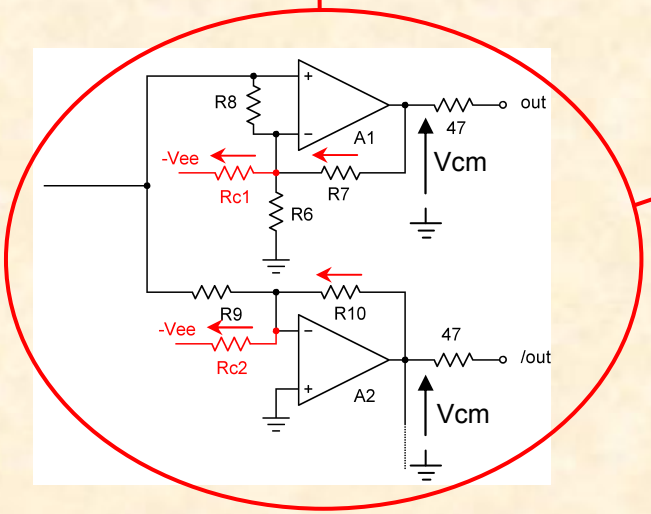
Changes in preamps



Simplified schematic diagram of AGATA preamplifiers



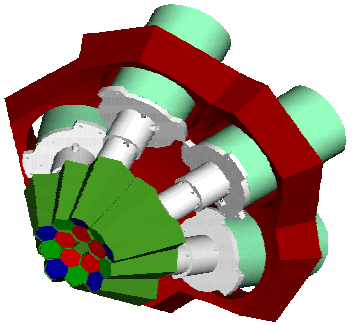
(1) Add Rc1, Rc2 → Common-mode voltage

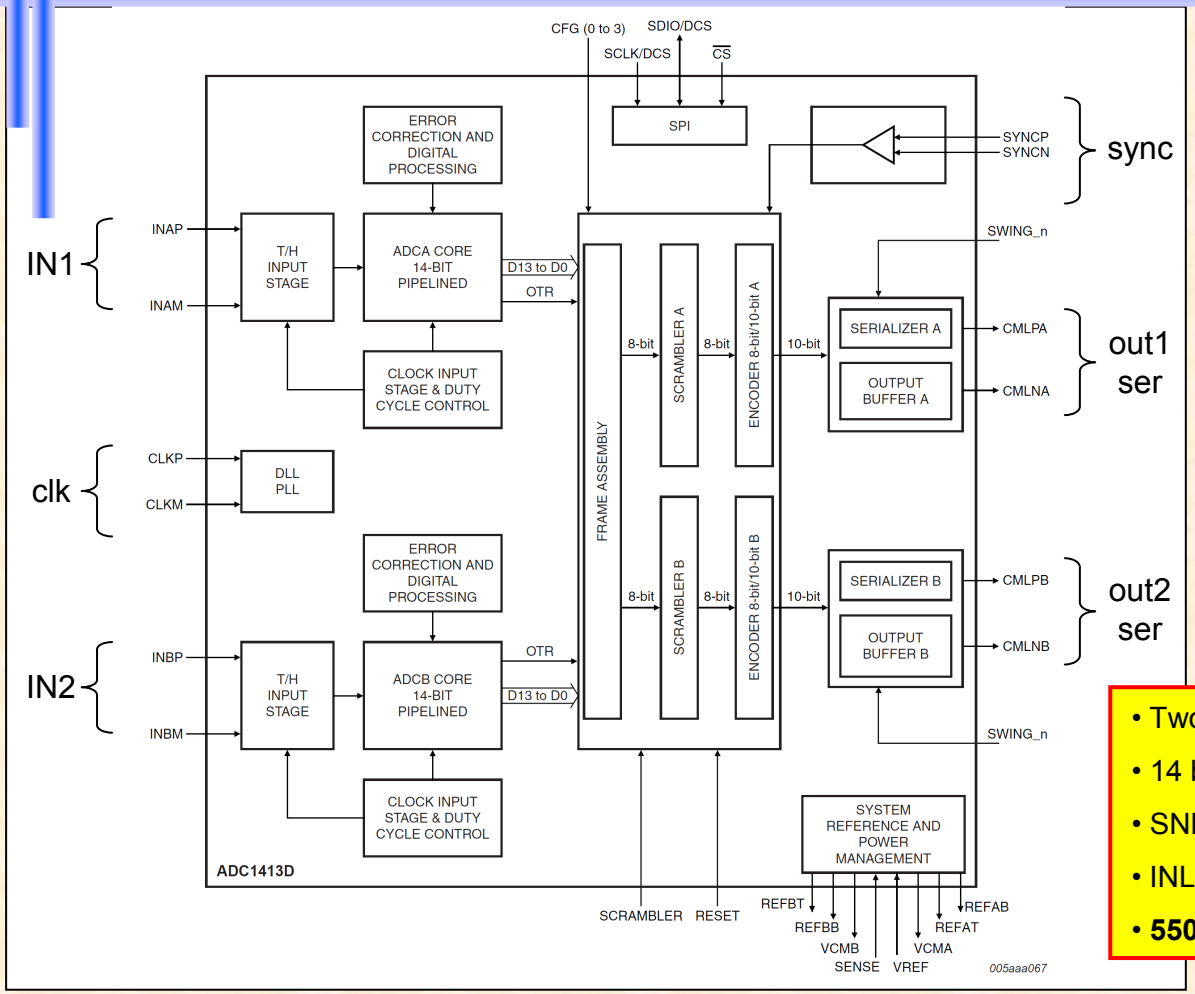


(2) Adjust ToT comparator thresholds

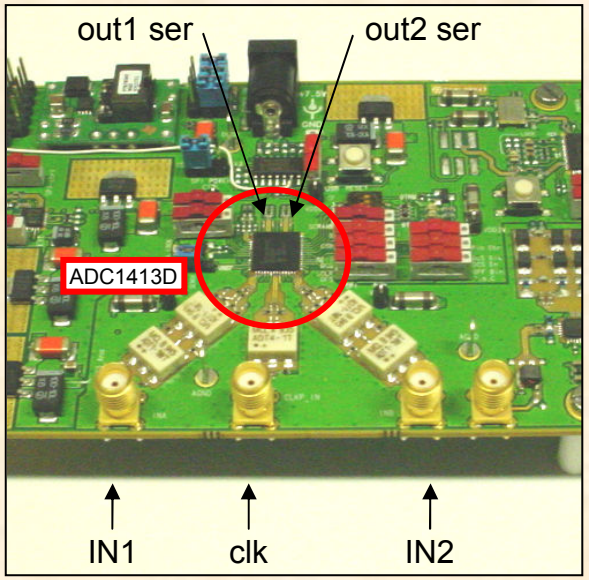
The ADC

NXP ADC1413D105





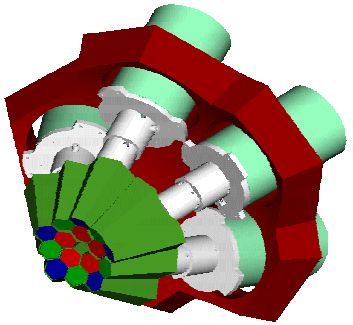
Demoboard PCB2115_V1

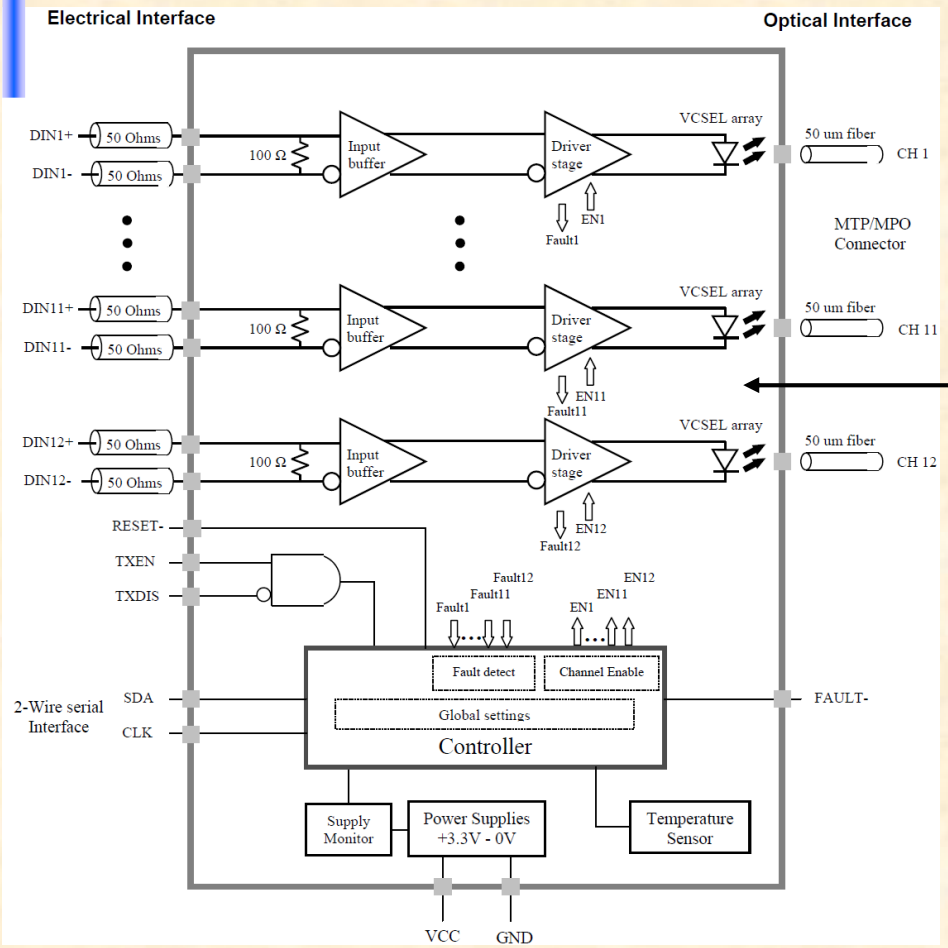


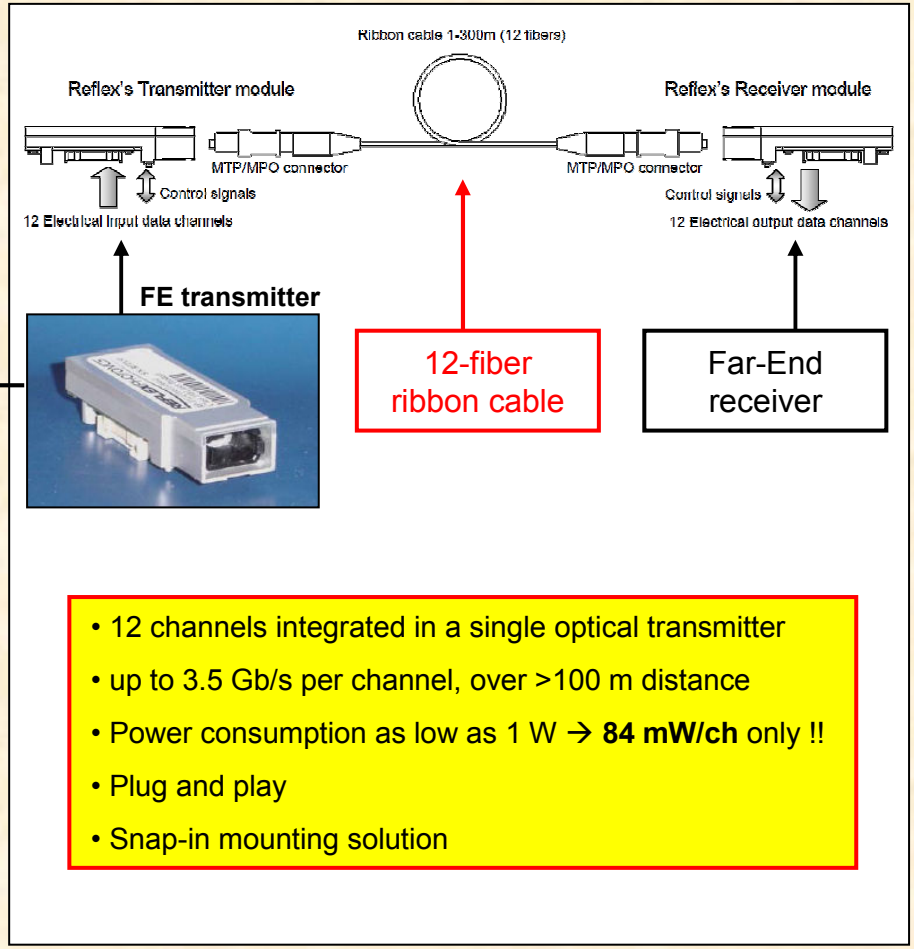
- Two channel with 8b/10b serializers @ up to 2.1Gb/s
- 14 bit, 100 Msps, 2V p-p input range (differential)
- SNR = 71.5 dB, ENOB=11.5 bit
- INL=±1LSB, DNL=±0.5LSB, no missing codes
- **550 mW/ch** with 8b/10b encoding and serializer

The optical transmitter

SN-T12_C00501 SNAP 12

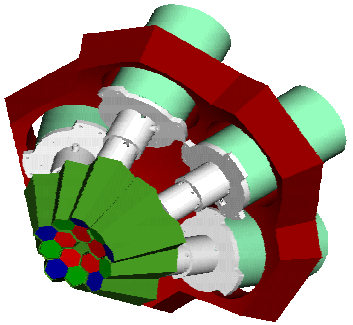






- 12 channels integrated in a single optical transmitter
- up to 3.5 Gb/s per channel, over >100 m distance
- Power consumption as low as 1 W → **84 mW/ch** only !!
- Plug and play
- Snap-in mounting solution

Schedule and cost



- Man Power: 1 FTE
- Time needed: 12 months after qualification of ADC
- Estimated cost of digitizer: ~Eur 200,00 / ch
- Qualification of NXP ADC1413D coming soon, with factory demoboard as linked to AGATA pre-processing electronics
- Prototype development to start immediately after qualification