# * AGAVA INTERFACE

Status Nov. 2010

## General Description.

AGAVA Interface is a 1-unit wide A32D32 type VME/VXI slave module. It is as well the carrier board for the GTS mezzanine card used in the AGATA for the global time stamp distribution. The main task of the Agava is to merge the triggerless time stamp based system with the acquisition system using trigger, based on the VME or VXI Exogam-like environment. It has also connections to the VME Metronome and Shark link systems. The logic and tasks are controlled by the FPGA Virtex II Pro. In Fig. 1 it is shown the block diagram of the Agava Interface. The AGAVA PCB includes all necessary connections for the trigger cycle and for the TDR (Total data readout) system (connectors on the Front Panel and connections to the Xilinx FPGA). AGAVA contains as well the Ethernet passive connection, providing directly Ethernet to the GTS mezzanine card.

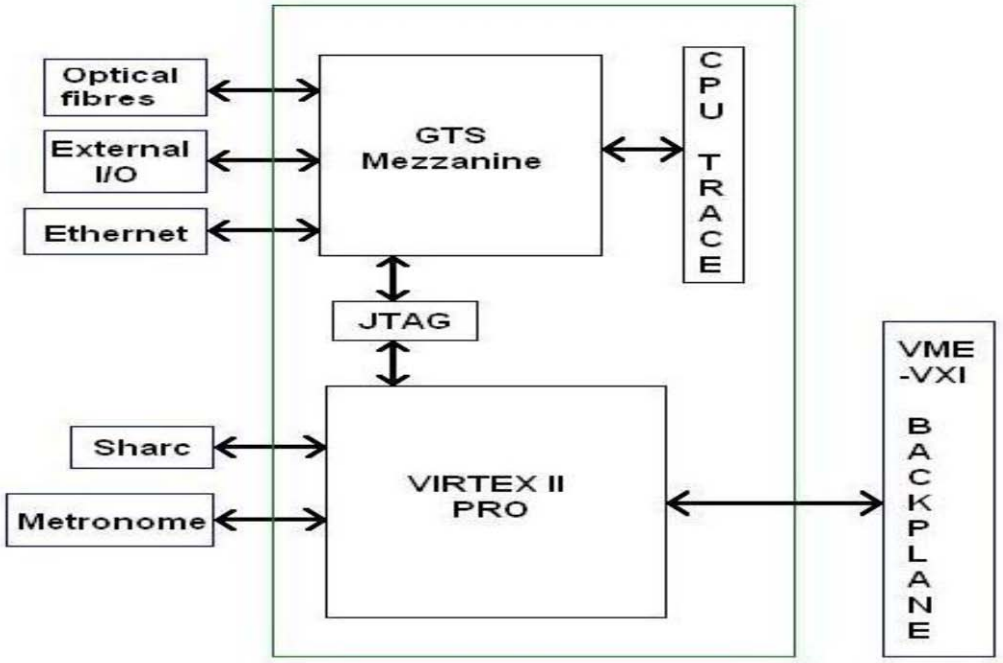



Fig.1 Block Diagram of AGAVA Module.

## Front Panel of AGAVA contains:

**Inputs:**

Back preasure (NIM standard) **(IN 1)**
Trigger request (NIM standard) (“external”) **(IN 2)**

**Outputs**

| | |
|---|---|
| Busy (NIM standard) | **(OUT 1)** |
| Local Trigger (NIM standard) | **(OUT 2)** |
| Rejection Trigger (NIM standard) | **(OUT 3)** |
| Validation Trigger (NIM standard) | **(OUT 4)** |
| Timeout (NIM standard) | **(OUT 5)** |
| Inspection_1 (NIM standard) | **(OUT 7)** |
| Inspection_2 (NIM standard) | **(OUT 8)** |
| Inspection_3 (NIM standard) | **(OUT 9)** |
| Inspection_4 (NIM standard) | **(OUT 10)** |

**LED Indicators:**

Data Ready
Validation
Rejection
Busy
Local Trigger

## VME Interface in the AGAVA.

In the AGAVA module few types of the VME/VXI access modes have been implemented. AGAVA can provide the VME single access read or write operations according to the standard VME handshake rules. It can also provide the block transfer readout in the CBLT (Chain Block Transfer) on the VME bus. On the startup special registers for CBLT mode have to be set in the AGAVA card. The CBLT readout uses one common address for all participating modules in the chain. They deliver their data in blocks of variable lengths starting from the module defined as the first in the chain, following by one or more intermediate and finished by the last one. The CBLT mode is used for faster readout and is helpful for event building. CBLT readout has been successfully tested at Legnaro. In the AGAVA interface there is also VXI Exogam-like readout implemented. It has been successfully tested at Ganil in the VXI environment.

## GTS Interface.

The AGAVA module receives the trigger requests from the ancillary detector (named here “external” trigger) and the trigger request is pass to the GTS system. An “internal” trigger request can provide for testing purposes. After the trigger request is pass to the GTS system AGAVA waits for the Local Trigger and Tag and Validation/Rejection Signal and Tag coming from the GTS System. The AGAVA module stores the data in registers or RAM (depending on the Slow or Fast mode) and sets the Data Ready Flag to inform the VME/VXI system that the data can be transferred to the event builder part.

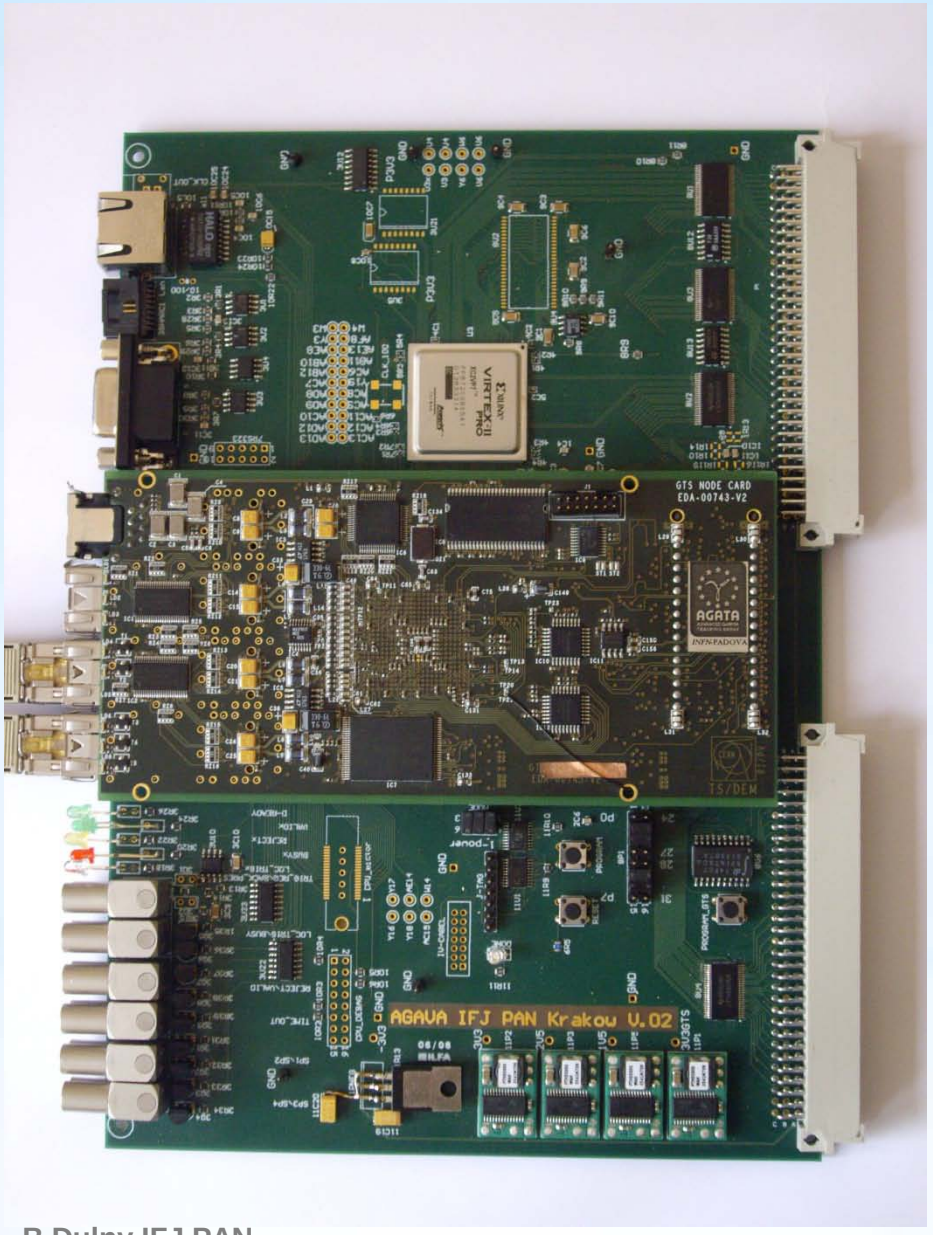
The Busy Flag is set after accepting a new Trigger Request. Release of the Busy (Dead time for new triggers) depends strongly on the VME/VXI readout mode and speed. The back pressure input is used by the GTS system for controlling trigger rates.

## Slow mode Trigger Cycle.

In the Slow Mode the Trigger Request from the ancillary detector arrives on the corresponding Front Panel Input. If there is no Busy status from the previous cycle, this signal is formed to a single 10 ns wide pulse and sent to the GTS mezzanine card. Then the Local Trigger and Local Trigger Tag are received from the GTS mezzanine card and AGAVA will wait for the GTS Supervisor response: either Validation Trigger with Validation Trigger Tag and Event Number or Rejection Trigger with Rejection Trigger Tag. After receiving them the Data Ready Flag is set in AGAVA module and the data can be read out by the VME system. Till this is done the Trigger Request input is disabled with the Busy Flag (can be observed on the Front Panel output and LED).
This mode was used in all tests in Cracow, Legnaro and Ganil.

## Parallel-like mode of Trigger Request.

In this mode, the trigger request from the ancillary detector arrives on the Front Panel Input (as in the Slow Mode), the Busy status is set and held till the Local Trigger and Local Trigger Tag are received from the GTS mezzanine card and stored in AGAVA module in RAM. At the same time AGAVA can receive the Validation or Rejection Trigger and Tag. They are also stored in the RAM with another marker. The data can be read by the VME system. The Busy Flag is set after accepting the new Trigger Request. Release of the Busy (Dead time for the triggers) depends strongly on the VME/VXI readout mode and speed. This mode is prepared for the future purposes and has not been tested in the real conditions.


GTS NODE CARD
EDA-00743-V2
AGATA
INFN-PADOVA
TS/DEM
AGAVA IFJ PAN Krakow V.02

## Status of AGAVA boards from 30th October 2010: (last test and changes done at Legnaro)

Boards with numbers, from GANIL (should be sent back)

01/07
06/07
07/07

loaded firmware ver. 12_a

Boards with numbers:

03/07
04/07

loaded firmware ver. 12_a

Board with number:

05/07

is modified
loaded firmware ver. 11_a

Boards with numbers:

4/09

5/09

7/09

need small modification (mount clock termination resistors)

loaded firmware ver. 11_a

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Board with number:

02/07

loaded firmware ver. 11_a

board has problem with Trigger Request Input, needs investigation

(I take this module to Cracow to repair it)

# * Summary

- IFJ PAN Krakow has produced 10 of AGAVA modules,

- 9 are fully working:
  5 at Legnaro (1 at GSI ?)
  1 at Milano
  3 at GANIL (or will be send soon from Legnaro)

- 1 with dead NIM input will be soon repaired

- More tests could be done at IFJ PAN if one of theGTS ver.3 would be available in Cracow