AGATA WEEK Nov 2010

REPORT ON THE PRE PROCESSING MEZZANINE SEGMENT CARD VHDL1 FIRMWARE INTEGRATION
AUGUST 30/2010 TO SEPTEMBER 10/2010

STATUS OF THE PREPROCESSING ELECTRONICS MANUFACTURING FOR THE GSI PHASE

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SUMMARY

- What's the difference between VHDL0 & VHDL1
- Installation setup
- Week1 and Week2 Planned actions
- Week 1 Real actions
- Week 2 Real actions
- Conclusion
- Orsay Test bench and mezzanine GUI
- Preprocessing electronics for the GSI phase

What is the difference between VHDL0 & VHDL1?

- Its the FPGA firmware for the online preprocessing code inside the mezzanine cards
- The VHDL0 Firmware:
  - uses I2C interface from the carrier card to setup the mezzanine registers.
  - It does not use the PPC integrated Processor inside the FPGA.
  - Its the minimum version to run the system
  - The Long Trace facility does not allow PPC to run (takes all BRAM)
  - Register Setup is done through script files
- VHDL1 :
  - Contains the VHDL0 functions plus :
  - ENX webserver embedded inside the FPGA PPC to control ALL the mezzanine registers and integrated facilities
  - Readback card temperature and send alarms in case of high temperature
  - Integrates the mezzanine ID (serial number OS and firmware versions etc…)
  - Long Trace interface is integrated with PPC
  - Register setup is done through GUI interface.
  - Contains monitoring parameters and counting rates

Installation setup

- To install the VHDL1 no extra hardware is needed.
  - Most of the setup was made from Orsay prior to the visit. All software packages were copied and installed.
  - New programs were developped to upgrade the FPGAs firmware automatically
  - Essential to get back to VHDL0 easily
  - Needs 2 hours to reprogram ALL mezzanine FPGAs
  - If VHDL0 is needed only 2 hours to get back to old version
- The procedure to install the VHDL1 is :
  - Take data from the system using VHDL0 as reference source to comparison
  - Upgrade partially the system with VHDL1
- Mezzanine LSC package,
- Mezzanine GUI package,
- and Long Trace readout package

Week 1 and Week2 planned results

- **Week 1:**
- Launch acquisition with the VHDL0 to collect data from all detectors to use them as reference data source for comparison. This is important to verify especially if there are bad channels to neglect them during results comparison.
- Install VHDL1 on 2 complete TCs out of the four TCs, and run acquisition with VHDL1, and store results.
- Compare and validate data with first VHDL0 acquisition.
- Qualify Long Trace and verify with virgu the results.
- Keep half channels with VHDL0 and qualify for 3 nights that the system is still alive and stable.
- **Week 2:**
- Switch to complete VHDL1 and start Phase 2 tests.
- Make several tens of start stop setup Run record data and look for failures.
- Make long period nonstop acquisition (2 to 3 complete days). Use ENX access to cards during acquisition to test system stability.
- Check for long traces (Start Stop DAQ procedure)

What happened really in Week1?

- All the crates were powered up except one because of water cooling.
- EF (thanks a lot for his help) makes a demonstration to make the system running with the actual VHDL0.
- The start.sh did not work properly (carriers not connected to network).
- 1 digitizer was not working DaB (thanks a lot for his help) and EF try to repair or to retrieve from the system.
- Some pizza boxes did not respond properly (narval 12, 8 ….)
- Training continued tens of, power on and off the system if carrier fails network,
- look for linko synchronization start/stop etc…
- Finally acquisition started with VHDL0 reference data as planned.Failed!! HV was not optimum
- In parallel the software packages were installed and tests started on them.
- Some modifications were made in parallel on the firmware so that the data structure seems compatible with the VHDL0. held in parallel (VHDL modification and system training).

What happened really in Week1?

- The system configuration was composed as follows:
- TC 1 VHDL0 TC 2 HS TC 3: VHDL0/1 TC 4: VHDL1
- FPGAs programmed new run started @ 13:50. Data recorded with Test_Acquisiton1 label. Daniele (thanks a lot for his help) participated in the data comparison.
- Test_acquisition 2: New system configuration (FPGA programming is long).
- TC 1 VHDL1 TC 2 HS TC 3: VHDL0/1 TC 4: VHDL0
- Test Failed (Narval 12 stopped working).all decided to retrieve it.
- Test_Acquisition 2 restarted @ 15:00 but new problems (BP on carrier continuously), all the chain of Narval12 out(carriers digitisers etc..)
- BP came from partial Trigger processor installation. (done by DaB) +
- all HW to Narval 12 (TC1) + TC2 (HS) was removed
- Finally only 2 TCs were still alive to make comparisons.

What happened really in Week1?

- 11 :30: after all these setup modification no major problems (hooooffffff).
- Error very short happiness !! because 15 minutes Narval8 went down. Bios problems reboot from computer room)
- After Lunch new acquisition was launched but the carrier GUI was blocked. ON/OFF crate wait few minutes, and setup is OK.
- 16h45: end of Xilinx prom programming and new run was launched but the data doesn't seem to be completely compatible.
- VHDL0 source files comparaison, and rough analysis showed differences in code for data frames and structure compatibility,
- Weekend Left to make detailed analysis and put VHDL1 uptodate
- During the weekend all the VHDL0 was checked to make the necessary changes in VHDL1 so that the data streams are the same, and tests were postponed to the next week.

What happened really in Week2?

- New run started -→ no data, Cat command did not work.
- Shut off /ON all crates (same thing RESET setup etc….,) CAT command OK (no explanation)

- 11:10: 2 hours to have data. Weird situation!!! (Several power ON/OFF always problems)

- VHDL0 frame nb was modified (100 instead of 80 or 160 + variable).
- The VHDL0 I2C code was completely modified wrt early version this year given to VHDL1.

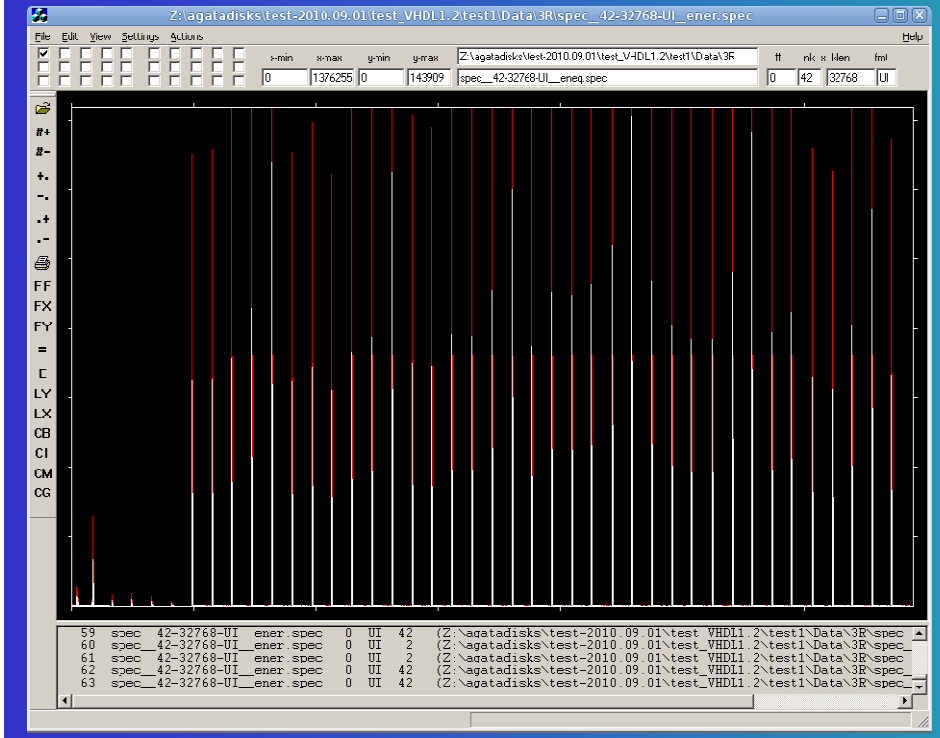
- The new configuration to qualify the VHDL1 is to use fully CSNSM LSC and GUI mezzanines.

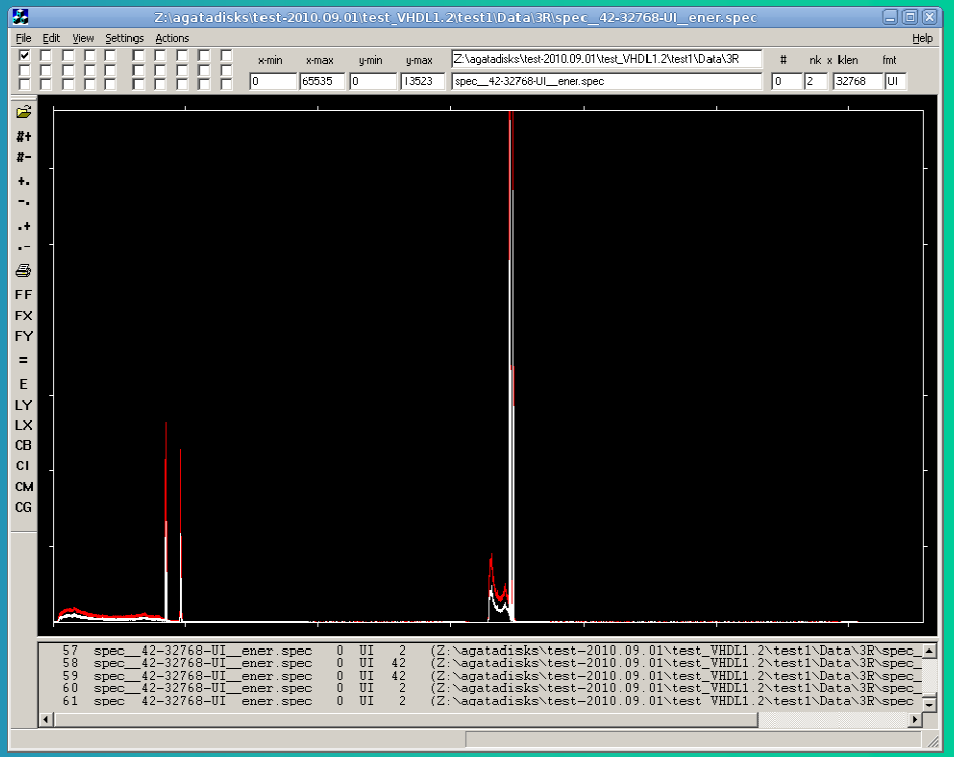
- Only 2 TCS were working for comparisons (TC3 and TC4).
- 14 :00: after lunch the counting rate on core was divided by 2. No panic EF explained that detector was moved away from source.

- 14 :30: Mirror test failed difficulty to reprogram the carrier couples Narval 8 had intermittent problems.

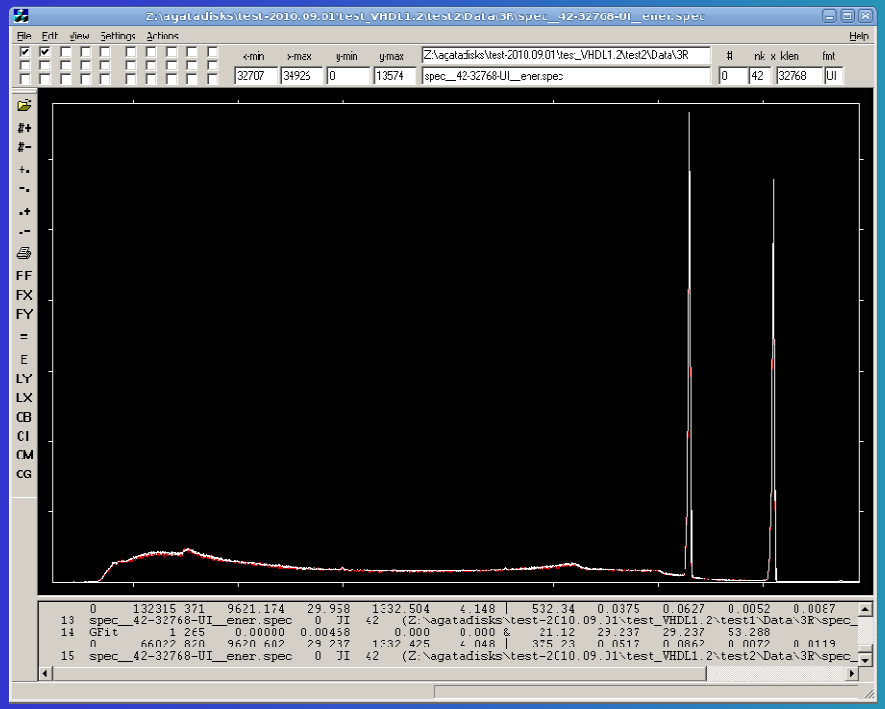
- 15 :10: system is bit stable : New run started …..
- Cluster3 => VHDL_1.2
- Cluster4 => VHDL_0
- 15h30: Data analyses with the precious help of Francesco (figures below)

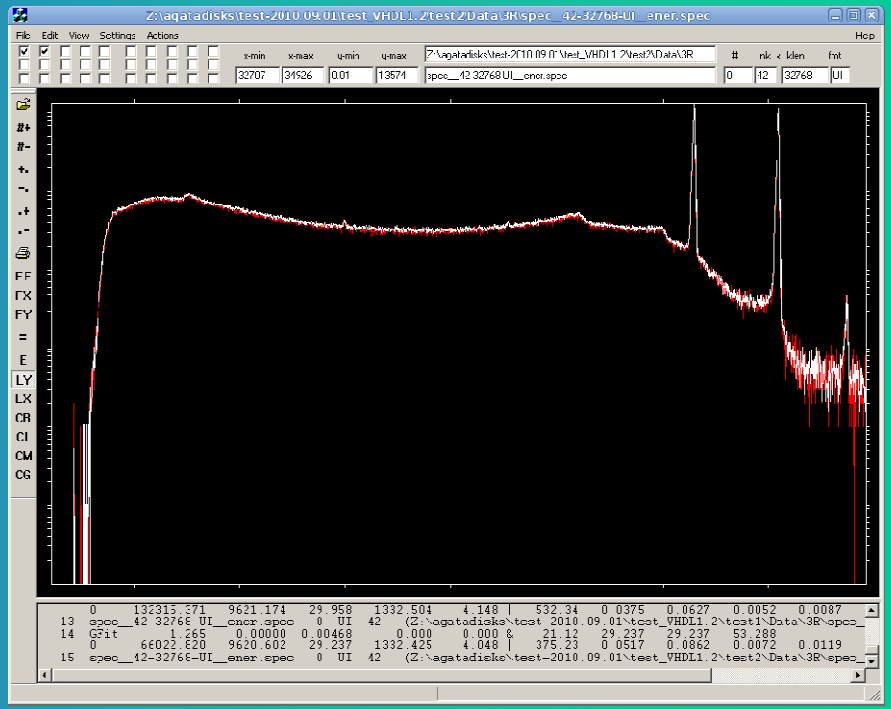
SOME FIGURES





SOME FIGURES





What happened really in Week2?

- data recorded from VHDL1 is completely the same as that in VHDL0 (first battle won !!).
- GUI carriers blocks; shut off and on 5 min later system OK.
- Narval 6 generated problems too “error opening file energy.bdat”…. No way to solve narval 6 errors, so LSC could not be executed properly. All HW Crystal was deleted.
- First night run acquisition (Test_acquisition5) was made on what was left as working crystals (5 out of 12!!).
- After night acquisition; first thing check all network connections all ok no ENX server crashed (excellent news). Acquisition is still running good news) except on narval06.
- Data analysis seemed ok same as the figures above. The counting rate was not significant to verify since detectors were not centered. The only important thing is that the system is stable as with VHDL1.
- LSC and GUI full integration tests started and updates Things started smoothly.
- 11h30: carrier couple 36 – 09 Damiano check why then deleting more crystals, because they were connected to Narval 8 and the linko synchronization with the carrier failed…..

What happened really in Week2?

- A warning (orange light on the PCI front panel) on narval10 … reboot trial were made but in vain…..
- 14h45: crystal 4R (couple de carrier 36 – 09) was also deleted from the system.
- Only 3 crystals were working from TC3 and TC4. This is too little so it was decided to have part of the other non working TCs to integrate te acquisition such as 1G and 1B to have at least 5 working crystals.
- New topology file is needed to exchange woring/non working mezzanines.
- 17h45: 1G => VHDL0 1B => VHDL0 3R => VHDL1.2 3B => VHDL1.2 4G => VHDL1.2
- 17h55: threshold value different on crystal 3R register was modified by the GUI.
- 18h15: reboot of narvals !!! (no investigation on this observation)
- 18h20: New run using full Orsay LSC
- 18h45: Run acquisition for 5min, data analysis seems OK
- 19h10: New night test run same configuration

What happened really in Week2?

- **Wednesday :**

- 9h20: Check system status from all night acquisition : Rio are OK Network OK,
- New strange observation counting rate of 1B (VHDL_0) very high w.r.t. other crystals (16000 VS 4750 for all others)… but the spectra analysis seems OK (no investigation on this observation).
- 9h40: First Long Trace tests (/agatadisks/test-longues-traces-2010.09.08)
- Using GUI options: « card by card » ; « current crystal » on 3R and 4G

- 10h00: test 2, like test1 to check file size.

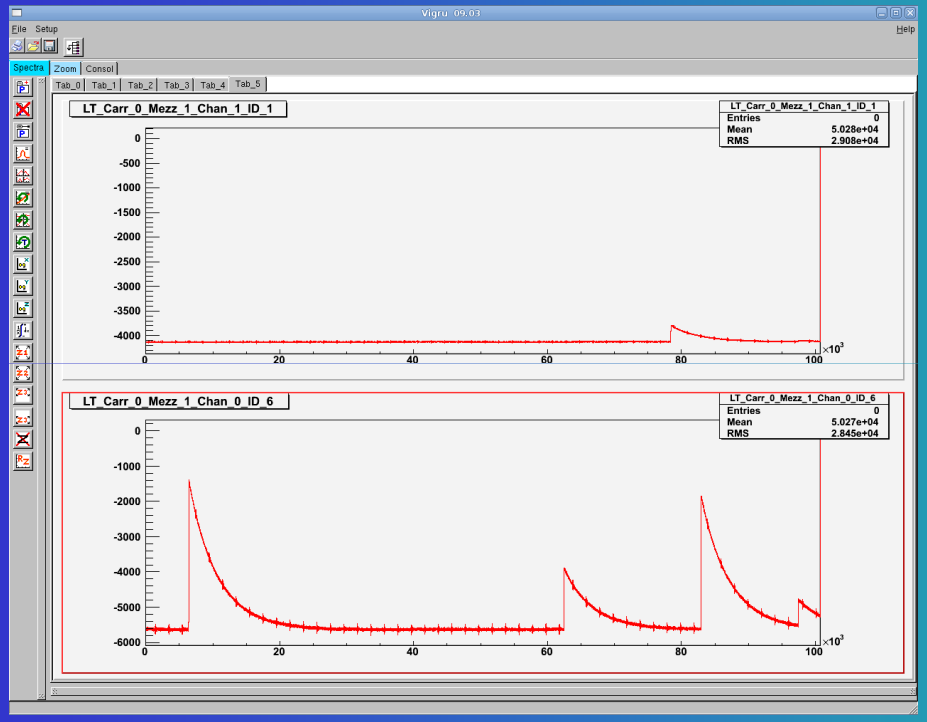
- 10h30: Virgu display did not work, Nico checking……..

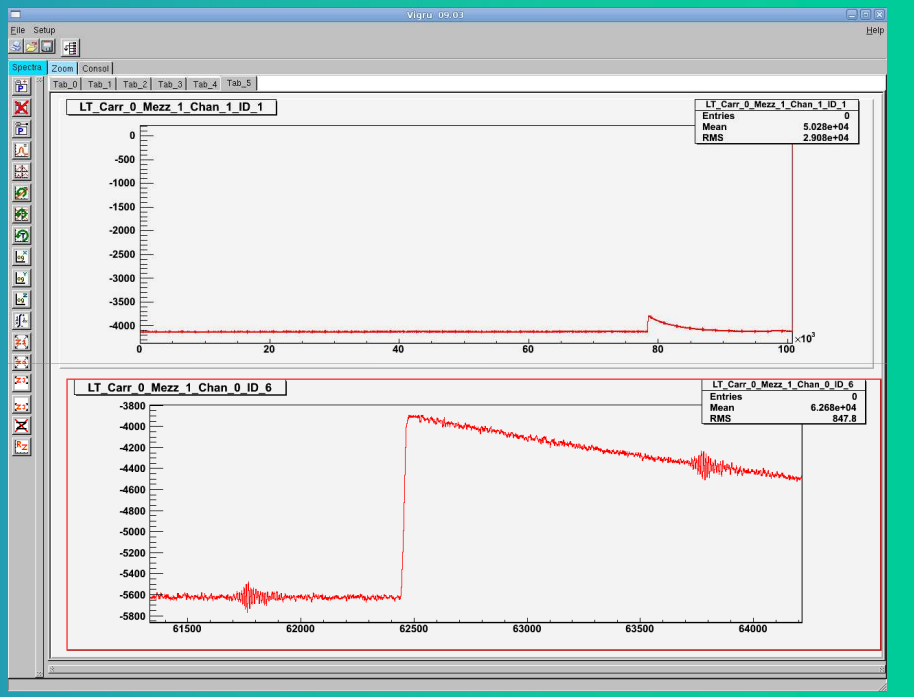
- 11h00: Found !! the carrier trace length was different (100 instead of 160) variable modified test again YESSSS!!

- 12h30: LT were shown with vigru !!! figure below showed the first LTs.

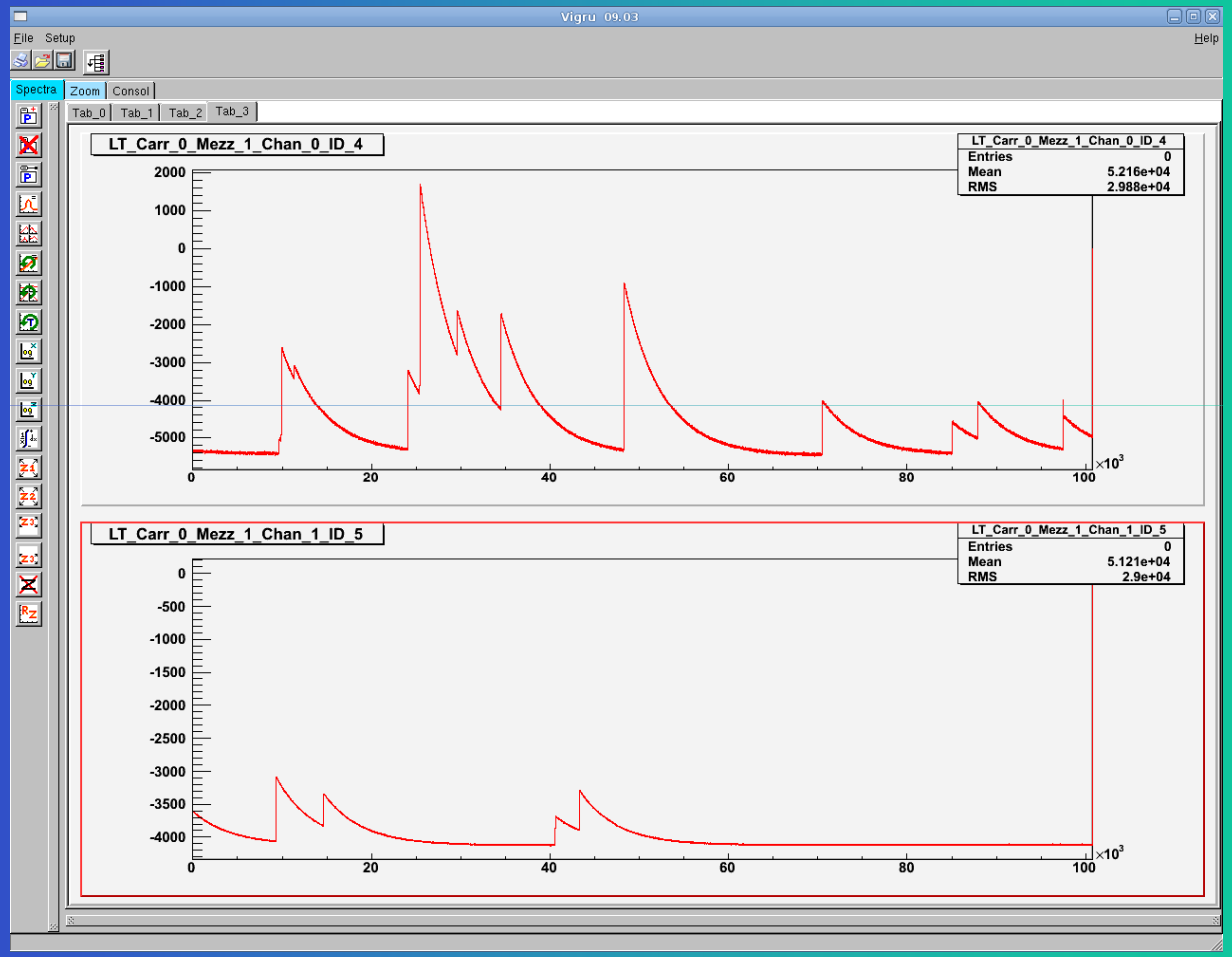
- **First core Long traces on left complete one and on the right zoom on noise**
- **Segment long trace with some noise zoomed.**

CORE LONG TRACE FIGURES

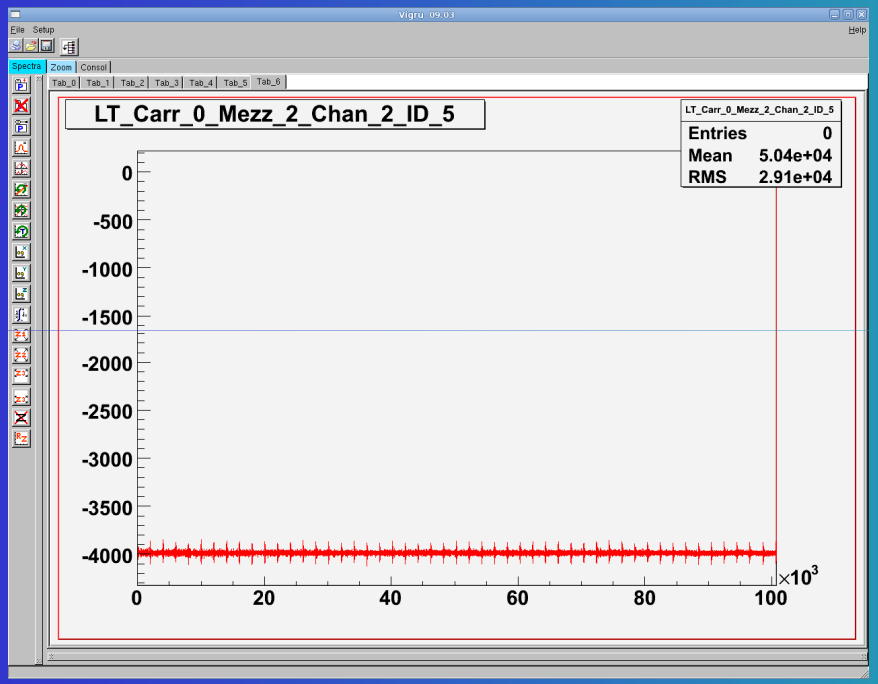


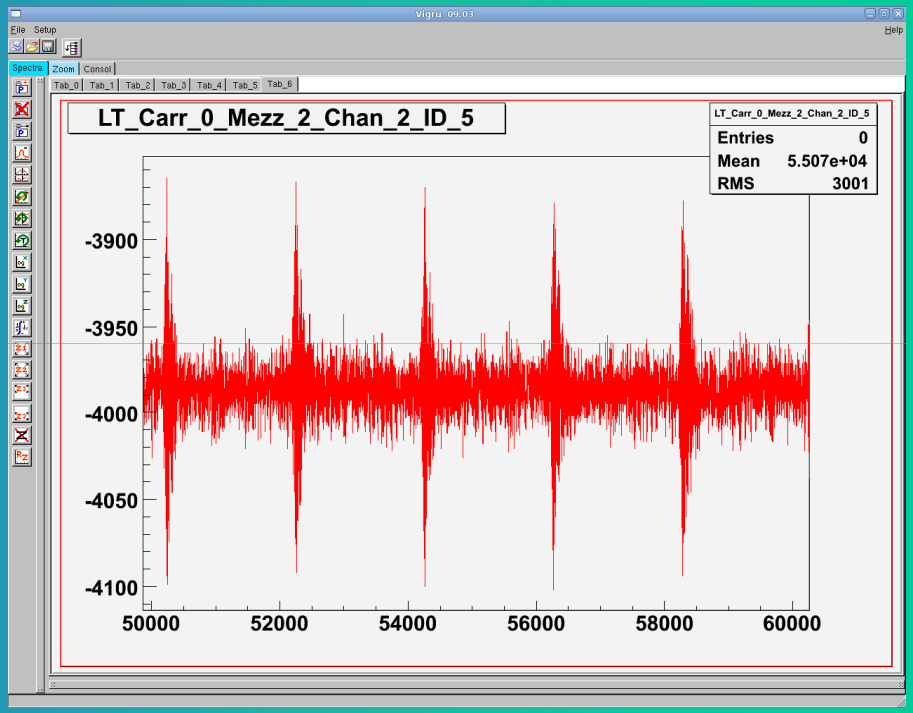


Other Long Trace Figures



Other Long Trace Figures

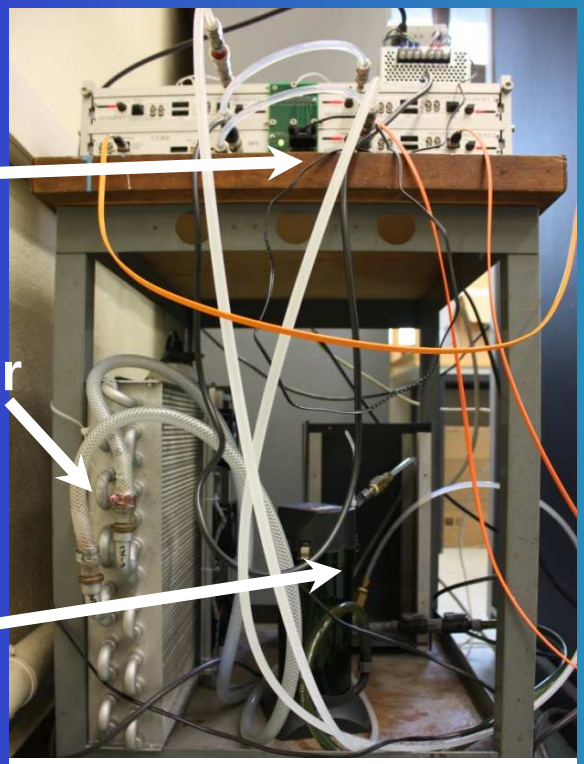




What happened really in Week2?

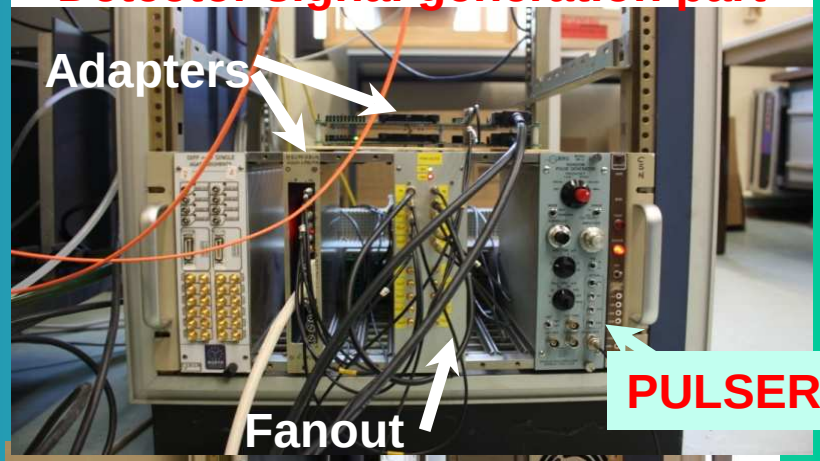
- Thursday Meeting to conclude :
- Orsay engineers explained all the problems occured.
- They all agreed that VHDL1 is working.
- VHDL1 was not Qualified (Long time tests according to CSNSM quality system procedures)
- No time left to make Long time qualification.
- System went back to VHDL0
- CSNSM suggested to place an engineer to help debugging the non stable system but things went worse later 2 TCs warmed up and everything was postponded now due to higher priorities
- It was decided that long time tests could be made after New Year beginning jan.2011.
- More news in next AGATA Week.

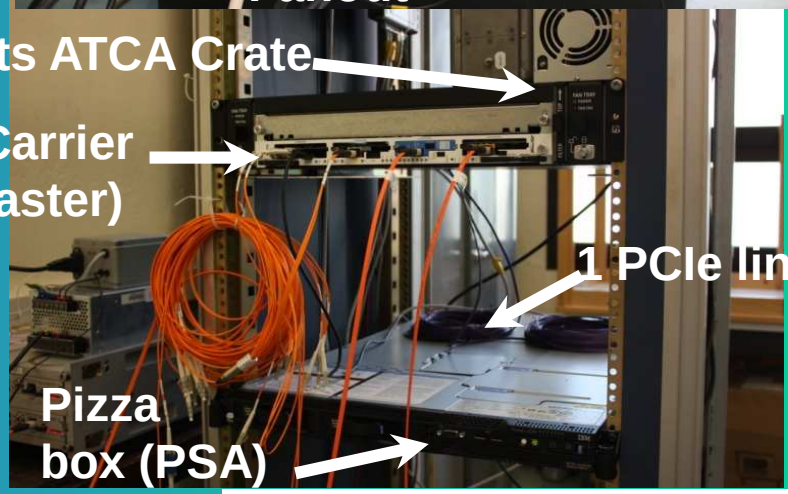
Few words on Orsay Testbench



Digitalization part

Detector signal generation part

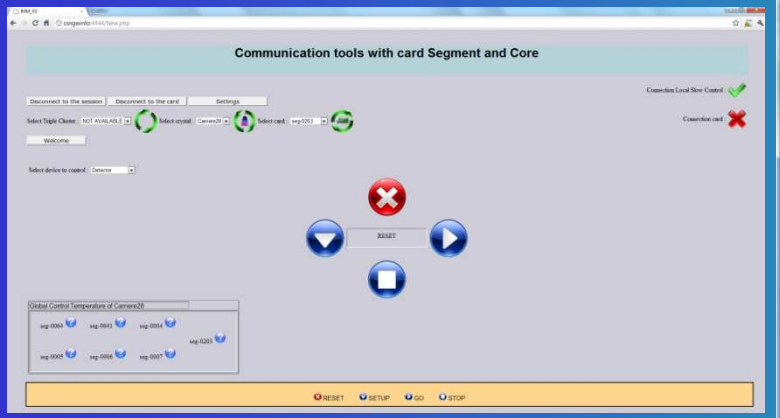


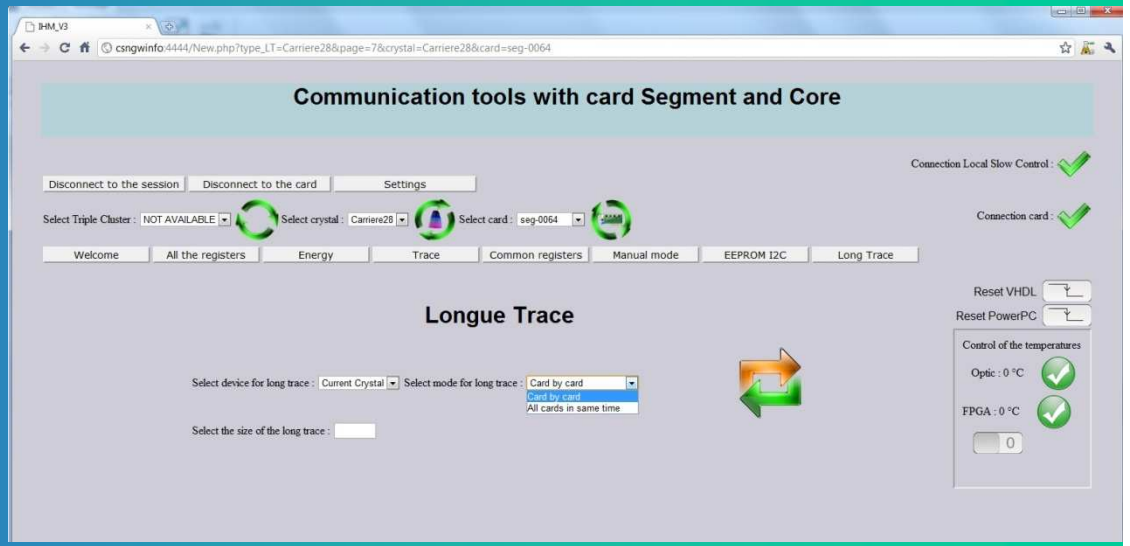


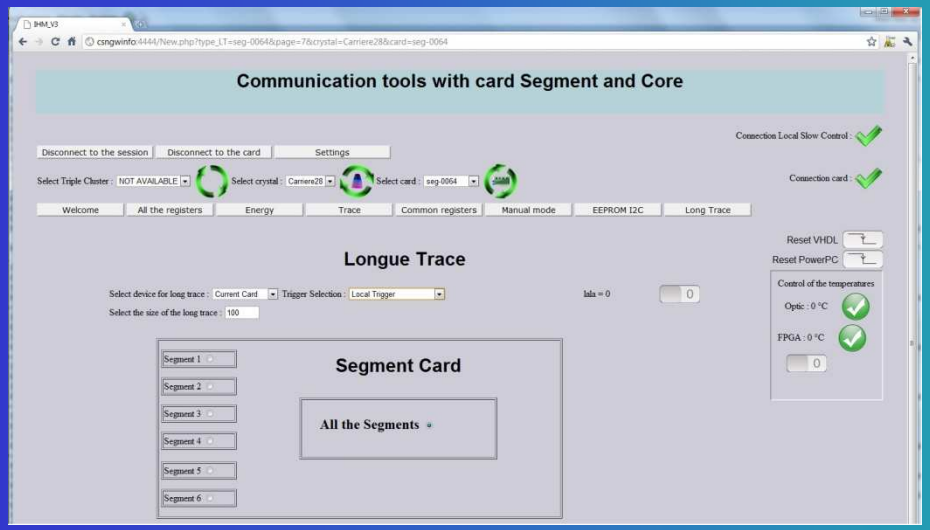
Processing part

➢ Wait 2nd Linco board ➔ complete crystal setup

Mezzanine GUI

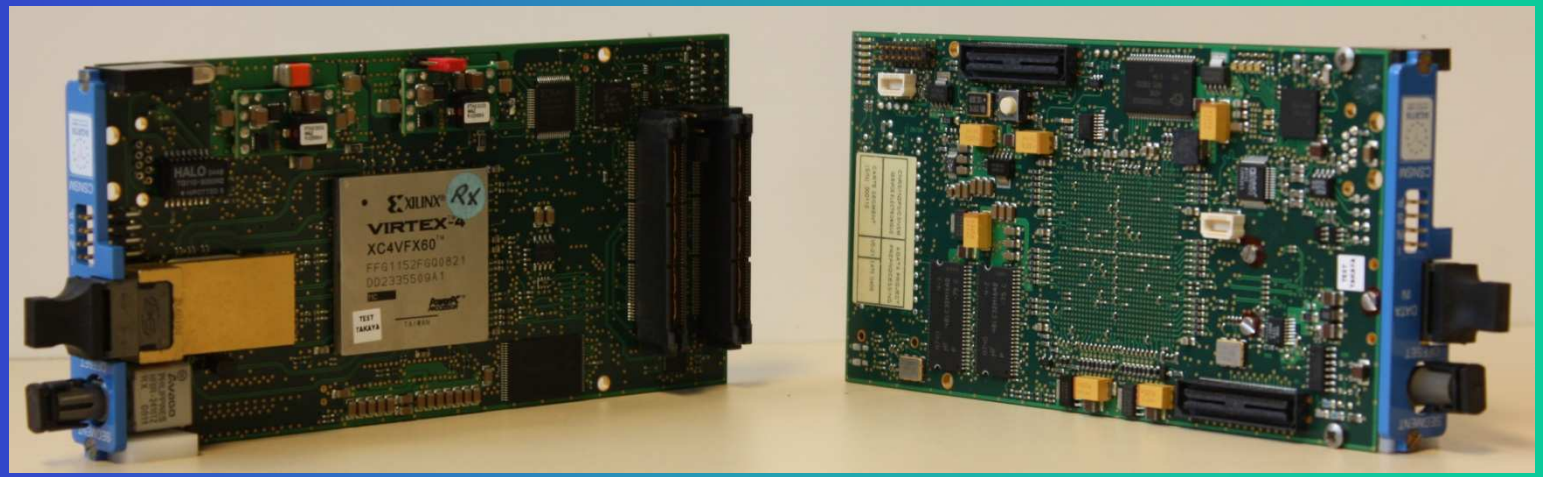






STATUS OF THE PREPROCESSING ELECTRONICS MANUFACTURING FOR THE GSI PHASE

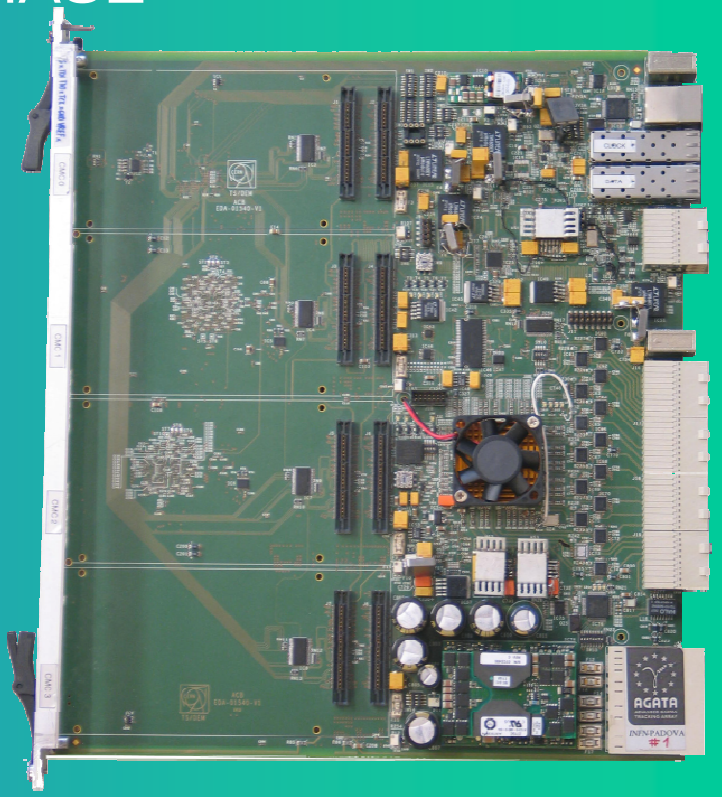
- **Goal** : equipment for ten additional crytals (5 ADC).
- **CSNSM part** : boards manufacturing
  - 80 Segment mezzanine boards ➔ in progress (**CSNSM expert**).



  - 30 Core mezzanine boards (used for GSI phase) ➔ 20 in progress (**CSNSM expert**).

STATUS OF THE PREPROCESSING ELECTRONICS MANUFACTURING FOR THE GSI PHASE

- 24 Carriers board **V4.0** (+ TCLK boards associated) from IPNO feedback, cabling company feedback (EMELEC) + IPNO procedures (1st powerup, Jtag, functional tests) ➔ V3.0 files Transfer have started (begining November)
  - Checks on PCB modifications and manufacturing files and compare with V4.0
  - Checks, with Padova team, results on first preproduction of V4.0 cards
  - Build a complete industrial package for the company (tests procedures).



Real work to prepare this phase (understanding, training and writing documentation) ➔ not only duplicate IPNO work.