The ATLAS Pixel Detector

- Introduction -

Pixel Detector Introduction

- Two main purposes of this (and the next) presentation:
  - Create a general understanding of the pixel detector, its services, operating conditions and basic calibration measurements
  - Introduce the terminology used in the pixel collaboration
    (You will need to communicate with the on-call shifters and/or other experts using this vocabulary)

Outline

- The Pixel Detector
- Pixel Detector Services
- Operating Conditions
- Basic Calibration Measurements

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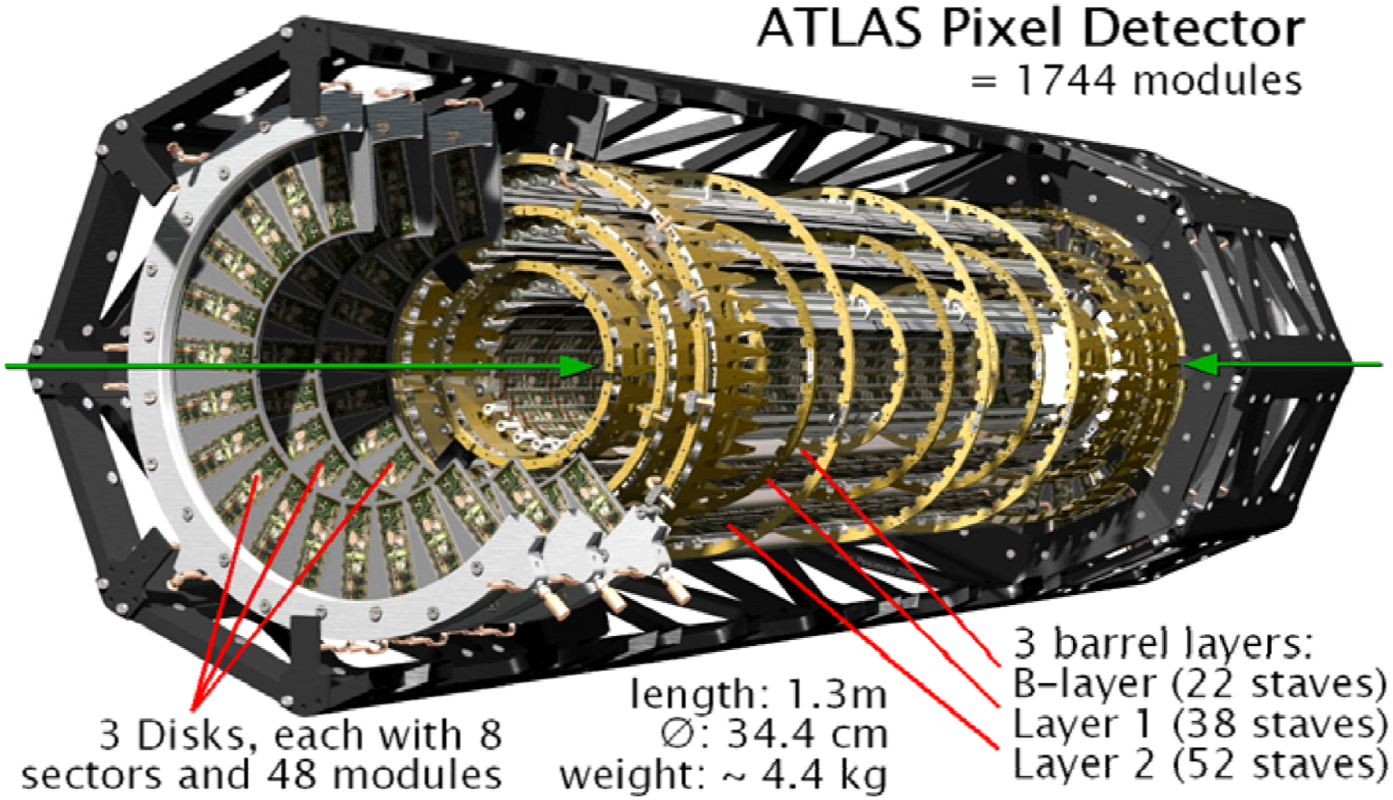
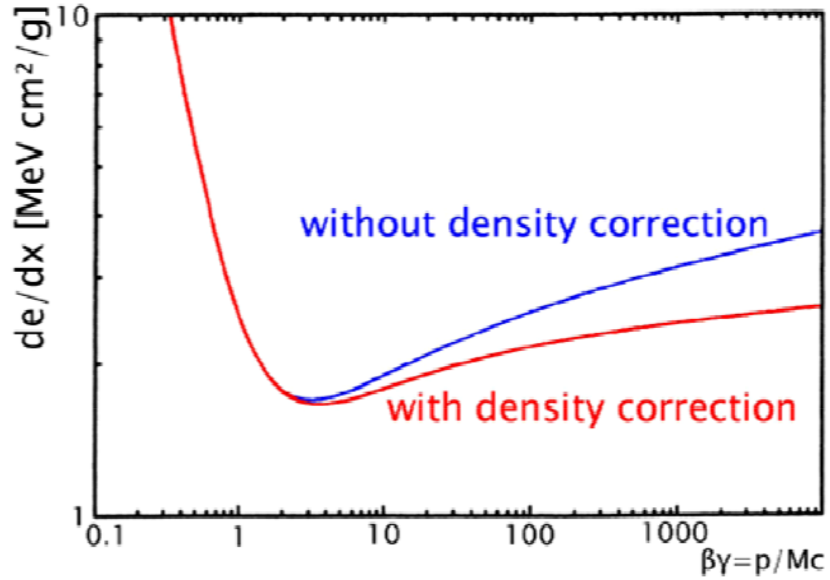
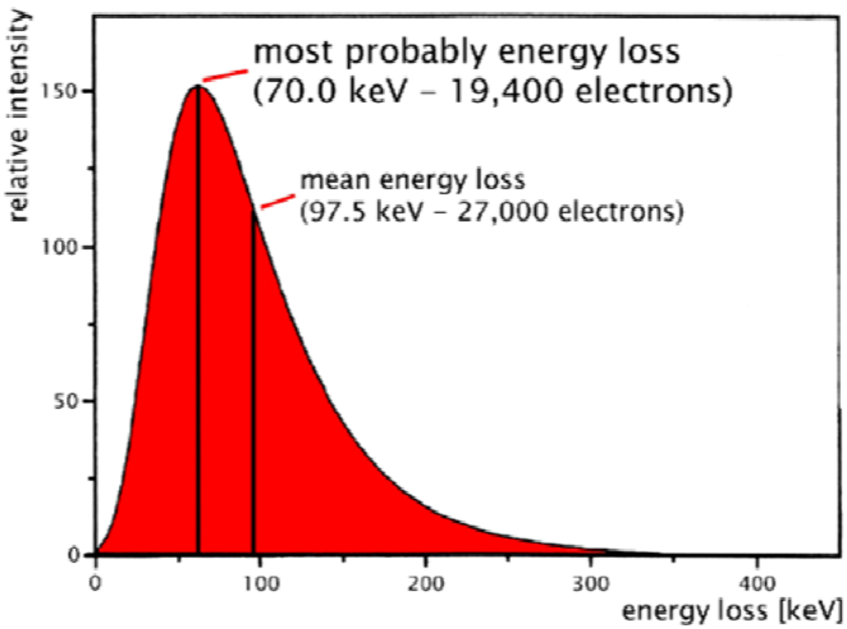
The Pixel Detector

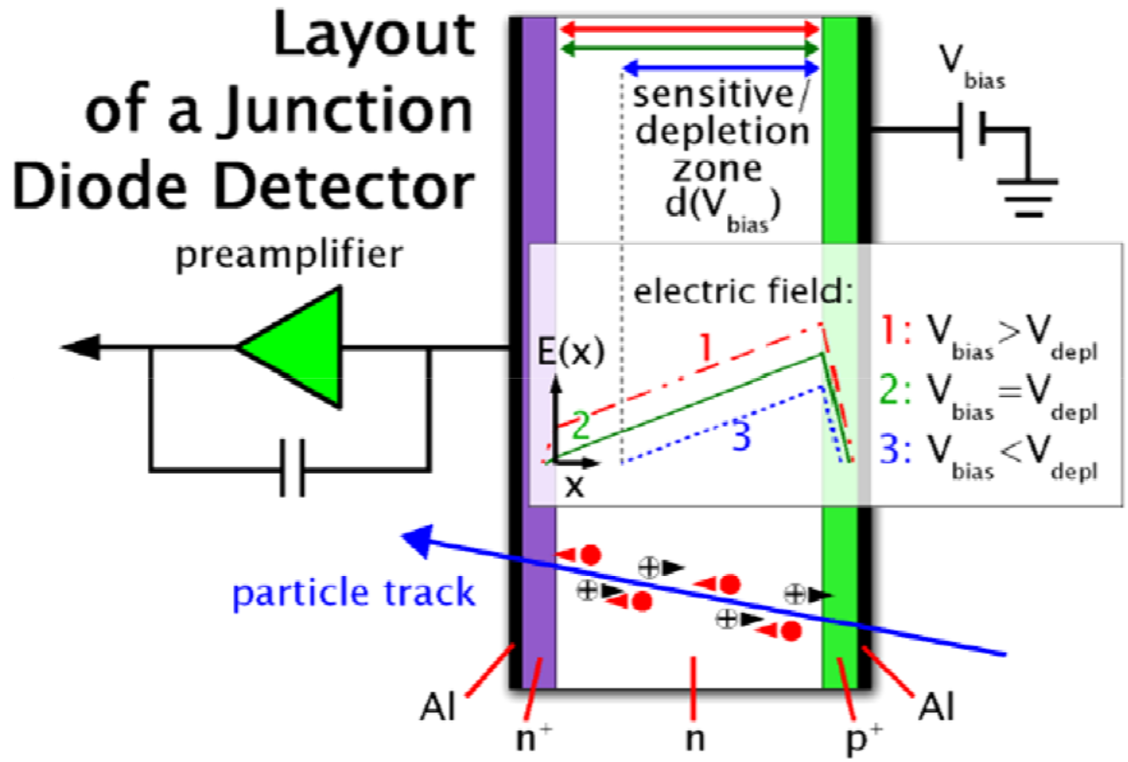


- 3 Barrels, 2 x 3 Disks
  - 3-hits for $|\eta| < 2.5$, innermost layer (B-layer) at R = 5 cm
- 1744 Modules with ~80 million readout channels, 1.8 m^2 active area
- Evaporative cooling integrated into support structures (sectors / staves)

Semiconductor Sensors

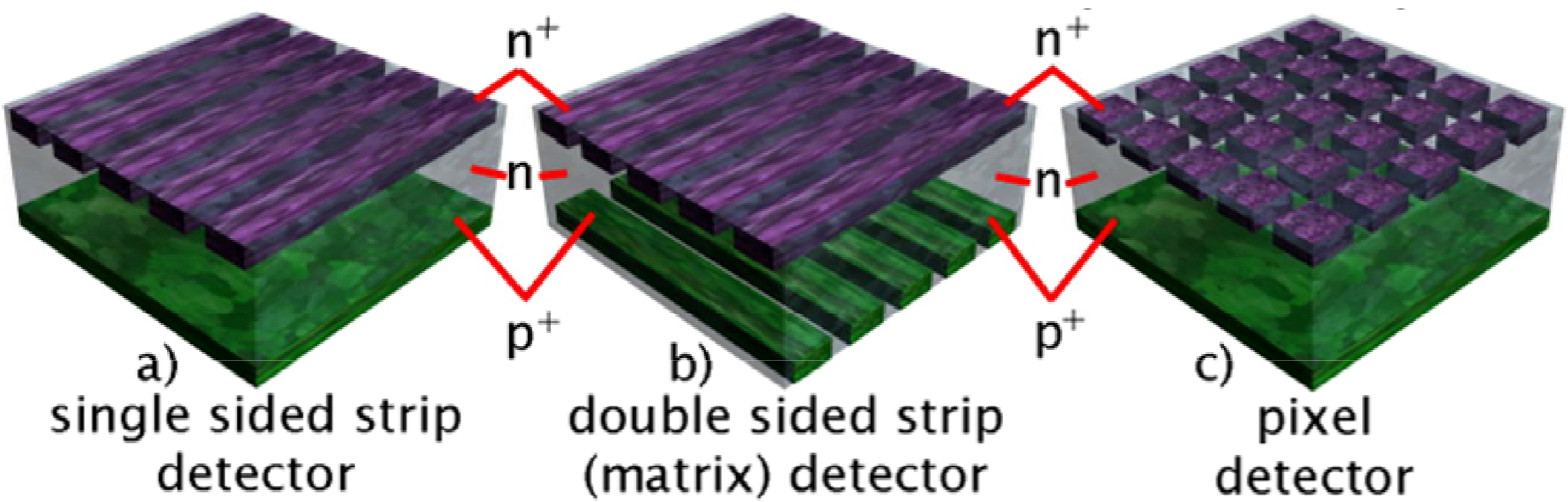




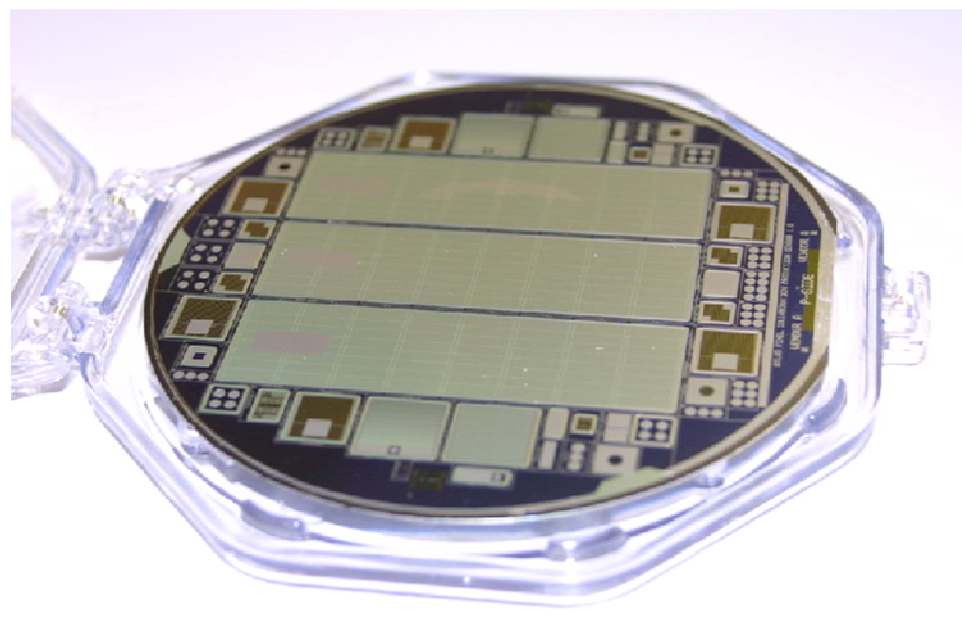


- Reverse-biased diode
- Charged particle generates free electric charge carriers in the depleted region
- Charge carriers are drawn to the electrodes by the electric field
- Mip-signal (mpv): ~20000 e in 250μm Si

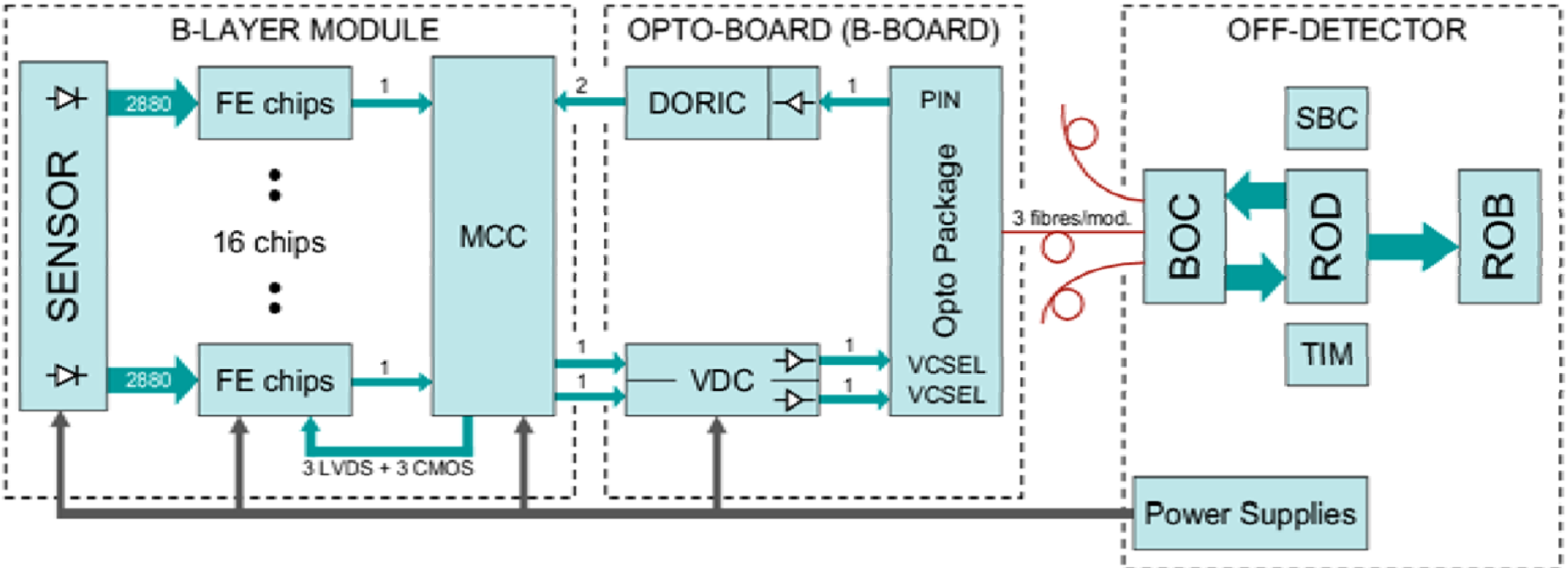
Position Sensitive Semiconductor Sensors



- Segment one (Strips, Pixels) or both (Strips) electrodes to obtain spatial information
- ATLAS pixel sensors: 60.8 mm x 16.4 mm active area with 47232 pixels
- Normal pixels: 400 μm x 50 μm
- Long pixels: 600 μm x 50 μm



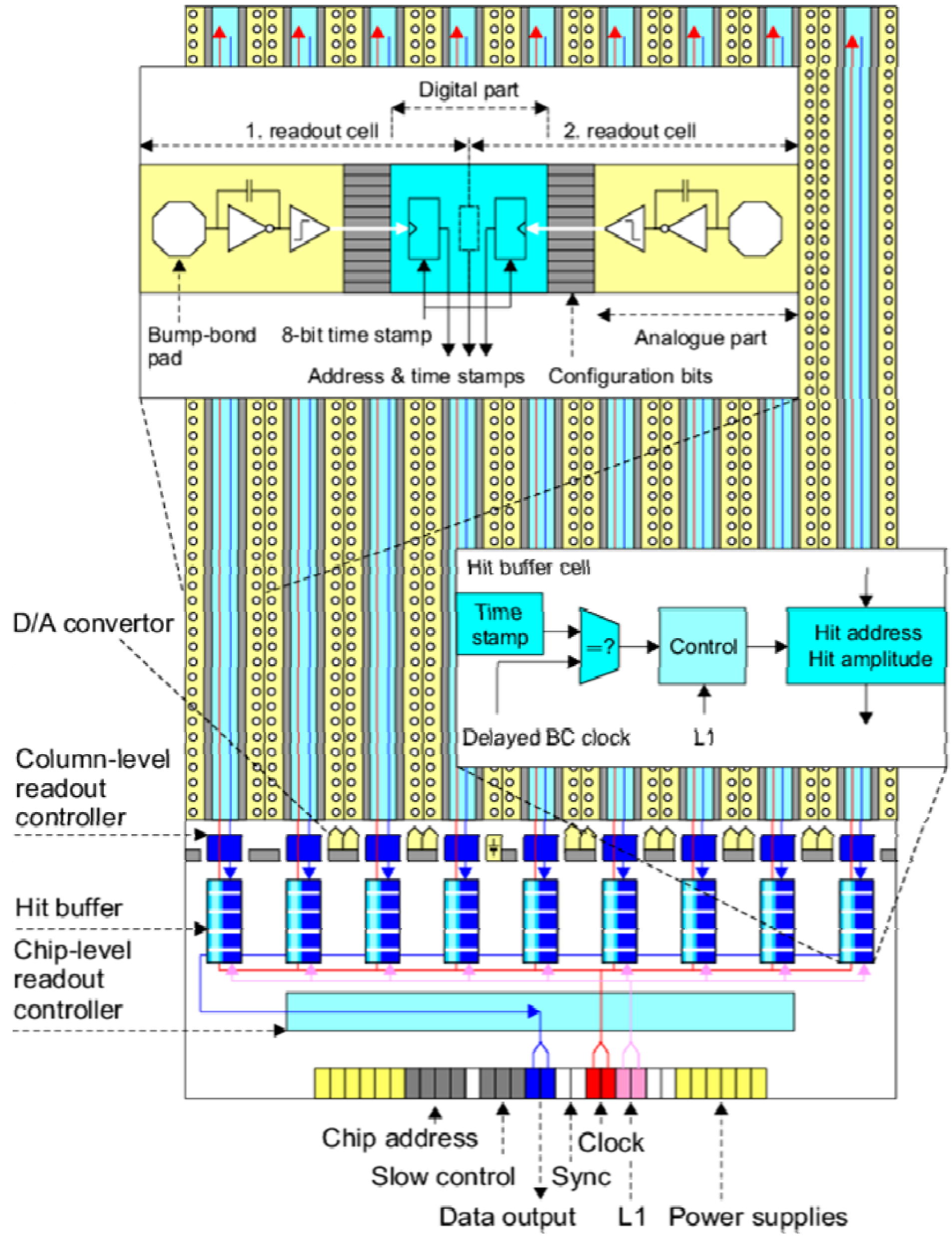
Readout Concept



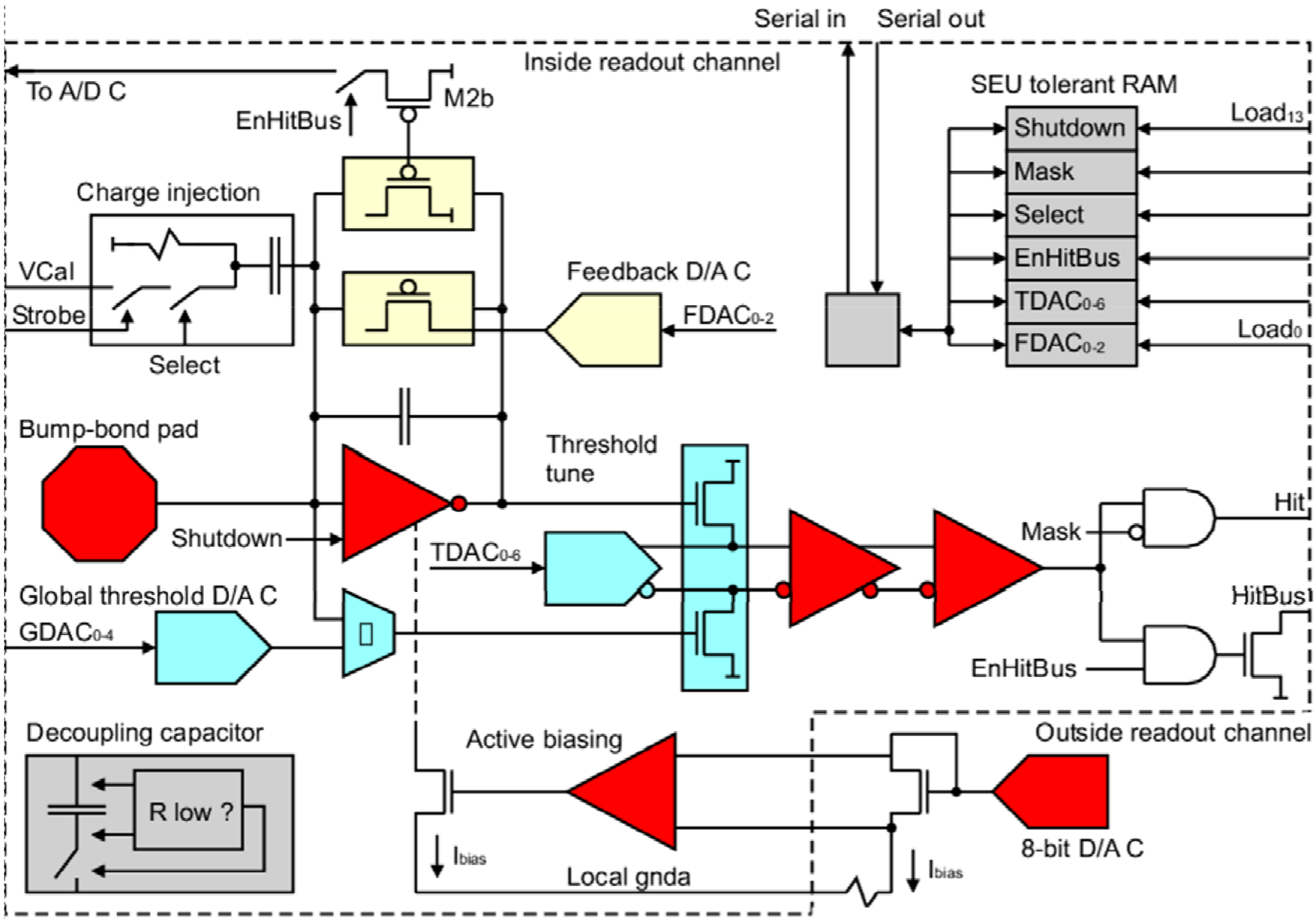
- Module
  - 1 Sensor is read out by 16 front-end (FE) chips (2880 pixels each)
  - FE chips of one module are controlled by Module control chip (MCC)
- Communication with off-detector electronic via optical signals
  - Electro-optical conversion on optoboards (1 per 6/7 modules)

The Front-end Chip

- A front-end chip contains 2880 pixels in 18 columns and 160 rows
- Each pixel cell contains preamplifier, discriminator and readout logic, which transfers hits to buffers at the bottom of the chip
- Peripheral region contains hit buffers, logic for trigger coincidence and data serialisation and programmable DACs for the currents and voltages needed for the operation of the chip.
- Hits are transferred by column pair
- Pixel configuration uses a 2880 bit shift register connected to all pixels

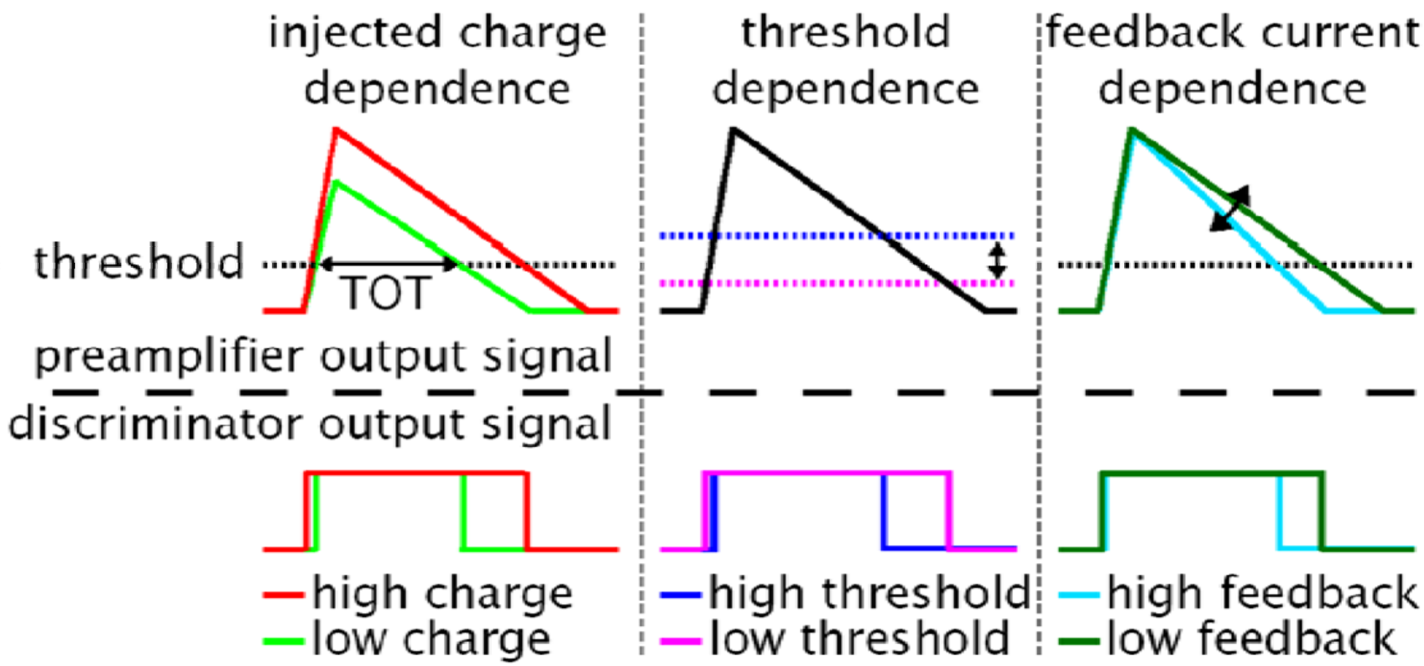


The Pixel Cell

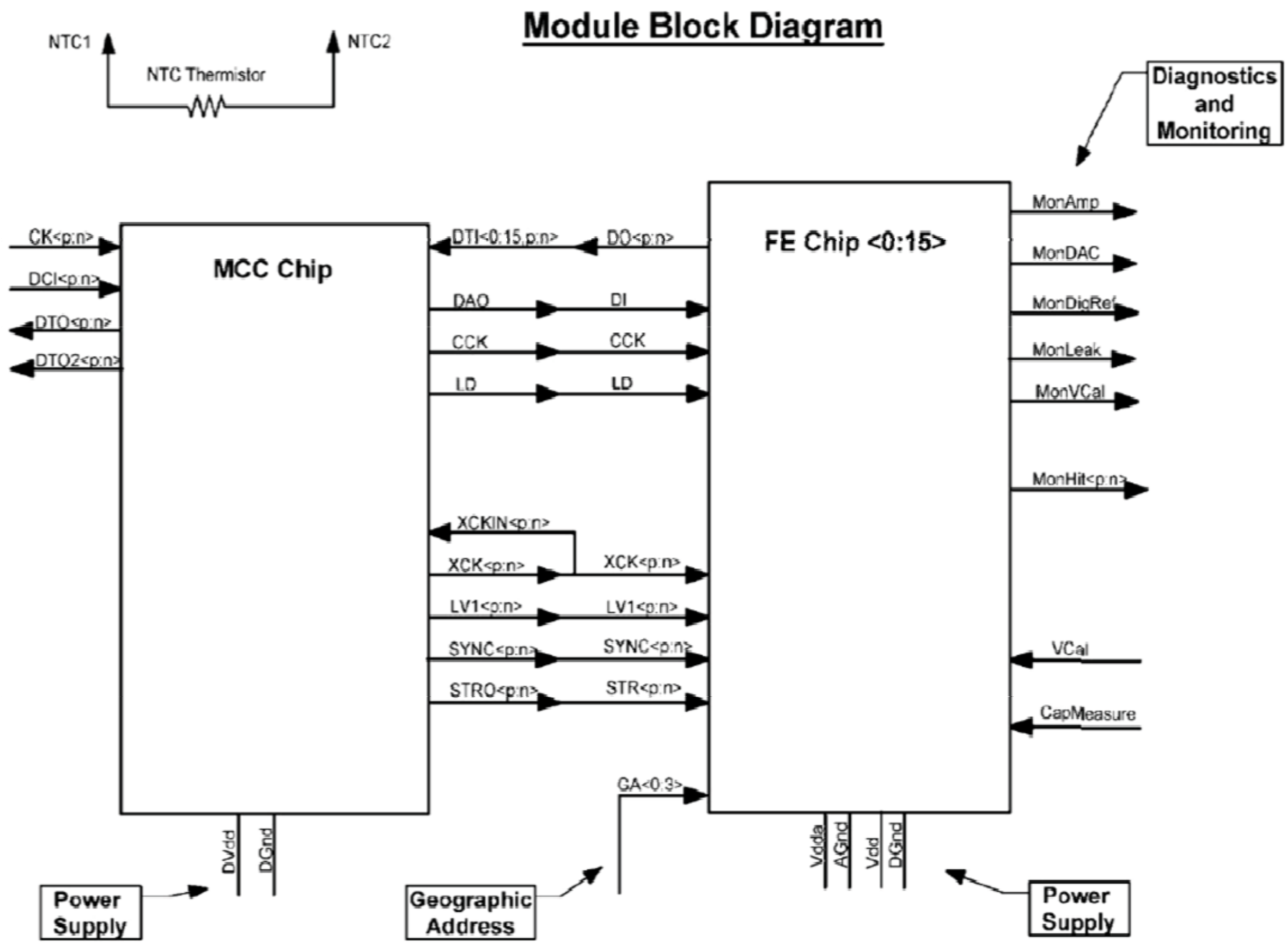


Preamplifier and Discriminator Signal Shapes

- Time over threshold (length of discriminator signal) depends on
  - Deposited charge
  - Discriminator threshold
  - Feedback current
- Information of the ToT (in units of 25 ns) is read out together with the hit information → can measure the deposited charge

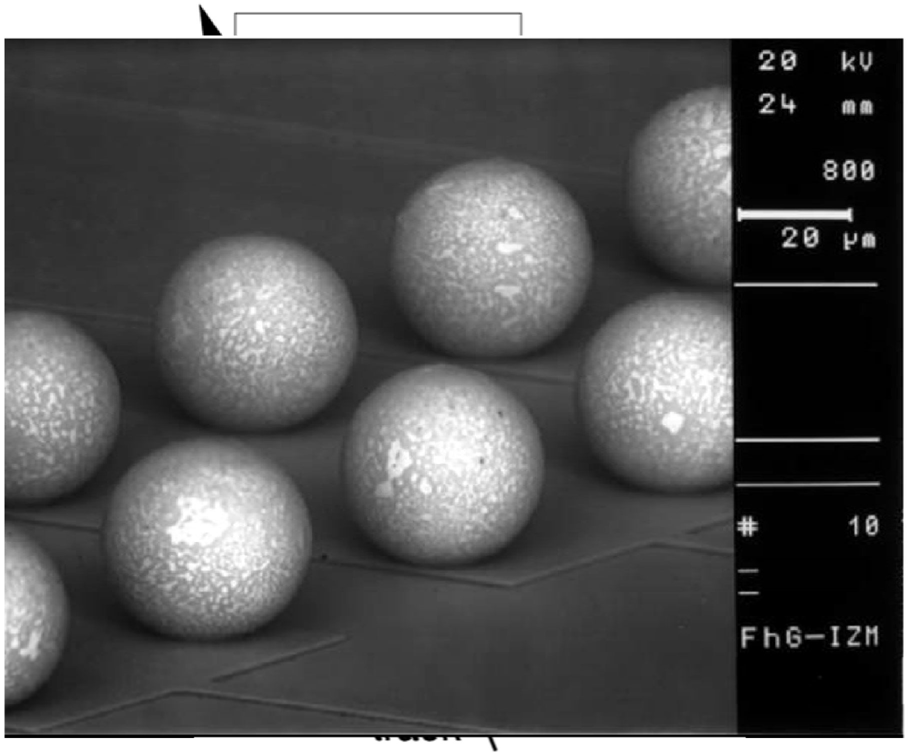


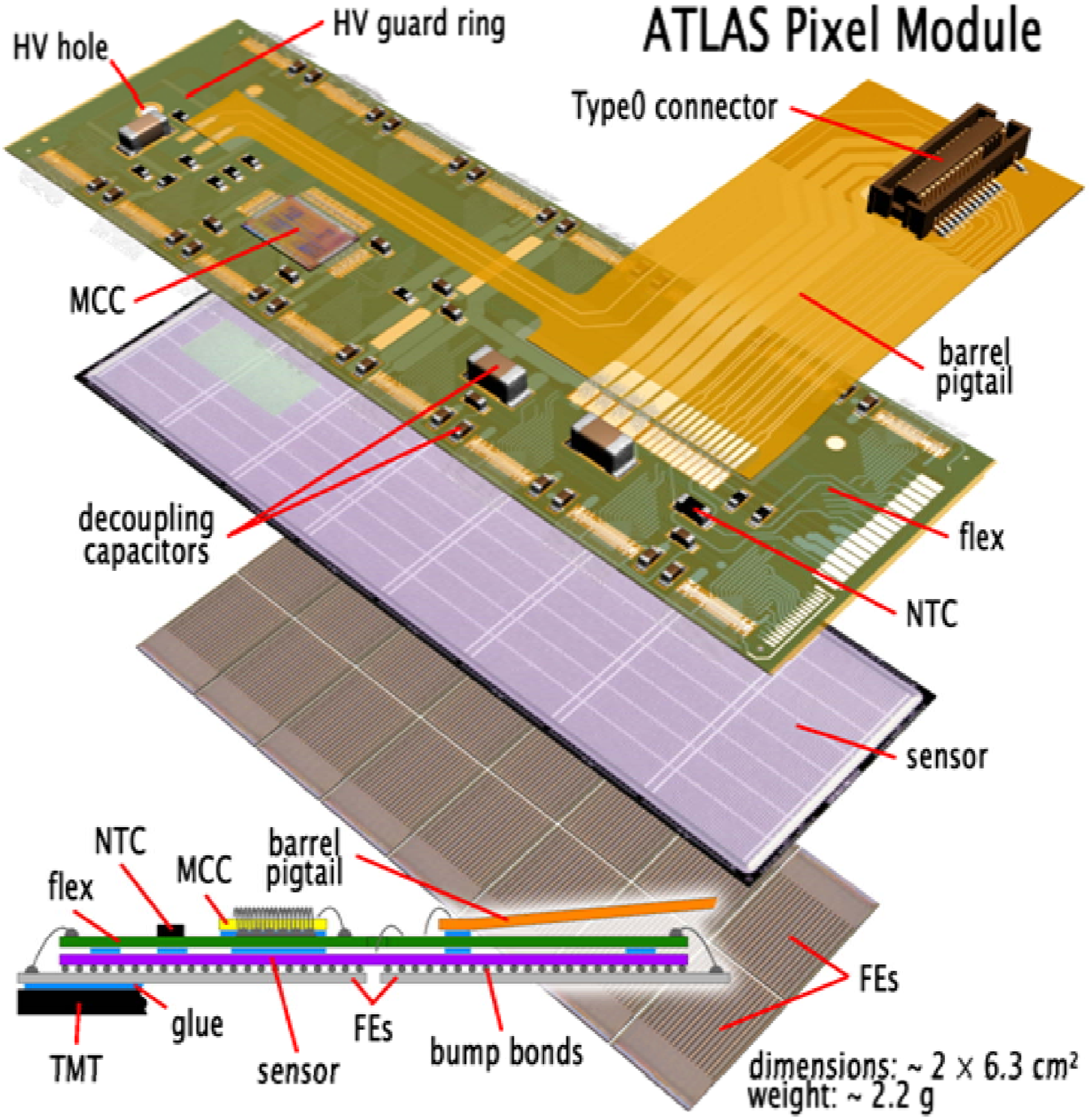
- Control of the 16 FE-chips
- Event-building



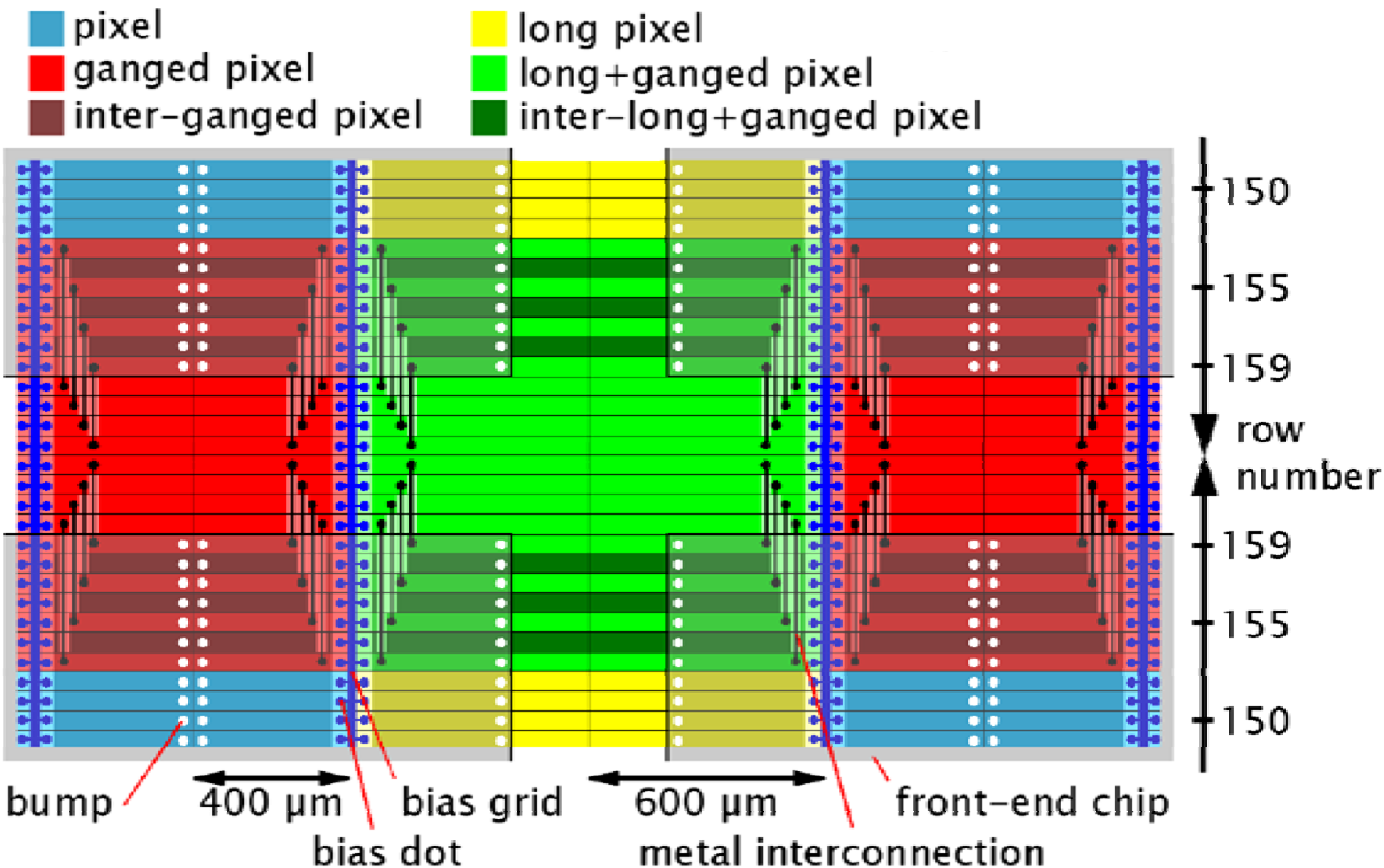
The Pixel Module

- FE chips bump bonded to sensor
- Routing of signal and power lines done on flex kapton circuit glued to sensor backplane
- Type0 cable soldered directly to flex (disc modules) or connected to pigtail (barrel module)
- Type0 cable connects module to PP0

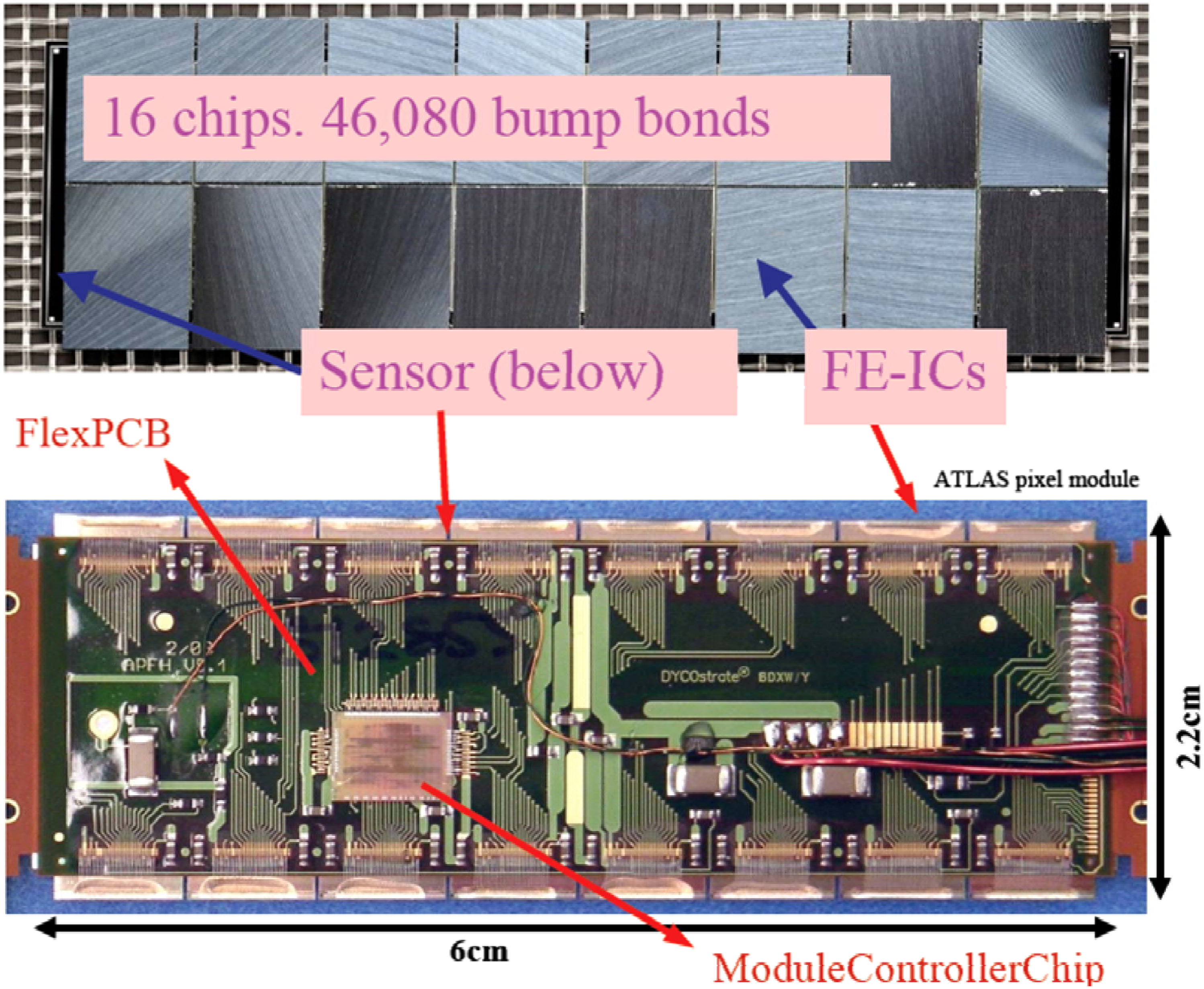




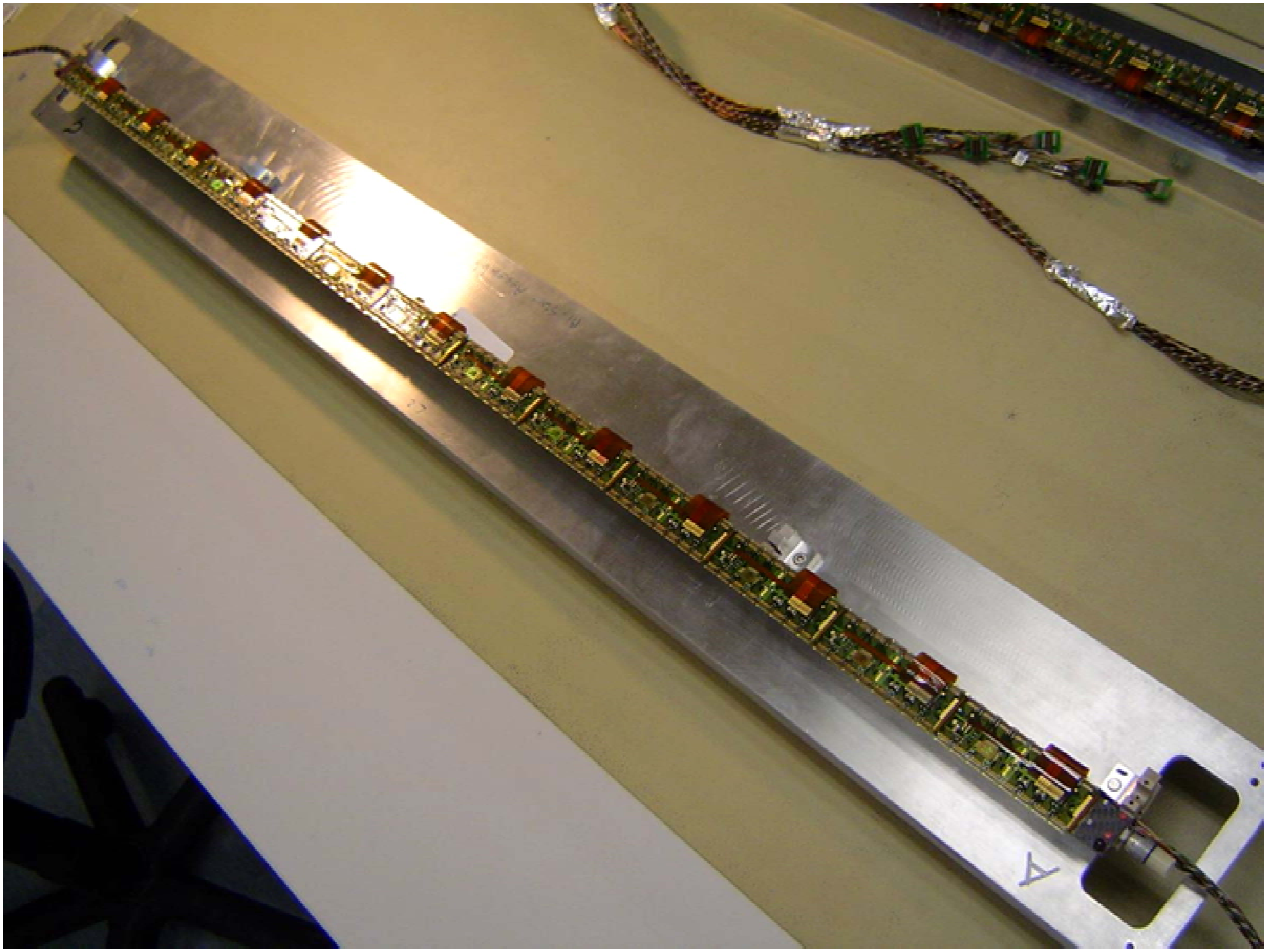
Interchip Region



Pixel Module

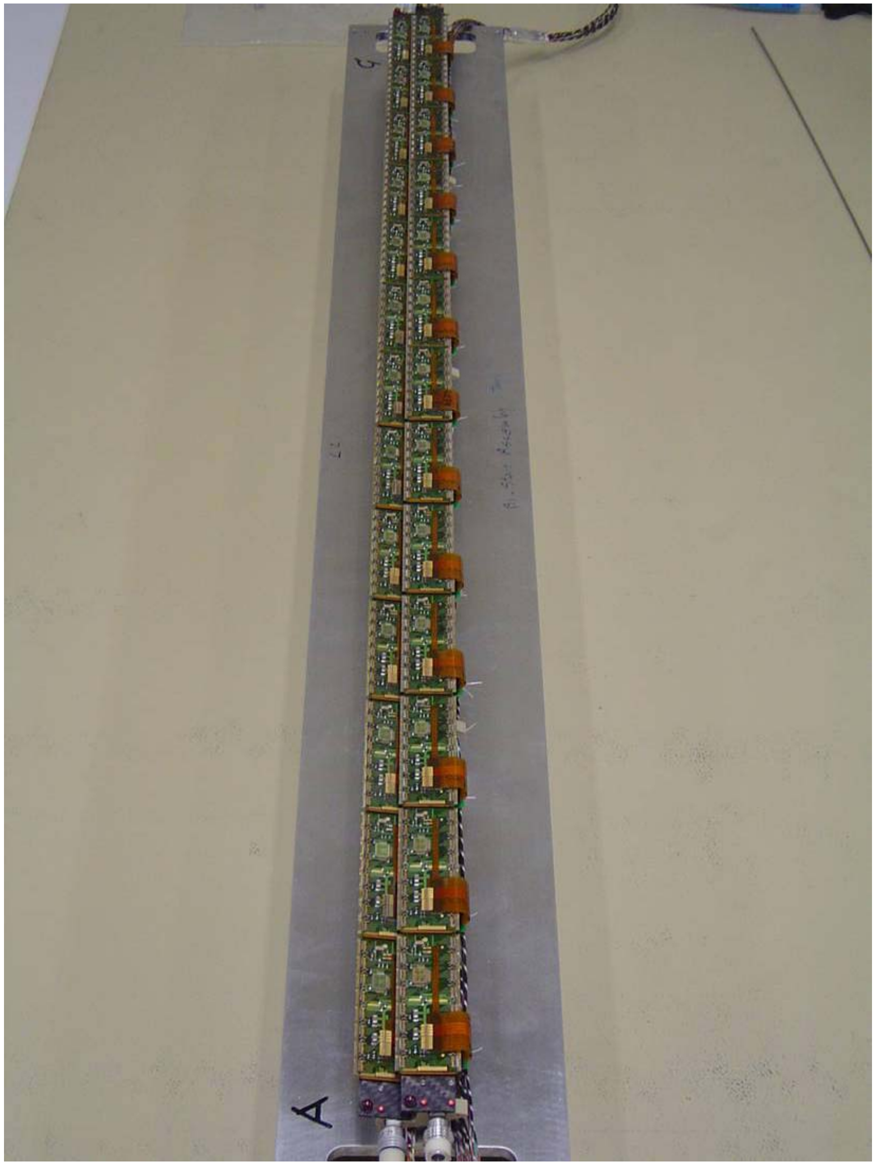


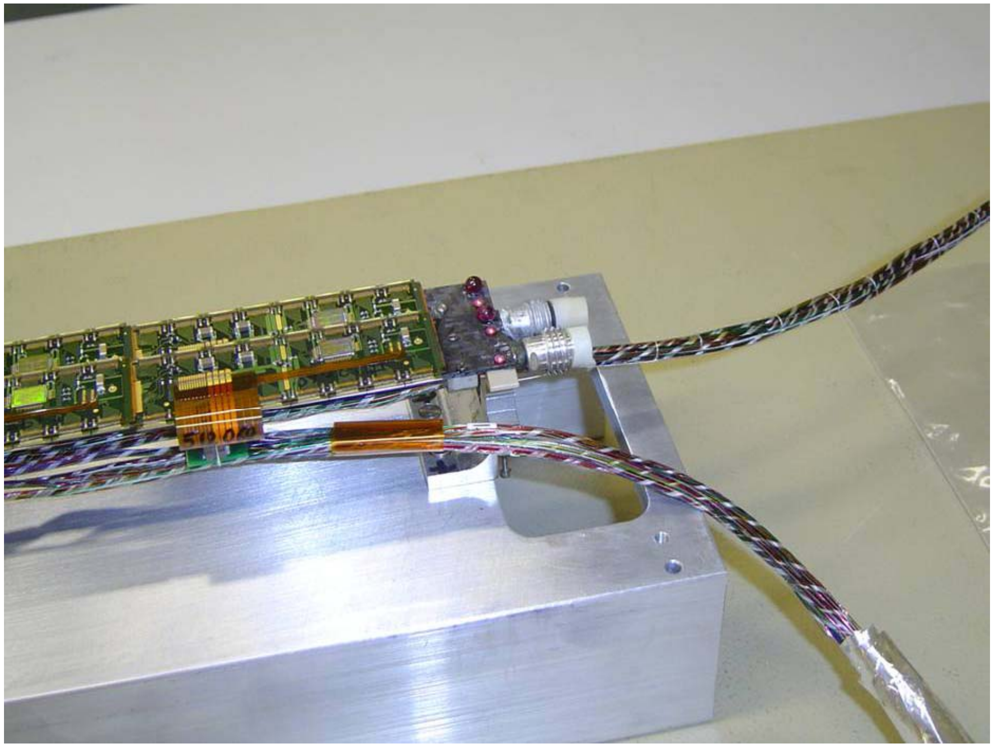
Integration (Barrel)



13 modules mounted on one stave with carbon-carbon support structure and cooling pipe

Integration (Barrel)

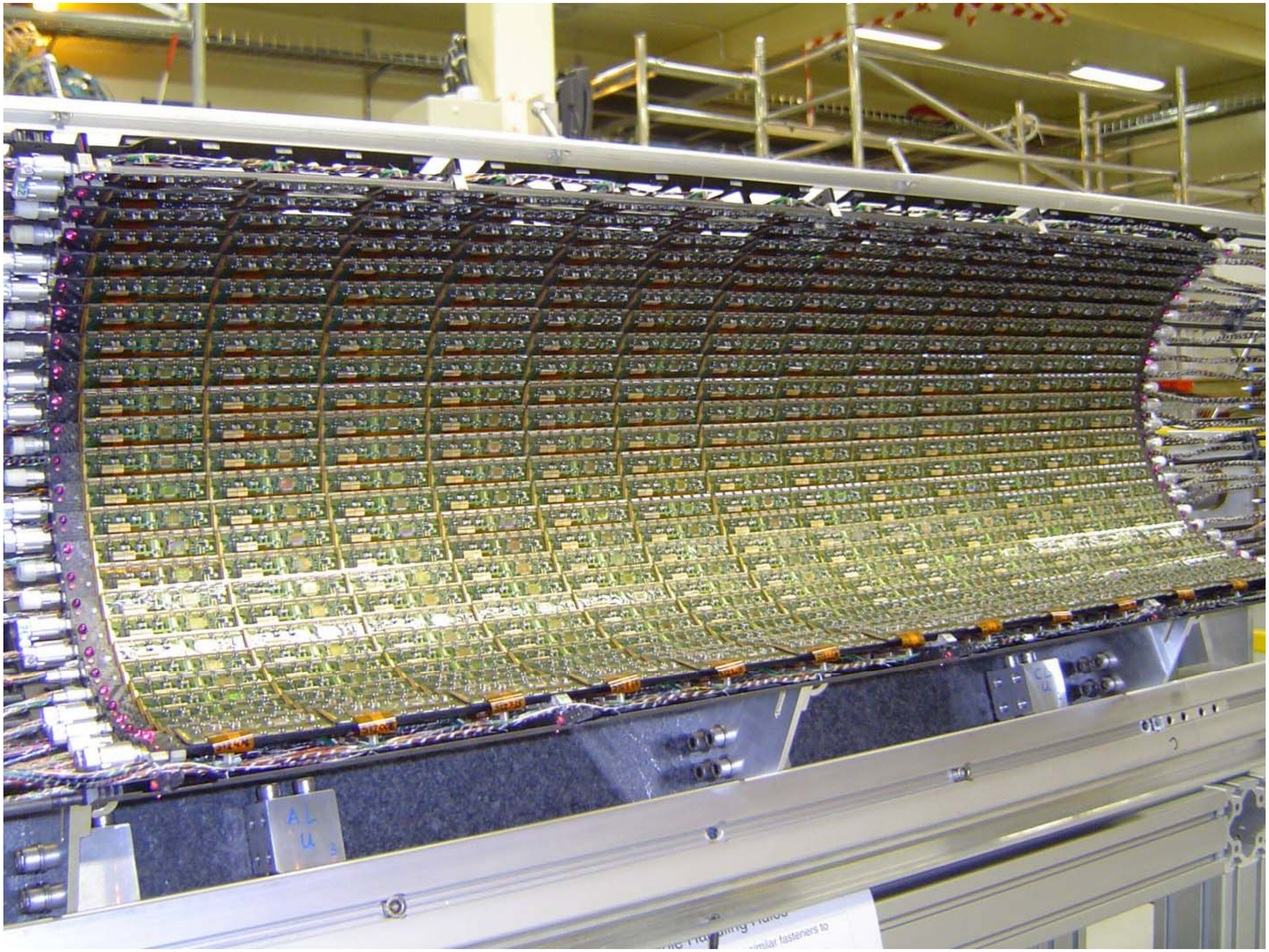




Detail with type-0 cables and cooling connections

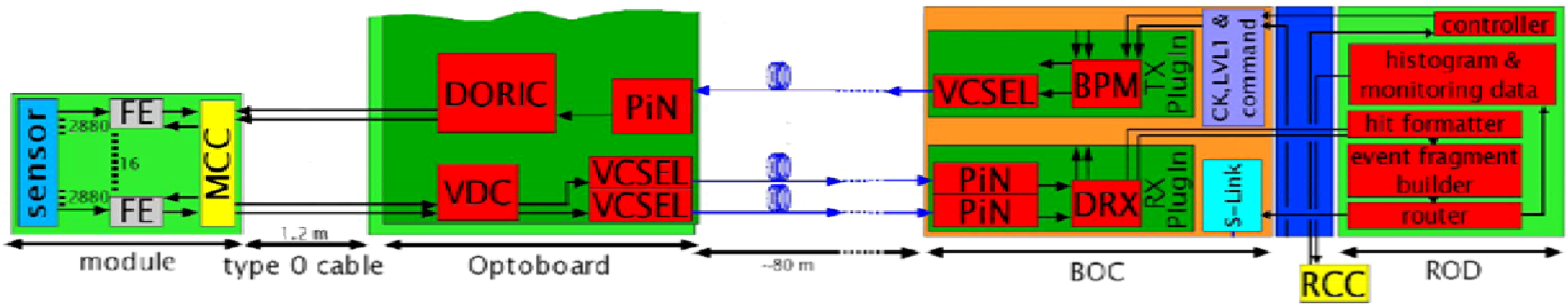
Two staves mounted to one bistave
(cooling circuit)

Integration (Barrel)



Bistaves mounted in the halfshell support structure

The Optical Link



- Data to and from the detector is transmitted over optical links
- Several parameters can be adjusted:
  - BOC Tx side:
    - Tx mark-space-ratio
    - Tx laser current
  - Optoboard:
    - (Fixed) supply voltages VVDC and VPin
    - Control voltage VISet (determines laser power of all optoboard channels)
  - BOC Rx-side:
    - Rx delay
    - Rx threshold

Detector "Partitioning"

- 1744 Modules

- 6 or 7 modules are connected to 1 PP0
  - The 6 or 7 modules connected to the same PP0 are usually referred to as "PP0 X"
  - X is the geographical name of this PP0, which is composed of layer/disc #, bistave/bisector #, stave/disc number, half-stave #, e.g.:
    - L1_B10_S2_C6 for a 6-module half-stave in the barrel
    - L1_B10_S2_A7 for a 7-module half-stave in the barrel
    - D3C_B01_S1 for a disc sector
  - A module is "adressed" by adding its number to the PP0 (e.g. L1_B10_S2_C6_M1C)

- Four barrel PP0s (2 staves = 26 modules) or 2 disc PP0s (2 sectors = 12 modules) share one cooling loop

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- Pixel Detector Services
- Operating Conditions
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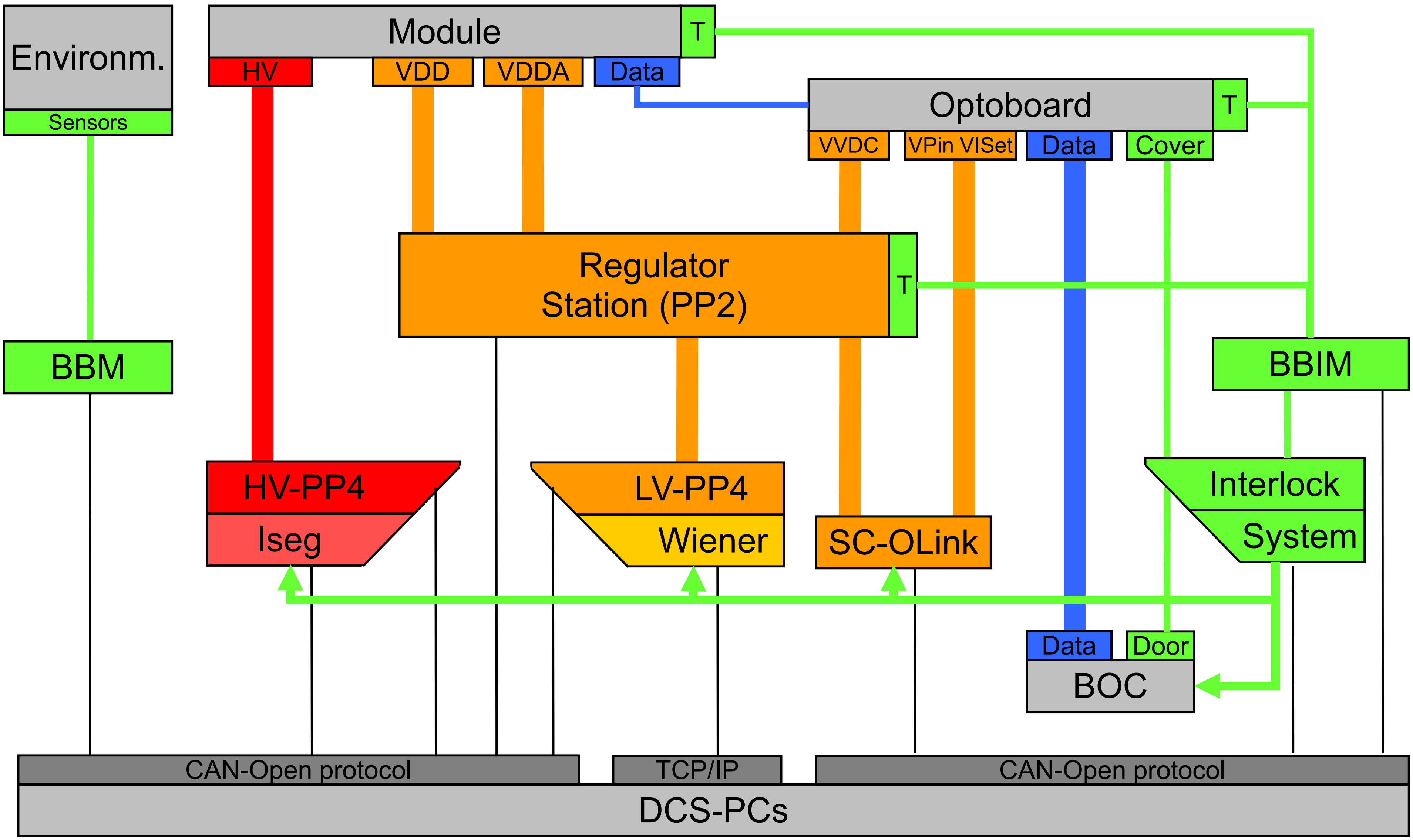
Services Requirements

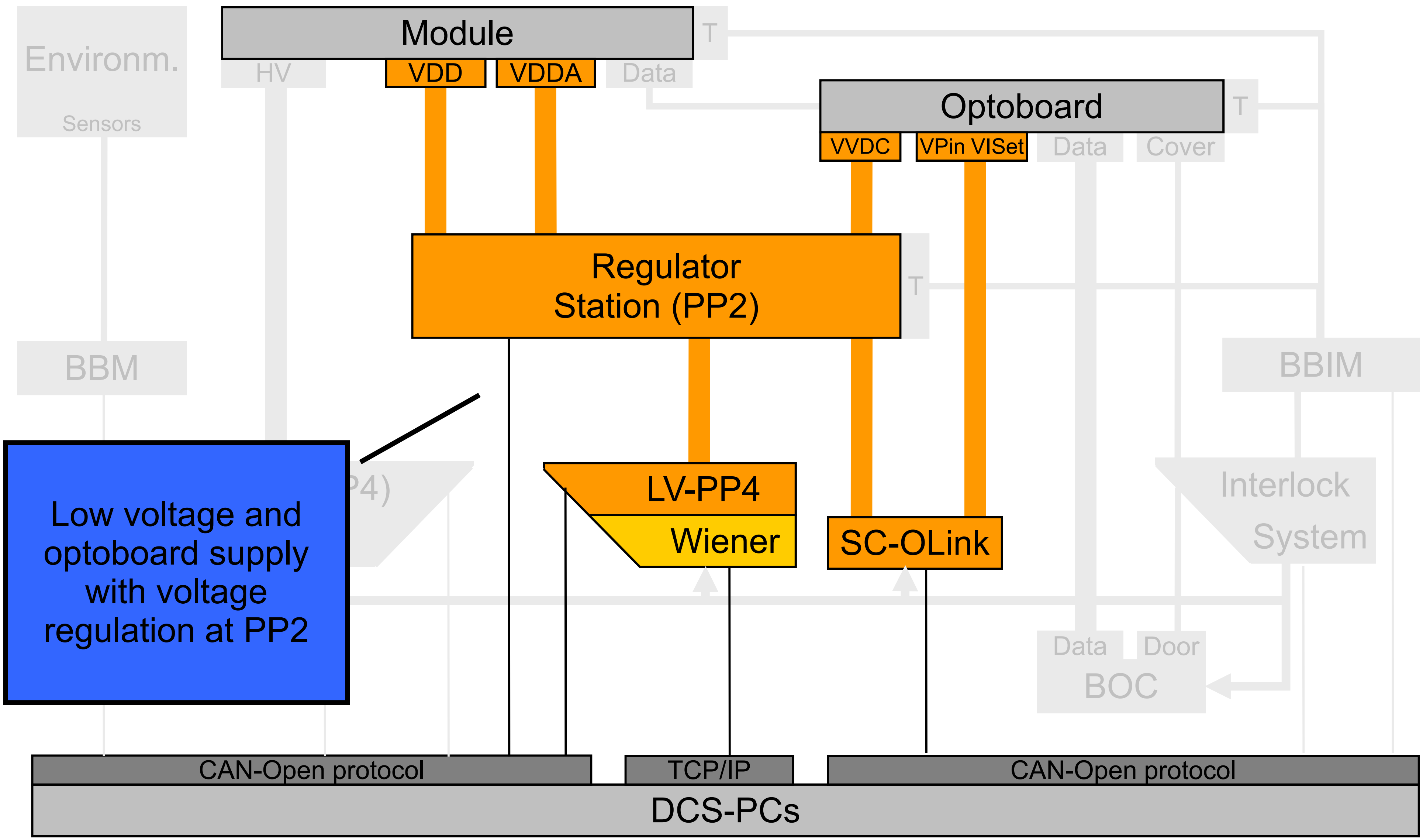
- Each module:
  - 1 sensor bias voltage (now 150 V, higher after irradiation)
  - 1 digital voltage (2.0 – 2.1 V) for FE chips and MCC
  - 1 analogue voltage (1.6 – 1.7 V) for FE chips
  - 1 NTC connection

- Each optoboard (1 per 6/7 modules):
  - 1 "high-current" (250 mA) voltage for the VCSEL driver chip (needs regulation)
  - Several low-current voltages (not regulated):
    - Bias voltage VPin for pin diode
    - Control voltage VISet to regulate light output of on-detector lasers
    - Reset signal
  - 1 NTC connection

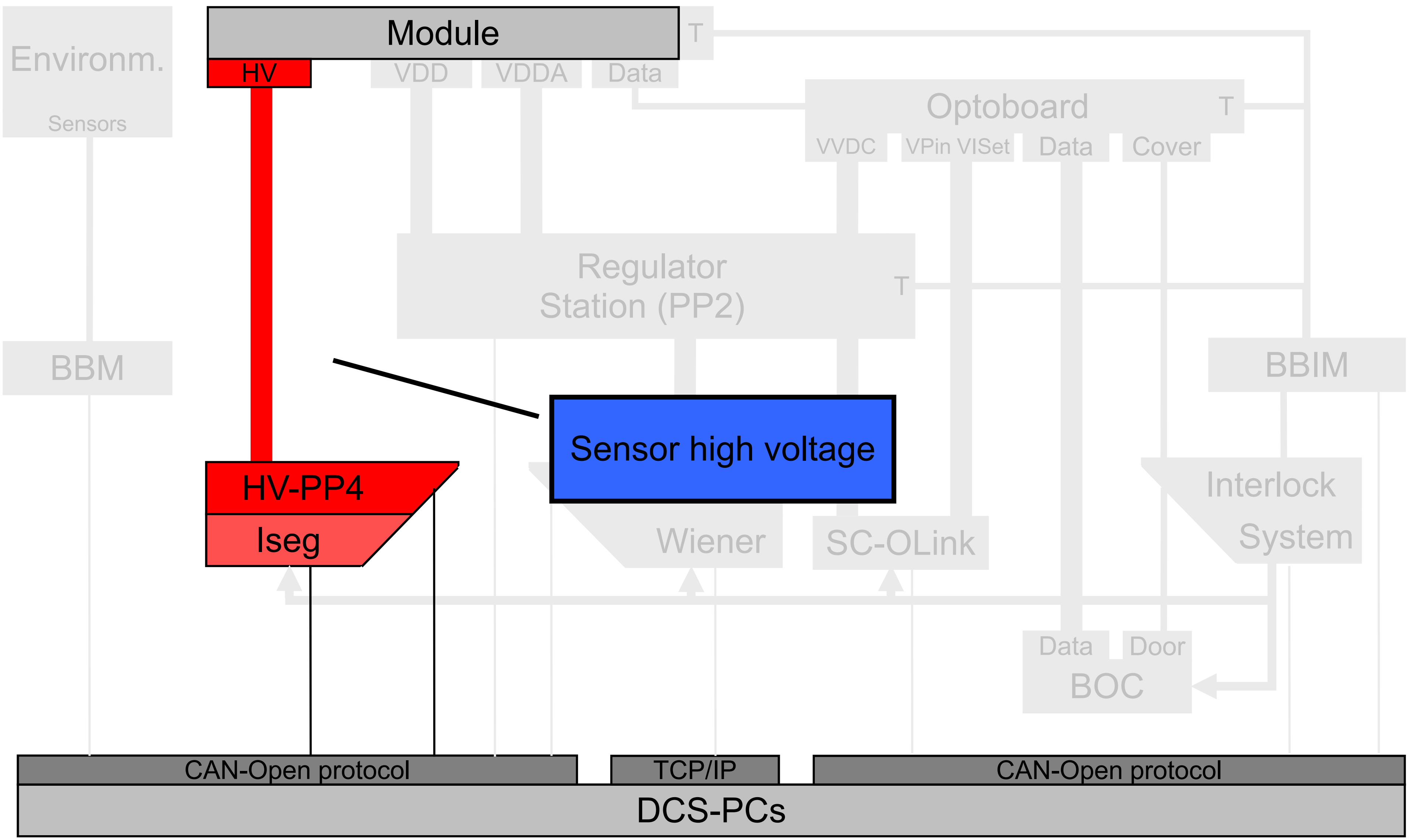
Services Setup



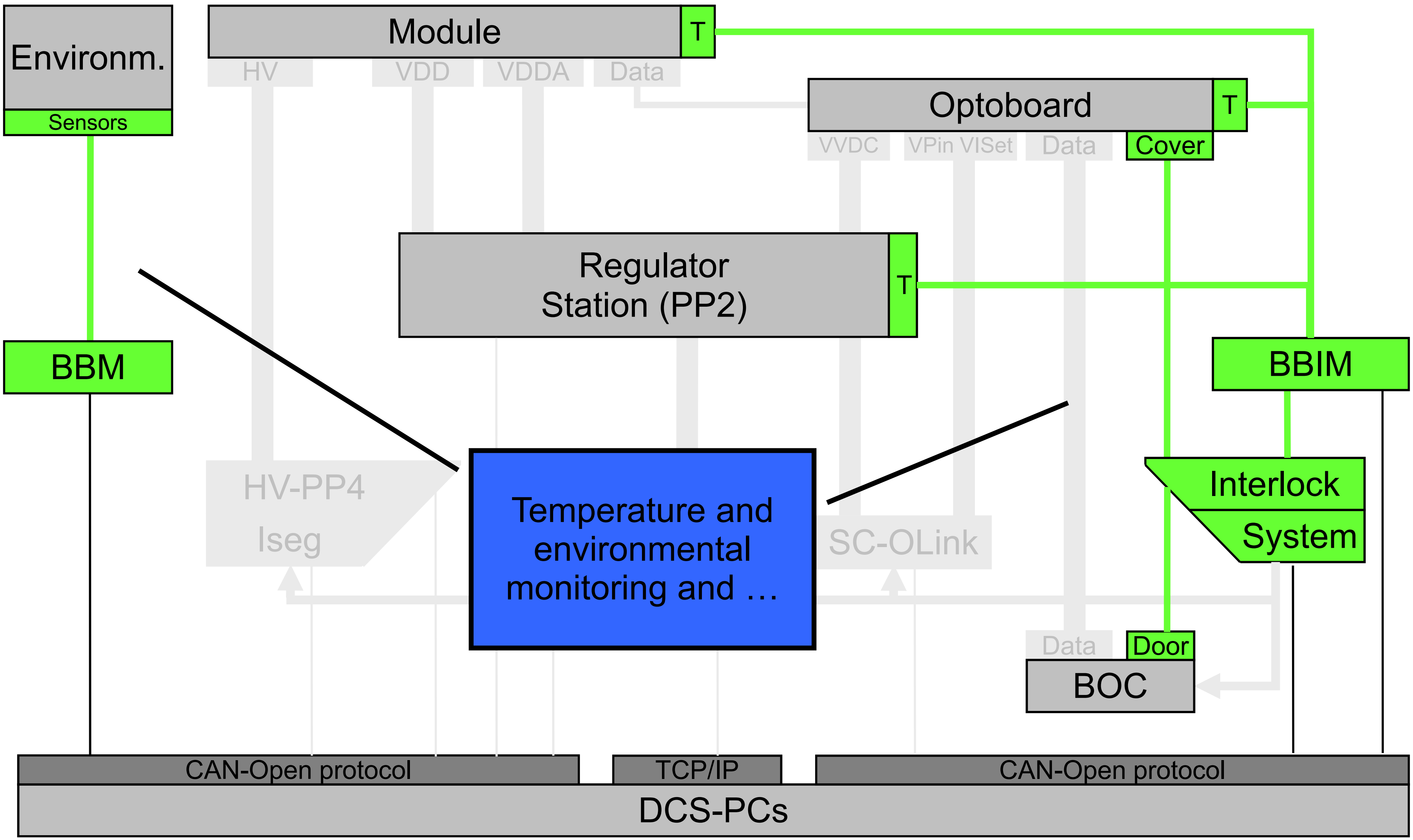
Services Setup



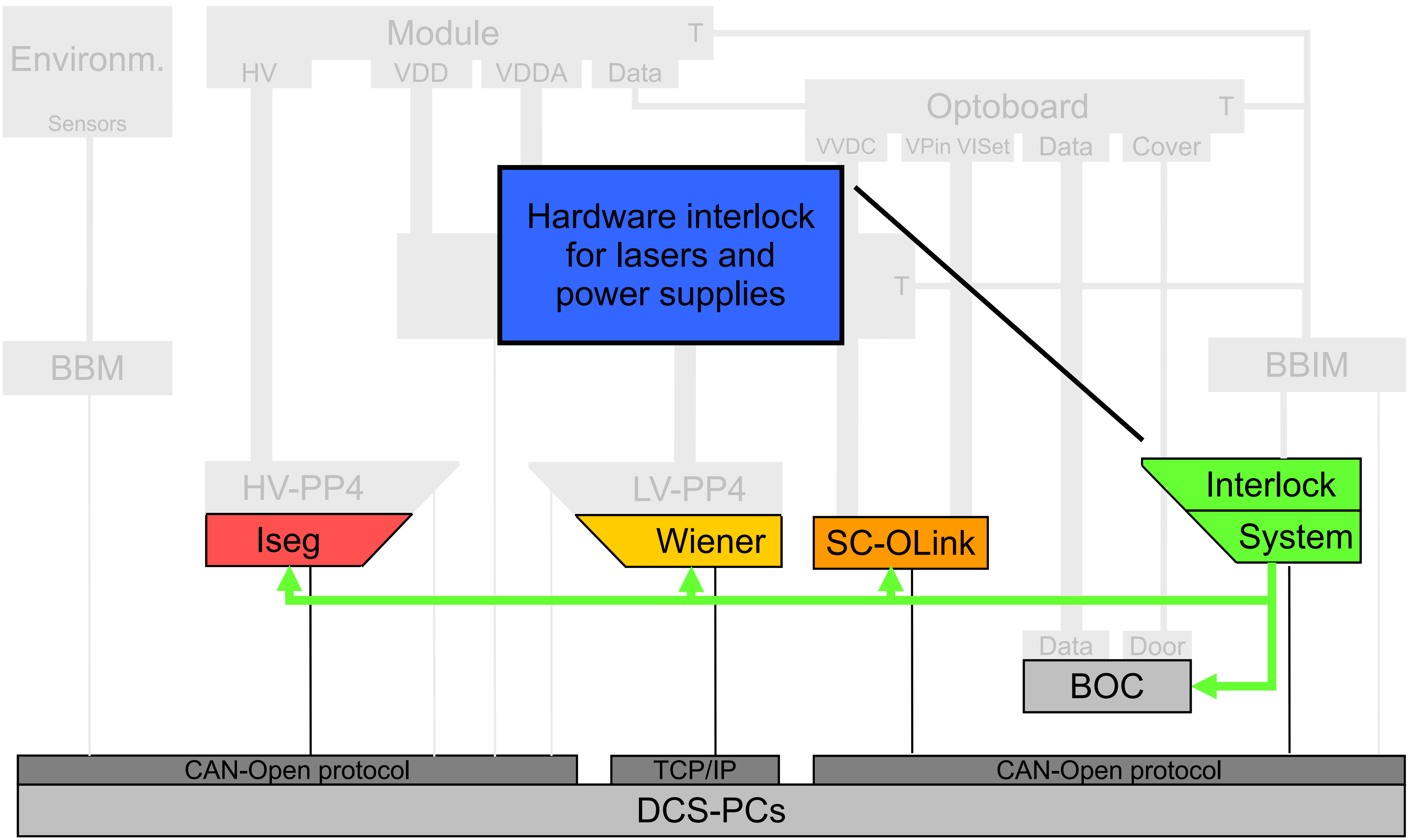
Services Setup



Services Setup



Services Setup



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Typical Operating Conditions

	Voltage	Current
VDD	2.1 V (Barrel) 2.0 V (Discs)	Unconfigured: ~350 mA Configured: ~700 mA
VDDA	1.7 V (Barrel) 1.6 V (Discs)	Unconfigured: ~80 mA Configured: ~1.2 A
HV	150 V	O(μA)

- Few remarks:
  - It looks like the digital current for an unconfigured, cold module can increase above the value given here (400-500 mA)
  - Note: Power of a configured module ~4 W (on only 12 cm^2)!
    - Will increase up to ~6 W with irradiation

Consequences of Power Dissipation

- Modules and optoboards need to be cooled when switched on / configured
- Several interlock layers to prevent damage:
  - Hardware interlock switches off power supply channels when modules or opto board temperature get too hot
    - Shooting points: 40 deg C (for modules and opto boards)
    - Switches off entire PP0 of the concerned module
  - Software interlock should switch off before from the FSM in a more controlled way and avoid that the hardware interlock temperature is reached.
    - Shooting points: 37 deg C (modules and opto boards)
    - Switches off entire PP0 of the concerned module
    - Note: Temperature is sampled every ~5 sec → if temperature rises fast hardware interlock can trip before software interlock reacts.
  - Additional interlock ("cooling script") switches off PP0s when cooling is lost. Without cooling PP0s cannot be switched on.
- Switching on and off means thermal cycling of the modules
- Optoboard special:
  - It was found out that the optoboards behave better at higher temperatures. Therefore heaters were added to keep the optoboards at a controlled temperature (20 deg C)

Not-so-typical Operating Conditions

- Module does not get clocked correctly
  - Digital current will decrease (< 300 mA unconfigured, < 600 mA configured)
  - Possible solution: Reset opto board
- Module is noisy
  - Noise hits will lead to an increase of the digital current of the module (> 1 A)
  - Check that HV is on, otherwise solutions need DAQ intervention (increase of threshold or masking of noisy pixels)
- Tx Laser switched off (e.g. during an Inlink scan)
  - Doric chip on the optoboard will try to adapt (which in this case means lower) the threshold and will trigger on noise
  - Data sent to the module (and if module is on and configured also its current consumption will be random → Do not do this when modules are switched on!

- No Cooling
  - In this situation a configured or even an unconfigured, but powered module will immediately go up to the temperature threshold and get interlocked
    → Do not switch on or even configure modules without cooling unless you really know what you are doing (expert only)!

One More Interlock…

- Worry:
  - Beam accidents could lead to a very high local charge deposition in the sensors, which would be high enough to locally short circuit the sensor high voltage and thus permanently damage the corresponding FE cells.

- Precaution:
  - Interlock high voltage with the stable-beam signal

- Pixel-LHC-Interlock:
  - Switching on the high voltage is only allowed when “beam stable” signal is ON.
  - Beam injection is “interlocked” as long as pixel high voltage is on

  - Beam stable interlock can be masked (for beam-off periods), but risky (=expert) operation; timeouts have been implemented to keep risk of erroneous masking to a minimum

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Basic Calibration Measurements

- This gives an overview over the most important calibration measurements.
- A more complete set of description is available from the pixel detector wiki
  - `https://twiki.cern.ch/twiki/bin/view/Atlas/CalibrationDescription`
- Or in the calibration document, available on the pixel detector wiki
  - https://twiki.cern.ch/twiki/bin/view/Atlas/PixelDetectorGroup

Basic Calibration Measurements

- Calibration means: Tuning and Calibration, i.e.
  - Determining the best operation parameters for the different parts of the detector (mainly optolink and FE chips) to satisfy the requirements
  - Do measurements to understand the exact behaviour of the detector and the readout (for control, monitoring, as input to simulations etc)

Requirements?

- Main requirement: Detect very small charges, very reliably and very fast

- Small charges: most probable value is 19400 e
  – Landau distribution extends also to the left of the mpv (down to ~12000e)
  – Particles can pass through the border of two pixels (worst case: divide by 2)
  – Collected charge will decrease with radiation damage
  → We are aiming for 6000 e now, less later

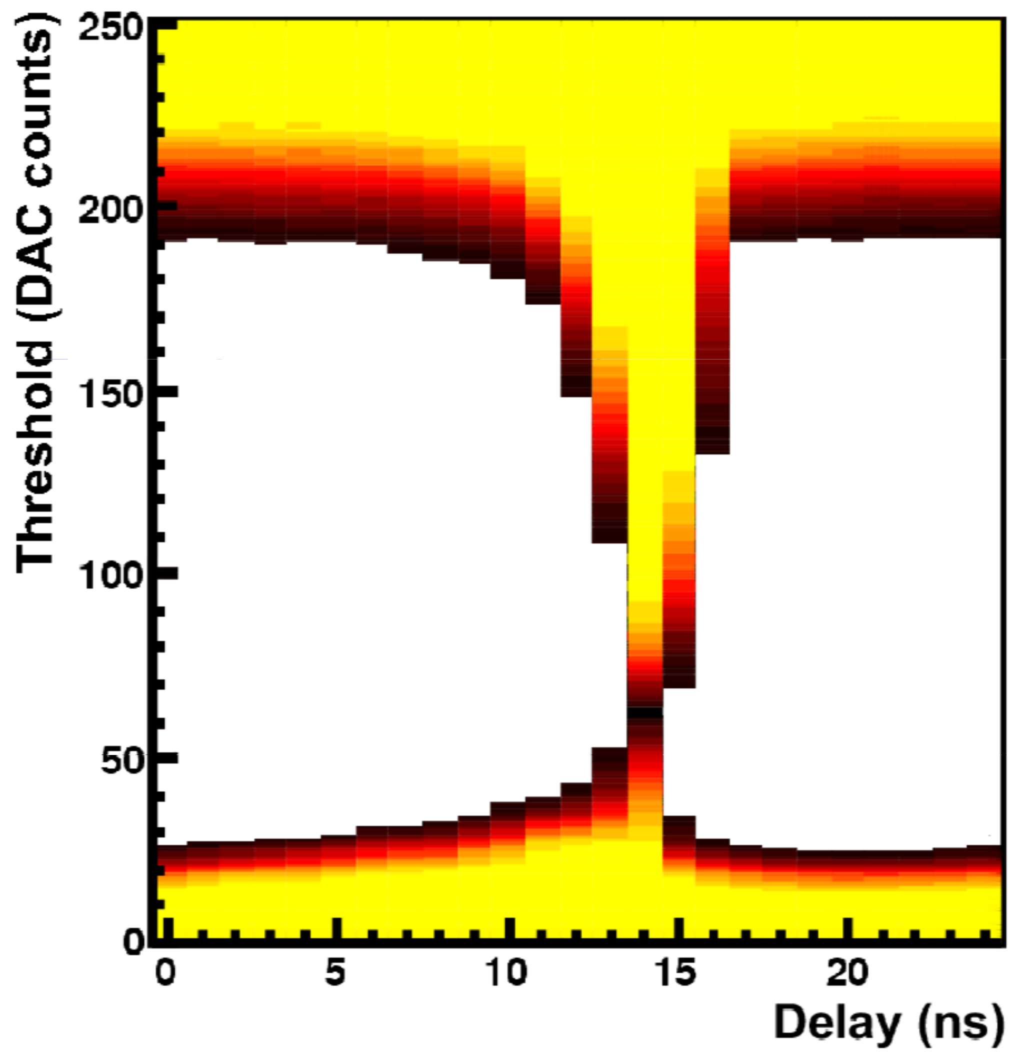
- Very reliably: Particle signals have to be efficiently distinguished from noise
  – If the nominal threshold is *X*, then the sum of it's error and the noise should be "far enough" away, to reduce the number of noise hits:

$$X \geq k \cdot \sqrt{noise^2 + thr.disp.^2}$$

- Very fast: charges have to be attributed to the correct bunch crossing
  – Error off the detection time has to be less than 25 (20) ns
  – Problem: Large charges are detected faster than small charges
  → The smallest charge, that is not only above threshold but has also a "timewalk" of less than 20 ns, should be less than 6000 e

Scans and Tuning of Optical Links

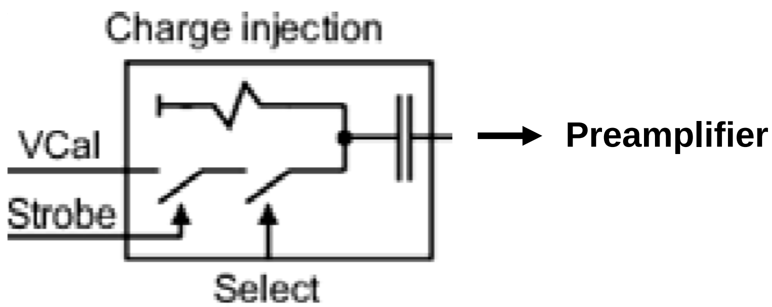
- Incoming data stream is sampled and digitised in the back-of-crate cards
- (Main) free parameters:
  - Sampling point (Rx delay)
  - Threshold 0/1
- Physical picture translates into 2D-scan, where we measure the bit-failure-rate
- Opto-tuning means choosing the correct operation point in this parameter space
- Additional parameter:
  - VISet (laser power, common to full optoboard)
  - There are several more…



Charge Injections

- Most of the module calibrations use charge injections over an injection capacitor to simulate charges deposited by particles

- A digital pulse issued from the MCC determines the timing of the charge injection, the pulse height of the resulting voltage step is chosen by a DAC in each FE chip



- Parameters:
  – Length and Delay (units of clock cycles): set in the MCC
  – Fine Delay (sub-clock-cycle): set in the MCC
  – Pulse height: set by FE DAC VCAL
  – Injection capacitance/conversion VCAL units to charge: production parameter, available in configuration data
  – Each single pixel can be selected / deselected for injection

Mask Staging

- Not all pixels of a module / FE chip can be scanned at the same time (occupancy would be too high for readout chip)
  - Use the possibility that each single pixel can be enabled/disabled (masked) for injection and for readout
  - Load a mask that enables only a limited number of pixels (usually 90 / FE chip) distributed over the whole chip
  - Stage this mask, such that after a limited number of mask stages (32) each pixel has been scanned once

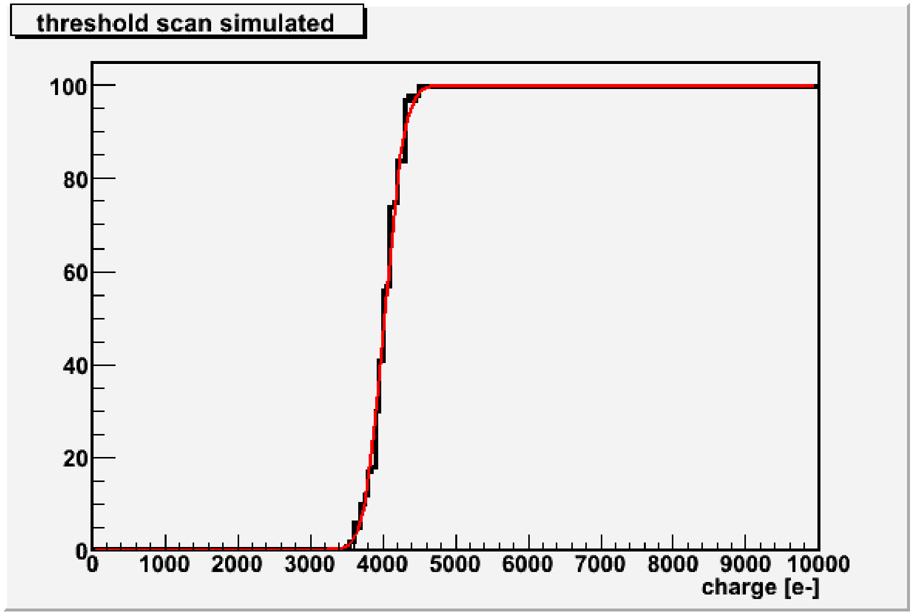
Digital and Analogue Scan

- Digital Scan:
  - Inject digital pulses into the pixel cell after the discriminator
  - Read out the hits and compare number of hits in each pixel with the number of injections
  - Checks the complete read out chain, starting in the single pixel cell

- Analogue Scan:
  - Inject test charges into the preamplifier
  - Count number of hits + evaluate TOT information
  - Checks functioning of the analogue parts of each pixel and (for a suitable test charge, e.g. 1 mip) can give an indication of the quality of the TOT tuning

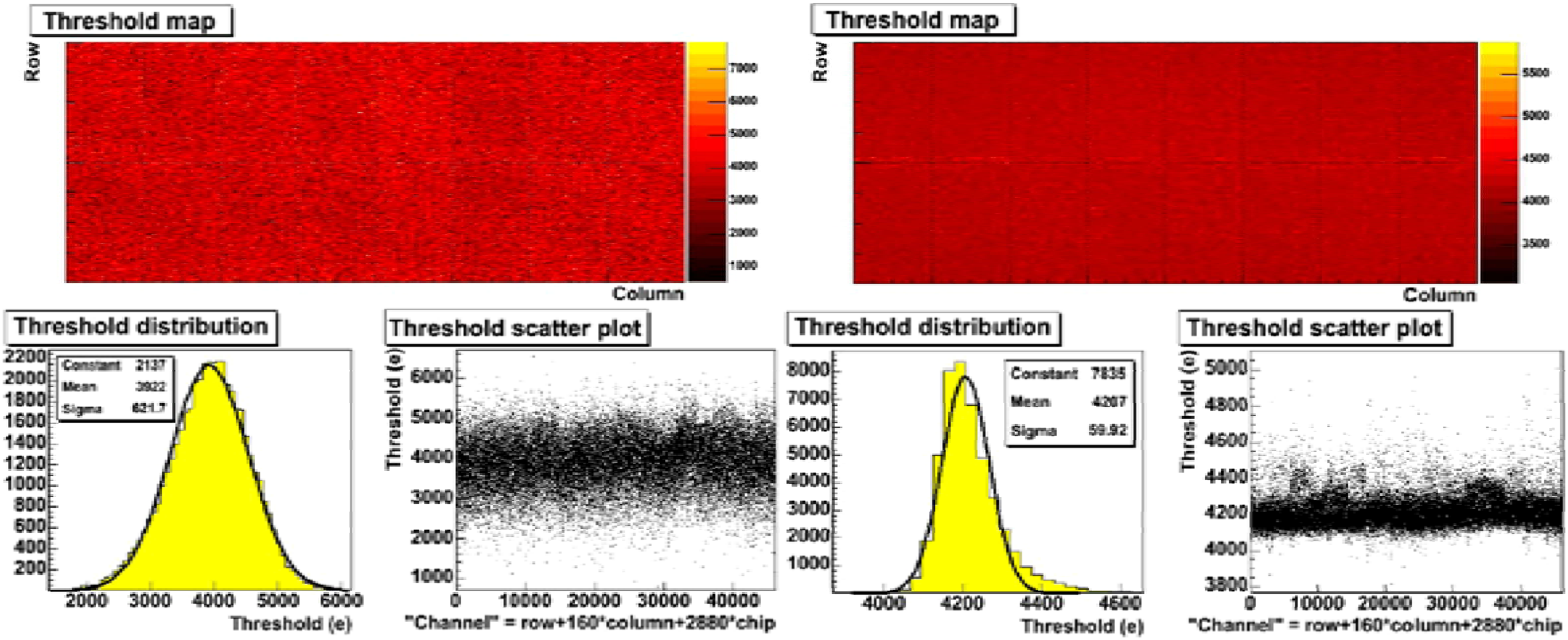
Threshold Scans and Tuning

- Threshold Scan:
  - Do test injections into each pixel looping over the injected charge
  - Measure response (hits/injections)
  - Response function: convolution of step function and noise
    → error function
  - Fit gives threshold and noise value



- Threshold tuning:
  - Threshold is determined by one GDAC per FE and one TDAC per pixel
  - Tuning chooses the pixel DACs such that the thresholds are homogeneous among the pixels and close to the desired threshold (typically 4000e)
  - Procedure similar to the scan, but keeping the charge fixed and varying the DAC setting

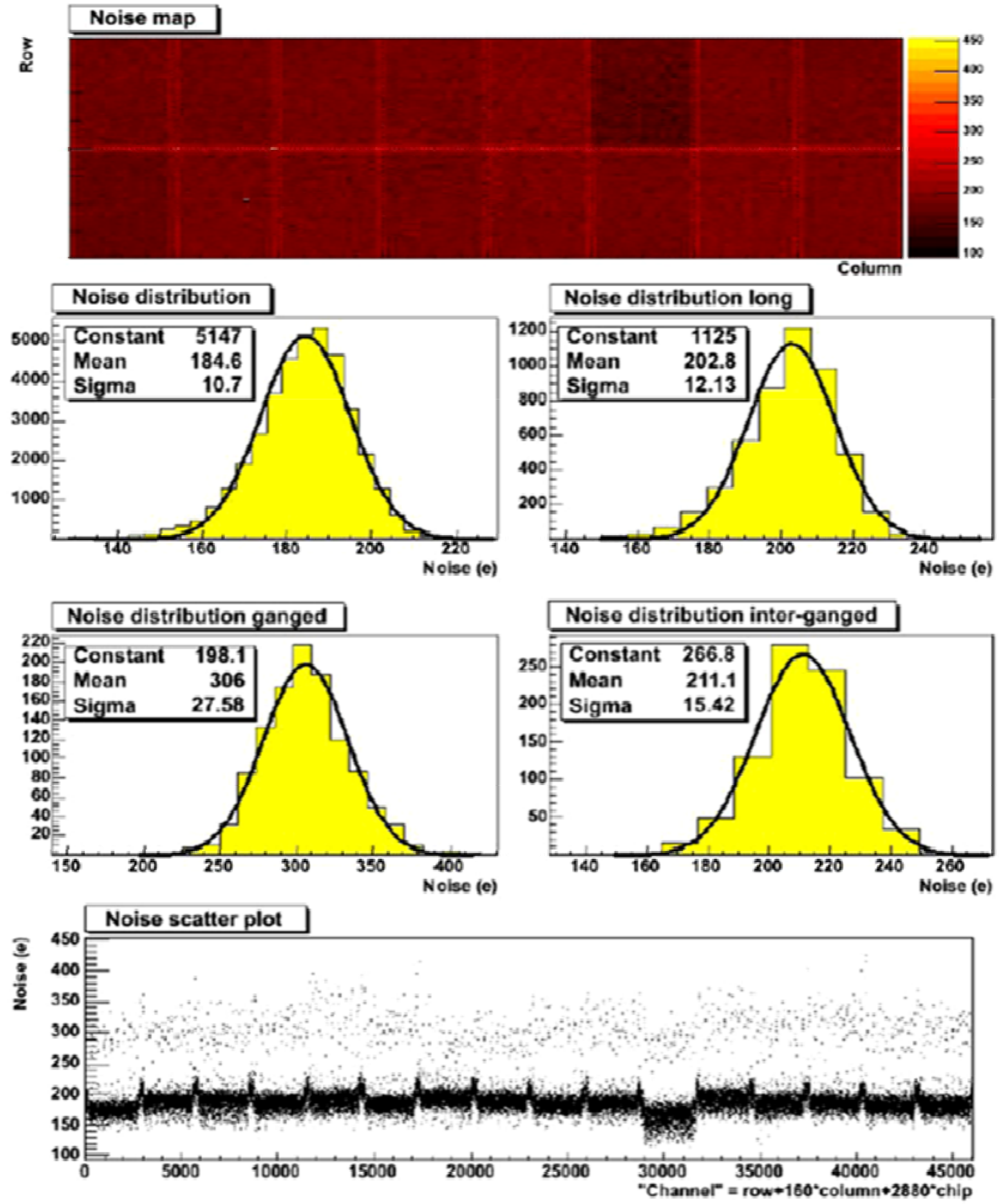
Threshold Distribution (Example)



- Untuned (left) and tuned (right) threshold distribution
- Typical values:
  - Threshold dispersion: 600 e (untuned), 50 e or better (tuned)
  - Operating threshold (i.e. tuning target value): 4000 e

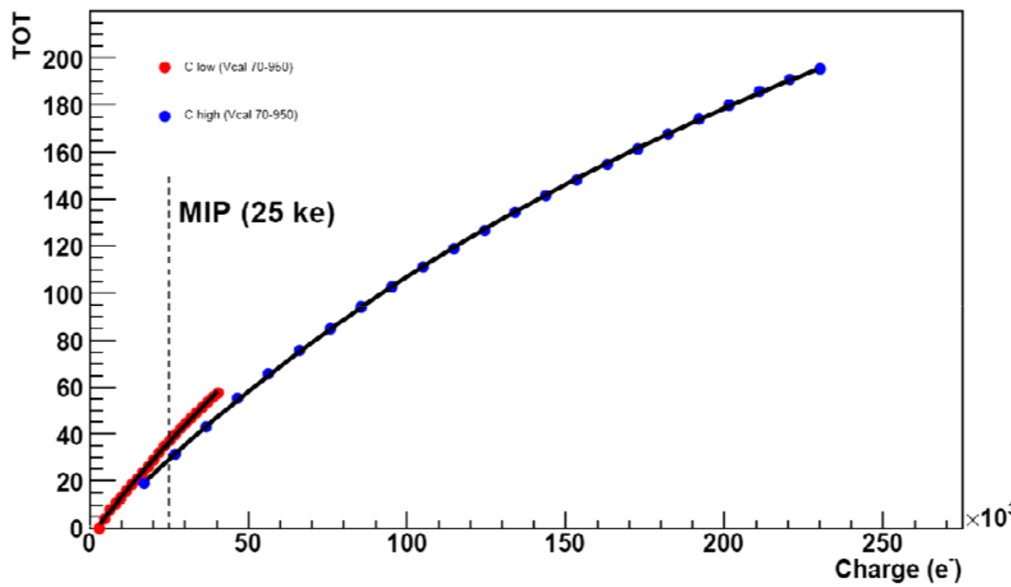
Noise Distribution (Example)

- Noise values determined from threshold scan
- Typical values:
  - 170-180 e (all pixels)
  - Special pixels higher:
    - long / inter-ganged ~200 e
    - ganged ~300 e

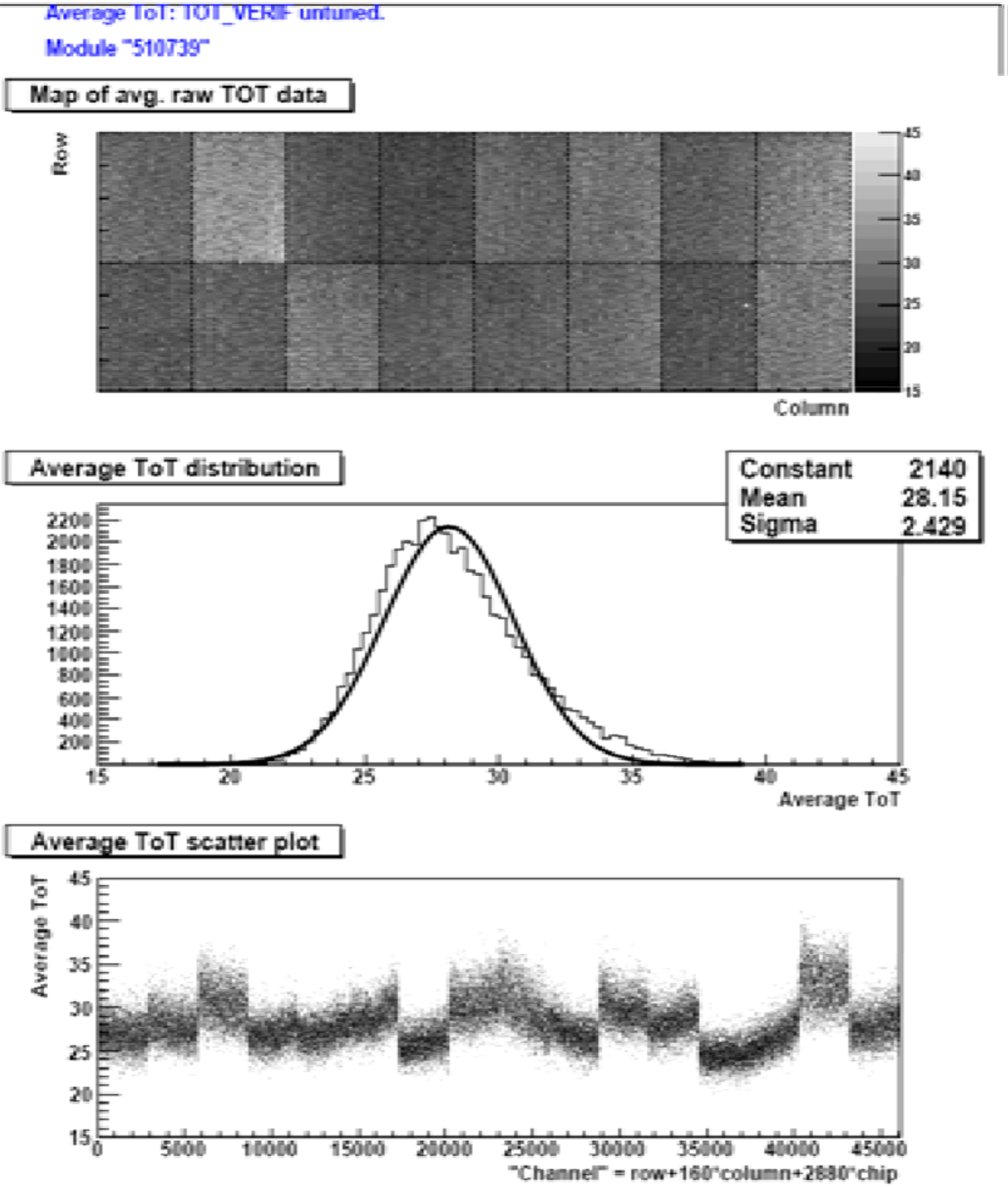


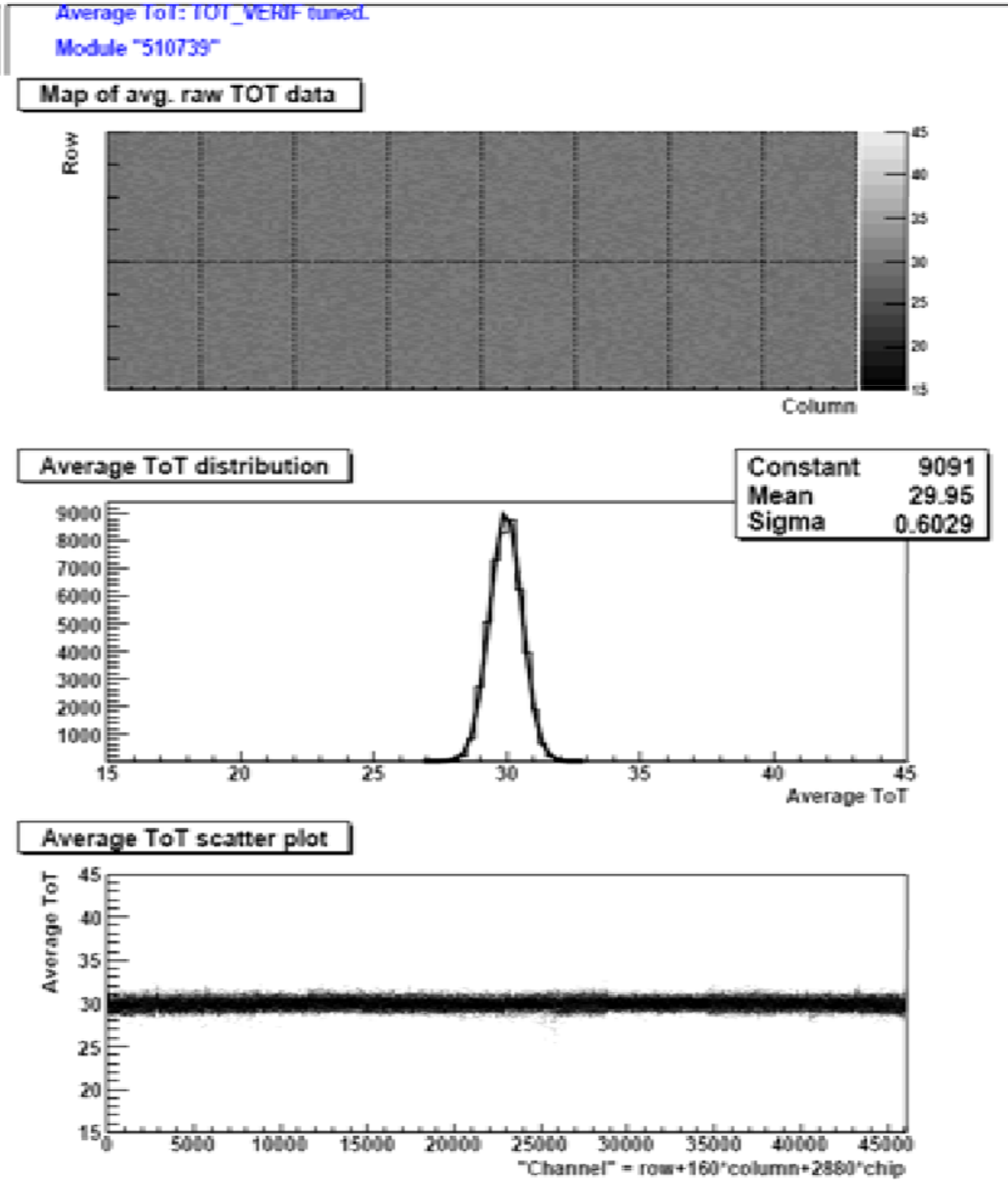
TOT Calibration

- Time over threshold gives measure for the deposited charge and is determined by the preamplifier feedback current
- To be useful in the offline reconstruction:
  - Response has to be homogeneous
  - TOT vs. charge has to be calibrated
- Calibration:
  - Do test injections with varying charges above threshold and measure the average TOT
- Tuning:
  - Feedback current (and thereby the TOT) is determined by a global current DAC per FE chip and a DAC in each pixel (FDAC)
  - Tuning chooses the feedback current such that the TOT response is as desired (typically 30 @ 1 mip)



TOT for a module - Untuned / Tuned

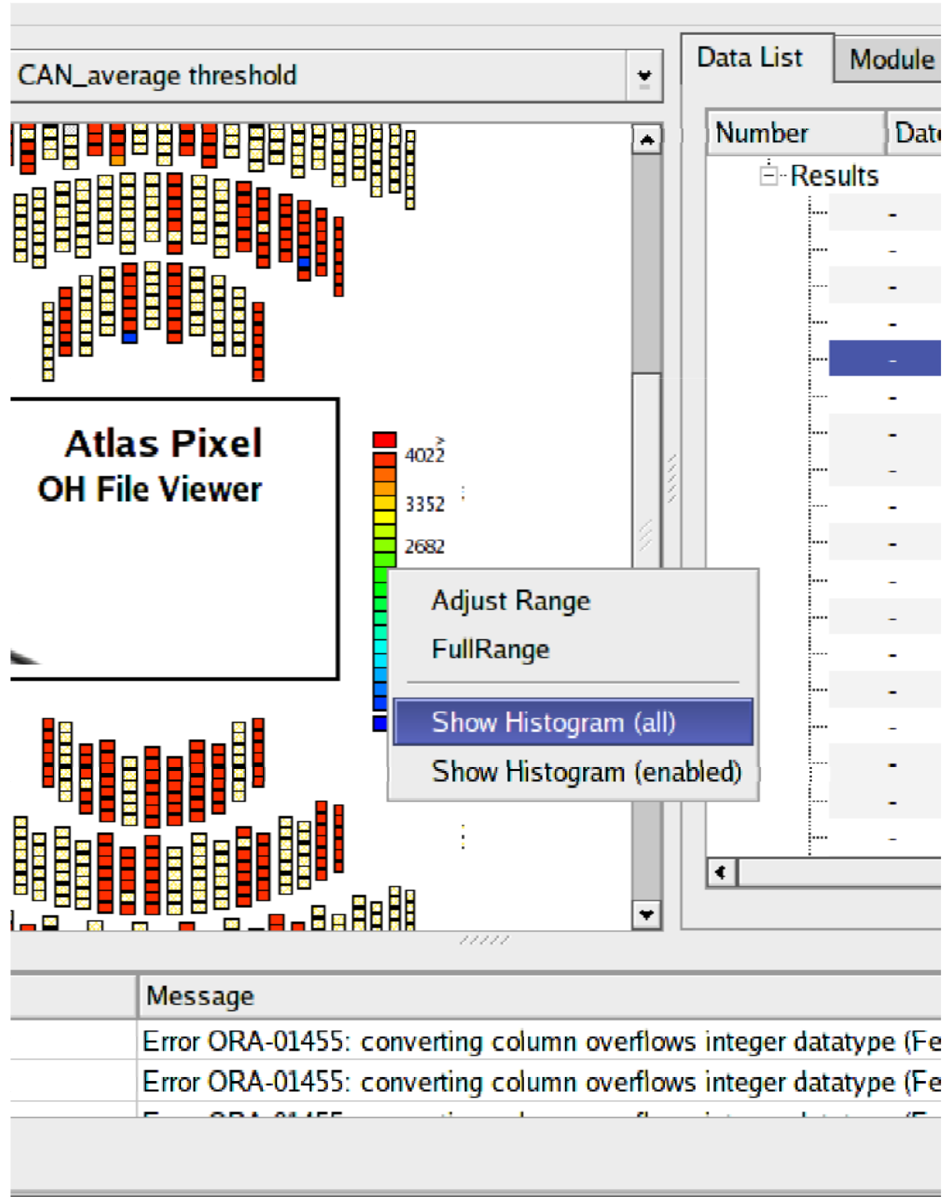




Detector Summary Histograms

- After a calibration analysis: Right-clicking on the colour scale in calibration console gives you the possibility to histogram the selected variable for the full detector (and to adjust the range)

→ Easy possibility to get a quantitative overview of the scan results



Detector Summary Histograms

- Examples for interesting module variables:

Digital Scan	Number of dead pixels Number of inefficient pixels
Analogue Scan	Number of dead / inefficient pixels Average TOT TOT Dispersion
Threshold Scan	Average Threshold Average Noise Threshold Dispersion
Inlink Scan	Pin Current
TOT Calibration	TOT and TOT Dispersion for 1 mip (not yet impl.)
…	…

"Vocabulary"

- On the modules:
  - FE: Front-end chip
  - MCC: Module controller chip
- In the readout crates:
  - BOC: Back-of-crate card
  - ROD: Readout driver
  - SBC: Single board computer
- In the services:
  - Wiener: Low voltage power supplies
  - Iseg: High voltage supplies
  - SCOLink: Power supplies for the optoboards
  - PPx: Patch panel x
    - **PP0: In the detector cryostat, contains the optoboards / often used as synonym for "all modules connected to this PP0"**
    - PP1: connection region at the ID endplate
    - **PP2: contains the low voltage regulators**
    - PP3: contains electronics for temperature measurement (BBIM), racks in the exp. cavern
    - PP4: Fan-outs for LV/HV (in the counting room racks)

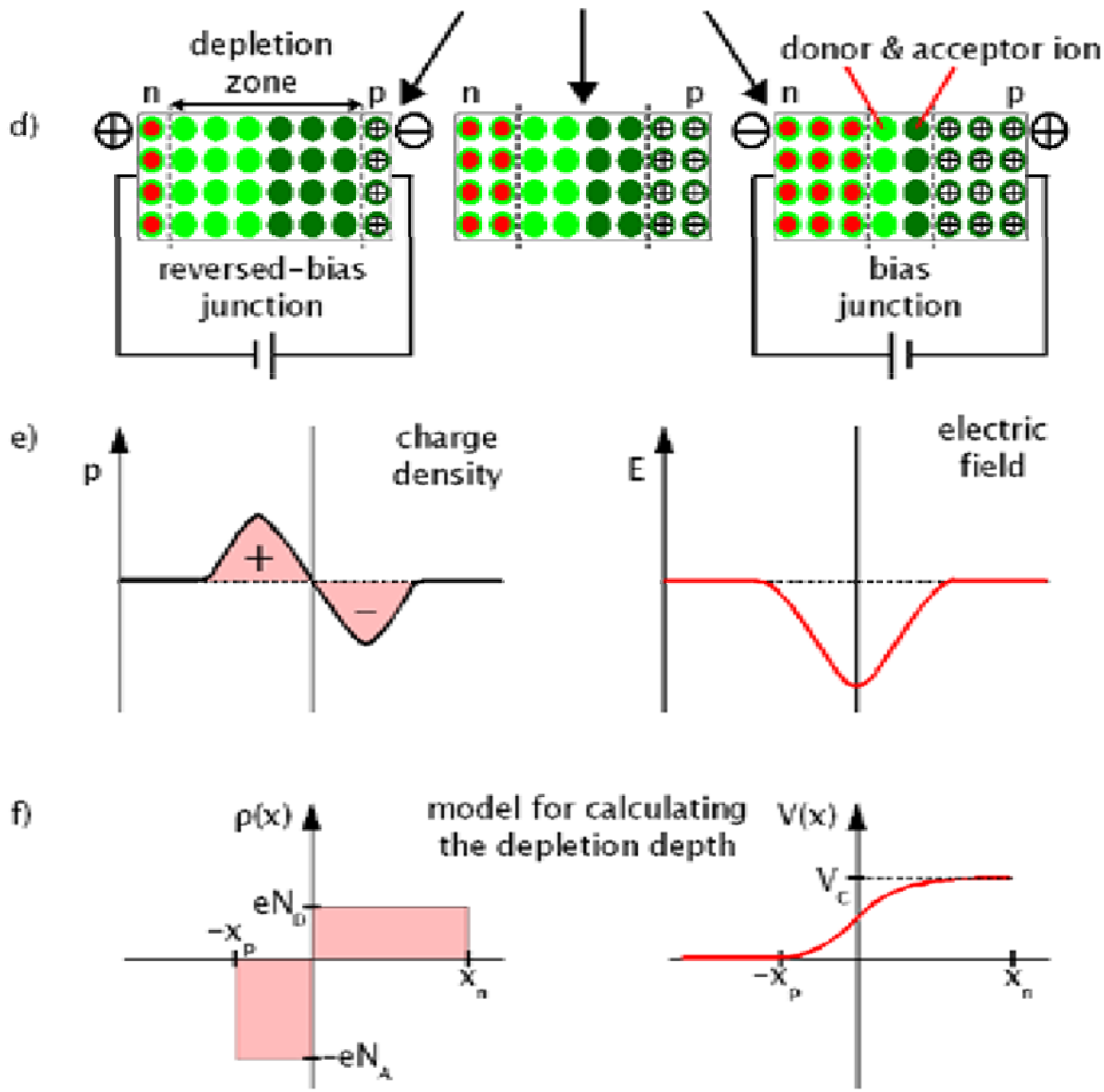
“Vocabulary”, part 2

- Voltages:
  - VDD: digital voltage for the modules (FE chips and MCC)
  - VDDA: analogue voltage for the modules (FE chips)
  - VVDC: supply voltage for the optoboards
  - VPin: Pin diode voltage for the optoboards
  - VISet: Control voltage for the optoboards (regulates light power of the Rx-link)

- Warning: This list is definitely incomplete. To be continued…

Backup ...

Pn-junction under forward- and reverse-bias



$$V_{depl} = \frac{d^2 e}{2\epsilon} \frac{N_A N_D}{(N_A + N_D)}$$

$$E(x) = -\left[\frac{V + V_{depl}}{d} - \frac{2 x V_{depl}}{d^2} \right]$$

d : thickness of detector (n layer)

x : depth in detector

$$x_n = \sqrt{\frac{2\epsilon (V_C + V_{bias})}{e N_D \left(1 + \frac{N_D}{N_A}\right)}}$$

$$x_p = \sqrt{\frac{2\epsilon (V_C + V_{bias})}{e N_A \left(1 + \frac{N_A}{N_D}\right)}}$$

ϵ : dielectric const.

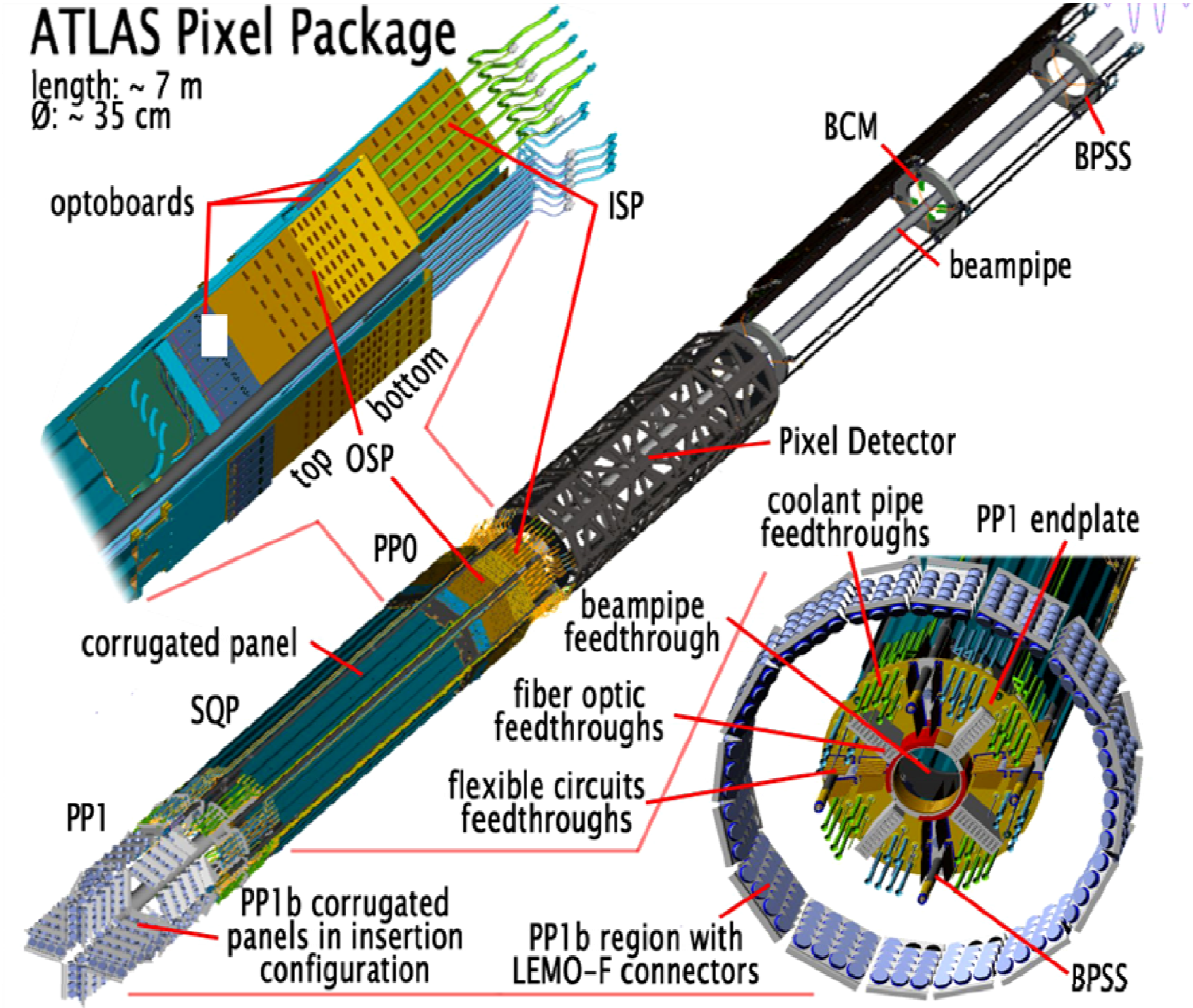
e : e^- charge

N_D : donor-

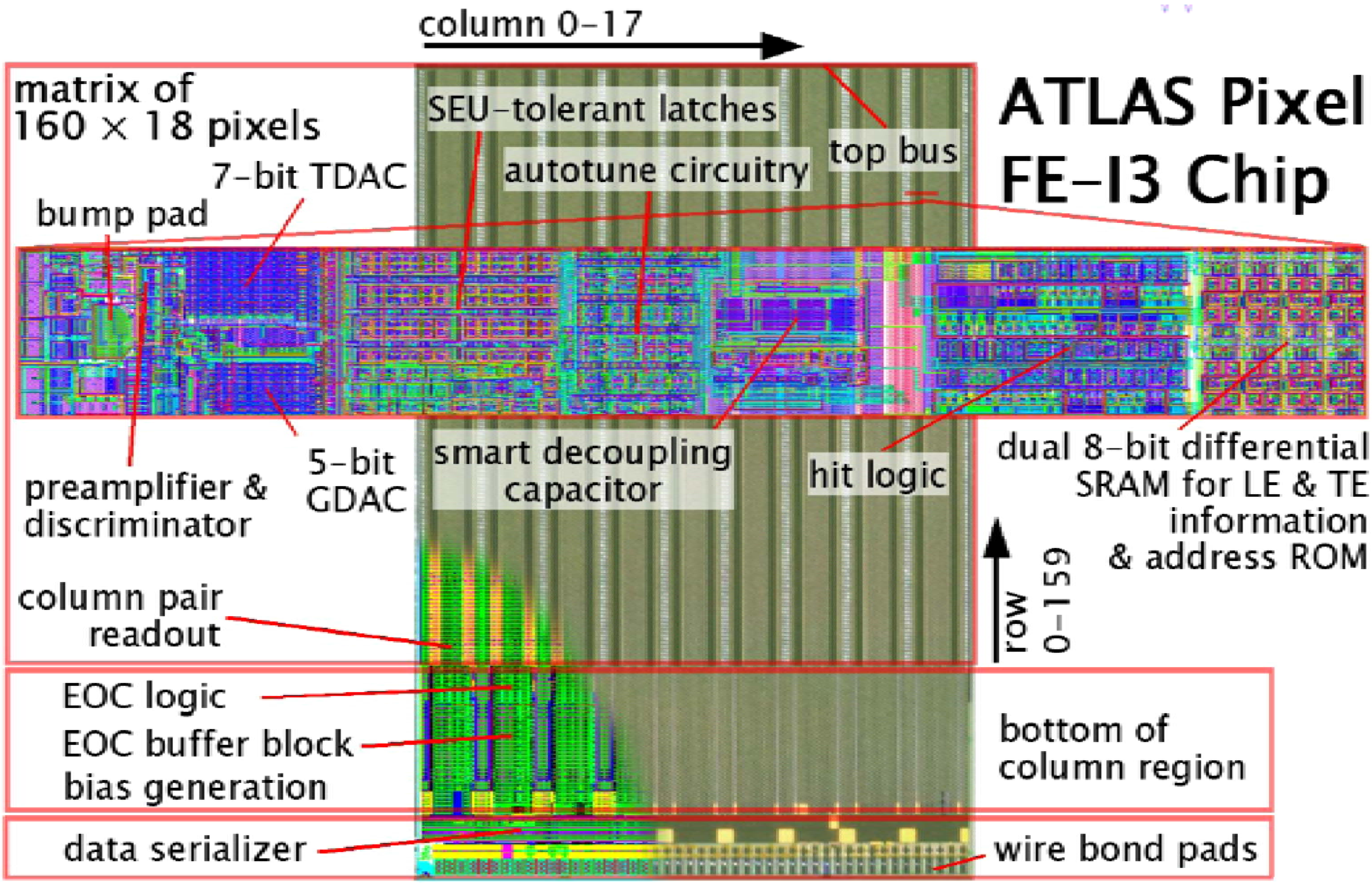
N_A : acceptor-

concentration

Pixel Package



FE-I3 Readout Chip



FE Configuration Registers