Optimisation des Capteurs CMOS pour le Dét. de Vertex

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pour DAPNIA/Saclay, LPSC/Grenoble, LPC/Clermont-F., DESY, Uni. Hamburg & IPHC/Strasbourg, coll. EUDET/JRA-1

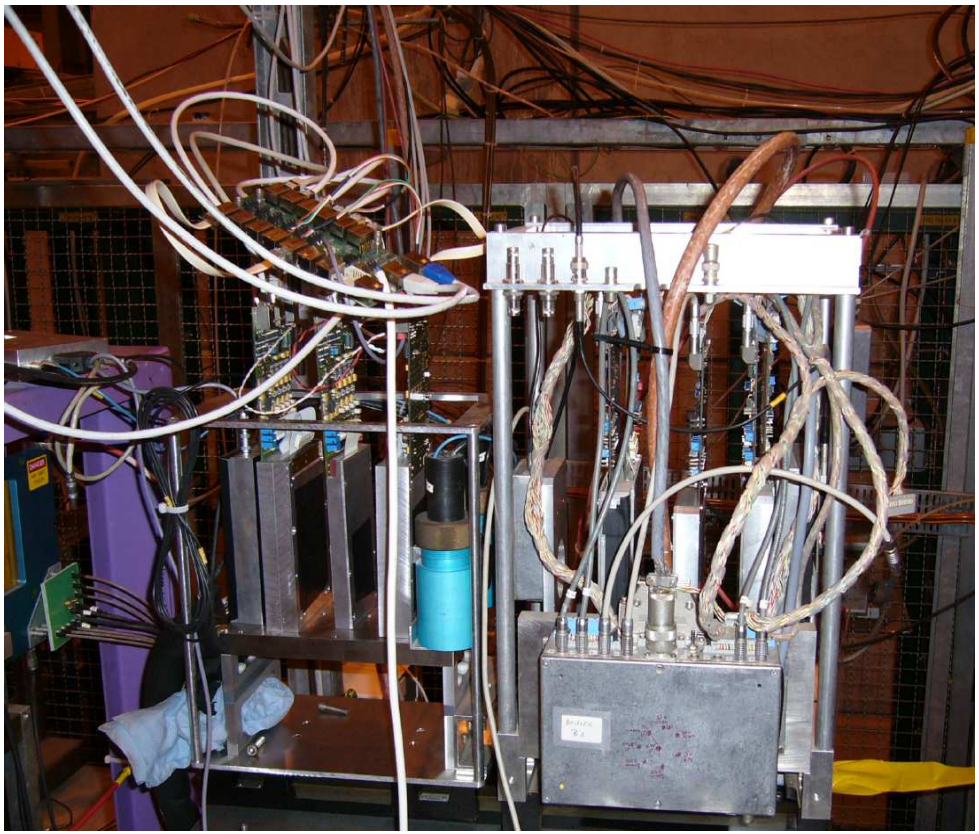
contributions de Uni. Frankfurt, GSI-Darmstadt, coll. STAR (LBNL, BNL)

PLAN

- **Progrès récents dans l'évaluation des performances génériques :**
  - *Résolution spatiale*
  - *Traces inclinées*
  - *Tolérance aux rayts*
  - *Perfo. de capteurs minces*
- **Progrès récents de la R&D de capteurs rapides :**
  - *matrices à sorties discriminées*
  - *ADC compacts*
  - *μcircuits de $\emptyset$*
  - *prochaines étapes*
- **Intégration système :**
  - *Amincissement*
  - *Concept d'échelle*
  - *CMOS / diamant*
- **Avancées des projets annexes :**
  - *Télescope EUDET*
  - *Télescope TAPI*
  - *STAR-HFT*
- **Résumé**

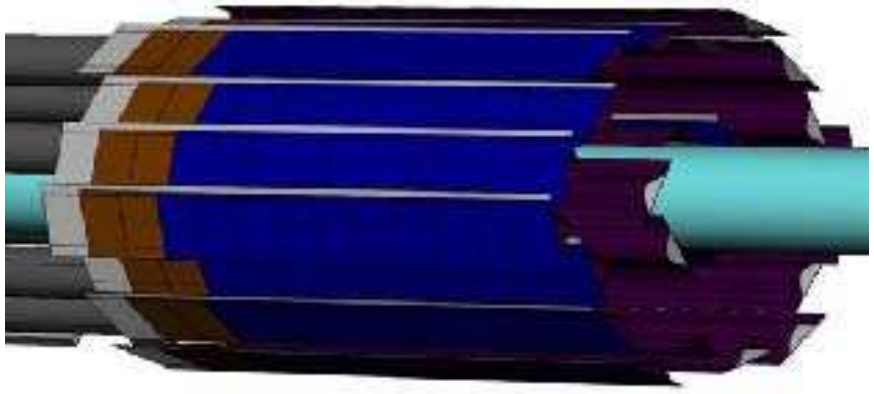
Characterisations on Test Beams

- **2 beam telescopes used at CERN-SPS:**
  - *Old Si strip telescope : 4 pairs of UV planes (2 pairs / arm)*
  - *New pixel telescope : T.A.P.I.*
    - *3 or 4 MIMOSA-17 or/and -18 sensors (more in future)*
    - *Commissionning in June '07 at DESY*
    - *Real data taking in Sep. & Nov. '07 at CERN-SPS*
    - *R.o. freq. $\sim$ 10 (M-18) or 25 frames/s (M-17)*
    - *Running in front of Si-strip telescope ▷▷▷▷▷ ▷▷▷*

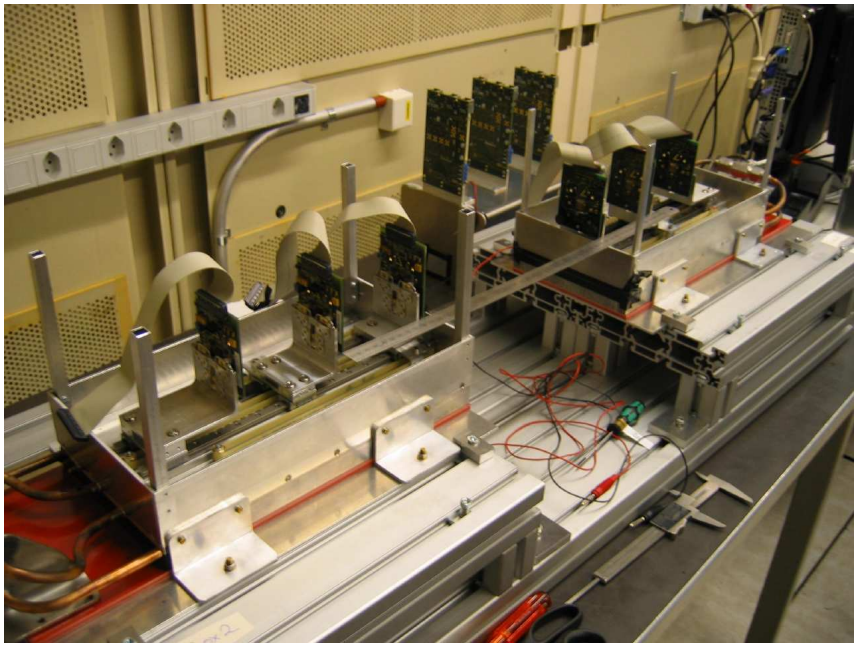


- **Several studies at CERN-SPS:**
  - *response of sensors to inclined tracks*
  - *performances of sensors exposed to non-ionising radiation*
  - *performances of thinned sensors*
  - *comparison of "14 μm" to "20 μm" epitaxy*

- Vertex Detector upgrade for STAR expt at RHIC
  - 2 cylindral layers : $\sim$ 1600 cm^2
  - $\gtrsim$ 160 million pixels ($\leq$ 30 μm pitch)
  - 3 steps :
  - ▷▷ 2007: telescope (3 MIMO-14) $\longrightarrow$ BG meast, no pick-up !
    - ◇ 2008/09: digital outputs without $\emptyset$ ($\leq$ 640 μs)
    - ◇ 2010/11: digital outputs with integrated $\emptyset$ ($\leq$ 200 μs)



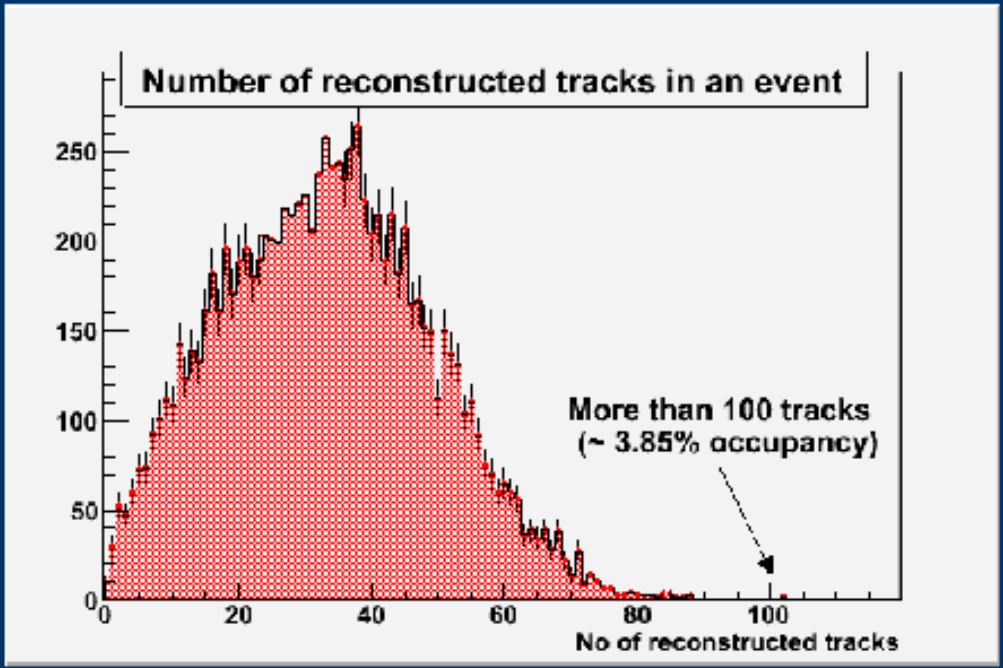
- Beam telescope (FP6 project EUDET)
  - 2 arms of 3 planes (plus 1 high resolution plane)
  - provide $\lesssim$ 1 μm resolution on 3 GeV e$^-$ beam (DESY)
  - 2 steps :
  - ▷▷ 2007: analog outputs
    - $\longrightarrow$ telescope commissionned & running ($\lesssim$ 100 tracks / frame)
      - $\longrightarrow$ used by non JRA-1 members at SPS (e.g. SILC)
    - ◇ 2008/09: digital outputs with integ. $\emptyset$ ($\sim$ 100 μs)



Example of EUDET tracking performance

Performances...

- This impressive plot is showing the pretty mature development stage of the tracking software.

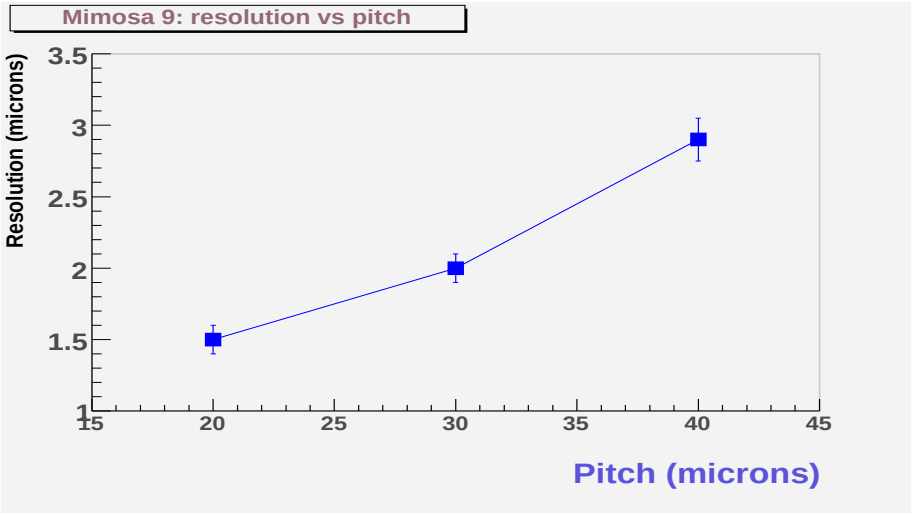


CERN large multiplicity data taken two weeks ago

Spatial Resolution

Single point resolution versus pixel pitch:

- clusters reconstructed with eta-function, exploiting charge sharing between pixels
- $\sigma_{sp} \sim 1.5\ \mu m$ (20 μm pitch) $\rightarrowtail \lesssim 3\ \mu m$ (40 μm pitch)
- obtained with signal charge encoded on 12 bits
- encoding charge on 3–5 bits $\Rrightarrow \sigma_{sp} \sim 2\ \mu m$ (20 μm pitch)



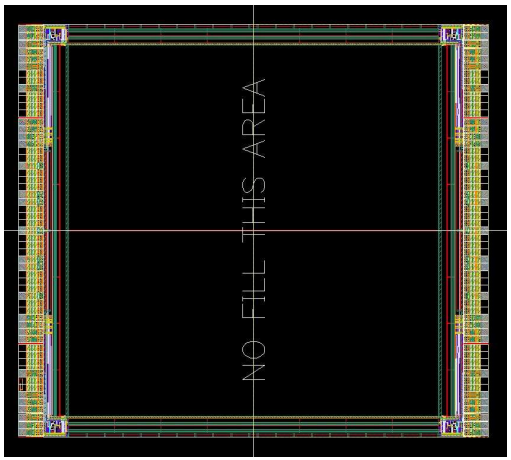
$\hookrightarrow$ requirements: $\lesssim$ 3–3.5 μm in inner layers ($\sim$ 5 μm in outer layers)

Recent result obtained with very small pitch :

- MIMOSA-18 : 512$\times$512 pixels with 10 μm pitch, analog output, S/N $\sim$ 30
- tested on Si-strip tele. at CERN-SPS (120 GeV π^-) in Nov. '07

$\Rrightarrow$ single point resolution observed (prelim.) $\lesssim$ 1 μm !!!

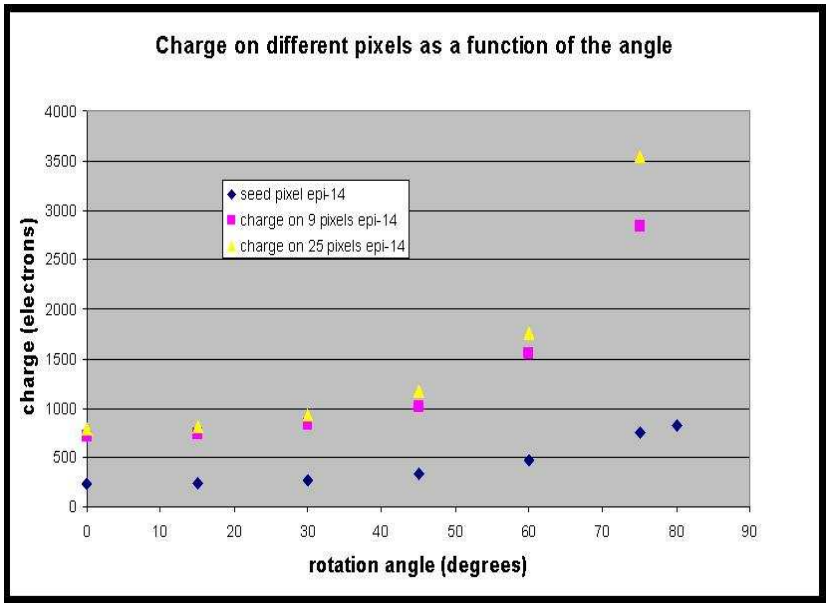
$\hookrightarrow$ for EUDET telescope to allow $\lesssim$ 1 μm on DUT surface with few GeV e^- beam



Response to inclined tracks

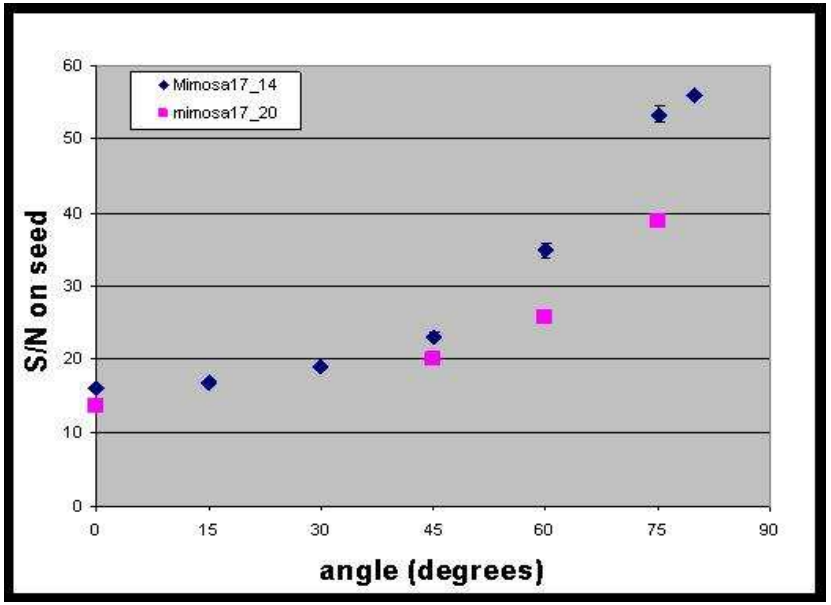
Motivation

- *simulate clusters from particules produced at shallow angle or from low $e^{\pm}_{BS}$ (low p $\longmapsto$ curling in ϕ)*
- *collect cluster data at various angles $\longmapsto$ data base*
- *adapt signal processing μcircuits and cluster rec. algo. to inclined tracks : 2–3 seed pixels, large signal, large clusters, ...*



Measurements performed with TAPI at CERN-SPS

- *MIMOSA-17 (30 μm pitch, rad. tol. pixel), T_{room}*
- *measure Q, S/N, σ_{sp}, σ_{θ} at θ = 0, 15, 30, 45, 60, 75, $>80^{\circ}$*
- *set-up data base for complete VD simulations (LoI)*
- *model cluster characteristics vs p & θ for "fast" VD simul.*
- *work performed together with Lukazc Maczewski (Warsaw) (also: gyroscopic sensor support installed on DESY beam)*



Radiation Tolerance: Summary of AMS-0.35 OPTO Evaluation

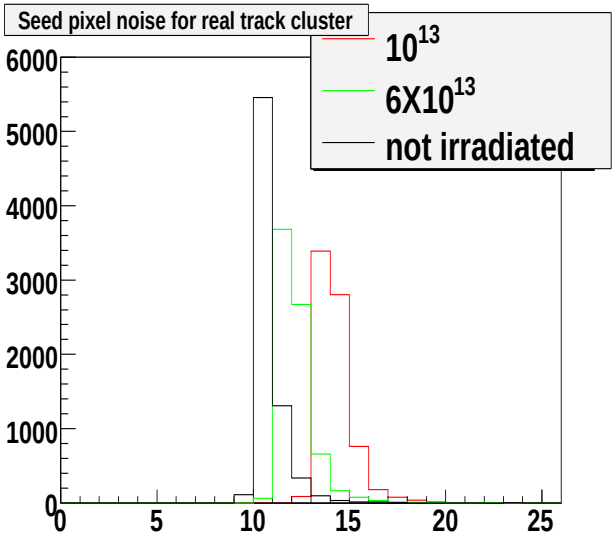
Requirements:

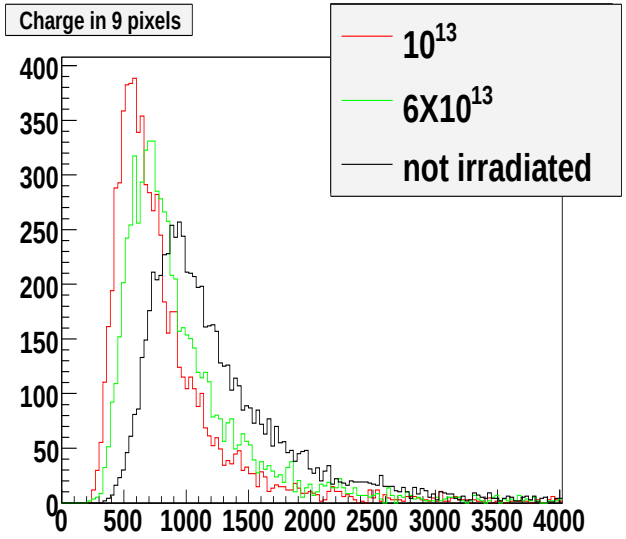
- **beamstrahlung (GuineaPig X 3) :** $\lesssim 10^3$ **e**$^{\pm}_{BS}$**/cm^2/25** μs $\rightarrowtail$ $\lesssim$ **2·10^{12}e**$^{\pm}_{BS}$**/cm^2/yr**
  $\hookrightarrow$ **O(100) kRad/yr – O(10^{11}) n$_{eq}$/cm^2/yr (**NIEL $\sim$ 1/30**)**
- **neutron gas:** $\lesssim 10^{10}$ **n$_{eq}$/cm^2/yr**

Established ionising radiation tolerance (reminder): 1 MRad – 2·10^{12} n$_{eq}$/cm^2 – 10^{13} e$^-_{10\ MeV}$/cm^2 OK

Non-ionising radiation tolerance (Summer / Autumn 2007):

- **MIMOSA-18 irradiated with** $\lesssim 10^{13}$ **O(1 MeV) n/cm^2 (+ 100–200 kRad** γ **gas)** $\Rightarrow$ **tested on** $\sim$ **120 GeV** π^- **beam (SPS)**
  - ▷ **Preliminary results:** • T = -20°C • $t_{r.o.} \sim 3$ ms • cuts at 5N (seed) & 2N (crown)





Fluence (n$_{eq}$/cm^2)	0	6·10^{12}	1·10^{13}
Noise (e$^-$ ENC) (20°C, 3 ms, 5N/2N)	10.8 ± 0.3	12.2 ± 0.3	14.3 ± 0.3
Q_{clust} (e$^-$)	1026	680	560
S/N (MPV)	28.5 ± 0.2	20.4 ± 0.2	14.7 ± 0.2
Det. Eff. (%)	99.93 ± 0.03	99.85 ± 0.05	99.5 ± 0.1

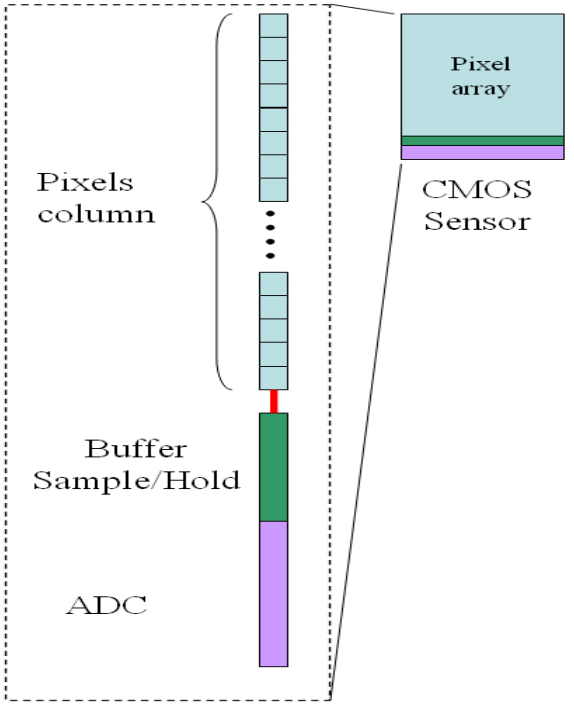
$\gtrsim$ 5–10 yrs of run affordable at T $<$ 0°C & $t_{r.o.} \lesssim 100\ \mu s \rightarrowtail$ continue assessing T_{room} performances

Integration of Signal Processing

Inside Pixels and on Chip Periphery

Fast Read-Out Architecture

- **Parallel development of 3 components (analog, mixed, digital):**
  - **column // arrays with CDS/pixel & discriminated outputs**
  - **4-5 bit ADCs intended to replace discriminators**
  - **$\varnothing$ μcircuits & output memories**



- **2 stage approach :**

  1) Develop sensors for mid-term (2009) applications

  $\hookrightarrow$ less severe requirements, almost suited to 3 outer layers:

  - **EUDET: 1x2 cm^2, t$_{r.o.}$ $\sim$ 100 μs, discri. binary charge encoding (no ADC);**
  - **STAR: 2x2 cm^2, t$_{r.o.}$ $\sim$ 200 μs, discri. binary charge encoding (no ADC);**

  $\hookrightarrow$ will be operated in real experimental conditions by 2009/2010

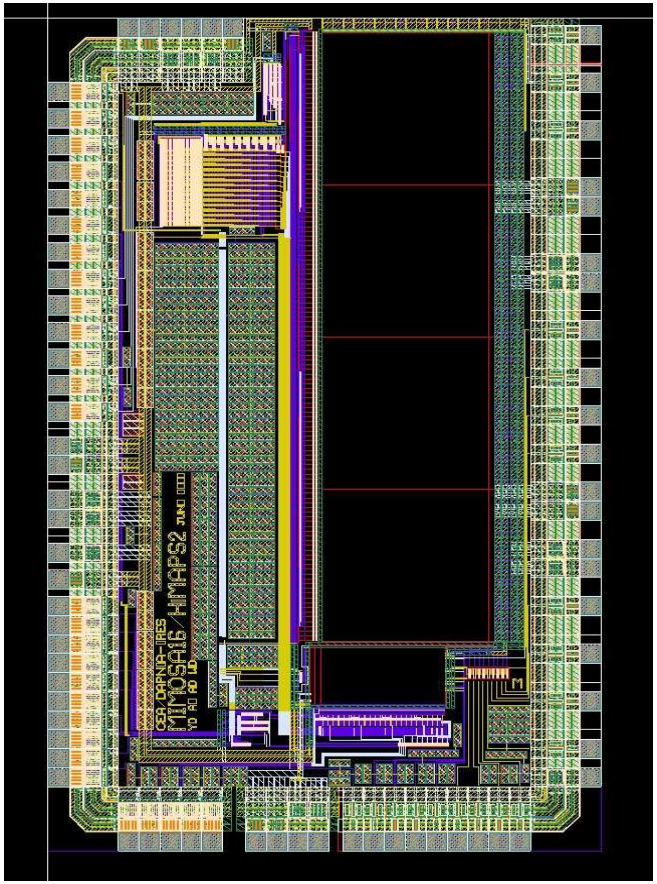
  2) Develop ILC sensors (mainly for inner layers) extrapolating from EUDET & STAR:

  - **increase row read-out frequency by $\sim$ 50 %**
  - **replace discriminators with ADCs**

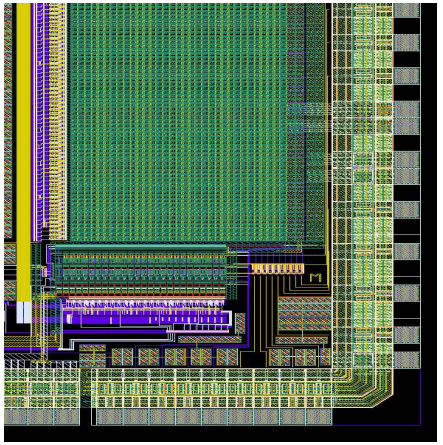
High R.-O. Speed Architecture : 2nd Prototype = MIMOSA-16

MIMOSA-16 design features :

- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–15 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (DS at end of each column)
- 24 columns ended with discriminator
- 4 sub-arrays :
  - **S1 :** like MIMOSA-8 (1.7x1.7 μm^2 diode)
  - **S2 :** like MIMOSA-8 (2.4x2.4 μm^2 diode)
  - **S3 :** S2 with ionising radiation tol. pixels
  - **S4 :** with enhanced in-pixel amplification
    (against noise of read-out chain)



$\Rightarrow$



Tests of analog part (”20” & ”14” μm epitaxy) :

- sensors illuminated with ^{55}Fe source and $F_{r.o.}$ varied up to $\gtrsim$ 150 MHz
- measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs $F_{r.o.}$

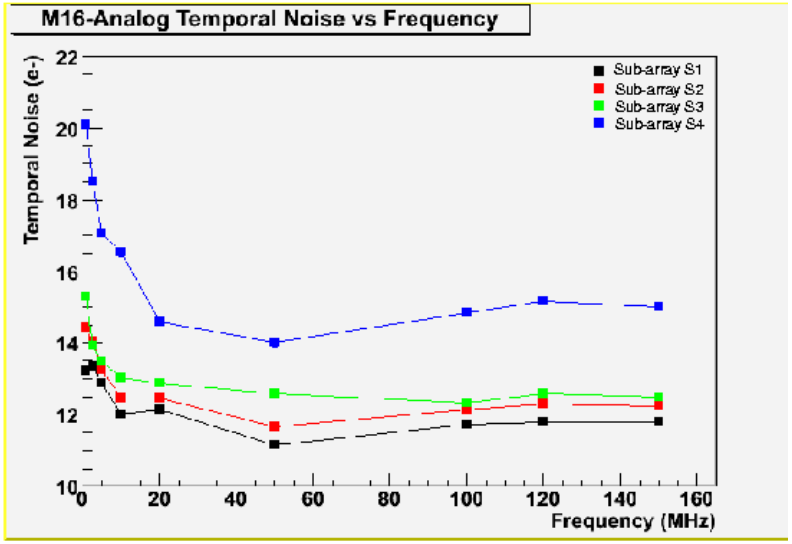
M.i.p. detection with Si-stip telescope studied at CERN in Sept. ’07 $\rightarrowtail$ characterisation of digital response :

- π^- beam of $\sim$ 180 GeV/c
- measurements of SNR, det. efficiency, fake rate, cluster characteristics, spatial resolution vs discri. threshold

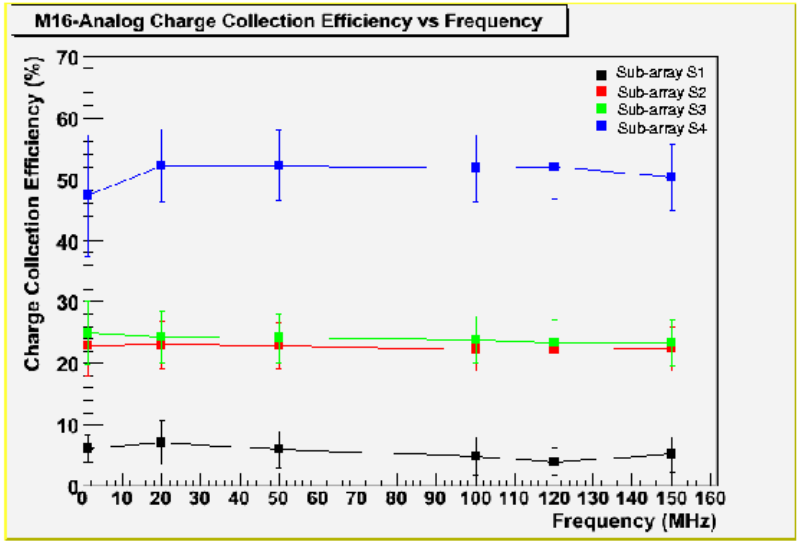
MIMOSA-16 Lab Test Results (Analog Part)

Pixel noise and charge collection efficiency (*"20 μm epitaxy* :

Temporal noise vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



Charge Collection Efficiency vs Frequency
Chip#0 (old mezzanine board)
Columns 28-31



08/01/07 Résumé résultats Mimosa-16 chip#0

08/01/07 Résumé résultats Mimosa-16 chip#0 4

⇛ **Noise performance satisfactory (**like MIMOSA-8 and -15**)**

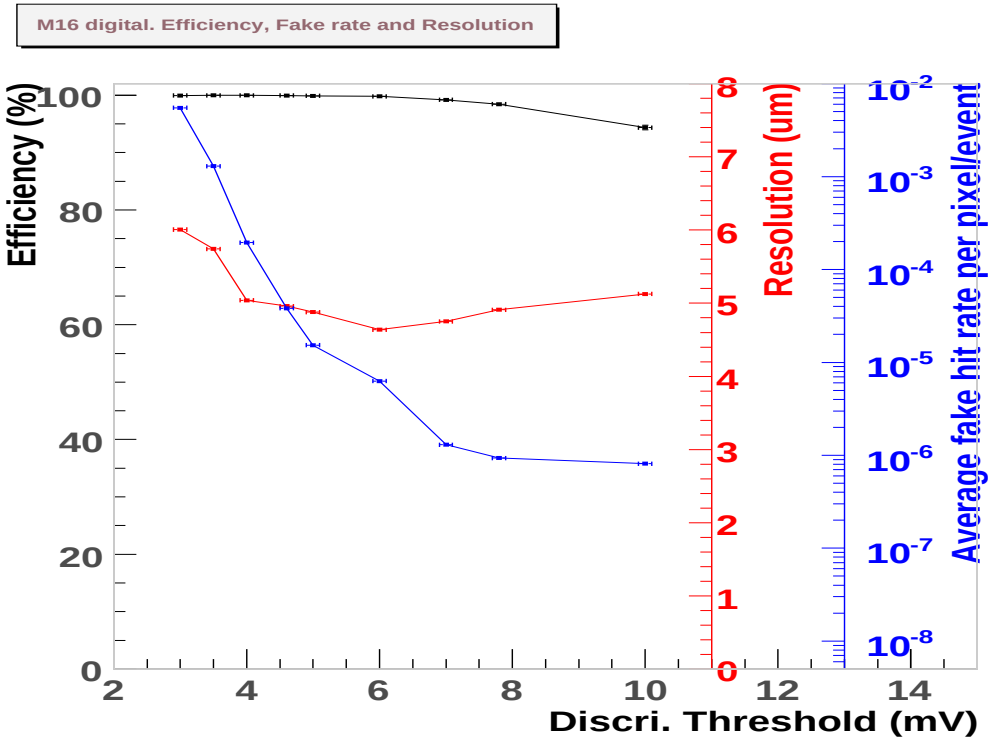
⇛ *CCE: very poor for S1 (*1.7x1.7 μm^2*) & poor for S2/S3 (*2.4x2.4 μm^2*)*

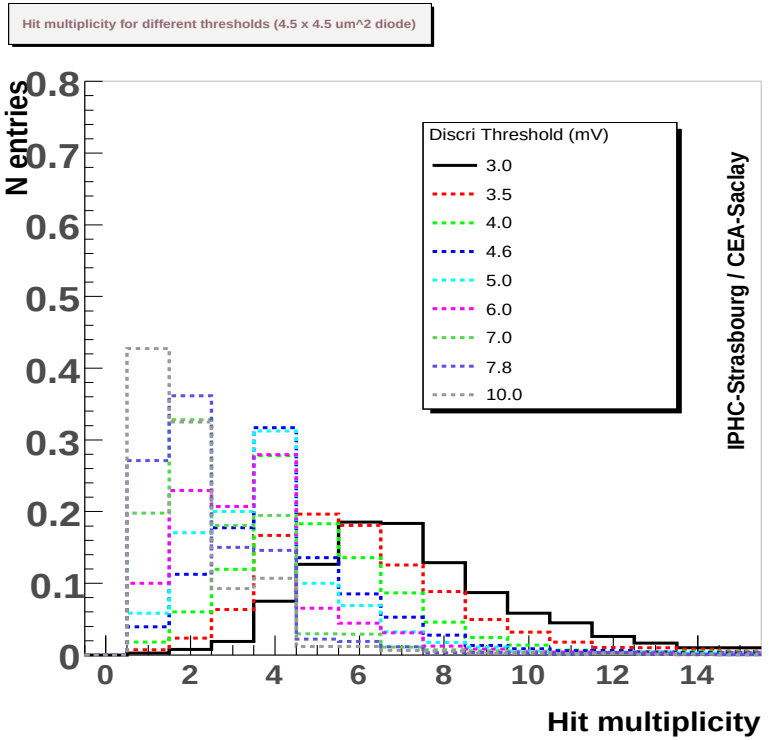
⟶ *already observed with MIMOSA-15 but more pronounced for "20 μm" option*

↪ suspected origin: diffusion of P-well, reducing the N-well/epitaxy contact, supported by CCE of S4 (4.5x4.5 μm^2 diode)

MIMOSA-16 Beam Test Results (Digital Part)

- **CERN-SPS ($\sim$ 180 GeV π^-) $\longmapsto$ preliminary analysis results of S4 ("14 μm" epitaxy)**
- **Read-out time $\sim$ 50 μs** *($\sim$ 1/4 of max. freq. due to DAS limitations)*





- **Major result $\longmapsto$ at least one pixel architecture validated for next steps : S4 (SNR $\sim$ 16)**

Discri. Threshold	*det. efficiency*	*fake rate*	*sgle pt resolution*
4 m V	*99.96 $\pm$ 0.03 (stat) %*	*$\sim 2{\cdot}10^{-4}$*	*$\sim$ 4.8–5.0 μm*
6 m V	*99.88 $\pm$ 0.05 (stat) %*	*$<10^{-5}$*	*$\sim$ 4.6 μm*

Next steps :

- *Mid-term : EUDET, STAR $\rightarrowtail$ real experimental conditions; $\sim$ ILC VD outer layer requirements*
- *Long-term full sensor prototyping : ILC (mainly inner layers), CBM*

Integrated $\emptyset \rightarrowtail$ real scale sensors without ADC ($\sigma_{sp} \sim$ 4–6 μm) :

- ⁂ *EUDET telescope (2008)*
- ⁂ *STAR-HFT (2010)*
- ⁂ *CBM-MVD ($\geq$ 2015)*

Integrated 4-5 bit ADC replacing discriminators and increased read-out speed :

- ⁂ *prototype for ILC-VD (2008/09)*
- ⁂ *read-out speed $\rightarrowtail$ CBM-MVD ($\geq$ 2015)*

- **Several different ADC architectures under development at IN2P3 and DAPNIA**
  - **LPSC (Grenoble): Ampli + semi-flash (pipe-line) 5- and 4-bit ADC for a column pair**
  - **LPCC (Clermont) : flash 4+1.5-bit ADC for a column pair**
  - **DAPNIA (Saclay) : Ampli + SAR (4- and) 5-bit ADC**
  - **IPHC (Strasbourg) : SAR 4-bit and Wilkinson 4-bit ADCs**

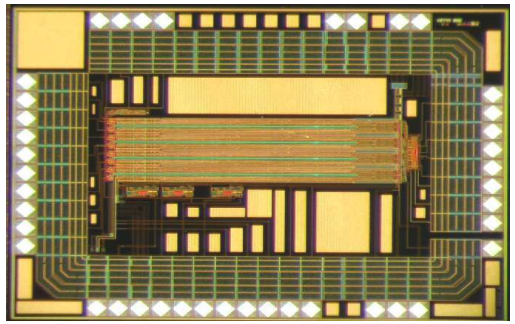
Lab	proto.	phase	bits	chan.	$F_{r.o.}$ (MHz)	dim. (μm^2)	P_{diss}^{stat}	eff. bits	Problems
LPSC	ADC1	tested	5	8	15-25	43x1500	1.1 mW	4	Offset & N
	ADC2	tested	4	8	25	40x943	0.7 mW		
	ADC3	fab	5	16 ?	25	40x1400	0.7 mW (sim)		
LPCC	ADC1	tested	5.5	1	5(T)–10(S)	230x400	20 mW	2.5	P_{diss} & bits
	ADC2	fab	5.5	1	10	40x1100	1 mW		
DAPNIA	ADC1	tested	5	4	4	25x1000	0.3 mW	$\gtrsim$ 2	Missing bits
	ADC2	fab	5	4	4	25x1000	0.3 mW		
IPHC	ADC1	under test	4	16	10	25x1385 (?)	$\lesssim$ 0.3 mW		
	ADC2	under test	4	16	10	25x900	$\lesssim$ 0.3 mW		

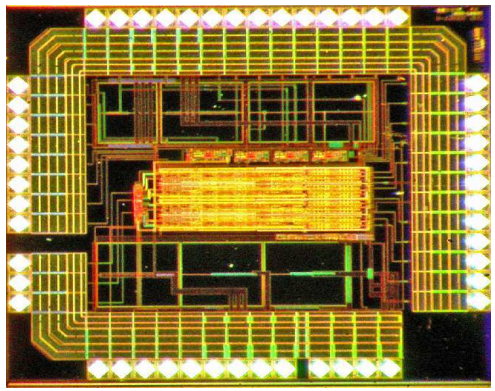
⇛ **1st mature ADC design expected to come out in 2008**

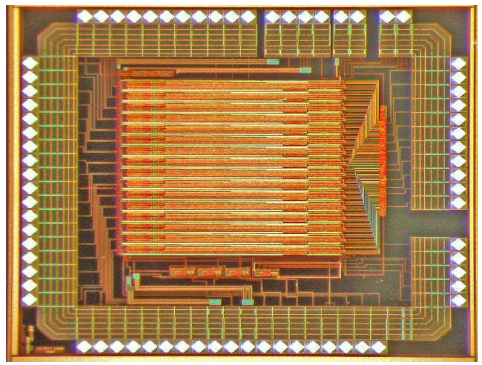
⇛ **Submission of 1st col. // pixel array proto equipped with ADCs in Autumn 2008 (?) ⟶ with integ. ∅ in 2009**

Status of ADC developped at LPSC

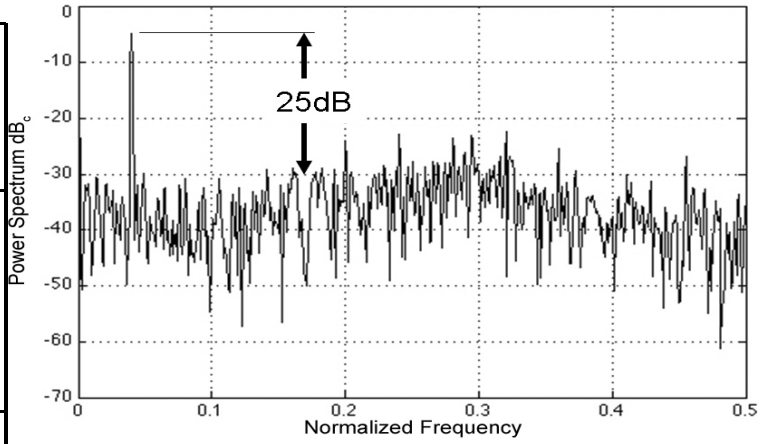
Very Low power S&H+ pipelined ADC from LPSC

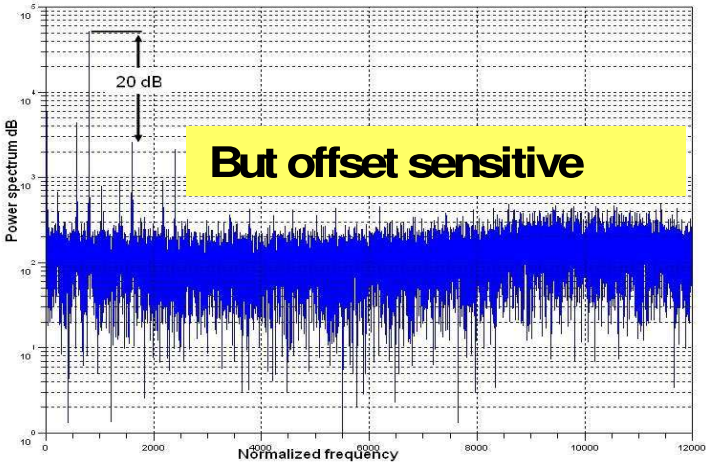






	Fréq. (MHz)	Dimension (µm*µm)	Conso (mW)
1er Proto (2006) 5bits	25	43*1500	1.04 3.3V
2ème proto (Jun 2007) 4 bits Double Sampling	25	40*900	0.72 3.3V
3ème proto (sep 2007) 5 bits Double sampling	25	40*1400	0.69 simu 2V

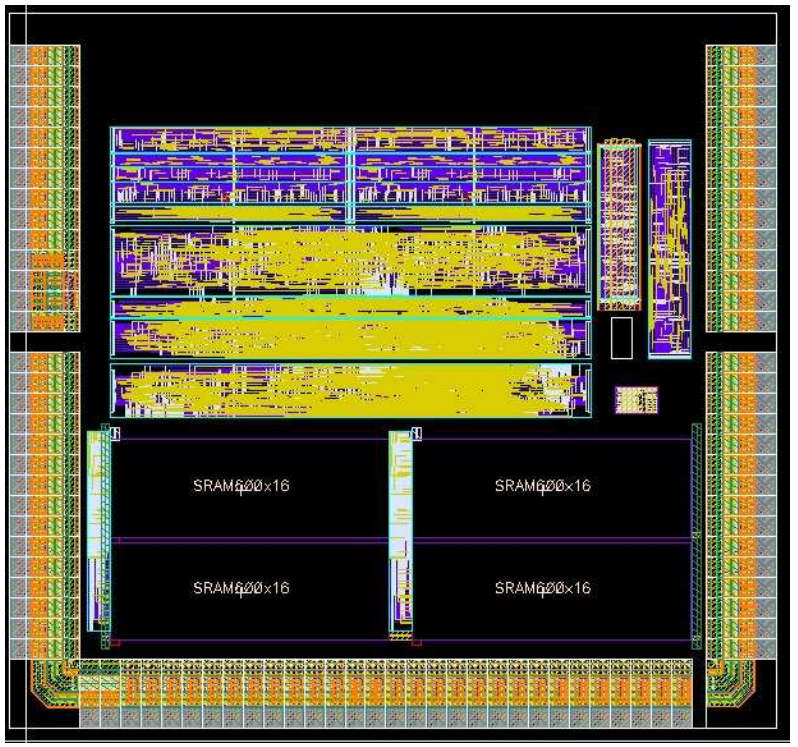




to be tested

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - ◇ step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - ◇ step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim 3.9 \times 3.6$ mm^2
  $\hookrightarrow$ 10 keuros (funding via EUDET)



Status :

- sent for fabrication end of July
- back from foundry end of Sept. $\rightarrowtail$ tests under preparation $\Rightarrow$ test completion expected by end of year

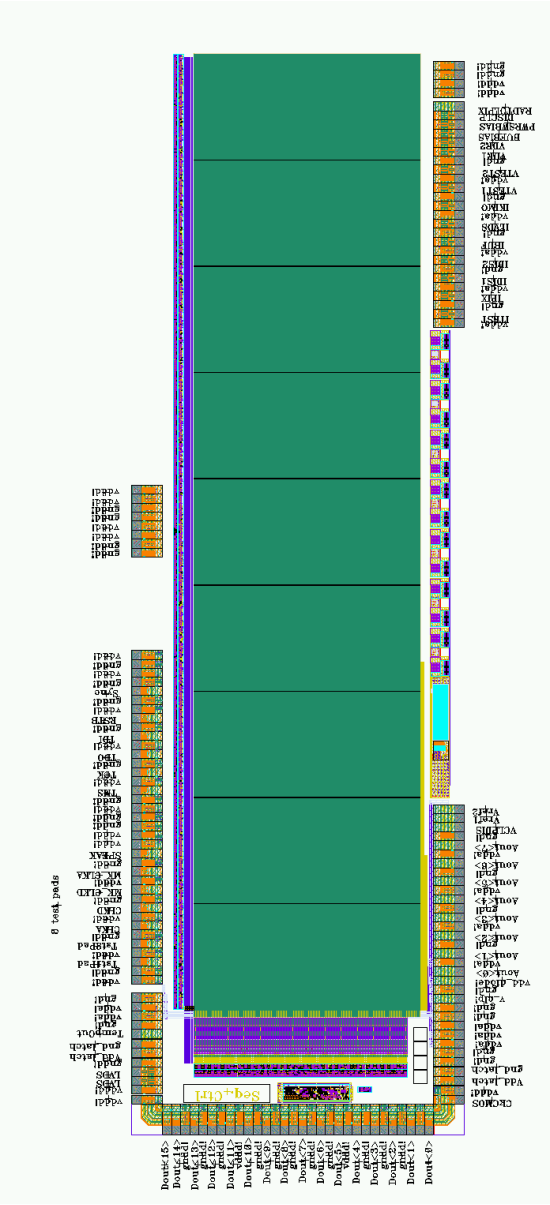
Final prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 $\longmapsto$ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

■ Pixel characteristics (*optimal charge coll. diode size ?*) :

- ⁂ pitch : 18.4 μm (compromise resolution/pixel layout)
- ⁂ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ⁂ 128 columns ended with discriminator
- ⁂ 8 columns with analog output for test purposes
- ⁂ 9 sub-matrices of 64 rows : various pixel designs w/o ionising rad. tol. diode

  $\Rrightarrow$ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)
- ⁂ read-out time $\sim$ 100 μs



■ Testability :

- ⁂ JTAG + bias DAC $\longmapsto$ programmable chip steering
- ⁂ 2 additionnal DC voltages to emulate pixel's output
  for independent discriminator performance assessment
- ⁂ output frequency $\leq$ 40 MHz

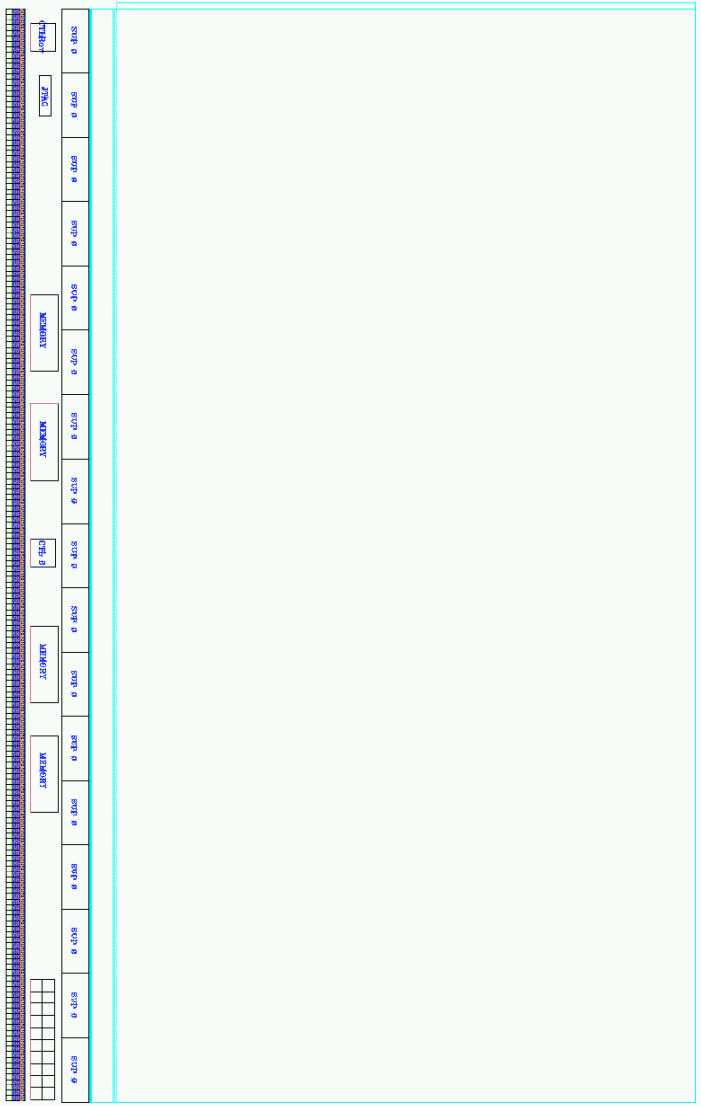
■ Status :

- ⁂ Submitted end of Oct. '07 (MP run) $\longmapsto$ tests will start in Feb.'08
- ⁂ Funding ($\sim$ 50 mm^2): $\sim$ 40 keuros (2/3 payed via EUDET)

Autumn 2008 : MIMOSA-22+ = Final EUDET Sensor

- **MIMOSA-22 complemented with ∅ (SUZE-01)**
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm^2)
- Read-out time $\sim$ 100 μs
- Chip dimensions : $\sim$ 20 x 12 mm^2

▷ Opportunity for an engineering run combining various chips (pixel+ADC ?):
$\sim$ 120 keuros for 6 diced and thinned wafers ($\sim$ 60 % via EUDET)



Devts performed in // :

- June 2008 : submission of final STAR-HFT1 sensor
  ▷ $\sim 2 \times 2$ cm^2 ; 400 kpix/sensor ; $\leq$ 640 μs ; 50 μm thin
  ↪ equip 2 or 3 sectors of 1 + 3 ladders (10 chips/ladder)
- Autumn 2008 (?) : MIMOSA-16 with ADCs replacing discri.
  (24 columns of 128 pixels r.o. in //, with 4- or 5-bit ADC ending each col.)

Beyond 2008:

- **MIMOSA-22** with ADCs replacing discriminators ⟼ outer layers (?) ⟼ inner layers
- **increase r.o. frequency** by $\sim$ 50 % (new ∅ & memory design) ⟼ inner layers

System Integration Studies

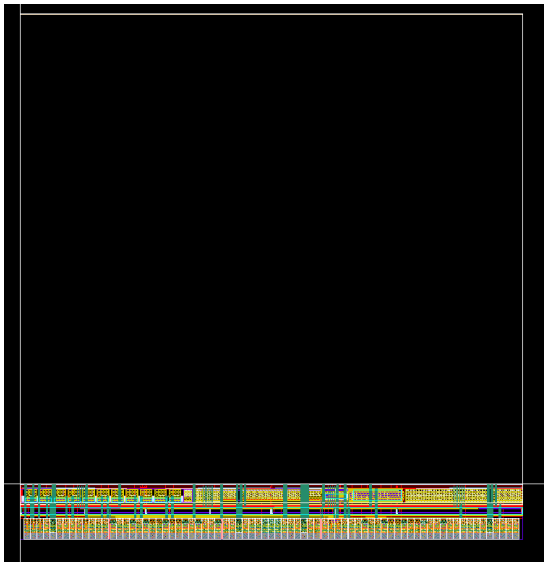
- Thinning
  - Ladder design
    - Power cycling
      - Data Flow

Thinning motivations and constraints :

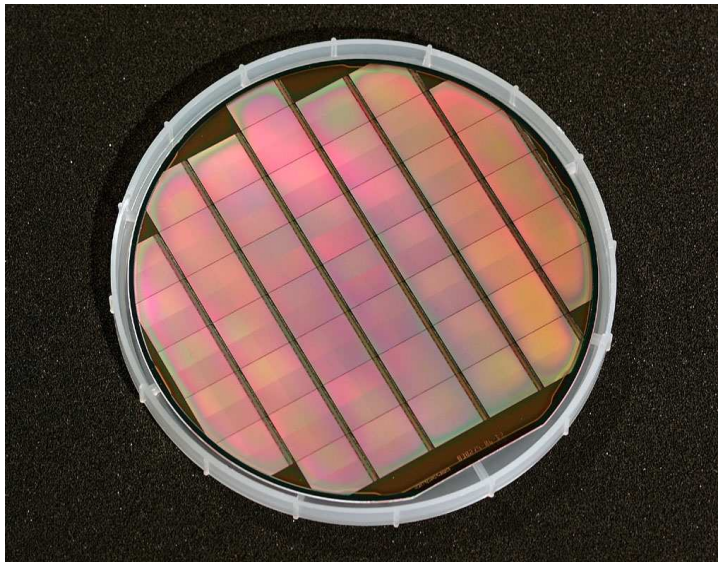
- *thin sensors to $\lesssim$ material budget of "mechanical support" (+ beampipe)*
- *minimal thickness of CMOS sensors :*

  10–15 μm (metal layers and SiO_2) + 15 μm (T + epitaxy) + 5–10 μm (substrate) $\approx$ 30–40 μm
- *thinned sensors should be "easy" to handle*
- *thinning procedure should have high mechanical yield and preserve detection performances*
- *CMOS technology fab. yield $\rightarrowtail$ foster diced sensors (despite few 10^{-4} X_0 add. mat. budget / ladder)*
- *thinning of individual sensors seems preferable to full wafer thinning : cheaper but same quality ?*

MIMOSA-17 : 8 x 9 mm^2



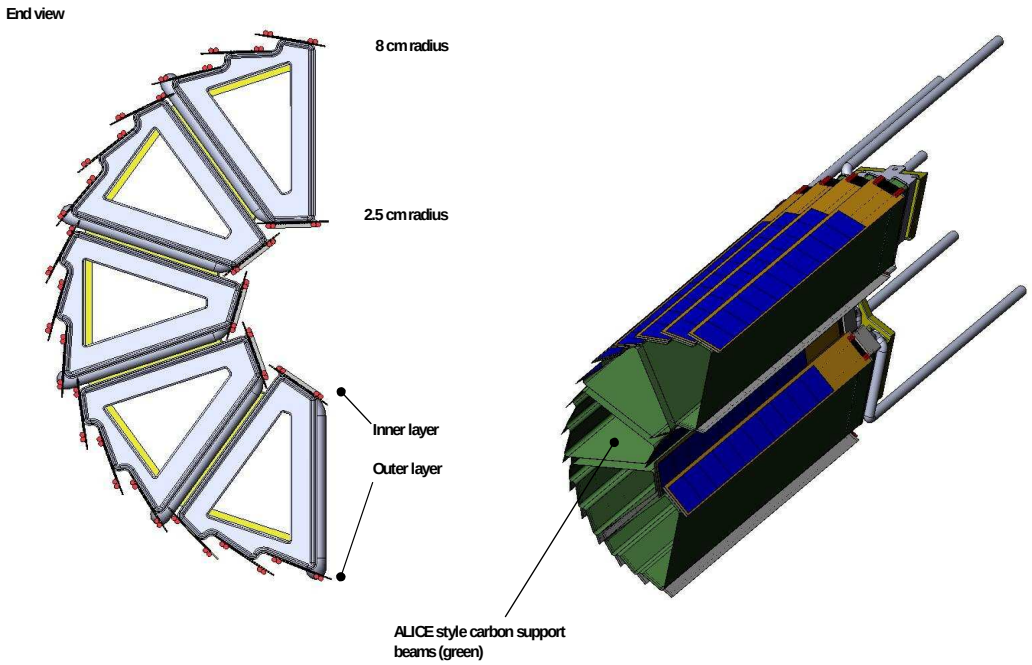
MIMOSA-5 : 6" wafer



Status of Thinning Studies and Ladder Prototyping (STAR)

- **Predominantly driven by STAR HFT project at LBNL**

Pixel support structure



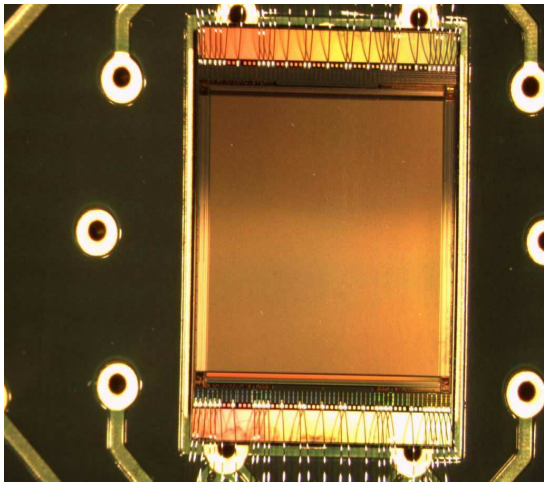
- **Thinning of MIMOSA-5 wafers :**
  - *3 wafers thinned via LBNL to 50 $\pm$ 5 μm*
  - *result satisfactory (after pre-dicing):*
    sensors can be manipulated and mounted on support
  - *3 ladder prototypes fabricated at LBL ($\gtrsim$ 0.25 % X_0)*
    $\longmapsto$ up to 9 sensors mounted on ladder and tested

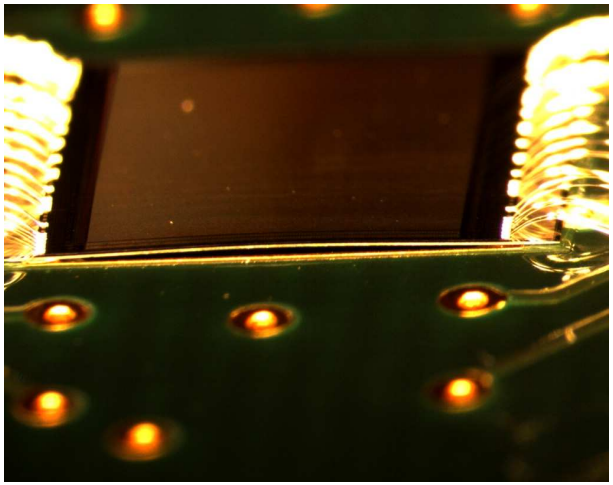
- **Thinning of individual sensors to $\sim$ 50 μm:**
  - *several chips of $\sim$ 0.2 – 3.5 cm^2 (MIMOSA-5, -10, -14, -17, -18, -20, etc.) thinned individually via LBNL*
  - *recent result: MIMOSA-18 prototype thinned to 50 μm was successfuly tested with ^{55}Fe at IPHC*
    $\longmapsto$ no change of performances (e.g. noise, gain, det.eff, ...) $\longmapsto$ next slide
  - *Plans :*
    - *replace present (thick) sensors (MIMOSA-17, -18) equipping telescopes (EUDET, TAPI, ...)*
    - *equip STAR-HFT1 with thinned sensors (2008/09) $\longmapsto$ 0.25 – 0.3 % X_0*
    - *extend ladder devt to ILC Vertex Detector (LBNL-ILC team ?) $\longmapsto$ goal $\leq$ 0.2 % X_0*

Thinning of Diced Sensors

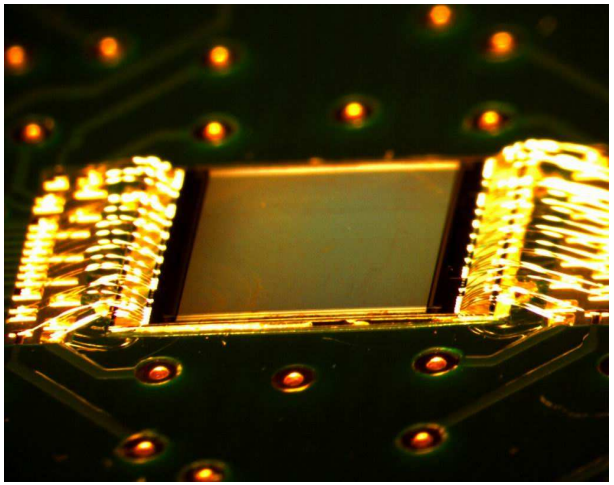
- **Thinning of AMS-0.35 engineering run reticles :**
  - *Thinning performed by APTEK (S.F. bay) via LBNL (STAR coll.)*
  - *Thickness claimed by provider : 50 μm $\rightarrowtail$ measured with IPHC bonding machine : $\sim$ 50–70 μm*
  - *MIMOSA-18 (5.5$\times$7.5 mm^2) & -17 (8$\times$9 mm^2) mounted on PCB for tests $\rightarrowtail$ keep them flat !*

MIMOSA-18: First gluing trial





Second gluing trial



  - *Tests with ^{55}Fe source show no performance loss (noise, gain)*
  - *Tests of MIMOSA-18 mounted on TAPI with 120 GeV π^- at CERN-SPS (Nov. '07)*
    $\rightarrowtail$ *no performance loss observed $\rightarrowtail$ $\epsilon_{\mathbf{det}}$ = 99.79 $\pm$ 0.15 % (prelim.)*

- **Preliminary conclusion : Thinning down to $\sim$ 50 μm seems on a good track**

Status of Other System Integration Studies

Power cycling

- *study performed with MIMOSA-5 at DESY*
- *though MIMOSA-5 not at all adapted to power cycling, it was operated with $\sim$ 1/8 duty cycle*
  - $\Rrightarrow$ *duty cycle $\lesssim$ 1/50 within reach with suited sensor design*

Data flow:

- *data flow / layer assessed at row, sensor, ladder, layer and full detector levels for BG $\times 1$ and $\times$ 3–5*
- *whole detector data flow expected to amount to $\sim$ 0.2 to 1 GB/s , depending on $e^{\pm}_{BS}$ rate*
- *instantaneous flow from row in inner most layer may be critical : up to 200 Bytes per 100 ns*

New concept of mechanical support & heat extractor:

- *objective : mount, connect & operate $\lesssim$ 10 MIMOSA-17 sensors, thinned to 50 μm, on 50–100 μm thin, aluminised, CVD diamond slabs $\equiv$ mech. support – heat extractor - cable support*
- *status : 3 diamond 3" wafers fabricated $\longmapsto$ electroplating and lithography*

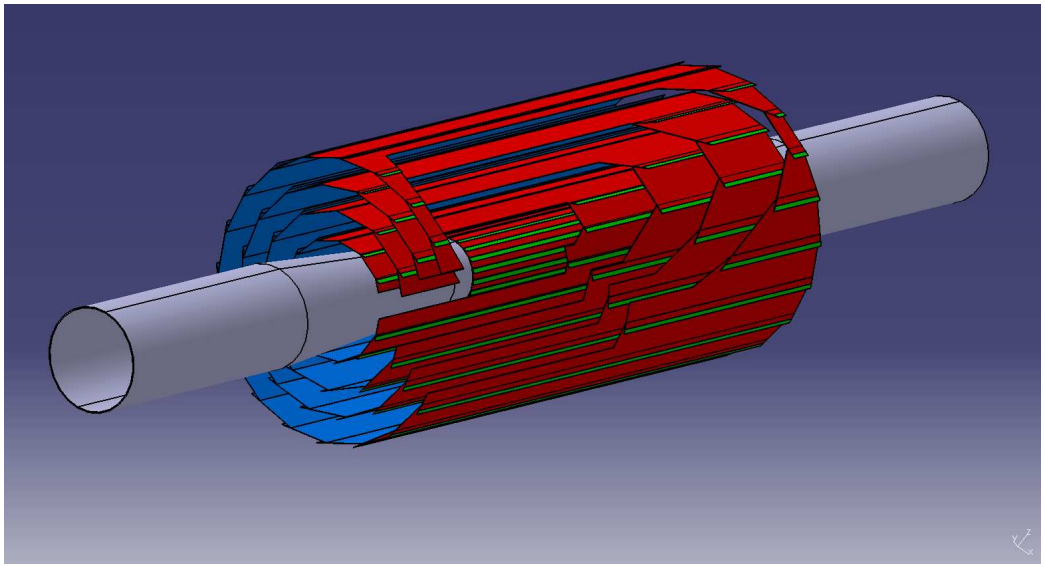
General remarks :

- *CMOS sensors call for* SPECIFIC *system integration solutions : connexions (flex cable), data flow, ...*
- **Lack of studies going on (expertised manpower) $\Rrightarrow$ may become a Problem**

Example of Basic Vertex Detector Design features

- *ILD geometry: $\gtrsim$ 5 cylind. layers (R = 15–60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96* ▷ *SiD: shorter barrel & fw/bw disks*
- *L0 and L1 : optimised against occupancy*
- *L2, L3 and L4 : optimised against power dissipation*
- *Pixel pitch varied from $\sim$ 20 μm (L0–L1) to $\gtrsim$ 30 μm (L2–L4) $\longmapsto$ minimise P_{diss}*

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P^{inst}_{diss} (W)	P^{mean}_{diss} (W)
L0	*15*	20	25	20	25	$<$100	$<$*5*
L1	$\leq$ *25*	25	50	$\leq$26	$\leq$ 65	$<$130	$<$*7*
L2	*37*	33	$\sim$100	24	50	$<$90	$<$*5*
L3	*48*	33	$\sim$100	32	80	$<$120	$<$*6*
L4	*60*	33	$\sim$100	40	150	$<$125	$<$*8*
Total				142	**330**	$<$600	**3–30**



- *Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; $\lesssim$ 40 μm thin sensors)*
- *Very low P^{mean}_{diss}: $<<$ 100 W (exact value depends on duty cycle)*
- *Fake hit rate $\lesssim 10^{-5}$ $\longmapsto$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)*
- *Design still evolving $\longmapsto$ optimisation with physics processes (R.De Masi) $\longmapsto$ input to LoI*

- **Steady progress towards perfo. adapted to running conditions with beam BG $>>$ MC simulations**

- **2007 :** ⁂ *several achievements (beam tests) and progresses on sensor R&D :*
  50 μm thinning, fast col. // architecture with discri. output, spatial resolution, rad. tol., etc.
  ⁂ *succesfull 1st experimental use of small sets of sensors $\rightarrowtail$ telescopes: EUDET-JRA1, TAPI, STAR*
  ⁂ *progress on syst. integration aspects : thinning, power cycling, ladder, Si/diamond, etc.*

- **2008 :** ⁂ *final EUDET telescope sensor fab.: 1$\times$2 cm^2; 0.6 Mpix; 100 μs; digital output with $\emptyset$; 50 μm thin*
  ⁂ *STAR-HFT1 sensor fab.: 2$\times$2 cm^2; 0.4 Mpix; 640 μs; digital output; 50 μm thin $\rightarrowtail$ D^0 phys. in 2010*
  ⁂ *several other R&D lines: fast archi. with ADC, new fab. proc., system integ., etc. $\rightarrowtail$ FP-7*
  ⁂ *vertex detector design optimisation with physics processes $\rightarrowtail$ LoI*

- **$>$ 2008 :** ⁂ **prototype ladder for outer/inner layers in 2009/2010 ($\leq$ 0.2 % X$_0$)**
  ⁂ **final sensor designs for outer/inner layers in 2010/2011**

- **Concern :** **system integration issues not covered $\rightarrowtail$ prototype ladder ????**

- **Perspective :** *3DIT MIMOSA $\equiv$ 4 chip sandwich of best techno. for sensing, for analog, for mixed, and for digital circuits*