A 130nm CMOS Evaluation Digitizer Chip for Silicon Strips readout at the ILC

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on behalf of

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Work in the framework of the SiLC (Silicon for the Linear Collider), R&D Collaboration and the EUDET I3-FP6 European Project

Outline

- Silicon strips readout
- Front-End Electronics
- A 4-channel evaluation chip in 130nm CMOS
- Conclusion

Silicon strips detectors at the ILC

Silicon tracker system, two cases considered:
ILD (Silicon tracking surrounding the TPC and
SiD (All Silicon tracking)

Both cases end up to:

- A few 10^6 Silicon strips
- 10-30 max (could reach 60cm in extreme case) strip length,
- Thickness ≤ 300 μm
- Strip pitch ≤ 50 μm
- AC coupled (could be DC if needed)

Millions of channels
→ Integration of k-scale channels readout chip

Silicon strips data

- Pulse height: Cluster centroid to get a few µm position resolution

→ *Detector pulse analog sampling*

- Time: 150-300 ns for BC identification

→ *Shaping time of the order of the microsecond depending upon strip length (capacitance)*

→ 80ns analog pulse sampling and on-chip digitization

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Functionalities to be integrated

- Full readout chain integration in a single chip

  - Preamp-shaper
  - Sparsification — Trigger decision on analog sums
  - Sampling — 8-deep sampling analog pipe-line
  - Analog event buffering: — Occupancy: 8-16 deep event buffer
  - On-chip digitization — 10-bit ADC
  - Buffering and pre-processing:
    Centroids, least square fits, lossless compression and error codes
  - Calibration and calibration management
  - Power switching (ILC duty cycle)

Front-End chip numbers

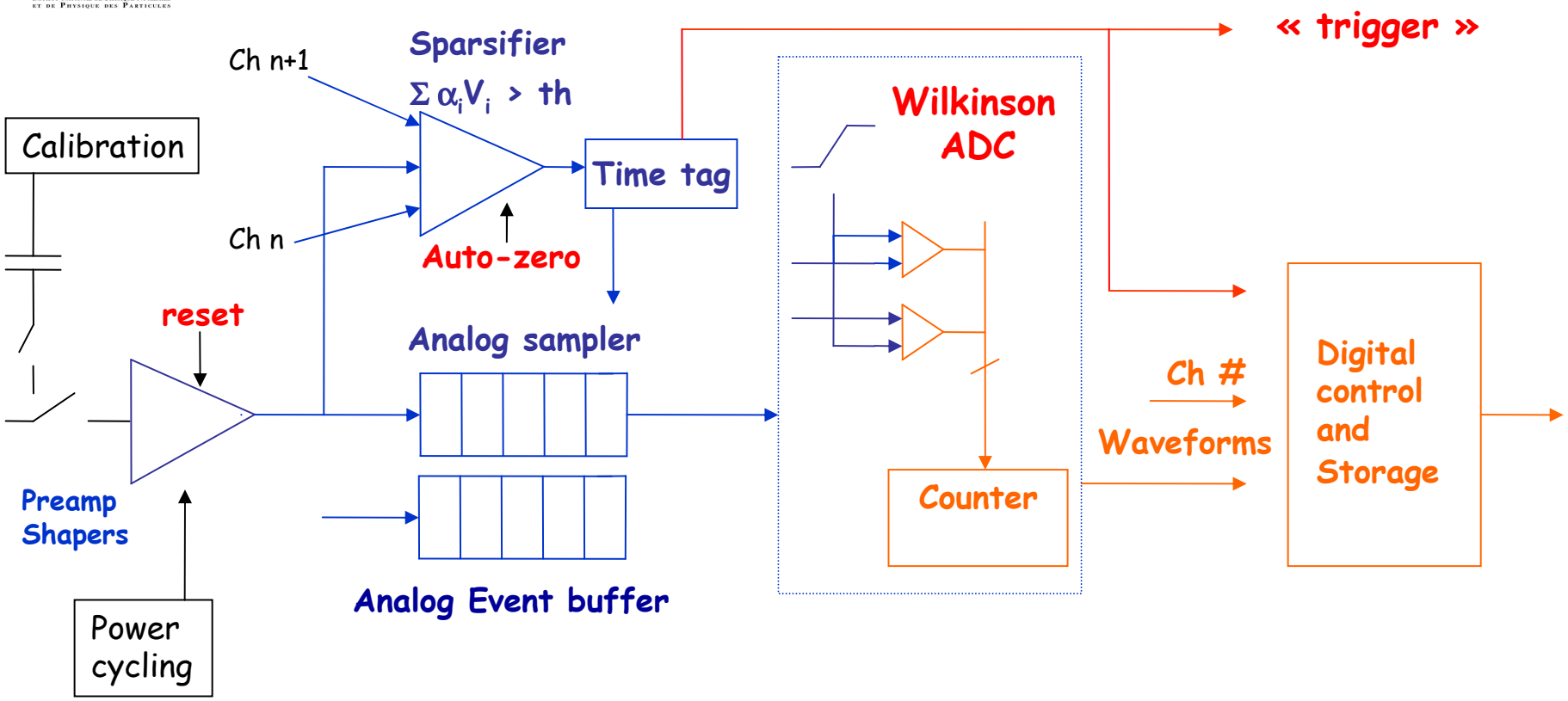
- Goal: Integrate 512-1024 channels in 90nm CMOS:

  - **Amplifiers:** - **30 mV/MIP over 30 MIP range**
  - **Shapers:** - **Two ranges: 500ns–1µs, 1µs-3µs**
  - **Sparsifier:** - **Threshold the sum of 3-5 adjacent channels**
  - **Samplers:** - **8 samples at 80ns sampling clock period**
    - **Event buffer 8-16 deep**
  - **Noise baseline:**

    Measured with 180nm CMOS:
    375 + 10.5 e-/pF @ 3 µs shaping, 210µW power
    S/N = 20 @ 90cm long strips
  - **ADC:** - **10 bits**
  - **Buffering, digital pre-processing**
  - **Calibration**
  - **Power switching can save a factor up to 200**

ILC timing: 1 ms: ~ 3000 trains @ 360ns / BC 199ms in between

Front-end architecture



Charge 1-30 MIP, Time resolution: BC tagging 150-300ns
80ns analog pulse sampling

Technology: Deep Sub-Micron CMOS 130-90nm

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Front-end in 130nm

Motivation for 130nm CMOS:

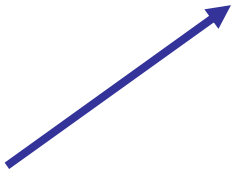
- Smaller
- Faster
- Less power
- Will be (is) dominant in industry
- (More radiation tolerant)

Drawbacks:

- Reduced voltage swing (Electric field constant)
- Noise slightly increased (1/f)
- Leaks (gate/subthreshold channel)
- Design rules more constraining
- Models more complex, not always up to date

UMC CMOS Technology parameters

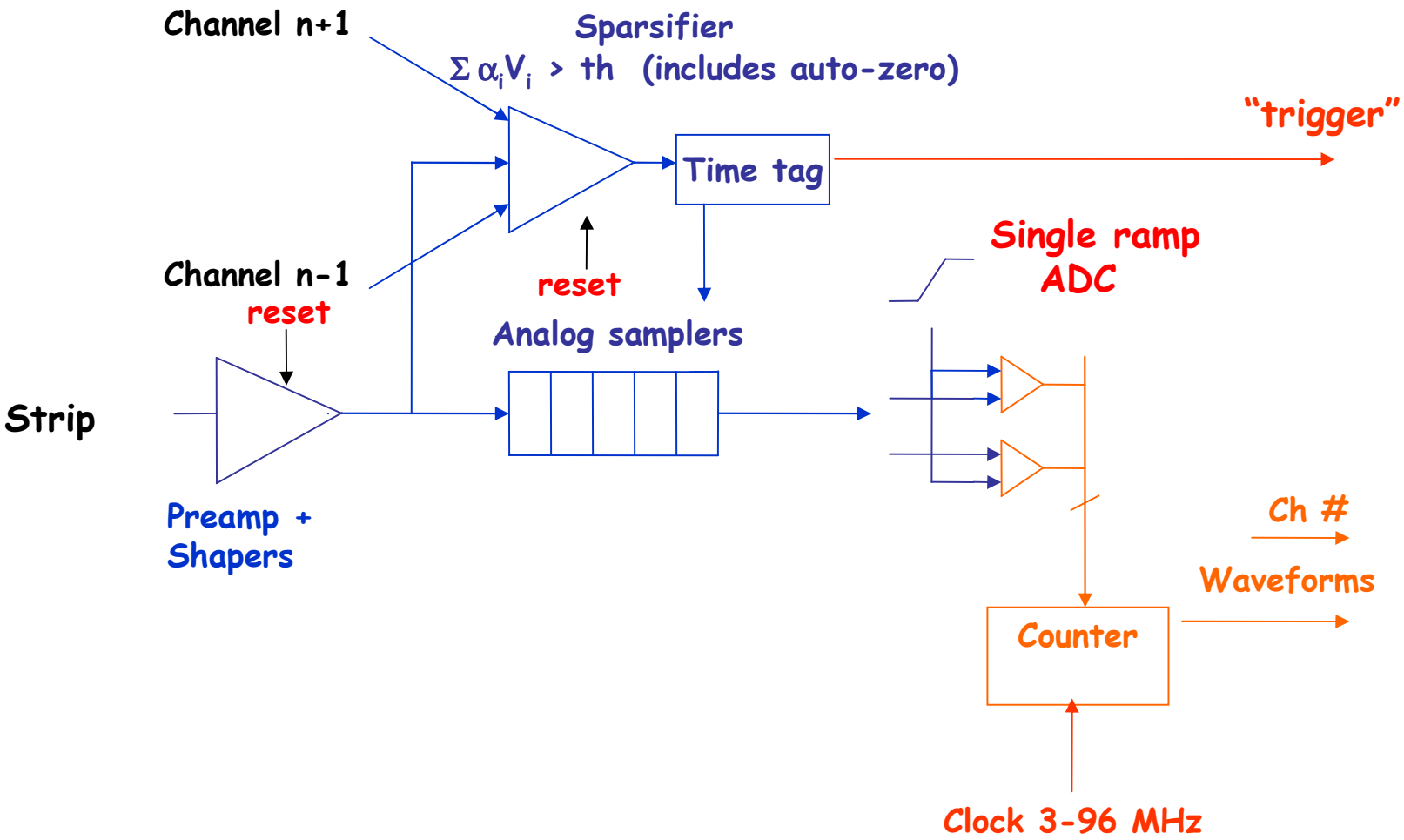
	180 nm	130nm
• 3.3V transistors	yes	yes
• Logic supply	1.8V	1.2V
• Metals layers	6 Al	8 Cu
• MIM capacitors	1fF/µm²	1.5 fF/µm²
• Transistors	Three Vt options	Low leakage option



May be used for analog storage during ~ 1 ms

Help from IMEC Europractice (Leuven, Belgium): Paul Malisse, Erwin Deumens

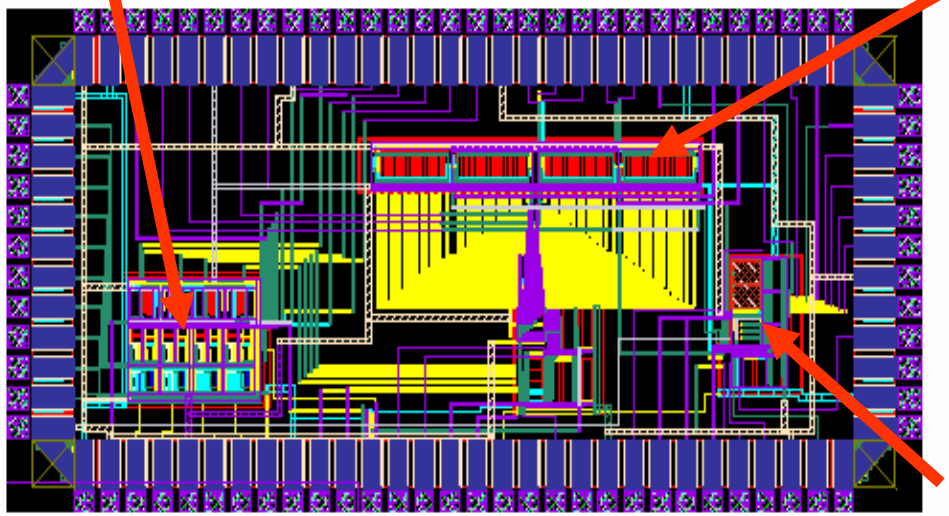
4-channel Chip



4-channel chip layout

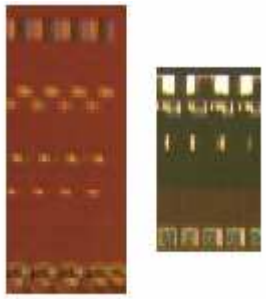
Amplifier, Shaper, Sparsifier 90*350 µm²

Analog sampler 250*100 µm²



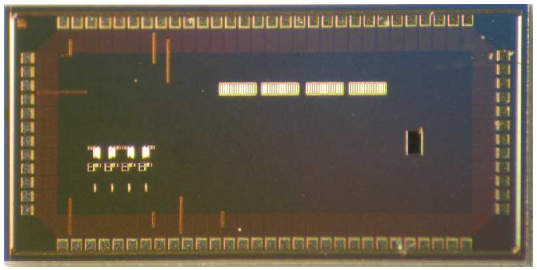
A/D 90*200 µm²

Layout of the 130nm chip including sampling and A/D conversion



180nm 130nm

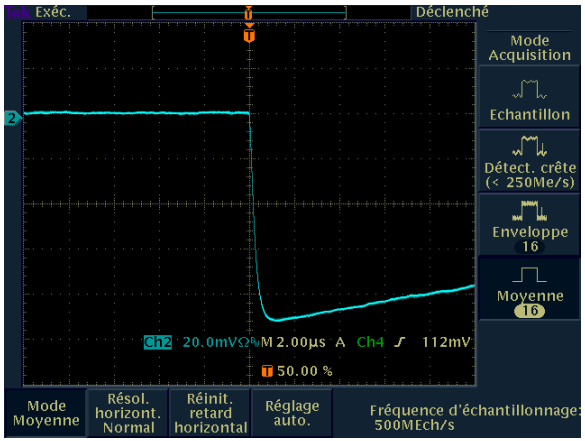
Photo



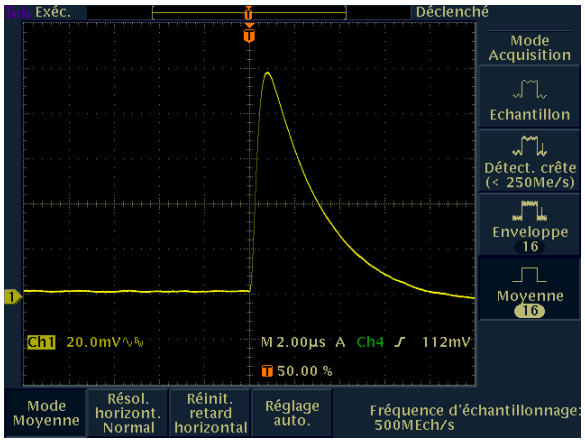
Preamp-shaper results

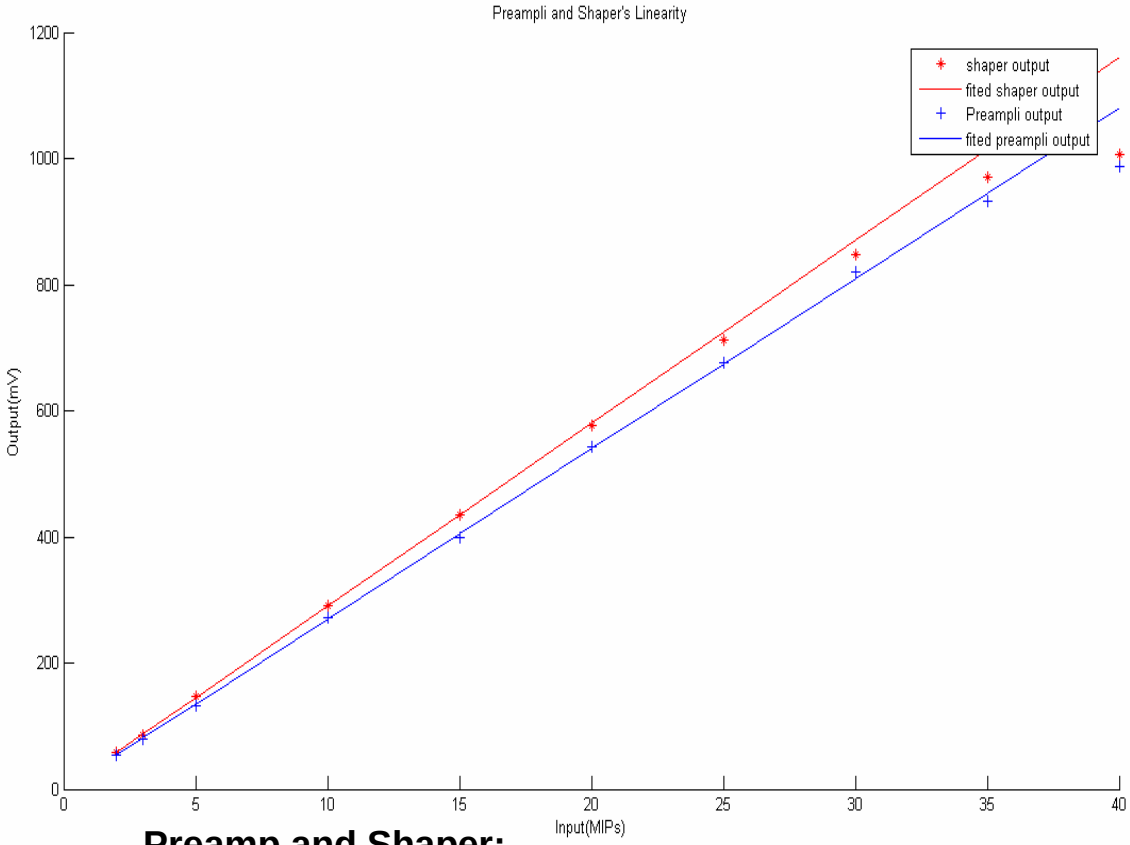
Measured gain - linearities

Preamp output



Shaper output

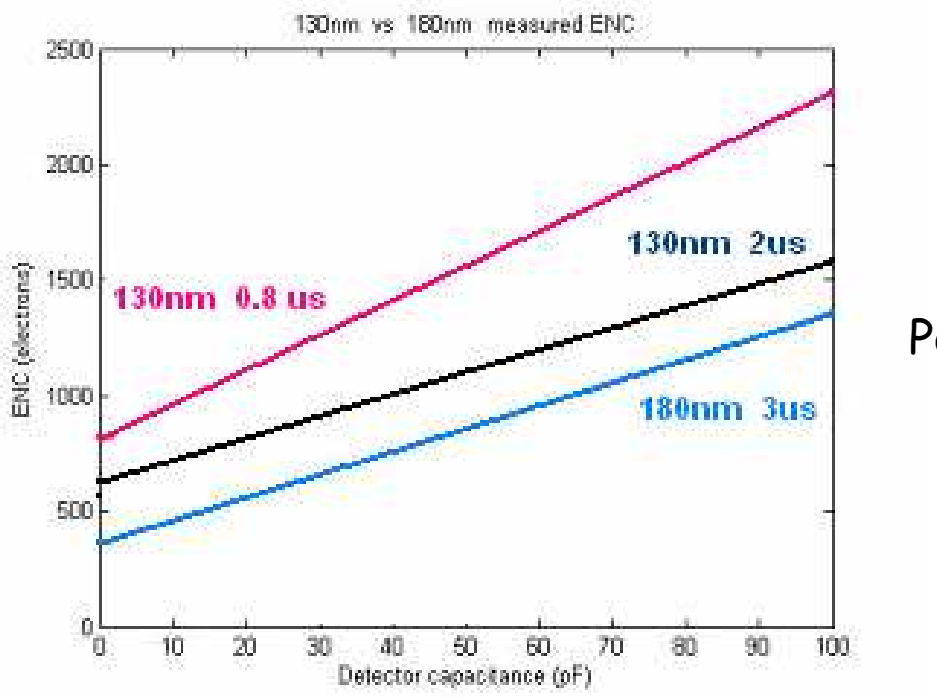




Preamp and Shaper:

Gain = 29mV/MIP
Dynamic range = 20 MIPs 1%
30 MIPs 5%
Peaking time = 0.8-2.5µs / 0.5-3µs expected

Noise results

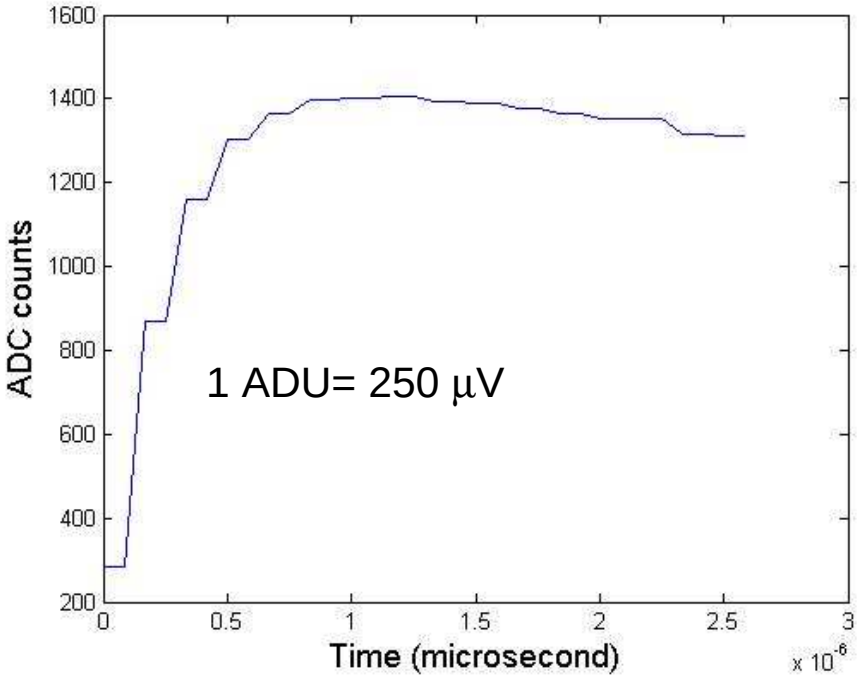


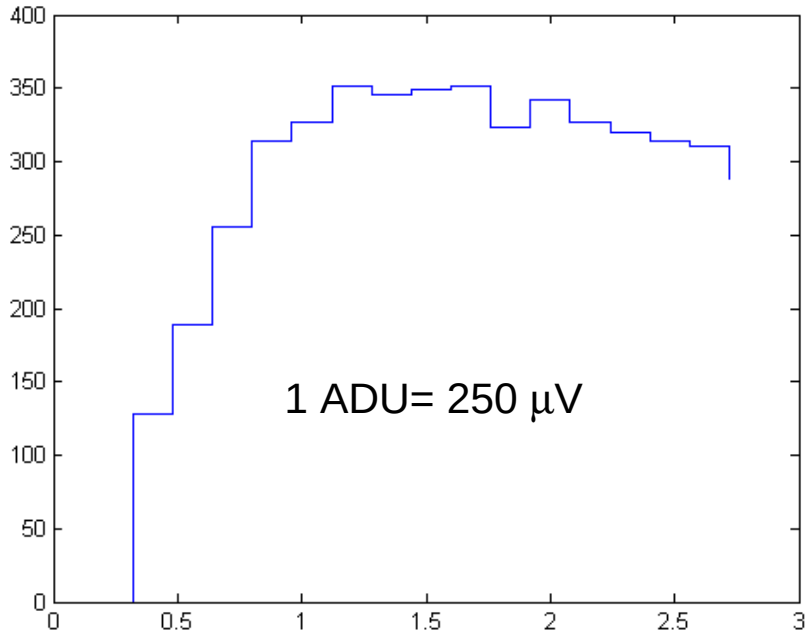
Power (Preamp+ Shaper) = 245 µW

Noise:	130nm @ 0.8 µs :	850 + 14	e-/pF	245 µW	(150+95)
	130nm @ 2 µs :	625 + 9	e-/pF		
	180nm @ 3 µs :	*375 + 10.5*	*e-/pF*	*210 µW*	*(70+140)*

Digitized analog pipeline output
Laser response of detector + 130nm chip

Digitized shaper output



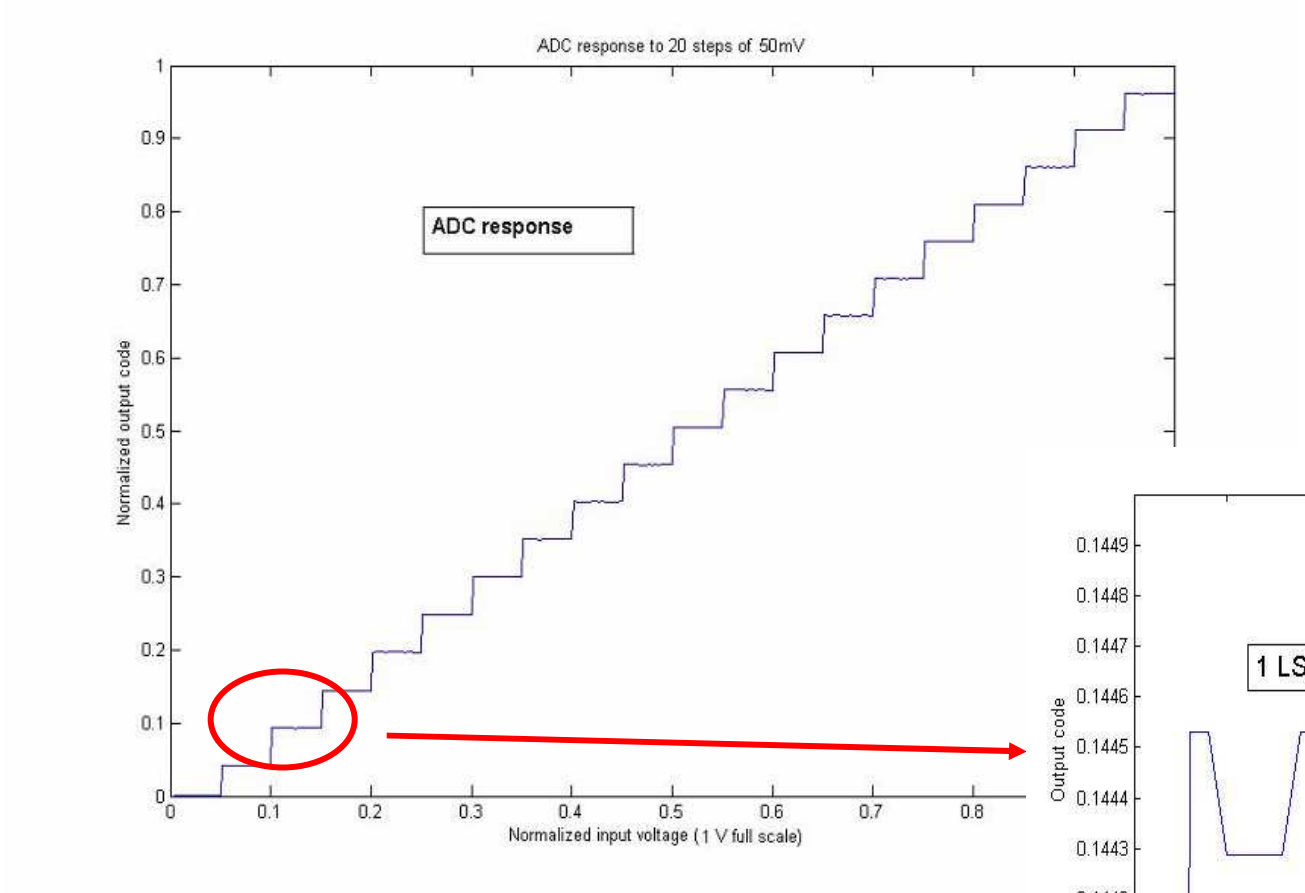


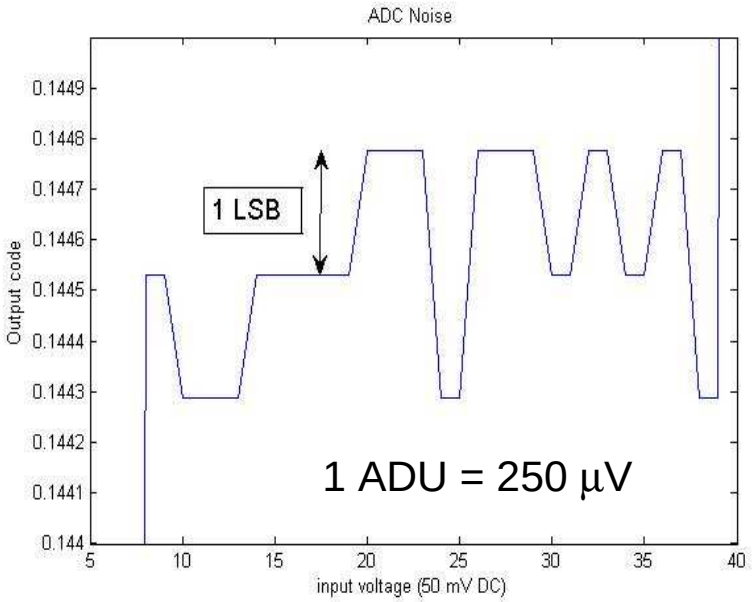
Sampling rate = 12 MHz
Readout rate = 10 KHz

From calibration pulser as input

From Laser diode + Silicon detector

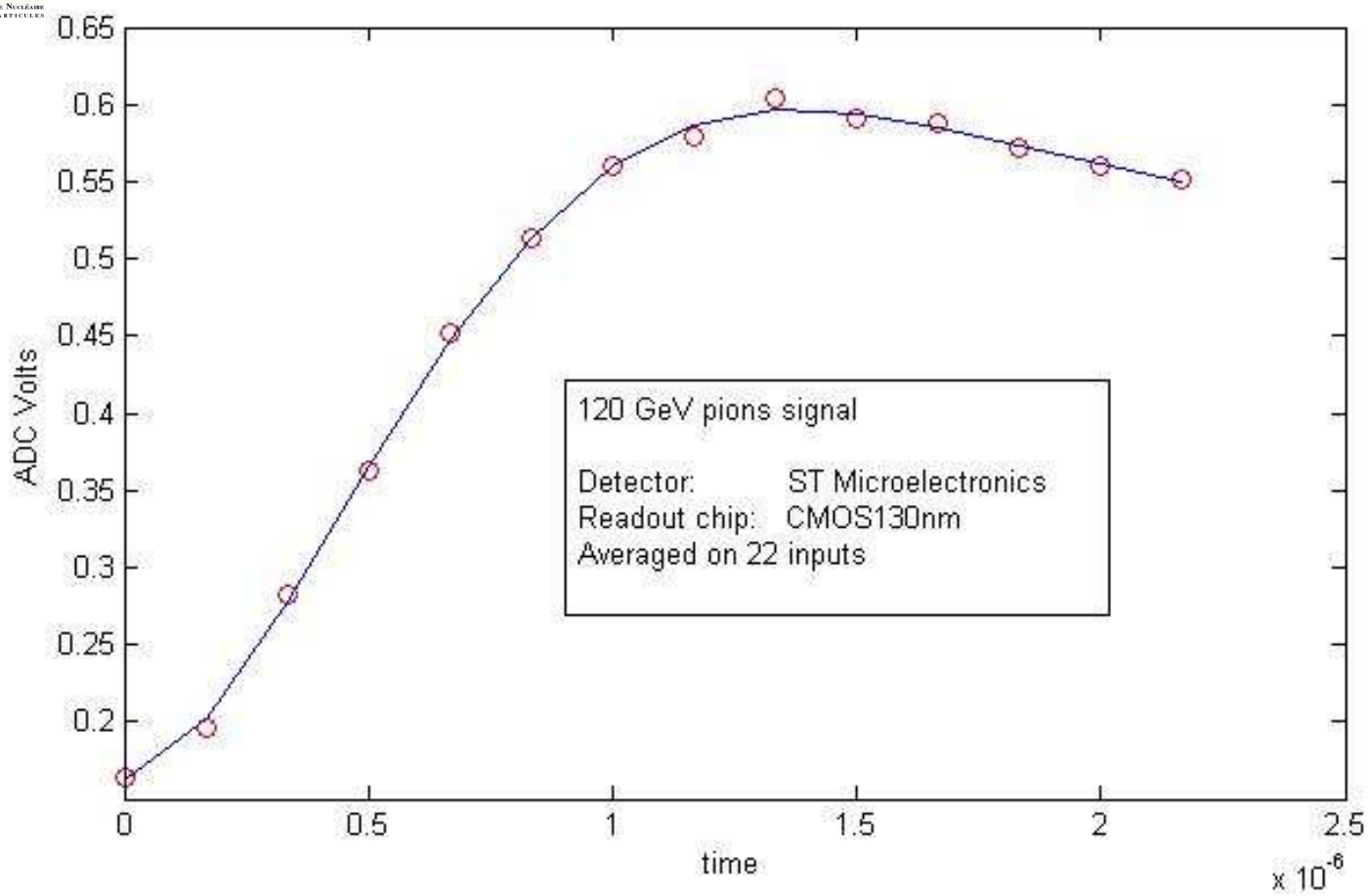
ADC evaluation





Noise= 4 LSBs 12 bits designed, 10 bits OK

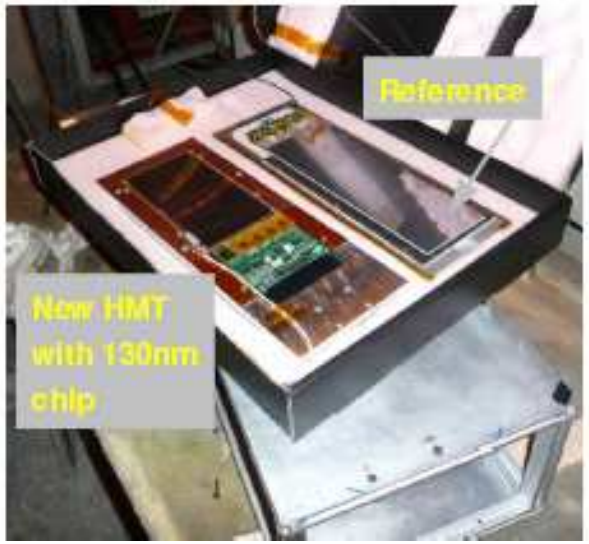
CERN Beam tests results

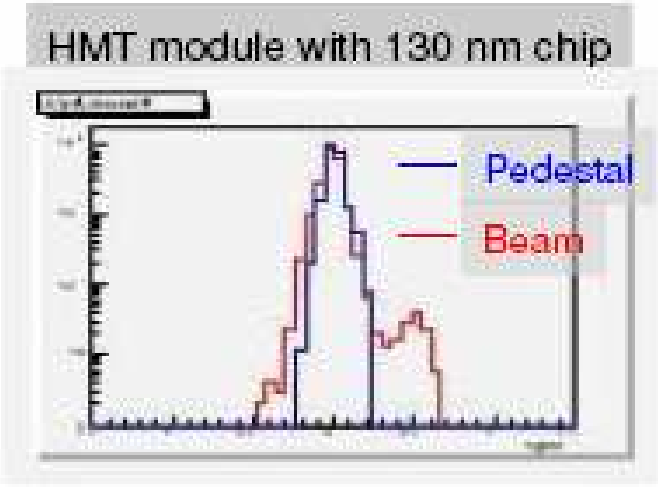


- **Averaged response of 120 GeV pions through 500 μm thick Silicon detector**
- **Actual pedestal spread: 100mV under investigation (decouplings on PCB)**
- **Pedestal subtracted off-line, then digitized shaper waveform OK.**

(see also Jacques David's presentation)

130nm chip pedestals/beam response





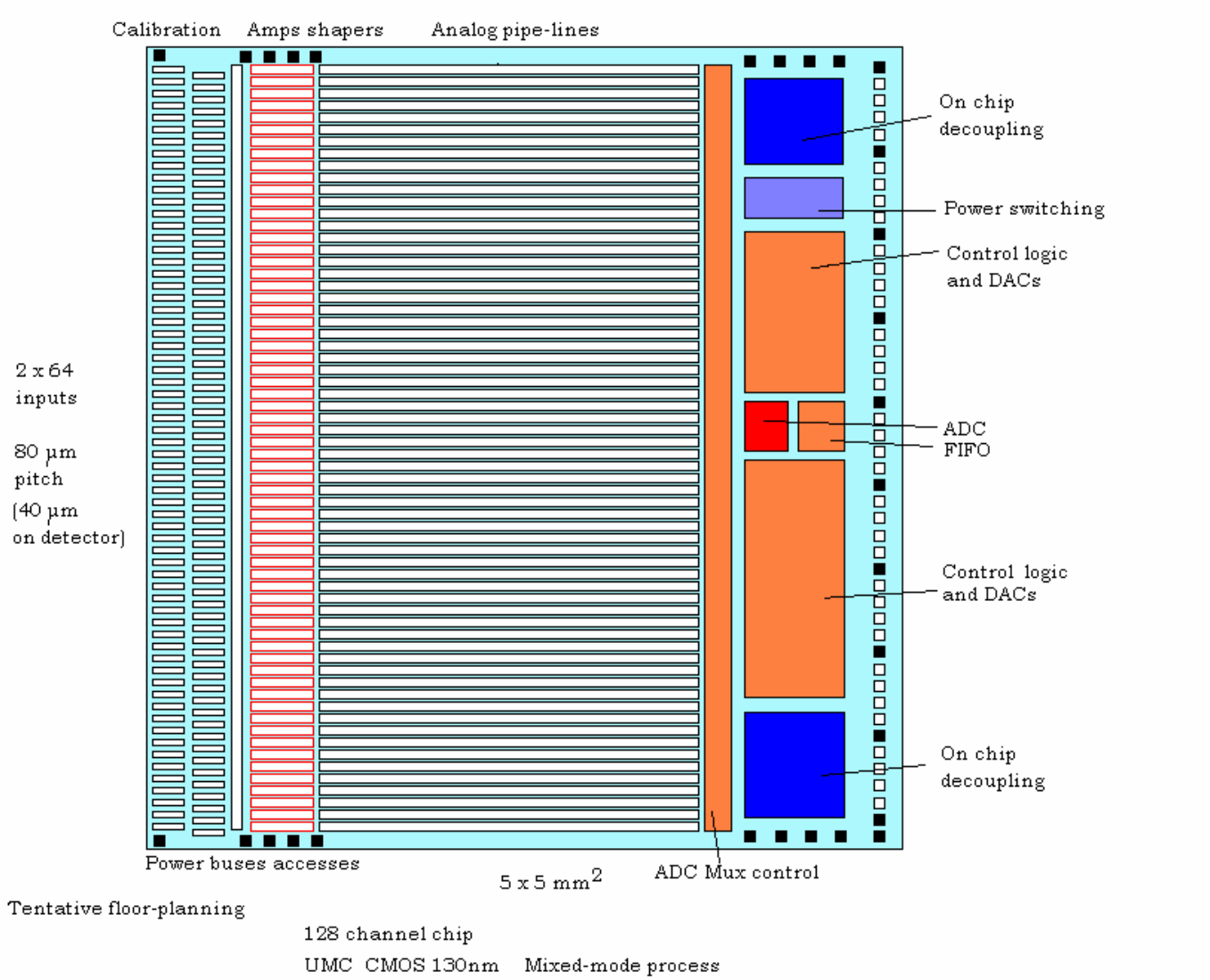
See also Jacques David's presentation

Next chip: Planned Digital

- 128 channels in 130nm CMOS
- Chip control
- Digital buffer
- Processing for :
  - Calibrations
  - Amplitude and time least squares estimation, centroids
  - Raw data lossless compression
- Tools
  - Cadence DSM Place and Route tool
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/Verilog
  - SRAM
  - Some IPs: PLLs

Needs for a mixed-mode simulator

128-channel chip



Conclusion

This CMOS 130nm design and first test results demonstrate the feasibility of a highly integrated front-end for Silicon strips (or large pixels) with

- DC power under 500μW/ch
- Silicon area under 100 x 500 μ²/ch

Allows to design a 128 channel chip starting from validated analog blocks

-> The 128 channel chip is one main deliverable of the EUDET FP6 EU Project within the JRA2-SiTRA task. It has to equip the forthcoming larger prototypes under construction

-> There is a growing effort within the SiLC collaboration for developing this new version and also starting to design the next step in the readout-DAQ system right after the FE chip (see Aurore's talk)

The End …